Technical Reference Manual for VP E2x/msd VME Intel® Atom™ Processor E3800 Product Family, Single or Dual PMC/XMC Sites

Manual Order Code 550 0049 Rev 02 March 2016

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CONVENTIONS

Throughout this manual the following conventions will apply:

- # or * after a name represents an active low signal - e.g. INIT# or INIT*
- 0x denotes a hexadecimal number - e.g. 0xFF45
- byte represents 8-bits
- word represents 16-bits
- dword represents 32-bits

NOTATIONAL CONVENTIONS

NOTE: Notes provide general additional information.

WARNING: Warnings provide indication of board malfunction if they are not observed.

CAUTION: Cautions provide indications of board or system damage if they are not observed.

ANSI	American National Standards Institute
APIC	Advanced Programmable Interrupt Controller
ATA	AT Attachment
BIOS	Basic Input Output System
BIT	Built In Test
bps	Bits per second
BSP	Board Support Package
CBIT	Continuous BIT
CFast	CompactFlash ATA Serial Transport
CMOS	Complementary Metal Oxide Semiconductor
CPLD	Complex Programmable Logic Device
CUTE	Concurrent Technologies Unified Test Environment
DDR3L	Double Data Rate Low Voltage, Third generation
DIMM	Dual In-line Memory Module
DPTF	Dynamic Platform and Thermal Framework
DRAM	Dynamic Random Access Memory
DVI-D	Digital Video Interface – Digital
DVI-I	Digital Video Interface - Integrated
ECC	Error Checking and Correcting
EPROM	Electrically Programmable Read Only Memory
EEPROM	Electrically Erasable Programmable Read Only Memory
Gbps	Gigabits per second
GPIO	General Purpose Input/Output
GPU	Graphics Processing Unit
HDD	Hard Disk Drive
IEEE	Institute of Electrical and Electronics Engineers
IA	Intel Architecture
I/O	Input/Output
IRQ	Interrupt Request
KBD	Keyboard
LAN	Local Area Network
LDT	Long Duration Timer
LED	Light Emitting Diode
LFM	Linear Feet per Minute
LPC	Low Pin Count
Mbps	Megabits per second
MTBF	Mean Time Between Failure
N/A	Not Applicable or Not Available
NC	Not Connected
NMI	Non Maskable Interrupt
NVRAM	Non Volatile Random Access Memory
OS	Operating System
PBIT	Power BIT
PC-AT	Personal Computer-Advanced Technology
PCI	Peripheral Component Interconnect
PCI-X	PCI Extended
PCIe	PCI Express
PIC	Programmable Interrupt Controller
PIT	Periodic Interrupt Timer
PLL	Phase Locked Loop
PMC	PCI Mezzanine Card
POST	Power-on Self-Test
PS/2	Personal System/2
PSD	Power Spectral Density
PXE	Pre-Boot Execution
RAM	Random Access Memory
RFU	Reserved for Future Use
RoHS	Restriction of Hazardous Substances
ROM	Read Only Memory
RST	Reset
RTC	Real Time Clock

RTM ..... Rear Transition Module or Transition Module
SATA ..... Serial ATA
SMBus ..... System Management Bus
SMI ..... System Management Interrupt
SMIC ..... Server Management Interface Controller
SoC ..... System on Chip
SODIMM ..... Small Outline Dual In-line Memory Module
SPI ..... Serial Peripheral Interface
SRAM ..... Static Random Access Memory
SSD ..... Solid State Disk Drive
SST ..... Source Synchronous Transfer
SYSFAIL ..... System Fail
TDP ..... Thermal Design Power
TPM ..... Trusted Platform Module
UART ..... Universal Asynchronous Receiver/Transmitter
UEFI ..... Unified Extensible Firmware Interface
USB ..... Universal Serial Bus
VGA ..... Video Graphics Array
VME ..... Versa Module Europa
VITA ..... VMEbus International Trade Association
XMC ..... Switched Mezzanine Card

REVISION HISTORY

Revision	Summary of Changes	Date
01	First release	April 2015
02	Updated Title Page, to show option for Single or Dual PMC/XMC sites Updated Figure 2-1, Default Switch Settings (changed SW5-1 to RFU) Updated Section 6.1, changed MBLT64 to MBLT Updated Section 6.5.2, Note to include reference to Push Button variant Updated Figure 7 2, Console Port Select options, COM3 console port removed Updated Section 9.3.6, Status Register 3 bits 6:5, COM3 console port removed Updated Section 9.3.10, Status Control Register 5 bits 1:0, changed to RFU Updated Section 9.5.1, VME Address Capture Control Register, bit 4 logic corrected Updated Section 9.5.1, VME Address Capture Control Register, bit 5 deleted the word IRQ from term BERR Flag Clarified Section 7.3 and Section A14.4, front panel DVI-I interface build option: both VGA and DVI-D signals are available, but not simultaneously. Updated the SATA Flash Drive Module part number AD 231/103 to show as AD 231/10x (allowing for either the AD 231/103 or AD 231/104) Minor non-technical updates and formatting	March 2016

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1 INTRODUCTION

1.1 General

This manual is a guide and reference handbook for engineers and system integrators who wish to use the Concurrent Technologies VP E2x/msd, a VME based 6U single board computer utilizing an ultra-low power SoC (22nm process) from the Intel® Atom™ processor E3800 product family. The board is designed for low power applications using a PC-AT™ architecture operating in a VMEbus environment.

The VP E2x/msd is available in different variants. These differ by the processor speed and type, the amount of fitted DRAM, front panel I/O configuration, and rear I/O configuration. Digits replace the "x/msd" in the board name to indicate some of these variations:

- x is the number of processor cores
- m is mechanical variations such as the front panel
- s is processor speed/type
- d is the DRAM total capacity

- The processor speed options are listed in Table 1-1.

Board Name	Processor
VP E24/m1d-yz	4-core 1.91 GHz (10W) Intel® Atom™ Processor E3845
VP E21/m1d-yz	1-core 1.46 GHz (5W) Intel® Atom™ Processor E3815

Table 1-1 VP E2x/msd Processor Variants

The board is available in standard, extended temperature, and rugged conduction-cooled versions. A summary of the key differences between these versions is provided in Section 1.2. Details of other board configuration options are given in Section 1.4. References to the board in this document will use the name VP E2x/msd unless they apply only to a specific variant, in which case the full name is used.

Other configuration options (for example, memory size, front and rear I/O configurations) are specified by a coded suffix appended to the board name Further details of the I/O configuration options are given in Section 1.4.

The information contained in this manual provides all the information necessary to configure, install and use the VP E2x/msd as part of a system. It assumes familiarity with the VMEbus and PC-AT architectures and features.

Optional on-board security features are supported using the Concurrent Technologies Board Level Security Package (refer to the TA GRD/nnn datasheet, available on the website www.gocct.com). Additionally, there is a VP E2x/msd factory build option to support Trusted Platform Module (TPM) hardware. For further details, contact your distributor or Concurrent Technologies directly.

1.2 Standard, Extended Temperature and Rugged Options

The VP E2x/msd processor board supports several factory build options, where one of the build options provides compatibility with the legacy VP A45/01x processor board. The factory build options are as follows:

- Upgrade for the legacy VP A45/01x with front I/O and rear I/O compatibility
- A standard VP E2x/msd rear I/O option, with 2 x PMC/XMC sites or with 1 x PMC/XMC site and additional front panel IO connections

NOTE: Refer to Section 1.4 for more details.

1.2.1 Standard (N-Series), Extended Temperature (E-Series and K-Series) Options

The VP E2x/msd is available as variants that are qualified to a standard or extended range of operating and non-operating temperatures. Please see Section A.2 for specifications for the temperature ranges and Section A.4 for the shock and vibration ranges supported by the VP E2x/msd.

NOTE: The VP E2x/msd can operate with zero airflow (0 LFM), please refer to the airflow graph in Section A.3 for further details.

For further details on the extended temperature options, contact your distributor or Concurrent Technologies directly.

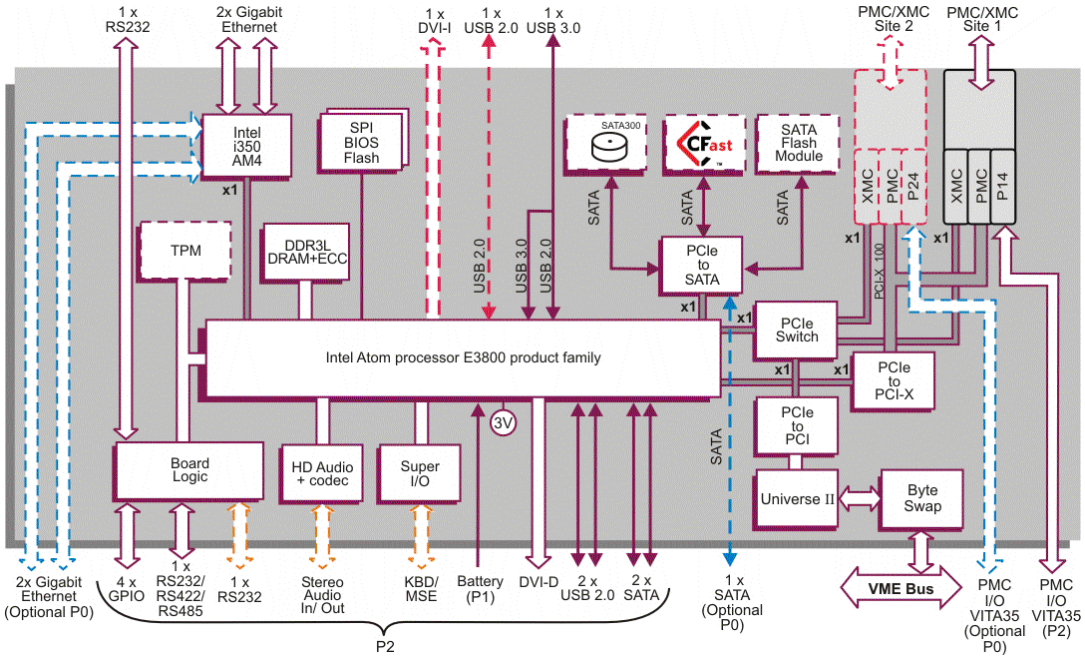


Figure 1-1 VP E2x/msd Overview

1.2.2 Rugged Conduction-Cooled (RC-Series) Options

The VP E2x/0sd is available as rugged conduction-cooled variants designated VP E2x/msd-yzRC. This offers extended temperature ranges, a higher specification for shock and vibration and does not require any forced airflow through the chassis. Please see Section A.2 for specifications on the temperature range and Section A.4 for the shock and vibration ranges supported by the VP E2x/0sd-yzRC.

Rugged conduction-cooled variants do not come with front panel interfaces.

For further details on the rugged options, contact your distributor or Concurrent Technologies directly.

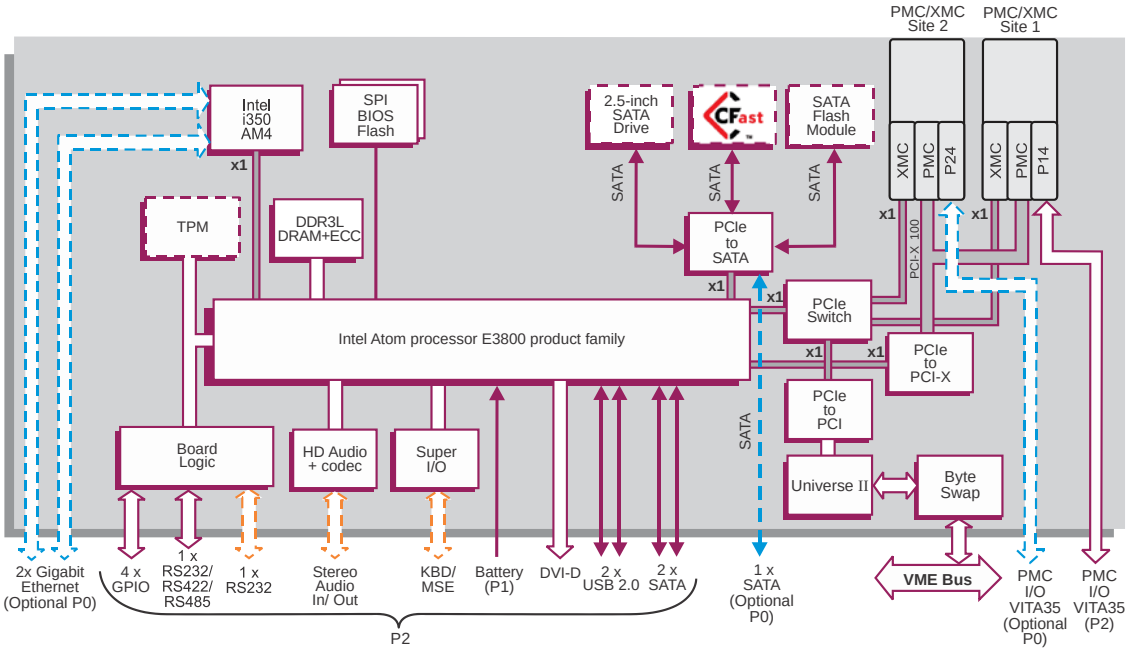


Figure 1-2 VP E2x/0sd-yzRC Overview

1.2.3 Differences between Standard, Extended Temperature and Rugged Options

Table 1-2 indicates the features supported by the extended temperature and rugged boards.

Version	Series	Mass Storage with HDD or SSD	Mass Storage with CFast™	Mass Storage with SATA Flash Module	Front Panel Interfaces
Standard Temperature	N-Series	HDD/SSD	✔	✔	✔
Extended Temperature	E-Series	SSD	✔	✔	✔
	K-Series	SSD	✔	✔	✔
Rugged Conduction-Cooled	RC-Series	SSD	✔	✔	x

Table 1-2 Differences between N, E, K and RC Series

NOTE: The RC-Series has a front stiffening bar fitted (as per VITA 20-2001). This can be removed (by the user) to enable PMC/XMC modules with front I/O connections to be fitted in a development environment.

1.3 VP E2x/msd Main Features

The VP E2x/msd is a member of the Concurrent Technologies range of single board computers for the VMEbus architecture. This is designed as an ultra-low power single board computer based on the Intel® Atom™ processor E3800 product family.

The VP E2x/msd can be factory configured as a standard build as an upgrade to the VP A45/01x. Depending on the configuration, the board features a range of interfaces including; quad channel Gigabit Ethernet, three SATA150/300, one USB 3.0, three USB 2.0, one DVI-D, one DVI-I, an on-board SATA HDD/SSD site and two PMC/XMC sites. Support is provided for an on-board SATA Flash module and CFast module.

1.3.1 Central Processor

The central processor used on this board is from the Intel® Atom™ processor E3800 product family utilizing ultra-low power 22nm process technology microprocessor. The two-processor types chosen from the product family are the 1-core 1.46 GHz Intel® Atom™ processor E3815 and the 4-core 1.91 GHz Intel® Atom™ processor E3845.

Board Variant	Processor	Cores	Base Frequency	DDR3L Frequency	L2 Cache Size	Power
VP E24/m1d-yz	E3845	4	1.91 GHz	1333 MHz	2 Mbytes	10W
VP E21/m1d-yz	E3815	1	1.46 GHz	1066 MHz	512 Kbytes	5W

Table 1-3 Processor Key Features

This Intel® Atom™ processor E3800 product family is based on Intel® Architecture (IA) System-on-Chip (SoC) technology that integrates the processor core, Gen7 Graphics controller, Memory Controller, and I/O interfaces into a single SoC solution. The SoC provides a dual channel DDR3L DRAM memory controller, a display graphics controller with integrated 2D/3D high definition video capabilities, four PCI Express® (PCIe®) ports and a variety of peripheral functions including a SATA controller, USB 2.0 and USB 3.0 controllers, Low Pin Count (LPC) Bus bridge, APIC interrupt controller, Real Time Clock and other legacy PC-AT architectural functions. The processor also supports Enhanced Intel® Speedstep® Technology.

The Intel® Atom™ processor E3800 product family is upwardly code-compatible with the other members of the x86 family of microprocessors.

1.3.2 Cache Memories

The Level 1 and Level 2 caches are both implemented on the processor die for maximum performance. The Level 1 cache is organized as 32 Kbytes of instruction cache and 24 Kbytes of data cache. The Level 2 cache stores both instructions and data. It supports up to 2 Mbytes 16-way L2 cache, operates at the core frequency and employs Intel's Dynamic Cache Sizing.

1.3.3 DRAM

The processor DRAM controller provides two DDR3L 64-bit channels. Memory Channel 1 is always used for DRAM data access. Memory Channel 2 is normally used for ECC data, limiting the maximum DRAM capacity to 4 Gbytes. However, when fitted with the 4-core processor, the VP E2x/msd may be factory configured to support 8 Gbytes DRAM without ECC support by using Memory Channel 2 for DRAM data access. In this dual channel configuration, the DRAM performance is also increased compared to the ECC (single channel) configuration.

The 4-core processor DRAM interface operates up to 1333 million 64-bit data transfers per second to provide a peak transfer bandwidth of 21.2 Gbytes/s (dual channel) and 10.6 Gbytes/s (single channel). The 1-core processor operates up to 1066 million 64-bit data transfers per second to provide a peak transfer bandwidth of 8.528 Gbytes/s (single channel only).

NOTE: There is no support for DIMM or SODIMM modules.

1.3.4 Non-Volatile Memory

The board contains two 8 Mbytes SPI Flash devices for the BIOS code and fixed data. One of the SPI Flash devices is used either as a redundant BIOS Flash or to hold the Fast Boot firmware.

The board also contains two 8 Kbytes serial EEPROM devices for user application data storage and Intel® fast boot feature.

1.3.5 PCI Express Ports

The SoC has a x4 PCIe Gen 2 interface which is configured as four x1 PCIe ports, and connected to the following devices:

- Gigabit Ethernet controller, Intel® i350-AM4
- PCIe switch, Pericom PI7C9X2G404
- PCIe-to-PCI-X bridge, Pericom PI7C9X130
- PCIe-to-SATA controller, Marvell 88SE9235

The PCIe switch provides a further three x1 PCIe Gen 2 ports which are connected to the XMC sites and a PCIe-to-PCI bridge (Pericom PI7C9X130) for VME Bridging.

1.3.6 PCI Bus

VP E2x/msd supports two PCI/PCI-X buses implemented using two PCIe-to-PCI/PCI-X bridge devices. One PCI bus is used for VMEbus bridging and the other one is extended to PMC sites.

A PCIe-to-PCI bridge (PI7C9X130) supports a 64-bit PCI interface that connects to an IDT®'s Universe™ II VME–to-PCI bridge. It operates in a fixed PCI mode at 33 MHz.

A PCIe-to-PCI-X bridge (PI7C9X130) supports a 64-bit PCI/PCI-X interface that is extended to PMC sites. It operates in PCI-X mode at 66 MHz by default, but supports both PCI and PCI-X bus modes at a range of bus clock speeds up to 100 MHz).

1.3.7 VME Interface

The VME interface is provided by a Universe™ II VME-to-PCI bridge. The VME interface supports transfers up to 64 bit data wide and up to 32 bit addressing. Hardware based endian swapping is implemented in board-logic and it is configurable via software control. The board can act as a system controller when it is installed in the first VMEBus slot.

1.3.8 USB

Up to four USB interfaces are provided with the following configurations, depending on the build option:

- One USB 3.0 port is available via a front panel connector and can support USB 1.1 (1.5 Mbps and 12 Mbps), USB 2.0 (480 Mbps) and USB 3.0 (5 Gbps).
- Two USB 2.0 ports are provided via the rear VME P2 connector, and can support both USB 1.1 (1.5 Mbps and 12 Mbps) and USB 2.0 (480 Mbps).
- One USB 2.0 port is available via an optional front panel connector, and can support both USB 1.1 (1.5 Mbps and 12 Mbps) and USB 2.0 (480 Mbps). This is a factory build option.

1.3.9 PMC/XMC Interfaces

The board provides two PMC/XMC sites. The PMC interfaces support single-width, 32 or 64-bit PMC modules complying with the IEEE 1386.1 standard. Both sites operate up to 66 MHz in PCI mode and up to 100 MHz in PCI-X mode, and support 3.3V and 5V signaling. The PMC interfaces also accept dual function PMC modules and Processor PMC modules. The latter will operate only in non-Monarch mode. Both sites also provide XMC connectors, each connected to the PCIe switch via a x1 PCIe port, supporting operation up to 5 Gbytes/s in each direction.

PMC/XMC site rear I/O is provided as per VITA35, connecting 64 rear I/O signals of site 1 (J14 connector) to backplane P2 (VITA35 P4V2-64ac), and 64 rear I/O signals of site 2 (J24 connector) to backplane P0 (VITA35 P4V0-64) connector.

NOTE: The VP E2x/4sd-12 or VP E2x/4sd-22 variants can support only one PMC/XMC site (site 1). The optional front I/Os are available in these variants instead of PMC/XMC site 2.

1.3.10 PMC Expansion Carrier Interface

The VP E2x/msd supports the AD CR3/PMC and AD CR6/XMC expansion carrier boards. The carrier boards support two single width PMC or XMC (AD CR6/XMC only) modules complying with the IEEE 1361.1 standard, in a second backplane slot adjacent to the VP E2x/msd. The carrier boards use one of the VP E2x/msd PMC/XMC sites to provide the interface to the additional sites on the carrier board.

1.3.11 Serial Communications

Up to three 16550 compatible serial data communication channels are provided, depending on the build option.

COM1 is an RS232/RS485/RS422 port accessible via rear VME P2 connector. It supports control signals CTS/RTS in RS232 mode and a direction control signal in RS485 mode.

COM2 is an RS232 port accessible via front panel and supports a full set of modem signals.

COM3 is an RS232 port accessible via VME P2 rear I/O connector and supports Transmit and Receive data signals only. It is a factory build option.

1.3.12 SATA Interfaces

A total of six SATA ports are provided and one of them is a build option. Two SATA300 ports are provided by the SoC and are available at the rear P2 connector. A Marvell SATA controller is used to provide the remaining four SATA150/300 ports. One port is available at the optional P0 connector and the other three ports are available on-board where a HDD/SSD site, a CFast site and SATA NAND Flash site are implemented.

1.3.13 SATA Flash Module and CFast Site

The VP E2x/msd supports the Concurrent Technologies SATA Flash Module AD 231/10x (AD 231/103 or AD 231/104), providing an option for removable non-volatile data storage. The SATA Flash Module interfaces to the VP E2x/msd via one of the SATA ports implemented by the Marvell SATA controller.

The VP E2x/msd supports a CFast site. One of the SATA ports from the Marvell SATA controller is used for the CFast Site.

Both the SATA Flash Module and CFast module are available at the same time.

1.3.14 Ethernet Controllers

A single Intel® i350-AM4 quad port Gigabit Ethernet controller provides up to four 10/100/1000 Mbps copper Ethernet ports. The configuration is dependent on the build options. Two ports are available on the front panel and the remaining ports are available via the optional rear P0 connector.

1.3.15 Graphics Controller

The internal graphics controller in the SoC contains an updated Intel® seventh generation graphics core. The graphics memory is shared with the system DDR3L DRAM memory. The 4-core processor supports a graphics frequency burst mode (GPU "turbo" mode). The VP E2x/msd supports a DVI-D interface at the rear P2 connector and an optional DVI-I port on the front panel, offering an option to connect two independent displays.

1.3.16 Keyboard and Mouse

The optional PS/2™ type keyboard and mouse interfaces, provided by the SCH3114 Super I/O controller, are available via the optional VME P0 connector.

The VP E2x/msd also supports USB based keyboard and mouse devices. These devices may be connected to any of the USB ports.

1.3.17 Real Time Clock (RTC)

A battery backed RTC device provides PC-AT clock, calendar, and configuration RAM functions. A battery can be installed on the board (non-rugged variants only).

The RTC device's clock and configuration RAM functions can be maintained from an external supply for battery free operation, if required.

1.3.18 HD Audio

The VP E2x/msd features an audio codec on-board to optionally provide analog stereo audio input and output capabilities via the P2 connector. The AD VP2/033 RTM provides audio jack sockets to offer line level I/O from the VP E2x/msd. The audio interface via P2 is a factory build option.

1.3.19 Trusted Platform Module (TPM)

The TPM provides a range of security features and is available on selected factory build variants. The TPM can also be used with the Concurrent Technologies Board Level Security Package, see Section 1.4.4.

1.3.20 User GPIO

The VP E2x/msd has 4 TTL compatible I/O signals accessible via P2 which are available for user defined I/O.

1.4 Board Configuration Options

The VP E2x/msd is available with several factory build options, some of which provide compatibility with the legacy VP A45/01x processor board. The basic factory build options are as follows:

- Upgrade for the legacy VP A45/01x with front I/O and rear I/O compatibility.
- New rear I/O options, with 2 x PMC/XMC sites or 1 x PMC/XMC site and additional front panel IO connections.

All of the factory build options are derived from VP E2x/msd-yz sales variants. As referred to earlier, there are several build options available. These options are summarized in Table 1-4:

	VP E2x/0sd-11 without P0 (VP A45/01x-5y compatible)	VP E2x/0sd-21 with P0 (VP A45/01x-6y compatible)	VP E2x/0sd-12 without P0	VP E2x/0sd-22 with P0	VP E2x/4sd-12 without P0, single PMC/XMC site	VP E2x/4sd-22 with P0, single PMC/XMC site
ETH A/B	Front	Front	Front	Front	Front	Front
ETH C/D	-	Rear	-	Rear	-	Rear
PS2 Keyboard/mouse	Rear	Rear	-	-	-	-
DVI-D	Rear	Rear	Rear	Rear	Rear	Rear
DVI-I & USB 2.0 (1xPMC/XMC site)	-	-	-	-	Front	Front
CFast Module Site	On-board	On-board	On-board	On-board	On-board	On-board
SATA Flash Module Site	On-board	On-board	On-board	On-board	On-board	On-board
SATA on P0 connector	-	-	-	Rear	-	Rear
COM3	-	-	Rear	Rear	Rear	Rear
P14 PMC I/O (VITA35 P4V2-64ac)	Rear	Rear	Rear	Rear	Rear	Rear
P24 PMC I/O (VITA35 P4V0-64)	-	Rear	-	Rear	-	Rear
Stereo Audio	-	-	Rear	Rear	Rear	Rear
Optional RTM	AD VP2/020-10	AD VP2/020-30	AD VP2/033-10	AD VP2/033-30	AD VP2/033-10	AD VP2/433-30

Table 1-4 VP E2x/msd I/O build options

Refer to Table 1-5 for the range of optional Rear Transition Modules.

Additional mass storage option kits are available for the VP E2x/msd:

- 2.5-inch SATA mass storage kit (AD 110/001)
- CFast Module
- SATA Flash Module (AD 231/10x)

NOTE: The optional 2.5-inch mass storage (HDD or SSD) kit utilizes the PMC/XMC Site 2 area. It is not possible to fit both a mass storage drive (HDD or SSD) and a PMC or XMC module simultaneously in the same site.

Contact your local Sales Office for ordering information for all these options.

1.4.1 Rear Transition Module Peripheral Functions

A range of VP E2x/msd rear I/O configuration options (Table 1-4) are supported by optional Rear Transition Modules (RTMs) which are fully described in Appendix B.

The table below summarizes the RTM variant interfaces.

Rear Transition Module	VME P2 Connector pins	VME P0 Connector	Serial ATA (SATA)	Ethernet	DVI-D	USB	PMC Site 1 Rear I/O	PMC Site 2 Rear I/O	Keyboard	Mouse	General Purpose I/O	Serial Port COM 1	HD Audio	High speed COM 3 Serial
AD VP2/020-10	160	-	2	-	✔	2	64-bit	-	✔	✔	4	✔	-	-
AD VP2/020-30	160	✔	2	2	✔	2	64-bit	64-bit	✔	✔	4	✔	-	-
AD VP2/033-10	160	-	2	-	✔	2	64-bit	-	-	-	4	✔	✔	✔
AD VP2/033-30	160	✔	3	2	✔	2	64-bit	64-bit	-	-	4	✔	✔	✔
AD VP2/433-30	160	✔	3	2	✔	2	64-bit	-	-	-	4	✔	✔	✔

Table 1-5 Rear Transition Module Variants and Options

1.4.2 Extended Temperature Options

All variants of the board are qualified for the standard operating and non-operating temperature ranges indicated in Section A.2. Some variants of the board are available which offer a wider range of operating and non-operating temperatures, but certain board features are no longer available with these variants. In particular the option for on-board mass storage using a commercial grade 2.5-inch rotating media Hard Disk Drive (HDD) is not supported for the extended temperature specifications.

Consult your distributor or Concurrent Technologies directly for more details of the extended temperature options.

1.4.3 Built-In Test Software

The Concurrent Technologies Built-in Test (BIT) software is an optional, full-featured diagnostic software package that can be ordered with the board. The package comprises of a factory-installed firmware component that supports automatic power-on testing of on-board hardware (PBIT), and a software component that integrates with the operating system and provides continuous run-time testing (CBIT).

Both BIT components include a dedicated console interface that supports interactive execution of individual test cases. The CBIT software also includes an API library, allowing test execution and results reporting to be integrated into application software.

The BIT package must be purchased with the board and cannot be supplied as an after-sales add-on. Please contact your local distributor or sales representative for ordering information.

1.4.4 Board Level Security Package

The Concurrent Technologies Board Level Security Package provides a means to enhance the security of equipment and thus prevent access to sensitive data and key Intellectual Property. The security is implemented on our single board computers using a combination of deeply embedded proprietary hardware, firmware and software countermeasures.

The Board Level Security Package must be purchased with the board and cannot be supplied as an after-sales add-on. Contact your local distributor or sales representative for further details.

1.4.5 Fast Boot Firmware

This board can be fitted with custom Fast Boot firmware as an alternative to the full-featured UEFI BIOS firmware normally installed on the board. The Concurrent Technologies Fast Boot firmware offers reduced boot times, when compared to the UEFI BIOS and allows the possibility of booting small operating system kernels directly from the on-board EPROM.

Depending on the target operating system, deployment of Fast Boot firmware may require additional configuration or programming operations before use.

Contact your local distributor or sales representative for further details.

1.5 VP E2x/msd Compatibility with the VP A45/01x

A benefit of the VP E2x/msd is that it can be used as a replacement or as an upgrade for the Concurrent Technologies VP A45/01x board. This section highlights the key differences between these products. In particular VP E2x/msd features likely to affect the user's application software or system integration are highlighted:

- The VP E2x/msd incorporates the Intel® Atom™ processor E3800 product family and faster memory, all of which will affect a program's execution speed. Also, the PCI bus enumeration for on-board and PMC/XMC devices will be different.
- For new projects/systems, specific VP E2x/msd variants incorporate one additional SATA300 port and HD stereo audio interfaces. The P2 connections and P0 connections on these variants are not compatible with the VP A45/01x P2 and P0 connector.
- The VP E2x/msd supports two XMC sites whereas VP A45/01x supports only one XMC site (site 1).
- The VP E2x/msd supports additional front panel DVI-I and USB 2.0 connectors in the 1x PMC/XMC site variants whereas VP A45/01x does not support this feature.
- The VP E2x/msd provides a USB 3.0/2.0 interface on the front panel in all variants, but the VP A45/01x supports only USB 2.0 on the front panel.
-

CAUTION: When selecting a VP E2x/msd board to upgrade from an existing VP A45/01x installation, take care to select a VP E2x/msd variant which is I/O compatible with the VP A45/01x board.

Refer to Section A.8 for full details on the backplane connector pin-out build options

1.5.1 List of Compatible VP E2x/msd Variants

The VP E2x/msd-yz variants compatible with the VP A45/01x are as follows:

- VP E2x/msd-11, VP A45/01x-5y compatible rear I/Os.
- VP E2x/msd-21, VP A45/01x-6y compatible rear I/Os.

NOTE: These two board variants are designed for I/O compatibility with the VP A45/01x board as an upgrade path for existing projects and are not recommended for new projects due to the legacy keyboard and mouse interfaces.

Refer to Section A.9 and Section A.9.1 for full details on the backplane connector pin-out build options.

1.5.2 VP E2x/msd Rear Connector Compatibility with VP A45/01x

The VP E2x/msd supports all the VP A45/01x front panel interfaces such as two Ethernet ports, one serial port, and one USB port. Single PMC/XMC site variants support extra front panel I/O connectors (DVI-I and one USB 2.0) in addition to the common front panel I/O.

Please refer to Table 1-6 for a summary of the P0/P1/P2 rear I/O compatibility with the VP A45/01x board.

P0, P1, and P2	VP A45/01x Rear I/O Interfaces	VP E2x/msd Compatible	Comments
P0	PMC Site 2 I/O (64 Bit) (signals 1 to 64)	Yes	Available only with VP E2x/msd-21 or 22 variants
	Ethernet Port (ETH C)	Yes	Available only with VP E2x/msd-21 or 22 variants
	Ethernet Port (ETH D)	Yes	Available only with VP E2x/msd-21 variants
	Ethernet Port LEDs Support	Yes	Available only with VP E2x/msd-21 variants
P1	VME Interface	Yes	VMEbus
P2	Serial Ports (COM1) with RS232/RS485 support	Yes	Always available
	USB (2 ports)	Yes	Always available
	SATA (2 ports)	Yes	Always available
	PS/2 Keyboard and Mouse	Yes	Available only with VP E2x/msd-11 and VP E2x/msd-21 variants
	DVI-D Interface	Yes	Always available
	GPIO (4)	Yes	Always available
	PMC site1 IO (64 bit)	Yes	Always available

Table 1-6 VP E2x/msd Rear Connector Compatibility with VP A45/01x

1.6 Compliance to RoHS 2011/65/EU

Unless otherwise stated, this product is offered in a form which complies with the RoHS 2011/65/EU directive.

2 HARDWARE INSTALLATION

This chapter contains general information on unpacking and inspecting the VP E2x/msd after shipment, and information on how to configure board options and install the board into a VME chassis.

CAUTION: It is strongly advised that an earthing strap should be worn at all times when handling the VP E2x/msd and its associated components in order to prevent damage to the board as a result of electrostatic discharge.

CAUTION: Care should be taken when handling the board as the heatsink and some components will be hot during and after use.

The list below outlines the steps necessary to configure and install the board. Each entry in the list refers to a sub-section which provides more details of that stage of the procedure. It is recommended that the board is prepared for installation by following this sequence:

1. Unpack the board - Section 2.1.
2. Check the board switch settings match the required operating mode - Section 2.1.1.
3. Locate the board's indicators and switches - Section 2.2.
4. Fit the battery, if required - Section 2.3.
5. Fit a CFast module - Section 2.4.
6. Fit a SATA Flash module (AD 231/10x) - Section 2.5.
7. Locate on-board Mass storages modules - Section 2.6.
8. Fit a PMC or XMC module, if required - Section 2.7.
9. Install the board - Section 2.8.1

CAUTION: It is strongly recommended that the user reads all of Section 2 before installing the board in a VME backplane, or before fitting a PMC or XMC module. In particular, additional cautionary notes will highlight areas needing special consideration.

HARDWARE INSTALLATION

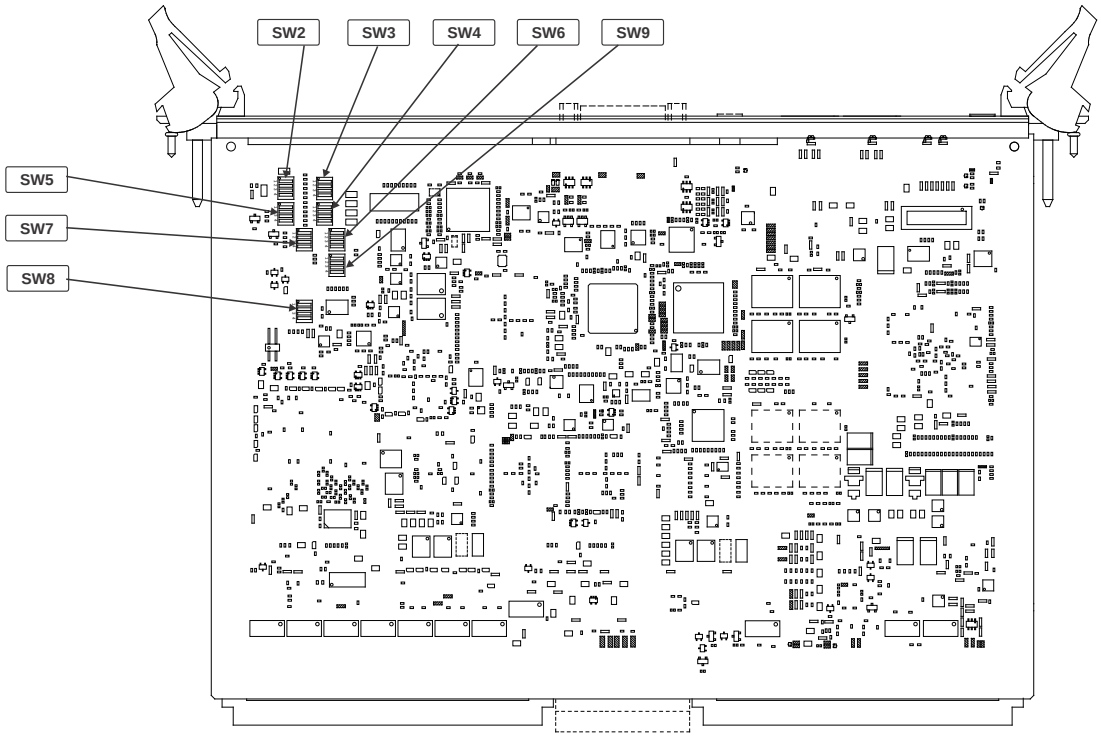
2.1 Unpacking and Inspection

Immediately the board has been delivered, a thorough inspection of the package should be carried out to check for any damage caused in transit.

CAUTION: If the packaging is badly damaged or water-stained, the carrier's agent must be present when the board is unpacked.

Once unpacked, the board should be inspected carefully for physical damage such as loose components. In the event of the board arriving in an obviously damaged condition Concurrent Technologies or its authorized agent should be notified immediately.

2.1.1 Default Switch Settings



SW2

OFF ON
1 Console COM Selection1 – COM2
2 Rx Termination COM1 – Disabled
3 PCI Bridge Mode – Auto
4 EXT_RST Enable - Disable

SW6

OFF ON
1 Ground Return – Ground
2 Ground Return – Ground
3 PMC V(I/O) – 3.3V
4 RFU

SW3

OFF ON
1 RFU
2 RFU
3 RFU
4 XMC Site2 support - Enable

SW7

OFF ON
1 User/PROCHOT LED – PROCHOT
2 Force Optimal Defaults – Disabled
3 VME Reset – Disabled
4 Watchdog – Disabled

SW4

OFF ON
1 Push Button - Reset
2 RFU
3 RFU
4 Wake-on-LAN - Enabled

SW8

OFF ON
1 Console Mode – DVI-D/KBD
2 Boot Mode - BIOS
3 Console COM Selection 0 – COM2
4 User / Test - 0

SW5

OFF ON
1 RFU
2 PCI CLK Freq Select – 66MHz
3 Boot Type – Normal
4 SPI Flash Select – Device1

SW9

OFF ON
1 GPIO0 – High
2 GPIO1 – High
3 GPIO2 – High
4 GPIO3 – High

Figure 2-1 Default Switch Settings

Switch	Default Function	Default Position	Section Reference
SW2-1	Console COM Selection1 – COM2	OFF	Section 7.1.1.1
SW2-2	Rx Termination COM1 – Disabled	OFF	Section 7.1.2.1
SW2-3	PCI Bridge Mode – Auto	OFF	Section 2.7.2
SW2-4	EXT_RST Enable - Disable	OFF	Section 6.5.3
SW3-1	RFU	OFF	N/A
SW3-2	RFU	OFF	N/A
SW3-3	RFU	OFF	N/A
SW3-4	XMC Site 2 support - Enable	OFF	Section 2.7.3
SW4-1	Push Button/LK1 Header - Reset	OFF	Section 2.2.7
SW4-2	RFU	OFF	N/A
SW4-3	RFU	OFF	N/A
SW4-4	Wake-on-LAN - Enabled	OFF	Section 5.3
SW5-1	RFU	OFF	N/A
SW5-2	PCI CLK Freq Select – 66 MHz	OFF	Section 2.7.2
SW5-3	Boot Type – Normal	OFF	Section 10.6
SW5-4	SPI Flash Select – Device 1	OFF	Section 8.1
SW6-1	Ground Return – Ground	ON	Section 7.1.2.1
SW6-2	Ground Return – Ground	ON	Section 7.1.2.1
SW6-3	PMC V(I/O) – 3.3V	OFF	Section 2.7.1
SW6-4	RFU	OFF	N/A
SW7-1	User/PROCHOT LED – PROCHOT	OFF	Section 11.2
SW7-2	Force Optimal Defaults – Disabled	OFF	Section 10.5
SW7-3	VME Reset – Disabled	OFF	Section 6.6
SW7-4	Watchdog – Disabled	OFF	Section 9.6
SW8-1	Console Mode – DVI-D/KBD	OFF	Section 7.1.1
SW8-2	Boot Mode - BIOS	OFF	Section 10.1
SW8-3	Console COM Selection0 – COM2	OFF	Section 7.1.1.1
SW8-4	User / Test - 0	OFF	Section 9.2.3
SW9-1	GPIO0 – High	OFF	Section 9.2.5
SW9-2	GPIO1 – High	OFF	Section 9.2.5
SW9-3	GPIO2 – High	OFF	Section 9.2.5
SW9-4	GPIO3 – High	OFF	Section 9.2.5

Table 2-1 Default Switch Setting Functions

2.2 Front Panel Indicators and Controls (Air-Cooled Variants Only)

Several LEDs are provided for development and debug on standard and extended temperature non-rugged variants. Rugged conduction-cooled variants do not have a front panel fitted; however some of the LEDs are still supported.

When installing or removing the board for the first time, or when checking its operation, it can be very useful to note the behavior of the LEDs on the front panel. Figure 2-3 shows the location of the LEDs, and their purpose is outlined below. A recessed push button switch is accessed through the front panel in some variants and this is described below.

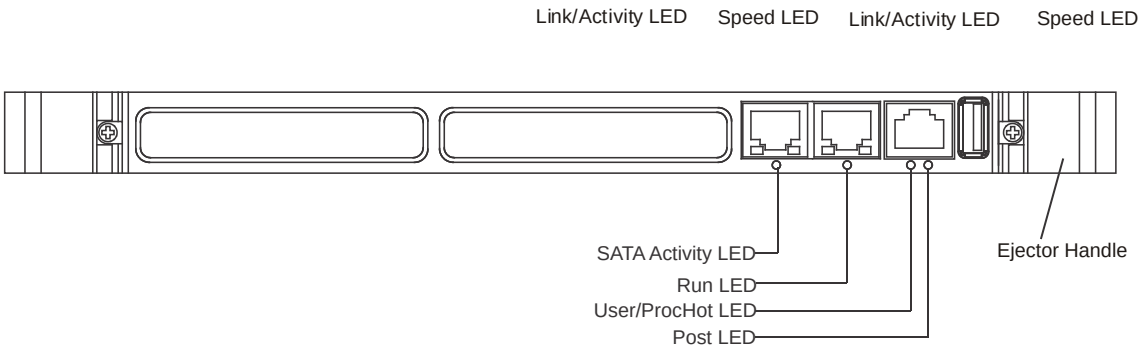


Figure 2-2 Front Panel Indicators and Controls - Dual PMC/XMC variants

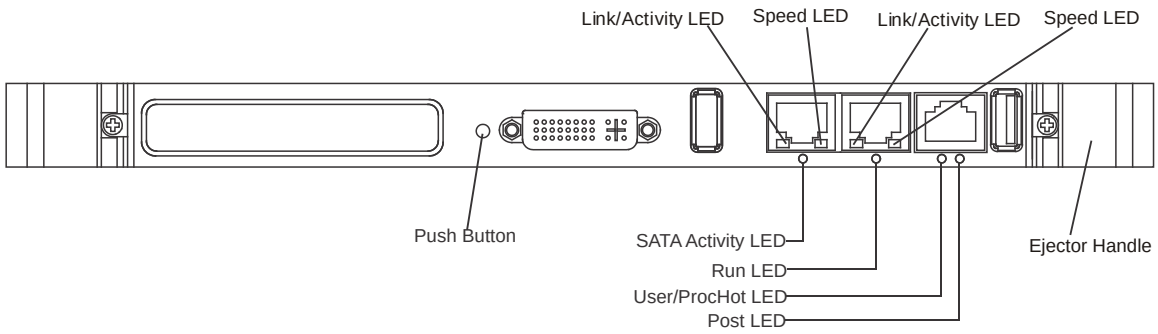


Figure 2-3 Front Panel Indicators and Controls - Single PMC/XMC variants

2.2.1 Run LED (R) Green

The Run LED indicates that activity is occurring on the LPC bus. This allows the user to quickly assess how active the bus is.

2.2.2 POST LED (P) Yellow

The POST LED is used to indicate that a Power On Self Test has failed. This LED flashes when outputting sound on the speaker.

2.2.3 Ethernet Speed LED Yellow

This LED indicates the operating speed of the Ethernet interfaces, as follows:

- Off = 10 Mbps
- Steady On = 100 Mbps
- Flashing = 1000 Mbps

2.2.4 Ethernet Link/Activity LEDs Green

These LEDs light when connection has been made on the Ethernet interfaces. They will flash to indicate link activity, and during periods of high Ethernet activity the LED may switch off for several seconds.

2.2.5 SATA Activity LED (SATA) Yellow

This LED lights when there is activity on any of the SATA interfaces.

2.2.6 User/Processor Hot LED (U) Red

This LED can be used either as a User LED or as a Processor Hot LED to indicate the thermal status of the processor, as selected by SW7-1 (User/PROCHOT LED Mode switch, described in Section 11.2).

In User mode, the LED is controlled by a bit in Status and Control Register 3, described in Section 9.2.4.

In Processor Hot mode, the LED will light when the processor is operating above its normal maximum die temperature. If the processor thermal management has been enabled, then the processor will automatically reduce its operating frequency to lower the die temperature. See Section 11.2 for further details. If this LED lights during normal operation, then it indicates that the chassis cooling system may have failed or is incapable of cooling the board.

2.2.7 Push Button

NOTE: This option is available only in variants that support a single PMC/XMC site, see Figure 2-3.

The push button can be configured via SW4-1 (Push Button/LK1 Header switch, see Figure 6-2) to perform either a board's system reset or a local Non-Maskable Interrupt (NMI).

2.3 Battery Installation/Replacement

When the board is powered off, the Real Time Clock used by the BIOS firmware and SoC management engine are powered by a 3V Lithium battery. It is advisable, though not essential, for the battery to be fitted prior to using the board, as shown in Figure 2-4.

NOTE: Rugged variants do not support an on-board battery.

One battery is supplied with non-rugged variants of the board, but it is not normally fitted when the board is shipped.

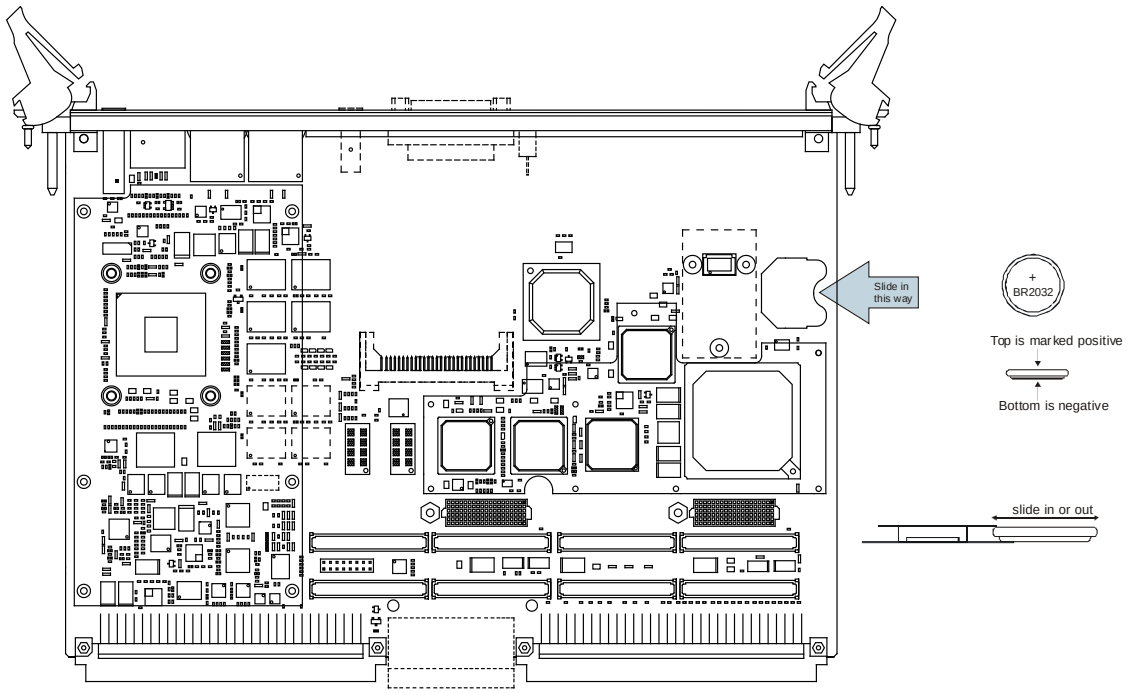


Figure 2-4 Fitting the Battery

The battery should be replaced when the voltage falls below 2.5V. Battery life depends on the way in which the board is operated and stored, but should be in excess of 3 years. This life expectancy will fall if the battery is subjected to long periods at temperatures of 45°C or above. They will also fall if the battery is fitted to a board that is stored in its conductive bag even at room temperature.

Operation without a battery is possible by connecting the VMEBus VCC_STDBY supply to an external 5V source. The contents of the RTC CMOS memory will be maintained and the Real-Time Clock will continue to function as long as the VCC_STDBY supply is maintained to the board.

NOTE: When replacing the board it is not necessary to remove power from the VCC_STDBY supply.

CAUTION: When replacing the battery, proper anti-static precautions must be observed.

WARNING: The date and time settings will need to be initialized if the battery is disconnected without maintaining the VCC_STDBY supply.

Battery

Never dispose of batteries in a fire.
Always dispose of batteries according to local regulations.
Please recycle when possible.
Do not dispose of batteries as household waste.
Always replace battery with manufacturer's recommended type.

2.4 On-board CFast Site

A CFast™ site is provided on the VP E2x/msd on PMC/XMC Site 2, the CFast site fully supports Type I modules. A Type II module may be fitted, but be aware that it is 5.0mm tall and therefore encroaches into the clearance zone between the main board and PMC or XMC module in Site 2. This may cause an interference problem if the PMC or XMC module also encroaches into this clearance zone. A retaining bar is provided which is suitable for Type I modules only.

The CFast site is located under PMC Site 2 as shown in Figure 2-5. The board must be removed from the chassis in order to insert or remove the module. To fit a module, first remove the retaining bar (if used) by removing its fixing screws from the underside of the board, taking care to keep the associated nuts and shake-proof washers. Then orientate the module such that the connector end is facing the socket and the label side is near to the board, and gently slide the module into the socket. Re-fit the retaining bar if required, as described below.

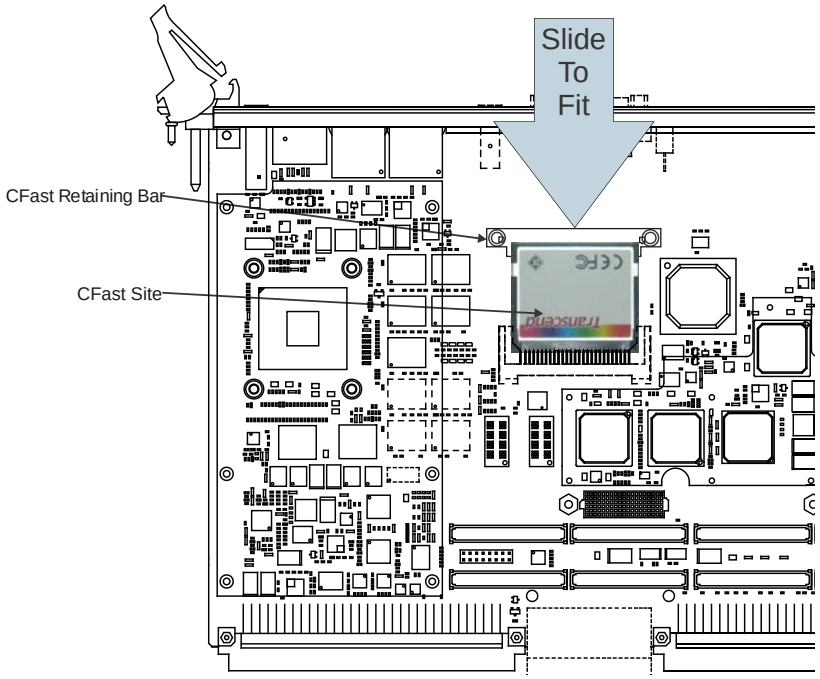


Figure 2-5 Location of CFast Site

To fit the retaining bar, place it over the module, insert the two screws supplied with the bar from the bottom side of the board, engage them with the supplied shake-proof washers and nuts, and then tighten the screws. Do not over tighten the screws.

NOTE: The CFast device needs to be inserted to the board properly by considering the polarization of the connector.

NOTE: If the board is likely to be subject to mechanical vibration, consider applying a suitable thread lock compound to the retaining bar screws.

NOTE: If the mass storage kit (AD 110/001) is fitted, it needs to be removed in order to gain access to the CFast site.

NOTE: The CFast module can be mounted simultaneously with the on-board 2.5-inch SATA mass storage kit (AD 110/001).

2.5 On-board SATA Flash Module

The VP E2x/msd supports an optional SATA Flash Module (AD 231/10x) within PMC/XMC Site 1.

2.5.1 Installing the SATA Flash Module

The following procedure describes the installation of a SATA Flash Module.

1. Locate SATA Flash Module site and S2 connector as shown in Figure 2-6.

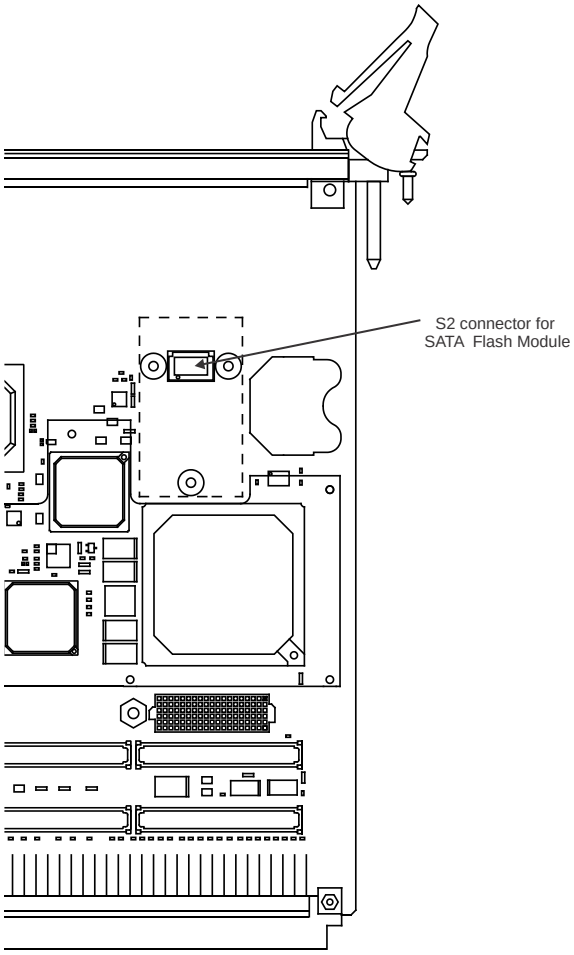


Figure 2-6 Location of SATA Flash Module and S2 connector

2. Align the connector on the underside of the SATA Flash Module with connector S2 on the main board. Press down the SATA Flash Module until it is firmly seated.

NOTE: The PMC/XMC card has to be removed from PMC/XMC Site 1 to gain access to the SATA Flash Module.

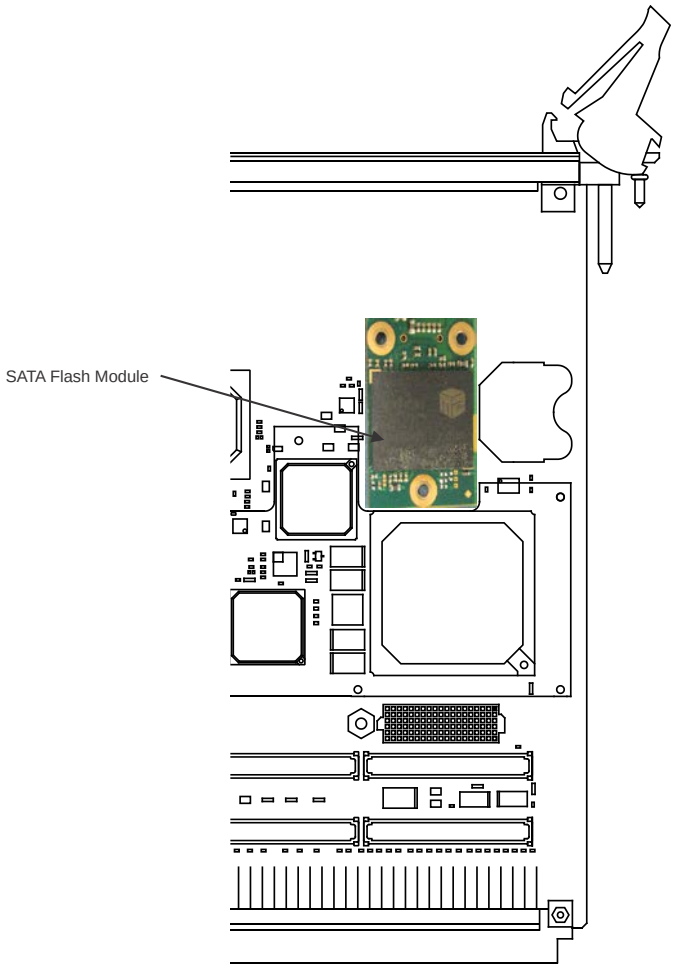


Figure 2-7 SATA Flash Module in Position

3. Turn the VP E2x/msd over and secure the SATA Flash Module to the main board using the three screws provided. Avoid over tightening the screws.

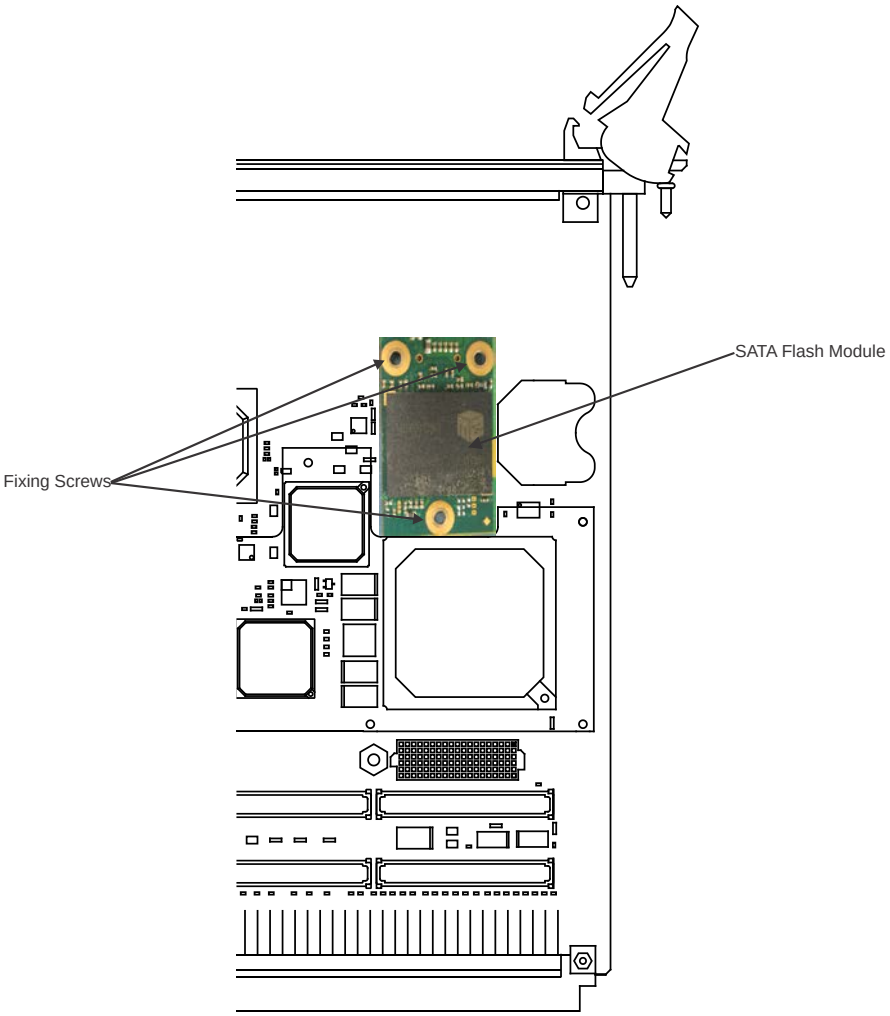


Figure 2-8 SATA Flash Module Fixing Screws

2.5.2 Removal of SATA Flash Module

This is the reverse of the procedure for installation.

1. Unscrew the three securing screws.
2. Gently ease the module clear of the connector.
3. Lift the module clear of the main board.

NOTE: Store the SATA Flash Module in a suitable anti-static environment, such as an anti-static bag, while it is not in use.

2.6 On-Board Mass Storage

The optional on-board 2.5-inch SATA mass storage drive (HDD or SDD) fits in PMC/XMC Site 2 as shown in Figure 2-9. An appropriate mounting kit (AD 110/001) is required, and may be ordered with or without a drive as a variant of the AD 110/001. Refer to your supplier for more details.

Section 2.6.1 describes the installation procedure for a non-rugged board, and Section 2.6.2 describes the procedure for a rugged air-cooled board.

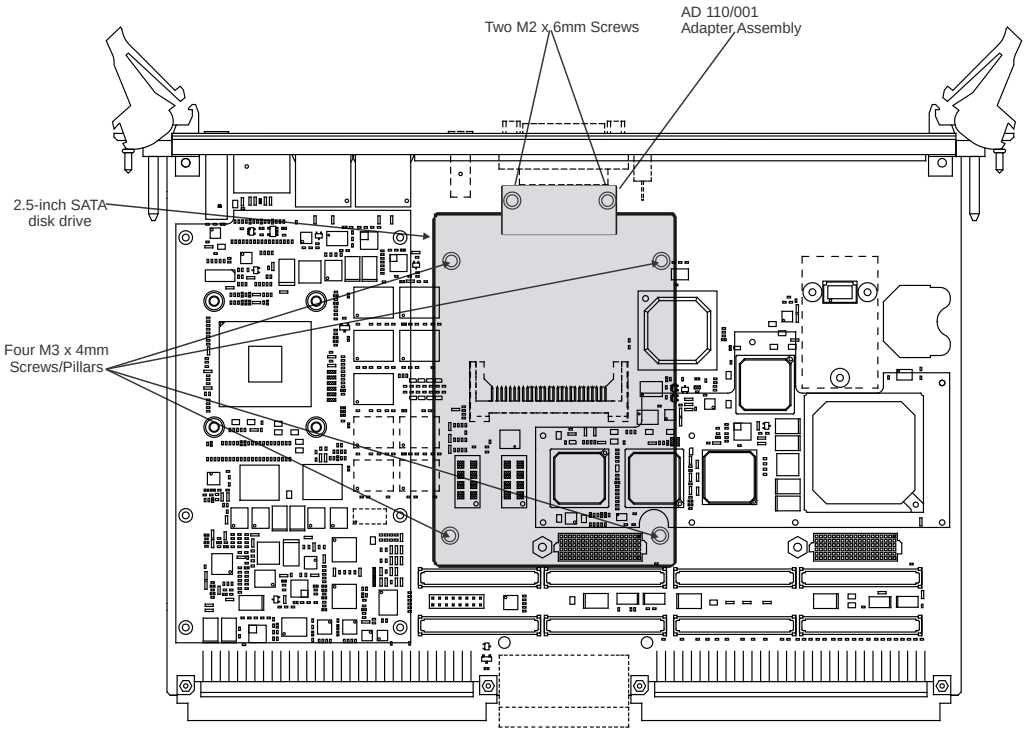


Figure 2-9 On-Board Mass Storage Location

NOTE: The optional mass storage drive (HDD or SSD) occupies the PMC/XMC Site 2 area. It is not possible to fit both a mass storage (HDD or SSD) and a PMC or XMC module simultaneously in the same site.

2.6.1 AD 110/001 Mass Storage Kit Installation (N, E and K variants)

This mass storage kit comprises of:

- A 2.5-inch SATA disk drive (type and capacity depends upon variant)
- An adapter assembly
- Four M3 x 4mm screws
- Four M3 x 5mm pillars
- Two M2 x 6mm screws

NOTE: The adapter assembly has a 22-way SATA connector on one side and a 20-way connector at 90 degrees to it. The 22-way SATA connector will plug into the disk drive and the 20-way connector will be connected to the base board.

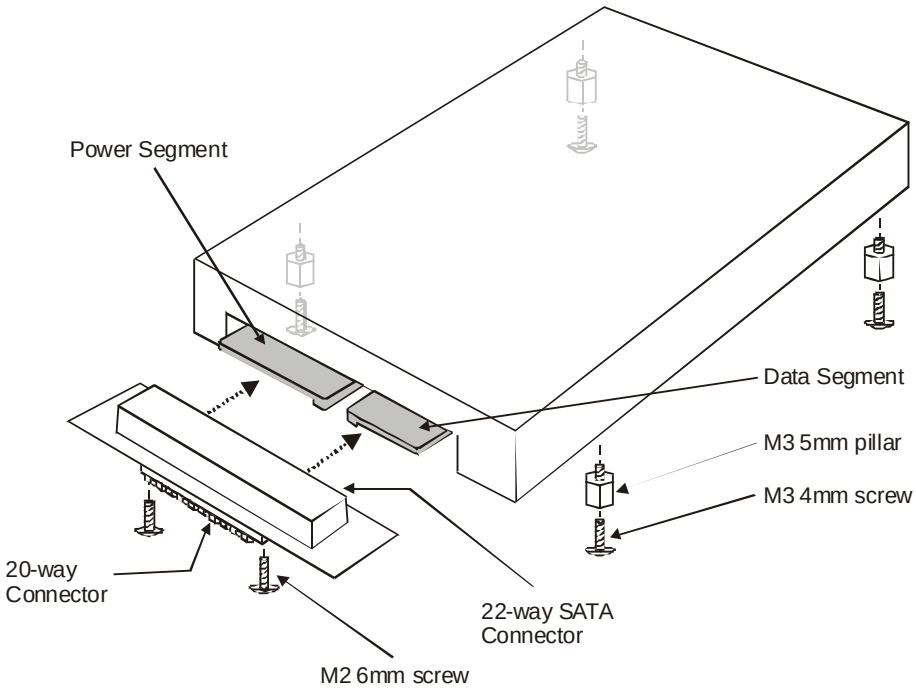


Figure 2-10 AD 110/001 Storage Kit Installation

1. Remove the PMC site polarizing key, if fitted, to avoid fouling the storage kit.
2. Remove the protective tape from the on-board SATA connector.
3. Screw the four M3 pillars into the base of the disc drive.
4. Plug the 22-way SATA connector of the adapter assembly into the disk drive as shown in Figure 2-10, ensuring correct orientation.
5. Offer the disk drive and adapter assembly to the base board and then screw the four M3 x 4mm screws through the mounting holes in the base board to mate with the threads in the pillars. Do not over tighten the screws.
6. Secure the adapter to the base board using the two M2 x 6mm screws.

NOTE: If the board is likely to be subjected to mechanical vibration, consider applying a suitable thread lock compound to the screws.

2.6.2 AD 110/001-RC Mass Storage Kit Installation (RC variants)

This mass storage kit comprises of:

- An adapter assembly (without a 2.5-inch SSD; the user must supply a suitable SSD of no more than 9.5mm height)
- Four M3 x 4mm screws
- Four M3 x 5mm pillars
- Two M2 x 6mm screws

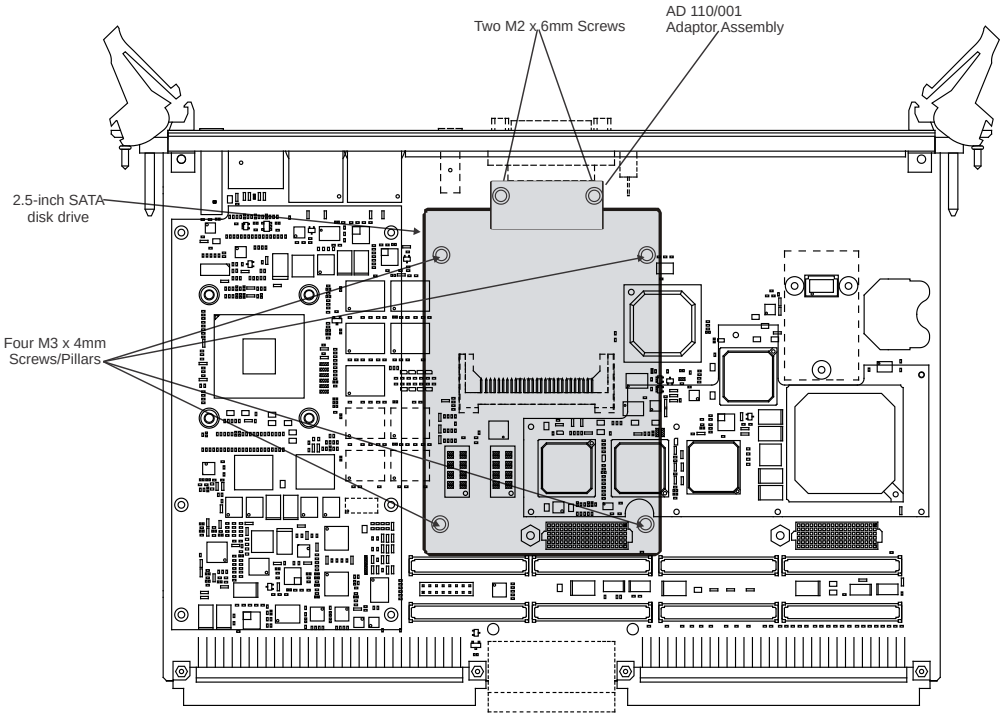


Figure 2-11 AD 110/001-RC Installation

The orientation and positioning of the drive and adapter assembly are shown in Figure 2-11. Installation and removal instructions are the same as for the non-rugged variants.

NOTE: If the board is likely to be subjected to mechanical vibration, consider applying a suitable thread lock compound to the screws.

2.7 PMC and XMC Modules – Installation and Removal

2.7.1 V(I/O) Selection for PMC Modules

The VP E2x/msd provides a voltage switch, SW6-3 (PMC VI/O Selection switch), for selecting 3.3V or 5V V(I/O) for both PMC sites, as shown in Figure 2-12. Before installing a PMC module, check that SW6-3 is configured to match the requirements and/or configuration of the PMC modules being used.

CAUTION: Do not fit a PMC module requiring 3.3V V(I/O) in one site and a PMC module requiring 5V V(I/O) in the other site. Doing so may cause damage to the module or the VP E2x/msd.

CAUTION: When installing a second PMC module and changing the PMC site's V(I/O) setting, ensure that the new setting is compatible with the original PMC module and with the configuration of SW6-3 (PMC VI/O Selection switch), as shown in Figure 2-12.

The position of both polarizing keys (see Figure 2-13) must match the configuration of SW6-3.

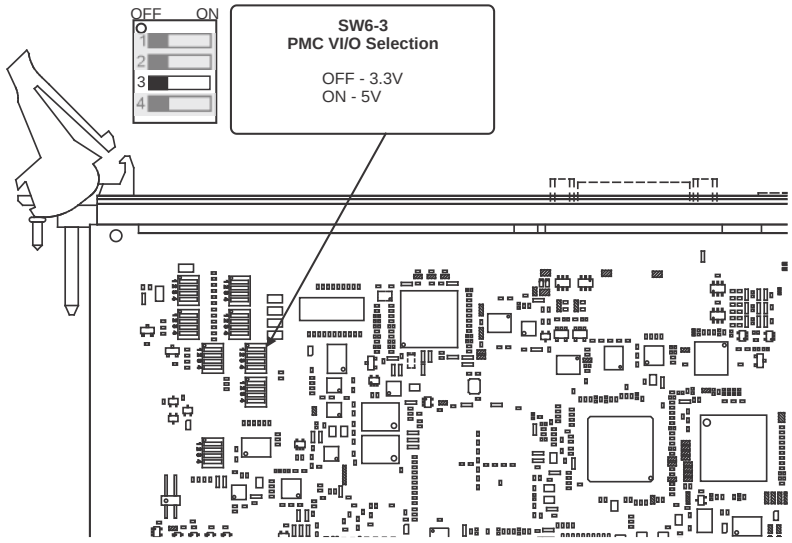


Figure 2-12 PMC V(I/O) Selection switch

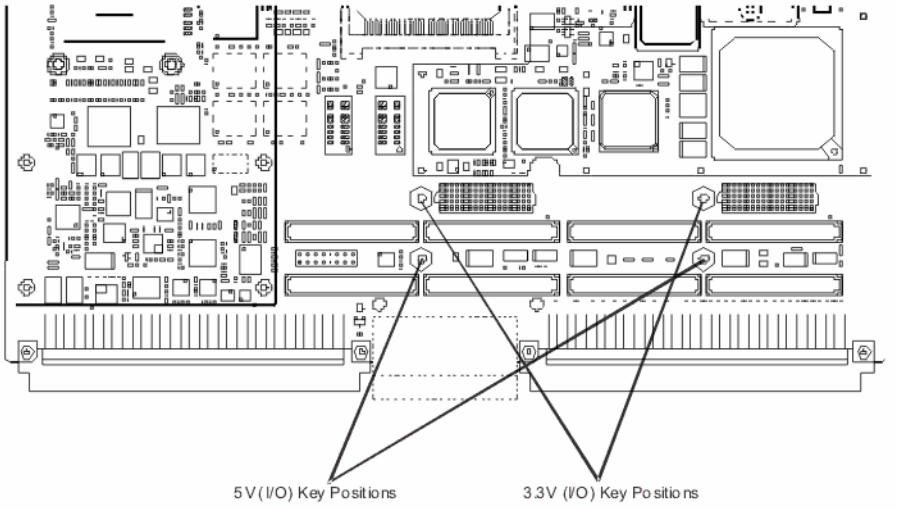


Figure 2-13 Polarizing Key Positions

2.7.2 PCI Bus Speed and PCI Bus Mode Selection for PMC Modules

The PCI bus connected to PMC Site 1 and Site 2 (as shown in Figure 2-14) can operate at various bus speeds in either PCI or PCI-X bus mode, namely:

- 25 MHz, 33 MHz, 50 MHz or 66 MHz in PCI mode
- 66 MHz or 100 MHz in PCI-X mode.

The bus speed and the bus mode for both PMC sites are determined by two factors, the setting of two switches and the specification of each PMC module. The switch settings are shown in Figure 2-14.

WARNING: The maximum performance of the PCI bus is determined by the slowest of the PCI devices fitted, or 100 MHz PCI-X mode if both the PMC modules support 100 MHz PCI-X mode operation.

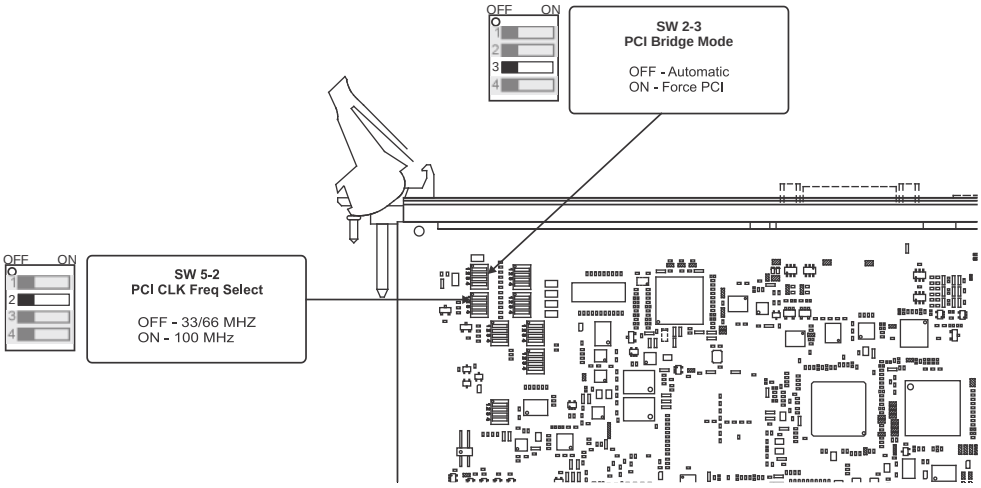


Figure 2-14 PMC Bus Speed and Mode Switches

SW2-3 (PCI Bridge Mode switch) should normally be in the OFF position so that the bus mode is automatically configured for the type of device connected to the bus. If a PCI-X device is

connected, it is desirable to operate in PCI bus mode and then set SW2-3 to the ON position.

SW5-2 (PCI CLK Freq Select switch) sets the speed range of the busses. If the switch is OFF this will be a multiple of 33 MHz. If the switch is ON, this will be a multiple of 25 MHz.

SW5-2 should normally be in the OFF position. If a PCI-X capable PMC module with a maximum speed greater than 66 MHz is fitted, the switch must be set to the ON position, which will limit the maximum frequency to 100 MHz.

WARNING: The VP E2x/msd cannot automatically determine the maximum speed capability of a PCI-X capable PMC module supporting speeds greater than 66 MHz, the PCI CLK Freq Select switch (SW5-2) must be set correctly. If the speed capability of the PMC module is uncertain, set SW5-2 to the ON position – however, this may reduce the performance of the PMC module.

2.7.3 XMC Site 2 Configuration

The XMC sites 1 and 2 both support a x1 Gen2 PCIe port on their XMC connector.

The PCIe ports for XMC sites are always supported by default. XMC Site 2 support can be disabled using SW3-4 (XMC Site 2 support switch) set to ON. PMC support is always enabled.

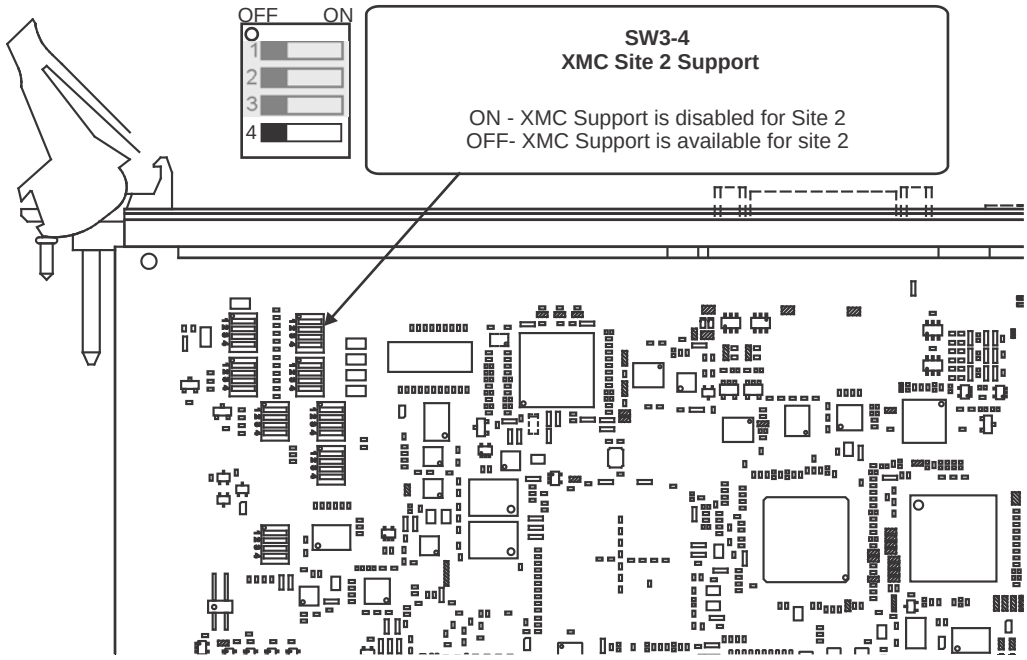


Figure 2-15 XMC Site 2 Support Switch

2.7.4 PMC/XMC Installation (except RC variants)

The Figure 2-16 shows the method for installation of a PMC module on the non-rugged variants of the VP E2x/msd. Use the same method when fitting an XMC module.

NOTE: The VP E2x/msd board is supplied with PMC blanking plates which must be removed before a new module can be fitted.

NOTE: On rugged variants, only PMC/XMC modules which meet the required standard for shock and vibration should be used.

1. Remove the blanking plate from the appropriate PMC slot on the main board.
2. If installing a PMC module, remove or install the voltage key post in the appropriate position, as shown in Figure 2-16. If installing an XMC module, remove this voltage key post.
3. Check that the standoffs are attached to the PMC and then align the front of the PMC with the opening in the front panel of the main board.
4. Install the PMC, component side down, aligning the PMC connectors with their mating connectors on the main board. Press them together so that the friction from the pins holds the PMC in place.
5. Screw the PMC in place using the four mounting screws.

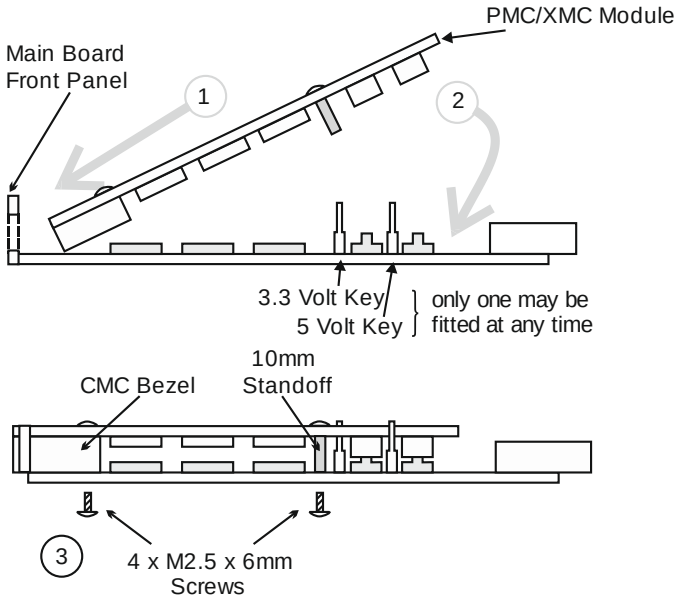


Figure 2-16 PMC/XMC Installation - except RC variants

2.8 Installation in a VME Backplane (all variants)

Before installation of the board in a VME chassis, check the following points:

When installing a variant of the board which is fitted with a P0 connector into a backplane which does not have the corresponding socket, check to see that no strengthening bars or other tall objects are present on the backplane before inserting the board. If bars or other objects are present, then verify that the P0 connector and/or the backplane will not be damaged when the board is fully seated in the slot.

Chassis Power Supply Unit current capabilities: The board draws current primarily from the +5V rail, and the details are provided in Section A.7.

The board can be installed in any standard VME slot. When installed in the first occupied slot the board will become a System Controller.

2.8.1 Installation of the Board

The board is installed and powered up as follows:

1. Ensure the system is powered OFF (VCC_STDBY may be left ON if used).
2. Slide the board into the designated slot, ensuring that the board fits neatly into the runners.

NOTE: For RC variants, first check that the wedge locks are in the relaxed state and that the handles are in the closed position.

3. Push the board into the card-cage until the P0, P1 and P2 connectors are firmly located and then use the ejector handles to push the board home.
4. For RC variants, tighten the wedge lock screws until the board is firmly locked in place.
5. Screw the ejector handles' retaining bolts into the holes in the chassis or cooling frame.
6. Connect the I/O cables to the connectors on the board's front panel and fix in place with the connectors' retaining screws.
7. If using an RTM, install it at the rear of the backplane and connect the I/O cables.
8. Power-up the system.

The following sequence of events should then occur:

- The green "RUN" LED and the yellow "POST" LED on the front panel will illuminate.
- The yellow "POST" LED will switch OFF.

If power-up does not follow the sequence described above, this indicates that the board is not operational.

NOTE: This sequence of events assumes the VP E2x/msd has Concurrent Technologies standard BIOS firmware and that the board is configured to the factory settings described in Section 2.1.1.

2.8.2 Removing the Board

To remove the board, shut down the application and operating system software before powering down the system, disconnecting any I/O cables, unscrewing the ejector handle retaining bolts, opening the ejector handles or loosening the wedge lock screws and extracting the board.

CAUTION: The VP E2x/msd is not hot swappable. The main system power must be off before attempting to install or remove the board.

3 SOFTWARE INSTALLATION

In most cases, installing operating system software on the VP E2x/msd follows the same sequence as installing on a PC. However, there are some additional points to note. The sections below summarize the special actions required for a few common operating systems.

3.1 Starting up for the first time

Many operating systems running on the board will need to use the standard Real Time Clock hardware. To maintain the date and time settings, and several other settings recorded by the BIOS, the battery must be fitted (or VCC_STDBY on the VME backplane interface connected). When the board is first installed, or after changing the battery, carry out the following steps to set up the board.

1. If required, fit a battery as shown in Section 2.3.
2. Ensure that SW8-1 (Console Mode switch, see Section 7.1.1) is set to the correct state for the console device which will be used (DVI-I/DVI-D monitor and keyboard, or serial terminal). Most operating systems which install on the target hardware will require a monitor and keyboard during installation, even if they can subsequently be re-configured to use only a serial terminal. See Section 7.1 for details of how to configure the board for this option.
3. Connect any additional modules and peripherals especially any mass storage devices.
4. Connect the console device and power up the board. Press <**F2**> as soon as possible and carry out the following:
    a. Set the time and date by using the cursor and function keys to move around the screen and select desired settings. Help information can be found in the right hand screen panel.
    b. When configuration is complete press <**F4**> to exit. Press the <y> to accept the changes and restart.
5. Check that all required mass storage devices are connected before continuing with software installation.

The BIOS restarts, runs the memory test again and begins boot-loading.

3.2 Boot-loading from CD-ROM

The operating system installed on the target hardware will generally be installed from a CD-ROM. To boot-load from CD-ROM, use the following procedure:

1. When the BIOS boot screen appears, press <**F12**>.
2. Wait for the pop-up boot device menu to display.
3. Select the CD-ROM drive using the cursor keys and then press <**Enter**>.

3.3 Installing Microsoft® Windows® Operating System

Installing a Windows operating system on the VP E2x/msd is generally very similar to installing it on a desktop PC.

Concurrent Technologies also offers a Board Support Package on DVD or CD-ROM (Part number: CD WIN/BSx-x0) which provides installation and configuration information, including appropriate drivers. For further details, please contact your supplier.

3.4 Installing RedHat® Linux®

Installing this operating system on the VP E2x/msd is generally very similar to installing it on a desktop PC.

Concurrent Technologies also offers a Board Support Package on CD-ROM (Part number: CD LNX/BS1-L0) which provides installation and configuration information, including appropriate drivers. For further details, please contact your supplier.

NOTE: If virtualization is to be used, it may be necessary to refer to the Board Support Package for further installation instructions.

4 MASS STORAGE INTERFACES

The VP E2x/msd has six Serial ATA (SATA) interfaces, one of which is optional and accessible via the VME P0 connector for connecting mass storage devices (build option). Two SATA300 interfaces are accessible via the VME P2 connector. Another three SATA150/300 interfaces are used to support on-board mass storage devices.

Two SATA300 ports are supported by the Atom™ SoC and four SATA150/300 ports are implemented using a quad port PCIe-to-SATA controller (Marvell 88SE9235).

The order in which the BIOS firmware tries to boot-load from these drives can be changed via the BIOS Setup screen for **Boot**. Refer to the BIOS Technical Reference Manual for details.

4.1 SATA Interfaces

The board provides six SATA interfaces which can support maximum transfer rates of up to 300 Mbytes/s (150/300 Mbytes/s for SSD/HDD) depending upon which port is used. Rear SATA interfaces can support up to 300 Mbytes/s and on-board SATA interfaces connected to on-board mass storage sites (HDD/SDD, CFast and SATA Flash Module) can support up to 300 Mbytes/s. Each interface supports the connection of a single SATA device.

The BIOS screen for **Advanced | Sata Configuration** allows the user to see what is connected to these interfaces, and to select some characteristics of the drives manually. Normally the BIOS firmware will automatically determine the drive characteristics from the drives.

4.2 SATA Flash Module Interface

SATA port 2 of the PCIe-to-SATA controller interfaces to the optional SATA Flash Module AD 231/10x within PMC/XMC Site 1. The module has a minimum capacity of 8 Gbytes.

4.3 CFast Module Interface

SATA port 3 of the PCIe to SATA controller interfaces to the optional CFast Module in PMC/XMC Site 2.

The VP E2x/msd fully supports Type I CFast modules. A Type II module may be fitted, but the user should be aware that it is 5.0mm tall and may therefore encroach into the clearance zone between the main board and PMC or XMC module in the same site.

4.4 On-board SATA Mass Storage Kit (HDD/ SSD) Interface

SATA port 1 of the PCIe to SATA controller connects to an optional on-board mass storage drive (HDD/SSD) using the AD 110/001 Mass Storage kit.

4.5 Rear SATA Interfaces

The rear SATA interfaces support SATA150/300 speeds.

The SATA0 and SATA1 ports are derived directly from the SoC and are used to support off-board SATA devices via the VME P2 connector.

The SATA2 port is derived from the PCIe-to-SATA controller (Port 4). SATA2 is connected to the optional P0 connector and is available only with specific VP E2x/msd compatible rear I/O variants. This is a factory build option. See Table 1-4 for more information.

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5 ETHERNET INTERFACES

The VP E2x/msd board is fitted with four 10/100/1000 Mbps Ethernet interfaces which are implemented with an Intel® I350-AM4 quad port Ethernet controller.

Two Ethernet interfaces are routed via the rear (for board variants that have a P0 connector fitted) and the remaining two Ethernet interfaces are routed to front panel connectors.

All Ethernet ports support Wake-on-LAN.

It is possible to boot-load the board through the Ethernet interfaces by setting the appropriate BIOS configuration options. See Section 10.3 for more details.

By convention in this manual, the front panel Ethernet interfaces are designated with suffix A and B, and the rear Ethernet interfaces with suffix C and D. The operating system drivers will enumerate these devices to conform to their driver conventions. See Table 5-1 for examples.

Variants with front panel connectors and P0 fitted				
	Front Panel		**Rear via P0**	
Ethernet port designations	ETH A	ETH B	ETH C	ETH D
Linux Instance	ETH3	ETH0	ETH1	ETH2
Windows Instance	Connection 4	Connection 1	Connection 2	Connection 3
Variants with front panel connectors but without P0 fitted				
	Front Panel		**Rear via P0**	
Ethernet port designations	ETH A	ETH B	-	-
Linux Instance	ETH1	ETH0	-	-
Windows Instance	Connection 2	Connection 1	-	-
Variants without front panel connectors but with P0 fitted				
	Front Panel		**Rear via P0**	
Ethernet port designations	-	-	ETH C	ETH D
Linux Instance	-	-	ETH0	ETH1
Windows Instance	-	-	Connection 1	Connection 2

Table 5-1 Ethernet Interface Identification

NOTE: Port numbering may be altered if additional Ethernet ports are added using a PMC or XMC module.

5.1 Front Panel Gigabit Ethernet (ETH A and ETH B)

Two Gigabit Ethernet ports are available at the front panel. Channel 0 of the Ethernet controller is named ETH B (labeled as ETHB on the front panel) and channel 3 of the Ethernet controller is designated as ETH A (labeled as ETHA on the front panel).

5.2 Rear Panel Gigabit Ethernet (ETH C and ETH D)

Two Gigabit Ethernet interfaces are routed to the optional P0 connector. Channel 1 of the Ethernet controller is designated as ETH C and channel 2 of the Ethernet controller is designated as ETH D.

The ETH C connection uses a pin-out which is compatible with the VITA 31.1 standard, but the ETH D connection is not compliant with that standard.

When the board is used with one of the Concurrent Technologies optional RTMs (see Appendix B), it may be necessary to check and configure switches on the RTM to ensure that the Ethernet connections are routed to the rear RJ45 connections.

5.3 Wake-on-LAN

All four Ethernet ports support waking of the system from the S5 low power state upon receiving wake events as configured by the OS before entering the sleep state. Receiving magic packets or change in link-state are the typical wake events supported.

The Wake-on-LAN functionality can be disabled by changing SW4-4 (Wake-on-LAN switch) to the ON position - see Figure 5-1.

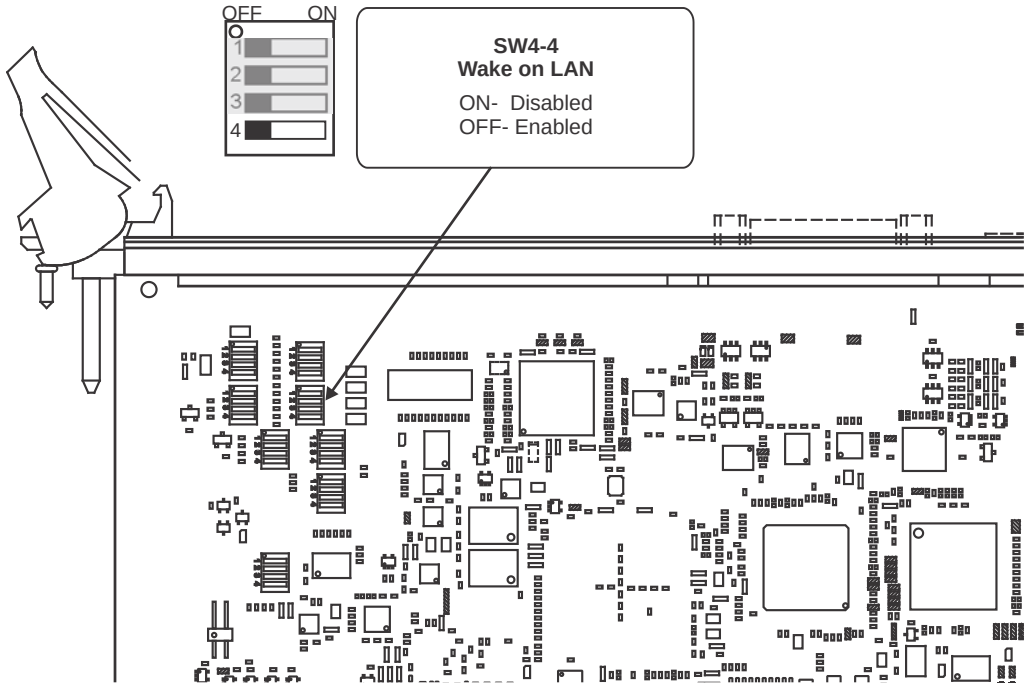

Figure 5-1 Wake-on-LAN Switch

6 VME INTERFACES

The VP E2x/msd board is fitted with an IDT® Universe™ II VME-to-PCI bus bridge device together with additional hardware byte swap logic. This hardware implements a flexible interface to and from the VMEbus with the following key characteristics.

6.1 VMEBus Interface Features

The VP E2x/msd can be programmed as a VME master supporting off-board VME memory addressing accessible by any PCI bus master. It can also be programmed as a VME slave allowing other VME masters to access any PCI bus slave. This access is achieved by programming the appropriate Universe™ II device register. The “PCI slave” registers are used for VP E2x/msd master accesses to the VMEbus and the “VME slave” registers for VMEbus accesses to the VP E2x/msd.

The VME interface supports A32/A24/A16/MBLT addressing modes and D64/D32/D16/D08 (EO) data widths in both user and supervisor address space. The 2eSST and 2eVME modes are not supported.

The VME interface performs auto-syscon detect at power-up to provide System Controller functionality, if the board is located in the first VME slot. As System Controller, the Universe™ II will arbitrate VME mastership of the bus using DEMAND request mode.

The VP E2x/msd can act as an interrupt controller for any combination of VME interrupts and can be an interrupter generating by either a software interrupt or any of the Universe™ II’s internal interrupt sources on any IRQ level. All VME interrupts are directly mapped between the Universe™ II registers and the VMEbus backplane. Of the LINT[7:0] lines, LINT [0] is mapped to PCI Interrupt and LINT1 is mapped to NMI through board logic.

The Universe™ II device uses the linear incrementing mode when being accessed by a PCI master. The Universe™ II supports VME mailbox interrupts. See the Universe™ II data sheet/User Guide for further details.

WARNING:	VMEbus access is allowed to the full VP E2x/msd memory map. Care must be taken to ensure that no accesses are made to areas that will corrupt the system memory or the configuration of any of the interfaces.

The BIOS firmware fitted to this board includes several setup screens which allow up to 2 PCI Slave and VME Slave access windows to be configured. The configuration is retained in Flash EPROM and is programmed automatically into the Universe™ II chip when the board starts up. This allows basic access to or from the VMEbus to be established without the need to write any operating software for the board, or for the Universe™ II chip. For further details, refer to the BIOS setup screens for the VME Bridge **`Vme | Outbound Images`** and **`Vme | Inbound Images`** options.

The VP E2x/msd board will assert the VME SYSFAIL signal after a power-on or system reset. In some cases it may be desirable to deactivate this signal early in the boot process, while in others it can be left to the operating software to do this at a later stage. The SYSFAIL signal is controlled by the Universe™ II chip. The BIOS provides a user setup option to allow this signal to be deactivated by the BIOS itself during its initialization sequence or to simply leave it unchanged after the restart. In the latter case, SYSFAIL will remain asserted until the operating software deactivates it. The setup option is provided on the menu for **`Vme.`**

The VP E2x/msd provides VMEbus error detection and reporting capabilities through board logic.

6.2 VME Byte Swapping

The VP E2x/msd provides hardware that performs fast byte swapping for aligned D16, D32 and D64 VME transfers. Byte swapping, implemented in a CPLD, can be enabled separately for master and slave transfers under software control using Status and Control Register 0 (see Section 9.2.1 for further details). The byte swapping is performed as follows:

D16 (Double Byte 2 - 3):

D[31...24]	< - >	D[23...16]
D[23...16]	< - >	D[31...24]

D16 (Double Byte 0 - 1):

D[15....8]	< - >	D[7.....0]
D[7.....0]	< - >	D[15....8]

D32 (Quad Byte 0 - 3):

D[31...24]	< - >	D[7....0]
D[23...16]	< - >	D[15....8]
D[15....8]	< - >	D[23...16]
D[7.....0]	< - >	D[31...24]

D64 (Octal Byte 0 - 7):

D[63...56]	< - >	D[39...32]
D[55...48]	< - >	D[47...40]
D[47...40]	< - >	D[55...48]
D[39...32]	< - >	D[63...56]
D[31...24]	< - >	D[7……0]
D[23...16]	< - >	D[15.....8]
D[15....8]	< - >	D[23...16]
D[7.....0]	< - >	D[31...24]

The CPLD hardware decodes the VME transfer taking place to see if it is swappable, checks to see if swapping is enabled and then configures a set of multiplexers to perform the required data swap. For master and slave read cycles, the byte swap hardware imposes negligible delay on the VMEbus cycle as the decoding and configuration occurs before the data is valid. For write cycles, the hardware imposes an approximate delay of 50ns in order to provide the required setup time before the data strobes are asserted. The delay applies to single cycle transfers and the first cycle of block transfers.

NOTE: The delay can be turned off under software control, but only if the user can guarantee that only swappable cycles will be run across the VME interface.

NOTE: Byte swapping is only supported for aligned transfers; 64-bit transfers are treated as dual 32-bit transfers. When swapping is enabled, the hardware will normally decode the VME cycle type as it takes place to determine if swapping is possible. It then configures a set of multiplexers to perform the swap. To meet the VMEbus timing spec for write cycles it is necessary to delay the cycle while the multiplexers are configured. Setting bit 5 of this register turns off the delay, but should only be done if all VME cycles are guaranteed swappable.

6.3 VMEBus Error Interrupt

The VP E2x/msd contains hardware to detect bus errors for VMEbus cycles in which the Universe™ II is the bus master. The hardware is controlled by VMEbus Error Capture Control Register (see Section 9.5.1). The bus error interrupt is connected to LINT0 of Universe™ II. The VMEbus error interrupt will be treated like an interrupt generated from Universe™ II. VMEbus address is captured when VMEbus error occurs (Refer to Section 9.5).

6.4 System Resets and Reset Sources

The VP E2x/msd has a number of options, implemented with BIOS setup items and via board switches, for the generation of board resets and responses to them.

The board may be reset from several external sources, as described below. Table 6-1 outlines how board and system resets can be achieved using the available DIP switch options.

Mode	Board Level Reset Sources	System Reset Sources	Section
System Controller (first VMEBus slot)	-VME_SYSRST# signal -EXT_RESET# signal - Front Panel Reset	Same as board level	6.6 6.5.3 6.5.2
Non- System Controller	-VME_SYSRST# signal -EXT_RESET# signal -Front Panel Reset	Same as board level	6.6 6.5.3 6.5.2

Table 6-1 Reset Sources

6.5 Incoming reset

There are three sources of reset accepted by the board:

- VME backplane.
- Front Panel.
- External via the rear P2 connector.

6.5.1 VME Backplane Reset

The VME backplane resets are signaled on the VME_SYSRST# pin and arrive to the Universe™ II controller through board logic. This reset source can be disabled by the VME Reset IN Enable bit in Status and Control Register 2 as described in Section 9.2.3.

6.5.2 Board/System Reset or Board NMI

The VP E2x/msd can be configured for either a board/system reset or for a processor Non-Maskable Interrupt (NMI) using SW4-1 (Push Button/LK1 Header switch, see Figure 6-2). The Push Button (front panel, Figure 2-3) is only available on VP E2x/4sd-yz variants supporting a single PMC/XMC site. The LK1 Header is available on all the variants.

NOTE: A shorting stub needs to be used on LK1 Header to generate reset / NMI (See Figure 6-1 for the position of LK1 Header)

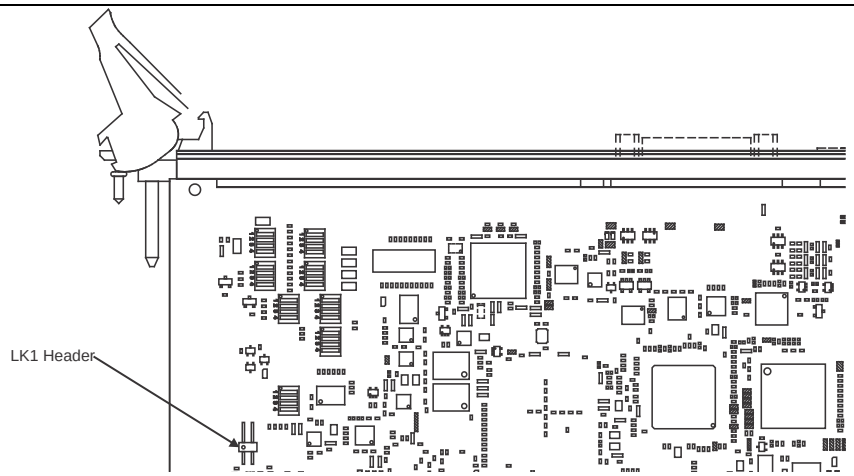

Figure 6-1 LK1 Header

When the Push Button/LK1 Header switch is in the "RESET" position, momentarily operating the Push Button or shorting LK1 Header causes a reset to be generated locally on the board. This reset action may also be propagated to the VME backplane via the VME_SYSRST# signal depending on the setting of SW7-3 (VME Reset switch, see Figure 6-2).

When the Push Button/LK1 Header switch is in the "NMI" position, momentarily operating the Push Button or shorting of LK1 Header causes an NMI to the local SoC.

The VME Reset switch enables or disables both the reset action of the front panel Push Button/ LK1 Header and the Watchdog Timer expiry event (see Section 9.6) from activating the VMEbus reset signal VME_SYSRST#. When the VME Reset switch is in the "Disabled" position, the Push Button reset/LK1 Header and Watchdog Timer expiry reset will only act locally on the board. When the VME Reset switch is in the "Enabled" position, both the Push Button/LK1 Header reset and Watchdog Timer expiry reset will cause a VMEbus reset via the VME_SYSRST# signal (see Section 6.4). Regardless of the setting of the VME Reset switch, the board will always generate a VMEbus reset both from power up and when the Universe™ II chip has been programmed to do this. The VME Reset switch status may be read from DIP Switch Status Register 1 (see Section 9.3.4).

The board's response to VME_SYSRST# being activated by another board is also configurable through **`Vme | VME System Reset`** BIOS setup option. It is used to allow or prevent the backplane VME_SYSRST# signal causing a reset to the board.

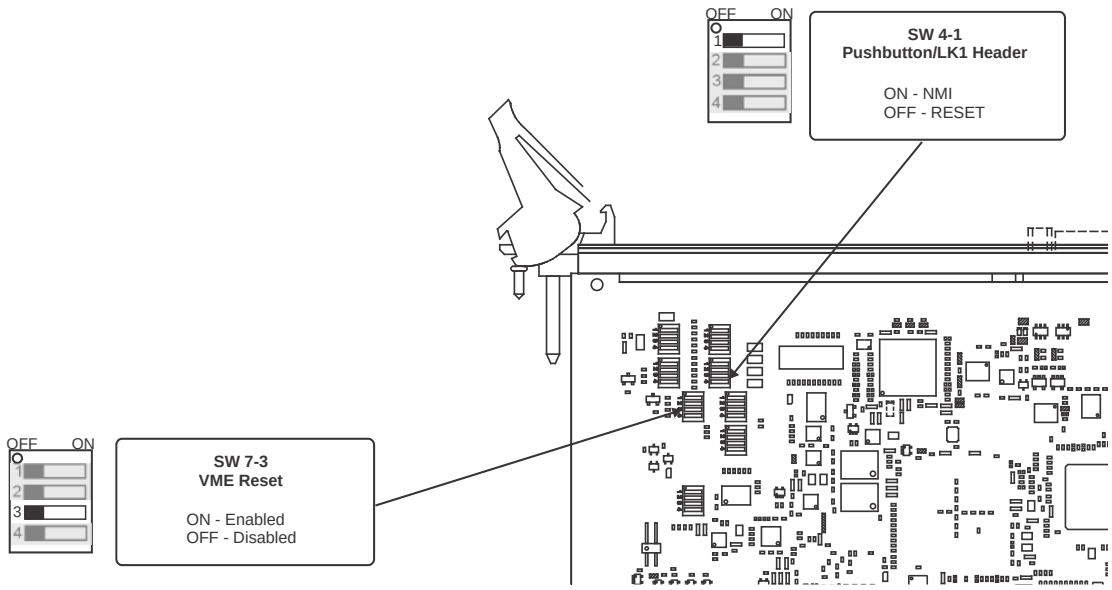

Figure 6-2 Push Button/LK1 Header Configuration Switches

6.5.3 EXT_RESET# signal

The reset generated by external hardware can be signaled via the rear P2 connector pin D27, the EXT_RESET# pin. Setting this pin to a logical '0' will activate the reset. This reset source may be disabled using SW2-4 (EXT_RST Enable) as shown in Figure 6-3. The AD VP2/020 and AD VP2/033 RTMs provide a Push Button switch to generate this signal and it is also available via a header for external wiring on the AD VP2/020 RTM.

6.6 Locally-generated reset sources

The board generates VME backplane resets via the Universe™ II. These resets are triggered whenever the Universe™ II is reset by a local power cycle event (including at power-up), when the front panel Push Button/shorting of LK1 Header generates a reset, when an external reset is asserted via P2 or when the Watchdog Timer expires. If the VP E2x/msd is the VMEbus System Controller, the Universe™ II can be programmed to generate a VMEbus reset as a result of a warm boot of the board, via Status & Control Register 1 (see Section 9.2.2). It is possible to disable the outgoing VME backplane reset by configuring the VME Reset switch to the “Disabled” position. The power-up reset always generates a backplane reset.

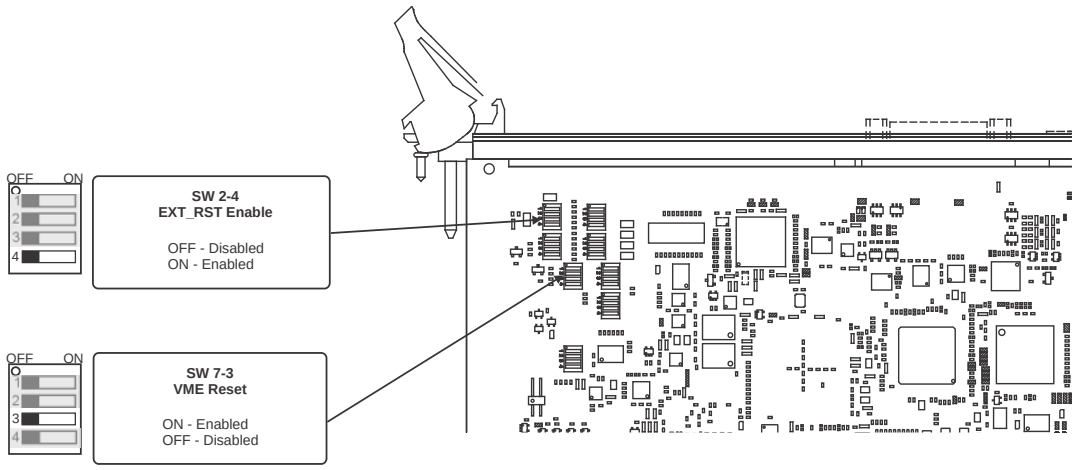

Figure 6-3 Reset Control Switches

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7 OTHER INTERFACES

Many additional standard interfaces are provided on the VP E2x/msd. These interfaces consist primarily of those found in a regular desktop or mobile PC and they are outlined below.

7.1 Serial Ports

The VP E2x/msd provides up to three serial data communication ports depending on the boards build option.

The serial port COM1 is connected via the rear P2 connector, and can support RS232, RS422 and RS485 operating modes.

The serial port COM2 is accessed via a front panel RJ45 connector, and operates only in RS232 mode. An adapter cable, such as the Concurrent Technologies CB 232/121-01, may be used to convert the RJ45 connector to a D-type connector of the appropriate size and gender.

The serial port COM3 is connected via the rear P2 connector, and operates only in RS232 mode. This is a factory build option. See Table 1-4.

The serial ports (COM1, COM2 and COM3) are implemented as 16550-style UARTs in board logic. COM1, COM2 and COM3 have I/O addresses of 0x03F8, 0x02F8 and 0x03E8 respectively.

The serial ports may be configured for speeds up to 115.2 kbaud. The board supports options to configure a serial port as the console for the PC BIOS firmware, and these options may be selected using DIP switches as described below.

7.1.1 Serial Console Mode Selection

With some operating systems, or in some applications, it is preferable to use a serial terminal as an operator console device for the board. In this case, it will be necessary to configure the board for operation with a serial console so that the PC BIOS firmware will direct its output to a COM port, and similarly will take its input from this port rather than using the video screen and PC keyboard. This configuration can be selected using SW8-1 (Console Mode switch) as shown in Figure 7-1.

NOTE: DVI-D is supported as a console port for all variants of the board (DVI-I is not available for all variants).

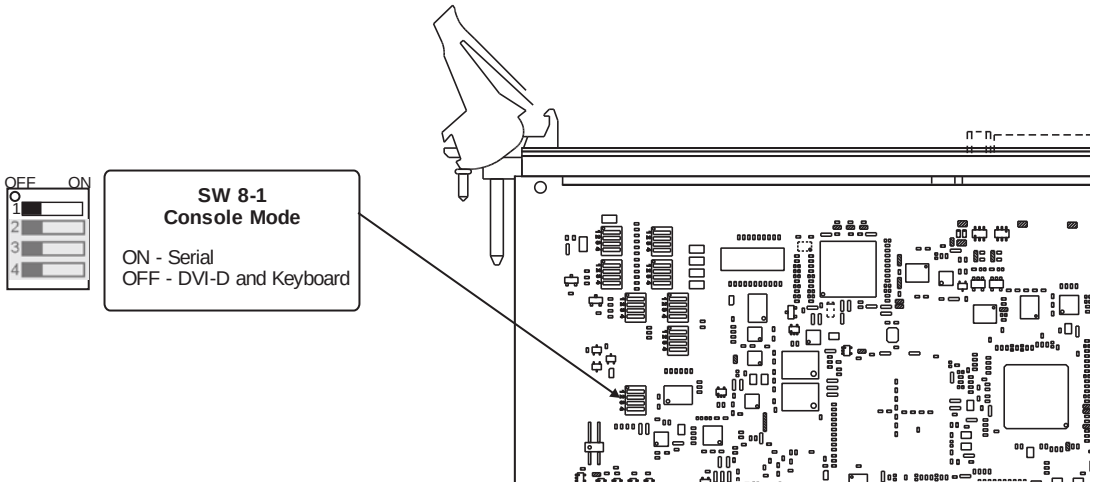
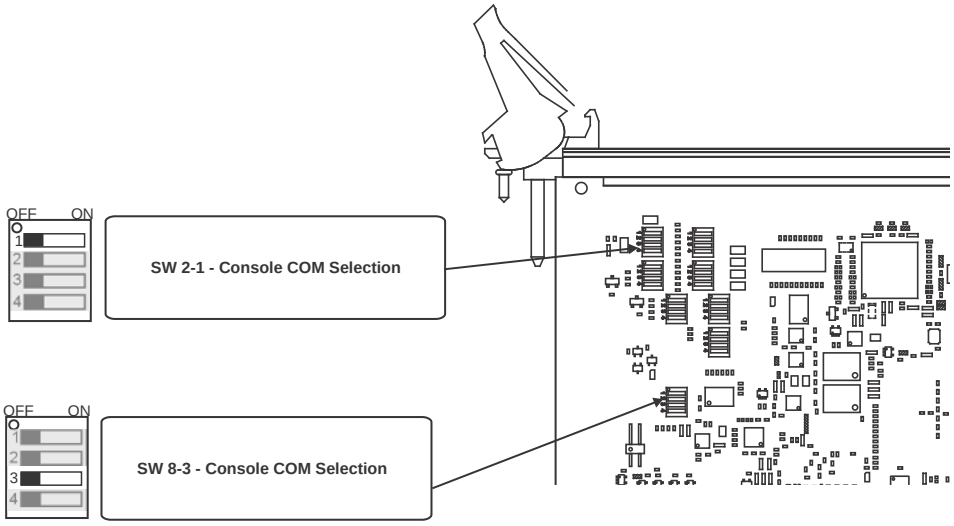


Figure 7-1 Console Mode Switch

7.1.1.1 Serial Console Port Configuration

When the Console Mode switch is set to “Serial”, any of the three serial ports may be used for the serial console as selected by SW8-3 and SW2-1 (Console COM Selection switches) as shown in Figure 7-2.



SW 8-3 Selection	SW 2-1 Selection	Result
OFF	OFF	COM2
ON	OFF	COM1
OFF	ON	Reserved
ON	ON	Reserved

Figure 7-2 Console Port Select

7.1.2 COM1 RS232 or RS422/485 Configuration

The Serial I/O Configuration Register (see Section 9.2.6) is used to configure the COM1 serial I/O port for operation at RS232 or RS422/485 signal levels. The PC BIOS configures the interface after power-on as determined by the setup options in **`Advanced | Peripheral Configuration`**. This will automatically enable the port drivers.

3	2	0	Register Bits
RS232/485	Duplex	Slew Rate	Configuration Selected
0	0	0	Interface Disabled
0	X	1	RS232 full duplex mode (standard interface)
1	0	0	RS485 full duplex, RTS = Tx enable, Slew = Slow
1	0	1	RS485 full duplex, RTS = Tx enable, Slew = Fast
1	1	0	RS485 half-duplex, RTS = Tx enable, slew = Slow
1	1	1	RS485 half-duplex, RTS = Tx enable, slew = Fast

Table 7-1 Serial I/O Interface Mode Settings

The COM1 port may also be configured for half or full duplex operation and, in RS422/RS485 mode, may be programmed for Slow or Fast signal slew rates. The supported operating modes, combining these options, are summarized as follows:

- RS232 full duplex mode is selected by the BIOS for initial configuration after power on, or when no specific configuration has previously been set up. The BIOS serial console mode does not support half duplex modes and it is advisable not to select these modes. The user application code can set up the required mode later via the Serial I/O Configuration Register.
- RS485 full duplex modes are for operation over two twisted pairs and can be used in RS485 and RS422 systems.
- RS485 half-duplex modes are for operation over a single twisted pair. The half-duplex modes use only the COM1_Tx/TX- and COM1_RTS/TX+ signals on P2. The transmitted data is also looped back to the receiver. The board has a provision to enable the termination on the RS485 transmit or receive data lines through DIP switches (see Section 7.1.2.1).

In RS485 half-duplex mode, no hardware flow control is available. Slew rate is only valid in RS485 mode and slow slew rate allows operation without termination resistors at low data rates only.

For RS485 full and half duplex mode the RTS or DTR signals control the transmit enable. There are BIOS options **`Advanced | Peripheral Configuration | Direction Control`** to select the transmit control configuration by using RTS or DTR signal.

CAUTION: When changing the configuration of the serial ports from RS232 to RS485 mode (or vice versa), or setting the ports up for the first time, it is recommended that the interfaces are disconnected to prevent any damage to connected equipment.

7.1.2.1 COM1 RS485 Termination

A series resistor can be configured in the return signal line if COM1 is configured for RS485 mode and is connected to a chassis with different GND potentials, by use of SW6-1 and SW6-2 (Ground Return switches). See Figure 7-3 for the location and settings of these switches.

> **NOTE:** Switches SW6-1 and SW6-2 need to be closed or opened together for ground return terminations.

In RS485 mode, Rx path parallel terminations for COM1 can be enabled by SW2-2. See Figure 7-3 for the location and settings of this switch.

> **NOTE:** Terminations should normally be enabled for RS485 mode, but when a slow slew rate is configured and the line speed is low, it may be possible to operate with terminations disabled.

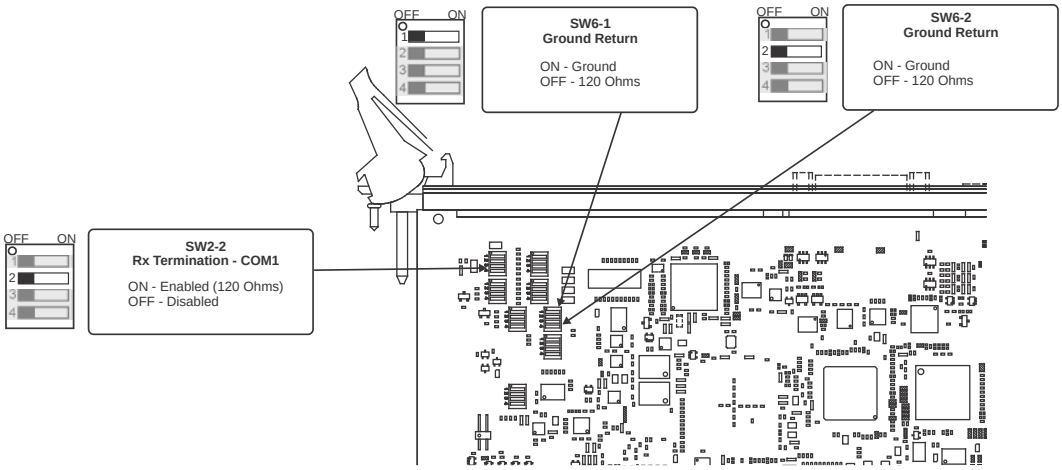


Figure 7-3 Serial Ports Terminations

7.2 PS/2 Keyboard and Mouse Ports

NOTE: This option is available only with VP A45/01x compatible (VP E2x/0sd-11 or VP E2x/0sd-21) rear I/O variants. This is a factory build option. See Table 1-4 for more information.

PS/2 PC keyboard and mouse interfaces are available via the VME P2 connector (pin-out detailed in Section A.9).

The power for the keyboard and mouse interfaces is protected by a self-resetting current limiting circuit. To reset, power the board off, remove and replace the faulty keyboard or mouse device, then power up again.

NOTE: External devices that derive power from the keyboard/mouse interface may be used provided that the total current taken by all devices is less than 500mA.

7.3 Graphics Controller

The SoC supports an internal graphics controller, providing one DVI-D video interface via the VME P2 connector and an optional DVI-I interface on the front panel. The controller uses main memory for the video buffers, the allocated amount being dependent upon interface configurations and display modes.

The graphics controller uses main memory for graphics RAM and supports many different modes of operation including DVI-I and DVI-D with resolutions up to 1600 x 1200 @ 60Hz for DVI-D and up to 2048x1536 at 60 Hz for VGA. It also provides 2D and 3D acceleration features.

On VP E2x/4sd Single XMC site variants, the front panel DVI-I interface comprises of both DVI-D and VGA interfaces on a single connector. Both VGA and DVI-D signals are available, but not simultaneously. This is a factory build option. See Table 1-4 for more information.

7.4 Real Time Clock

A conventional PC Real Time Clock (RTC) is included on the VP E2x/msd. This clock is powered by an external auxiliary power supply or an on-board battery, as described in Section 2.3.

The RTC internal registers and RAM are organized as two banks of 128 bytes each, called the standard and extended banks. The first 14 bytes of the standard bank contain the RTC time and date information along with four registers, A to D, that are used for configuration of the RTC. The extended bank contains a full 128 bytes of SRAM.

7.5 Universal Serial Bus

The VP E2x/msd provides up to four USB interfaces with the following configurations:

- 1 x USB 3.0/2.0 interface via the front panel USB 3.0 connector, supporting USB 1.1 (1.5 Mbps and 12 Mbps), USB 2.0 (480 Mbps) and USB 3.0 (5 Gbps).
- 2 x USB 2.0 interfaces via VME P2 connector supporting both USB 1.1 (1.5 Mbps and 12 Mbps) and USB 2.0 (480 Mbps)
- 1 x USB 2.0 interface via the front panel connector supporting both USB 1.1 (1.5 Mbps and 12 Mbps) and USB 2.0 (480 Mbps). This USB 2.0 connector is only available in VP E2x/msd variants that support a single PMC/XMC site. This is a factory build option. See Table 1-4 for more information.

Table 7-2 and Table 7-3 detail how the SoC's USB ports are mapped through to the connectors on the VP E2x/msd front panel connector and the optional Rear Transition Modules.

VP E2x/msd Internal Port	Hardware Port (from the SoC)
USBA	USB 2.0 port 0
USBB	USB 2.0 port 1
USBC	USB 2.0 port 2
USBD	USB 2.0 port 3
USBE	USB 3.0 port 0

Table 7-2 Internal USB Port Mapping

VP E2x/msd		AD VP2/020		AD VP2/033	
USB1 Front Panel	**USB0 Front Panel (Optional)**	**USB0 Front Panel**	**USB1 Front Panel**	**USB0 Front Panel**	**USB1 Front Panel**
USB 2.0	USB 2.0	USB 2.0	USB 2.0	USB 2.0	USB 2.0
USB 3.0	-	-	-	-	-
USBA_D±	-	-	-	-	-
-	USBB_D±	-	-	-	-
-	-	USBC_D±	-	USBC_D±	-
-	-	-	USBD_D±	-	USBD_D±
USBE_Tx±, USBE_Rx±	-	-	-	-	-
OC0 Pin	OC0 Pin	OC1 Pin	OC1 Pin	OC1 Pin	OC1 Pin

Table 7-3 USB Interface Signal to Panel Connector Mapping

Table 7-3 also identifies the internal USB over-current signal pin (OC pin) of the SoC that is used for each interface.

NOTE: Due to the design of the Intel® Atom™ processor E3800 product family, two or more internal ports share the same OC (over-current) pin, which means that an over-current indication on any of the ports connected to that pin will be reported as an over-current indication for all of those ports.

7.6 Power On Self Test LED / Speaker

The Power On Self Test (POST) LED is connected to the SoC speaker port. The speaker port is also connected to the Audio Codec.

7.7 High Definition (HD) Audio

The VP E2x/msd provides Analog Line-In and Line-Out via the VME P2 connector. An on-board high definition audio codec (IDT® 92HD81) in the VP E2x/msd provides the analog audio interfaces.

The AD VP2/033 RTM provides audio connectors to access the analog Line-in and Line-out interfaces.

The HD Audio interface is a factory build option. See Table 1-4 for more information.

CAUTION: The HD Audio interface is not available on the variants that are compatible with the VP A45/01x rear I/O pin-outs. For details on VP A45/01x compatibility, please refer to Section 1.5.

7.8 Trusted Platform Module (TPM)

The Trusted Platform Module (TPM) is an additional hardware system which can be ordered as a factory build option for the board. It provides a secure repository for a variety of items which can be used to authenticate the product, its operating software or the system containing it. It may also be used to store measurements to be used to ensure that the product, or the platform, remains trustworthy. The TPM can be used with the Concurrent Technologies Board Level Security Package to enhance the overall security of the platform. Consult Concurrent Technologies directly for more information about the security options for this board.

NOTE: The TPM hardware incorporates encryption technologies which may be subject to export restrictions.

7.9 General Purpose I/O

There are four configurable GPIO signals available at the VME P2 connector. When configured as inputs, they can also be used to interrupt the CPU. Their function is software controlled via the General Purpose I/O register. Refer to Section 9.2.5 for more details. The GPIOs are 5V tolerant.

8 FLASH EPROM AND DRAM

8.1 BIOS Flash EPROM

The VP E2x/msd is fitted with two 8 Mbyte SPI Serial EPROM Flash devices. These devices are soldered to the board and are programmed at the factory with BIOS and factory test firmware. One device is the primary boot device and the other is the secondary boot device, used if the primary device becomes corrupted. The SPI Flash Select switch (SW5-4) controls the selection of the boot device as shown in Figure 8-1.

The Flash EPROM devices are not normally reprogrammed by the user, but Concurrent Technologies has programming software which allows BIOS updates to be carried out in the field when necessary.

A Recovery BIOS is programmed into the device at the factory, which allows the board to be restarted in a basic functional mode, even if the main BIOS firmware in both devices becomes corrupted. See Section 10.6 for further details of this feature.

Concurrent Technologies also use the devices to store factory test firmware. If necessary, the factory test firmware can be overwritten by the user, but it may be re-instated if the board is returned to Concurrent Technologies for repair or upgrade.

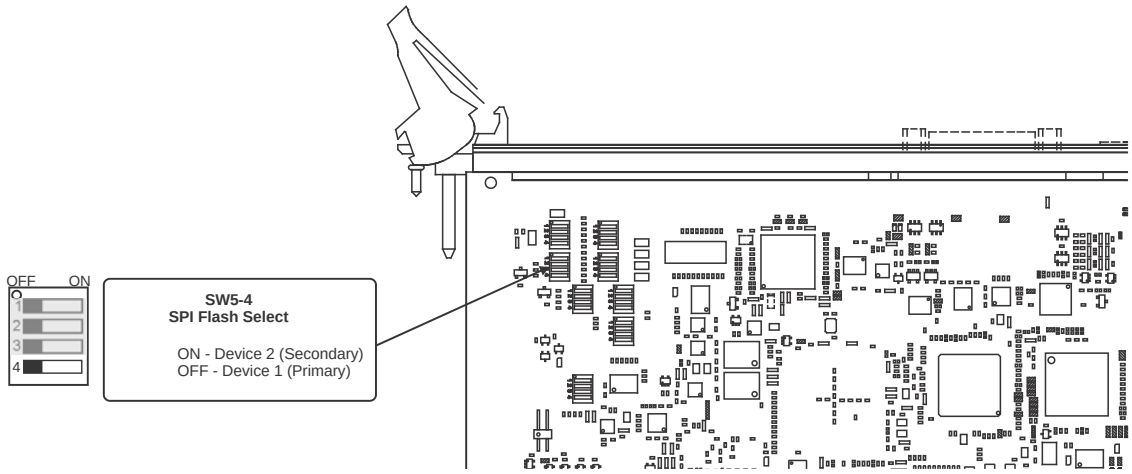


Figure 8-1 SPI Flash Select Switch

8.2 DRAM

The SoC DRAM controller supports 64-bit DDR3L memory configured for either dual or single channel operation. The DDR3L memory chips are soldered on-board and operate at 1.35V. Factory build options are available for up to 8 Gbytes dual channel without ECC (4-core processor only) or 4 Gbytes single channel with ECC.

The DRAM can be accessed from the processor, the local PCI busses and the VME backplane.

NOTE: The DDR3L data transfer rate for the 1-core CPU is limited to 1066 million 64-bit data transfers per second to provide a peak transfer bandwidth of 8.528 Gbytes/s (single channel). The 4-core processor operates up to 1333 million 64-bit data transfers per second to provide a peak transfer bandwidth up to 21.2 Gbytes/s (dual channel) and up to 10.6 Gbytes/s (single channel).

NOTE: There is no support for DIMM or SODIMM modules.

8.3 Serial EEPROMs

The VP E2x/msd has four serial EEPROM parts. Two EEPROMs are programmed at the factory with the configuration data for the i350-AM4 Ethernet controller and the PCIe-to-SATA controller. These devices must not be modified by the application software.

A user EEPROM of 8 Kbytes in size is available to the user to store data (for example VxWorks® boot configuration parameters).

To support the optional Intel® Fast boot feature (see Section 1.4.5), another 8 Kbytes EEPROM is also available on-board.

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9 ADDITIONAL LOCAL I/O FUNCTIONS

The VP E2x/msd supports a variety of I/O functions. The I/O addresses of the ports controlling these functions are summarized in Table 9-1.

I/O Address Range	Description
0x0020-0x002D	Interrupt Controller (SoC)
0x002E-0x002F	Configuration Index & Data Registers (Super I/O)
0x0030-0x003D	Interrupt Controller (SoC)
0x0040-0x0043	8254 Timers (SoC)
0x0050-0x0053	8254 Timers (SoC)
0x0060	PS/2 Controller (Super I/O)
0x0061,0x0063, 0x0065,0x0067	NMI Controller (SoC)
0x0064	PS/2 Controller (Super I/O)
0x0070-0x0077	RTC Data (SoC)
0x00800x0083	Port 80 Debug Port
0x0092	Port 92 Init Register (SoC)
0x00A0-0x 00A1	8259 Slave Interrupt Controller (SoC)
0x00F0	Math Coprocessor Error
0x0210-0x024F	Control & Status Registers, Long Duration Timer (Board Logic)
0x02F8-0x02FF	COM2 Serial (Board Logic)
0x0310-0x031F	GPIO and Serial I/O Configuration Registers (Board Logic)
0x0320-0x0325	VMEbus Error Address Capture Registers
0x03E8-0x03EF	COM3 Serial (Board Logic)
0x03F8-0x03FF	COM1 Serial (Board Logic)
0x04D0-0x04D1	Interrupt Control (SoC)
0x0CA0-0x0CAF	SMIC Interface (Microcontroller)
0x0CF9	Reset control Registers (SoC)
0x0D00-0xFFFF	PCI Free I/O Space

Table 9-1 I/O Address Map

Most of the addresses are standard PC-AT compatible values, but at addresses 0x0210 to 0x024F and 0x0310 to 0x031F, the board provides custom Status & Control Registers for the board specific features.

ADDITIONAL LOCAL IO FUNCTIONS

9.1 Onboard Status & Control Registers

The VP E2x/msd provides a number of onboard status and control registers, some of which are mapped out for compatibility with the VP A45/01x, and others specifically for the VP E2x/msd.

The onboard status and control registers compatible with the VP A45/01x are accessed at the following I/O addresses (see Section 9.1, Section 9.6 and Section 9.7 for more details):

- 0x0210 for Status & Control Register 0
- 0x0211 for Status & Control Register 2
- 0x0212 for Status & Control Register 1
- 0x0214 for Watchdog (board logic) Status & Control Register
- 0x0218 for Long Duration Timer / Periodic Interrupt Timer Low Byte
- 0x0219 for Long Duration Timer / Periodic Interrupt Timer Mid-low Byte
- 0x021A for Long Duration Timer Mid-High Byte
- 0x021B for Long Duration Timer High Byte
- 0x021C for Long Duration Timer / Periodic Interrupt Timer Status & Control Register
- 0x021D for Status & Control Register 3
- 0x031C for GPIO Status and Control Register
- 0x031D for Serial I/O Configuration Register
- 0x031E for VME Slot ID Register

The VP E2x/msd specific registers are accessed at the following I/O addresses (see Section 9.3 for more information):

- 0x0220 for Hardware Version Register
- 0x0221 for Scratch Pad (Software Controlled) Register 1
- 0x0222 for Scratch Pad (Software Controlled) Register 2
- 0x0223 for DIP Switch Status Register 1
- 0x0224 for DIP Switch Status Register 2
- 0x0225 for DIP Switch Status Register 3
- 0x0228 for Scratch Pad (Software Controlled) Register 3
- 0x0229 for Interrupt Control Register
- 0x022A for Status and Control Register 4
- 0x022B for Status and Control Register 5
- 0x31A for GPIO IRQ Control Register 0 and Register 1
- 0x31B for GPIO IRQ Control Register 0 and Register 1
- 0x0320 for VMEbus Error Address Capture Control Register
- 0x0321 for VMEbus Error Address Capture Register 1
- 0x0322 for VMEbus Error Address Capture Register 2
- 0x0323 for VMEbus Error Address Capture Register 3
- 0x0324 for VMEbus Error Address Capture Register 4
- 0x0325 for VMEbus Error Address Capture Register 5

The VP E2x/msd also includes registers used to communicate with the optional microcontroller fitted to some variants of the board. These SMIC registers are accessed at the following I/O addresses (see Section 9.4 for more information):

- 0x0CA9 for SMIC Data Register
- 0x0CAA for SMIC Control/Status Register
- 0x0CAB for SMIC Flags Register

The Watchdog Timer and Long Duration Timer are described in Section 9.6 and Section 9.7.

The following abbreviations are used in the next sections to describe the attributes of the register bit settings:

RO – Read Only
RW – Read / Write
RC – Read / Clear (writing 0 to this bit clears it to 0; writing 1 leaves it unchanged.)
RS – Read / Set (writing 0 to this bit leaves it unchanged; writing 1 sets it to 1)

WARNING: RFU (Reserved for Future Use) bits should be left unchanged when written, and their values should be ignored when read.

9.2 VP A45/01x Compatible Registers

9.2.1 Status & Control Register 0

Register		**Status & Control Register 0**	
Address		**0x0210**	
Bit	Type	Name	Description
7	RO	**CONSOLE SELECT**	Console Mode switch. Indicates the setting of SW8-1 (Console Mode switch) which defines the BIOS default standard input/output mode. See Section 7.1.1 for more details. 0 = input via keyboard/output via DVI-D 1 = input/output via selected Serial port
6	RO	**BIOS DEFAULTS**	BIOS Defaults switch. Indicates the setting of SW7-2 (Force Optimal Defaults switch). It is used to define which configuration is restored to the BIOS setup settings should they become corrupt or are cleared. See Section 10.5 for more details. 0 = restore optimal defaults 1 = restore user defaults
5	RW	**BYTE SWAP MODE – FAST SWAP**	VME hardware byte swapping - fast byte swapping, i.e. partial cycle type decode 0 = Disabled (default) 1 = Enabled
4		**BYTE SWAP MODE – SLAVE SWAP**	VME hardware byte swapping - swapping for slave. 0 = Disabled (default) 1 = Enabled
3		**BYTE SWAP MODE – MASTER SWAP**	VME hardware byte swapping - swapping for master. 0 = Disabled (default) 1 = Enabled
[2:0]	RO	**HARDWARE PCB REVISION**	PCB Revision 000 = Rev A, 001 = Rev B, 010 = Rev C ….

NOTE: Byte swapping is only supported for aligned transfers; 64-bit transfers are treated as dual 32-bit transfers. When swapping is enabled, the hardware will normally decode the VME cycle type as it takes place to determine if swapping is possible. It then configures a set of multiplexers to perform the swap. To meet the VMEbus timing spec for write cycles it is necessary to delay the cycle while the multiplexers are configured. Setting bit 5 of this register turns off the delay, but should only be done if all VME cycles are guaranteed swappable. See Section 6.2 for more details.

9.2.2 Status & Control Register 1

Register		**Status & Control Register 1**	
Address		**0x0212**	
Bit	Type	Name	Description
7	RC	**NMI EVENT (FROM PB SWITCH)**	This bit indicates the status of Push Button (PB)/LK1 Header switch when it is configured for NMI generation. 0 = NMI event has not occurred. 1 = NMI event has occurred.
6	RO	**RFU**	Reserved.
5	RO	**RFU**	Reserved
4	RW	**WARM BOOT ENABLE**	This bit controls the warm boot enable to peripheral boards. 0 = System controller's warm boot is not shared to Peripheral boards. 1 = System controller's warm boot is shared to Peripheral boards through VME_SYSRST# signal.
3	RO	**PMC2 EREADY**	This bit indicates if PMC Module on site 2 is ready for PCI enumeration. 0 = PMC2 module is not ready for enumeration 1 = PMC2 module is ready for enumeration.
2	RO	**PMC2 PRESENT**	This bit shows the status of PMC2 presence. 0 = PMC2 is not present 1 = PMC2 is present
1	RO	**PMC1 EREADY**	This bit indicates if PMC Module on site 1 is ready for PCI enumeration. 0 = PMC1 module is not ready for enumeration 1 = PMC1 module is ready for enumeration.
0	RO	**PMC1 PRESENT**	This bit shows the status of PMC1 presence. 0 = PMC1 is not present. 1 = PMC1 is present.

9.2.3 Status & Control Register 2

Register		**Status & Control Register 2**	
Address		**0x0211**	
Bit	Type	Name	Description
7	RO	**BOOT MODE**	Boot Mode. This indicates the setting of SW8-2 (Boot Mode switch) which defines the operating mode following a reset. See Section 10.1 for more details. 0 = CUTE 1 = BIOS operation (default)
6	RO	**TEST MODE SELECT SWITCH**	User/Test switch. This indicates the setting of SW8-4 (User/Test switch) as shown in Figure 9-1. When the board is configured for BIOS mode operation (see Bit 7), this switch can be used for any application-defined purpose. 0 = switch is OFF(default) 1 = switch is ON
5	RW	**VME RESET IN ENABLE**	This controls the effect of the VME_SYSRST# input from the VMEbus. 0 = incoming System Reset is disabled (default). 1 = incoming System Reset is enabled.
4	RO	**XMC2 NOT READY**	This is used to report if an XMC module on site 2 is not ready for PCI enumeration. If an XMC module is fitted, the BIOS will normally wait until this bit clears before completing its boot sequence. 0 = XMC2 module is not ready for enumeration. 1 = XMC2 module is ready for enumeration.
3	RO	**XMC1 NOT READY**	This is used to report if an XMC module on site 1 is not ready for PCI enumeration. If an XMC module is fitted the BIOS will normally wait until this bit clears before completing its boot sequence. 0 = XMC1 module is not ready for enumeration. 1 = XMC1 module is ready for enumeration.
2	RO	**XMC1 PRESENT**	This is used to report the presence of an XMC module in site 1. 0 = module not fitted. 1 = module fitted.
1	RO	**XMC2 PRESENT**	This is used to report the presence of an XMC module in site 2. 0 = module not fitted. 1 = module fitted.
0	RO	**PMC PCI MODE CLOCK FREQUENCY (PMC_M66EN)**	This bit indicates the PMC PCI Clock frequency (i.e. status of M66EN signal of PCI). 0 = 25/33/MHz 1 = 50/66/ MHz (default)

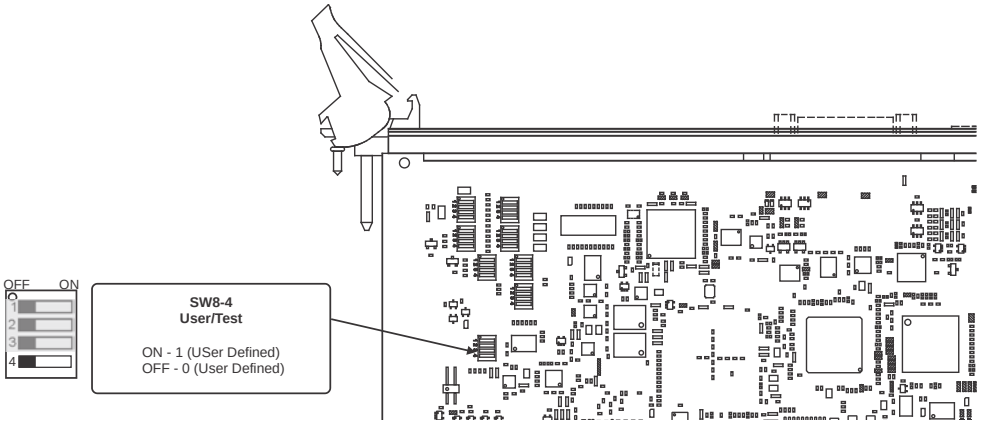

Figure 9-1 User/Test Switch

9.2.4 Status & Control Register 3

Register		**Status & Control Register 3**	
Address		**0x021D**	
Bit	Type	Name	Description
7	RO	**RFU**	Reserved
6	RO	**RFU**	Reserved
5	RO	**RFU**	Reserved
4	RO	**RFU**	Reserved
3	RO	**RFU**	Reserved
2	RO	**RFU**	Reserved
1	RO	**RFU**	Reserved
0	RW	**USER LED**	This bit controls the User LED output when the User LED function switch is in the User position. When DIP switch is in the PROCHOT position, this bit will have no effect on the User LED. 0 = turn off User LED 1 = turn on User LED.

9.2.5 GPIO Status and Control Registers

Four general purpose I/O (GPIO) signal lines are provided on this board. All the lines are also connected to individual on-board switches and pull-up resistors. Each line also has a direction control (bits 7-4 of this register), allowing them to be individually specified as inputs or outputs. Following power ON or board reset, all the GPIO signals are configured as inputs by default.

If a GPIO line is configured as an input, it can either report the switch setting or the external signal status. To allow the external signal status to be reported, the appropriate switch (see Figure 9-2) must be set OFF. To allow the switch status to be reported, the external signal must not be connected. In this case, status bits 3 to 0 of this register are decoded as follows:

0 = switch is ON
1 = switch is OFF

Register		**GPIO Status & Control Register**	
Address		**0x031C**	
Bit	Type	Name	Description
7	RW	**GPIO3 _DIR**	These bits control the direction of the GPIOs. 0 = Input (default) 1 = Output
6	RW	**GPIO2 _DIR**	
5	RW	**GPIO1 _DIR**	
4	RW	**GPIO0 _DIR**	
3	RW	**GPIO3 _Data**	Data written to these bits will be output on the GPIO pins when the direction is set for output. Data read back from these bits will be the data present on the GPIO pins when the direction is set for input
2	RW	**GPIO2 _Data**	
1	RW	**GPIO1 _Data**	
0	RW	**GPIO0 _Data**	

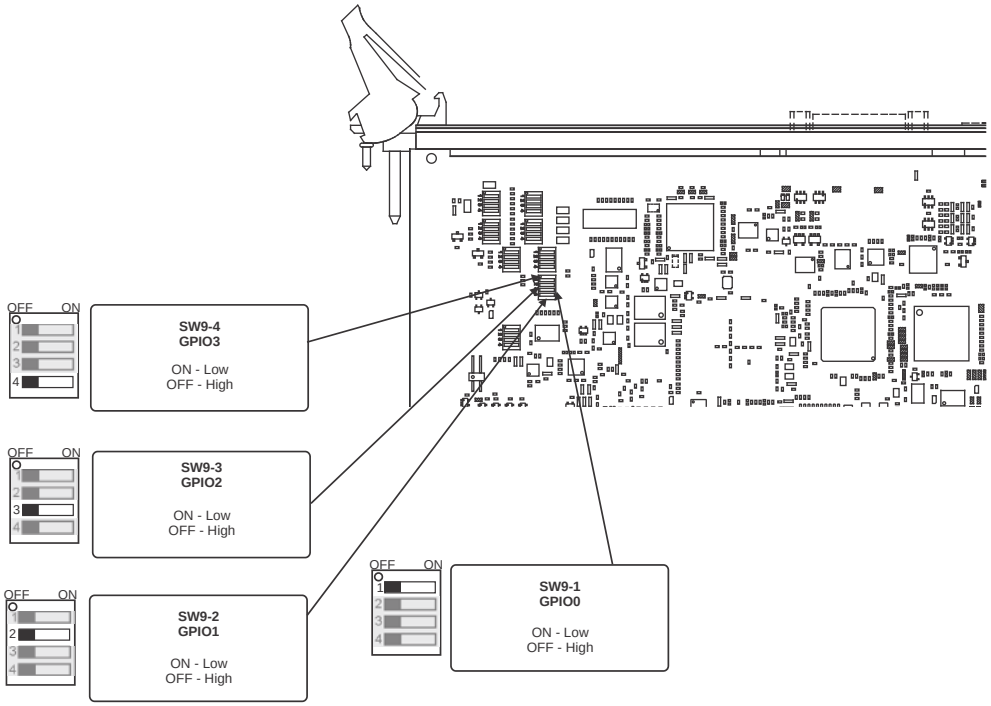

Figure 9-2 General Purpose Input/Output Switches

NOTE: To allow the external signal status to be reported by the GPIOx DATA status bits, the appropriate switch must be set to OFF.

9.2.5.1 GPIO IRQ Control Register 0 and Register 1

On the VP E2x/msd, all four GPIO signals support interrupt generation based on a level change or edge change. Refer to the register descriptions below for more detail on GPIO IRQ.

Register	**GPIO IRQ Control Register 0**		
Address	**0x031A**		
Bit	**Type**	**Name**	**Description**
7	RW	**GPIO1 IRQ ENABLE**	GPIO1 IRQ Enable 0 = Disable (Default) 1 = Enable
6	RW	**GPIO0 IRQ ENABLE**	GPIO0 IRQ Enable 0 = Disable (Default) 1 = Enable
5	RW	**GPIO1 IRQ MODE**	GPIO1 IRQ Mode 0 = Positive edge (Default) 1 = Negative edge
4	RW	**GPIO0 IRQ MODE**	GPIO0 IRQ Mode 0 = Positive edge (Default) 1 = Negative edge
3	RW	**GPIO1 IRQ TYPE**	GPIO1 IRQ Type 0 = Edge based (Default) 1 = Level based
2	RW	**GPIO0 IRQ TYPE**	GPIO0 IRQ Type 0 = Edge based (Default) 1 = Level based
1	R/CLR	**GPIO1 IRQ FLAG**	GPIO1 IRQ Flag 0 = Not detected 1 = Detected
0	R/CLR	**GPIO0 IRQ FLAG**	GPIO0 IRQ Flag 0 = Not detected 1 = Detected

Register	**GPIO IRQ Control Register 1**		
Address	**0x031B**		
Bit	**Type**	**Name**	**Description**
7	RW	**GPIO3 IRQ ENABLE**	GPIO3 IRQ Enable 0 = Disable (Default) 1 = Enable
6	RW	**GPIO2 IRQ ENABLE**	GPIO2 IRQ Enable 0 = Disable (Default) 1 = Enable
5	RW	**GPIO3 IRQ MODE**	GPIO3 IRQ Mode 0 = Positive edge (Default) 1 = Negative edge
4	RW	**GPIO2 IRQ MODE**	GPIO2 IRQ Mode 0 = Positive edge (Default) 1 = Negative edge
3	RW	**GPIO3 IRQ TYPE**	GPIO3 IRQ Type 0 = Edge based (Default) 1 = Level based
2	RW	**GPIO2 IRQ TYPE**	GPIO2 IRQ Type 0 = Edge based (Default) 1 = Level based
1	R/CLR	**GPIO3 IRQ FLAG**	GPIO3 IRQ Flag 0 = Not detected 1 = Detected
0	R/CLR	**GPIO2 IRQ FLAG**	GPIO2 IRQ Flag 0 = Not detected 1 = Detected

9.2.6 Serial I/O Configuration Register

Register		**Serial IO configuration Register**	
Address		**0x031D**	
Bit	Type	Name	Description
7	RO	**RFU**	Reserved
6	RW	**COM3 PORT DISABLE**	This bit is used to disable COM3 port. 0 = COM3 port is available (Default) 1 = COM3 port is disabled
5	RW	**COM2 PORT DISABLE**	This bit is used to disable COM2 port. 0 = COM2 port is available (Default) 1 = COM2 port is disabled
4	RW	**COM1 PORT DISABLE**	This bit is used to disable COM1 port. 0 = COM1 port is available (Default) 1 = COM1 port is disabled
3	RW	**COM1 MODE**	Serial Port (COM1) configuration is defined as in Table 9-2 based on these bits. Refer to Section 7.1.2 for further details of these options. Bit 1 is valid if Bit 2 and 3 are set. 0 = RTS signal is used for direction control in RS485 Half Duplex 1 = DTR signal is used for direction control in RS485 Half Duplex
2	RW	**COM1 DUPLEX MODE**	
1	RW	**COM1 TX ENABLE (RS485 HALF DUPLEX MODE)**	
0	RW	**COM1 SLEW RATE**	

Mode (Bit 3)	Duplex Mode (Bit 2)	Slew Rate (Bit 0)	Configuration
0	0	0	Interface is disabled
0	0	1	RS232 full duplex (Default)
1	0	0	RS485 full duplex, Slew = Slow
1	0	1	RS485 full duplex, Slew = Fast
1	1	0	RS485 half-duplex, Slew = Slow
1	1	1	RS485 half-duplex, Slew = Fast

Table 9-2 Serial Port (COM1) Configuration Options

9.2.7 VME Slot ID Register

Register		**VME Slot ID Register**	
Address		**0x031E**	
Bit	Type	Name	Description
7	RO	**RESERVED**	Reserved, Read as zero
6	RO	**RESERVED**	Reserved, Read as zero
5	RO	**VID PARITY**	This indicates parity bit for the VID bits. When the VMEbus backplane Geographic Address pins are not connected, the VME Slot ID parity bit will read as 0.
[4:0]	RO	**VID [4:0]**	The VME Slot ID (Geographic Address) on the outer row D of the rear P1 connector can be read via these bits. Not all VMEbus backplanes connect these P1 connector pins to indicate Geographic Address, and they are only available when using a backplane with 160-way (5-row) connectors. When these pins are not connected, the VME Slot ID bits will read as 0.

9.3 VP E2x/msd Specific Registers

9.3.1 Hardware Version Register

Register		**Hardware Version Register**	
Address		**0x0220**	
Bit	Type	Name	Description
[7:4]	RO	**RFU**	-
[3:0]	RO	**BOARD LOGIC VERSION**	This indicates Board Logic Version: 0000 = AA, 0001 = AB, 0010 = AC, 0011 = AD ….etc. 1000 = BA, 1001 = BB, 1010 = BC, 1011 = BD ….etc.

9.3.2 Scratch Pad (Software Controlled) Register 1

Register		**Scratch Pad Register 1**	
Address		**0x0221**	
Bit	Type	Name	Description
[7:0]	RW	**SCRATCH PAD**	This register can be used by software

9.3.3 Scratch Pad (Software Controlled) Register 2

Register		**Scratch Pad Register 2**	
Address		**0x0222**	
Bit	Type	Name	Description
[7:0]	RW	**SCRATCH PAD**	This register can be used by software

9.3.4 DIP Switch Status Register 1

Register		**DIP Switch Status Register 1**	
Address		**0x0223**	
Bit	Type	Name	Description
7	RO	**WATCHDOG ENABLE**	This indicates WatchDog switch status 0 = WatchDog is disabled (default). 1 = WatchDog is enabled.
6	RO	**VME RESET OUT ENABLE**	This indicates VME reset switch status. 0 = VME reset out is disabled (default). 1 = VME reset out is enabled.
5	RO	**USER/PROCHOT LED FUNCTION SELECT**	This indicates User/PROCHOT LED select switch status. 0 = User Defined function 1 = PROCHOT/Thermtrip (default)
4	RO	**RFU**	Reserved
3	RO	**BIOS TYPE SELECT**	This indicates BIOS Type switch status. 0 = Factory Defaults/Settings. 1 = User BIOS (default).
2	RO	**BOOT MODE**	This indicates Card Boot mode switch status. 0 = Test software (CUTE). 1 = BIOS (default).
1	RO	**RESERVED**	Reserved, Read as '0'
0	RO	**CONSOLE SELECT**	This indicates Console Redirection Status switch status. 0 = input via keyboard/output via DVI-D (default) 1 = input/output via selected Serial port

9.3.5 DIP Switch Status Register 2

Register		**DIP Switch Status Register 2**	
Address		**0x0224**	
Bit	Type	Name	Description
7	RO	**SPI FLASH SELECT**	This indicates SPI Flash Select switch status for BIOS. 0 = Device 2. 1 = Device 1 (default).
6	RO	**RECOVERY BIOS SELECT**	Boot Type switch status 0 = Boot from Recovery BIOS. 1 = Normal Boot (default).
5	RO	**RFU**	Reserved
4	RO	**RFU**	Reserved
3	RO	**WAKE-ON-LAN ENABLE**	This indicates Wake-On-LAN (WoL) switch Status. 0 = WoL is disabled. 1 = WoL is enabled (default).
2	RO	**RFU**	Reserved
1	RO	**SPR_SW0**	This indicates Spare switch0 status. 0 = TBD. 1 = TBD (default).
0	RO	**PUSH BUTTON/LK1 HEADER SWITCH FUNCTION SELECT**	This indicates Push Button/LK1 Header Switch Function status. 0 = configured for NMI. 1 = configured for RESET (default).

9.3.6 DIP Switch Status Register 3

Register		**DIP Switch Status Register 3**	
Address		**0x0225**	
Bit	Type	Name	Description
7	RO	**RFU**	Reserved
[6:5]	RO	**COM PORT SELECT[1:0]**	This indicates serial port selection for serial console: 00 = Reserved 10 = COM1 01 = Reserved 11 = COM2 (default)
4	RO	**XMC SUPPORT DISABLE**	This indicates site 2 XMC support switch status: 0 = Site 2 supports XMC (default). 1 = Site 2 does not support XMC.
3	RO	**RFU**	Reserved
2	RO	**RFU**	Reserved
1	RO	**RFU**	Reserved
0	RO	**PMC IO VOLTAGE SELECT**	This indicates PMC IO voltage level select switch status. 0 = 5V 1 = 3.3V (default)

9.3.7 Scratch Pad (Software Controlled) Register 3

Register		**Scratch Pad Register 3**	
Address		**0x0228**	
Bit	Type	Name	Description
[7:0]	RW	**SCRATCH PAD**	This register can be used by software.

9.3.8 Interrupt Control Register

Register		**Interrupt Control Register**	
Address		**0x0229**	
Bit	Type	Name	Description
7	RW	**MICROCONTROLLER NMI FLAG**	This indicates the status of NMI from microcontroller. 0 = NMI has not occurred. 1 = NMI has occurred.
6	RC	**M51-TO-X86 IRQ FLAG**	The microcontroller sets this bit to request an interrupt. If "**M51-TO-X86 IRQ ENABLE**" bit is set, an interrupt is generated to processor. 0 = no interrupt request. 1 = Interrupt request.
5	RC	**SMS_ATN INTERRUPT FLAG**	SMS_ATN interrupt flag. 0 = Event has not occurred. 1 = Event has occurred.
4	RC	**SMIC_NOT_BUSY INTERRUPT FLAG**	SMIC not busy interrupt flag. 0 = Event has not occurred. 1 = Event has occurred.
3	RO	**RFU**	Reserved
2	RW	**M51-TO-X86 IRQ ENABLE**	This bit is used to enable IRQ from microcontroller to processor. 0 = Interrupt disabled. 1 = Interrupt enabled.
1	RW	**SMS_ATN INTERRUPT ENABLE**	0 = Interrupt disabled. 1 = Interrupt enabled.
0	RW	**SMIC NOT BUSY INTERRUPT ENABLE**	0 = Interrupt disabled. 1 = Interrupt enabled.

9.3.9 Status and Control Register 4

<table>
<tr><td colspan="2">Register</td><td colspan="2">Status & Control Register 4</td></tr>
<tr><td colspan="2">Address</td><td colspan="2">0x022A</td></tr>
<tr><td>Bit</td><td>Type</td><td>Name</td><td>Description</td></tr>
<tr><td>7</td><td>RW</td><td>SPI CS SELECT 0 (BIOS)</td><td rowspan="2">SPI Chip Select for BIOS flash
<table>
<tr><th>CS Select1</th><th>CS Select 0</th><th>CS for Dev1</th><th>CS for Dev2</th></tr>
<tr><td>0</td><td>0</td><td>CS0+</td><td>CS0+</td></tr>
<tr><td>0</td><td>1</td><td>CS0</td><td>CS1</td></tr>
<tr><td>1</td><td>0</td><td>CS1</td><td>CS0</td></tr>
<tr><td>1</td><td>1</td><td>CS0/CS1*</td><td>CS0/CS1*</td></tr>
</table>
+ -> Based on DIP switch SW5-4, Refer to Section 8.1, CS0 is routed to selected device.
* -> Based on DIP switch SW5-4 (SPI Flash Select, bit 7 of 0x224) , CS0 is routed to selected device and CS1 is routed to other device
NOTE: The processor has 2 SPI chip selects and this register is used to select the chip select from processor for SPI BIOS flash access.</td></tr>
<tr><td>6</td><td>RW</td><td>SPI CS SELECT 1 (BIOS)</td></tr>
<tr><td>5</td><td>RO</td><td>OPTIONAL FRONT IO SUPPORT</td><td>This bit indicates the status for Optional Front IO support in board.

0 = Optional Front IO is not supported.
1 = Optional Front IO is supported.</td></tr>
<tr><td>4</td><td>RO</td><td>P0 CONNECTOR PRESENCE STATUS</td><td>This bit indicates the status for P0 connector present in board.

0 = P0 connector is not present.
1 = P0 connector is present.</td></tr>
<tr><td>3</td><td>RO</td><td>SATA FLASH MODULE PRESENCE STATUS</td><td>This bit indicates the status for SATA Flash Module present.

0 = SATA Flash Module is not present.
1 = SATA Flash Module is present.</td></tr>
<tr><td>2</td><td>RO</td><td>TPM PRESENCE STATUS</td><td>This bit indicates the status for TPM present

0 = TPM is not present.
1 = TPM is present.</td></tr>
<tr><td>1</td><td>RO</td><td>CFAST PRESENCE STATUS</td><td>This bit indicates the status for CFast present.

0 = CFast card is not present.
1 = CFast card is present.</td></tr>
<tr><td>0</td><td>RO</td><td>SUPERIO PRESENCE STATUS</td><td>This bit indicates the status for super IO Presence in board.
0 = Super IO is not present
1 = Super IO is present</td></tr>
</table>

9.3.10 Status and Control Register 5

Register		**Status & Control Register 5**	
Address		**0x022B**	
Bit	Type	Name	Description
7	RO	**REAR IO CONFIGURATION**	This bit shows rear IO hardware strap status 0 = VP E2x/msd Rear IO 1 = VP A45/01x Rear IO (default)
6	RO	**RFU**	Reserved
5	RW	**SATA FLASH MODULE WP ENABLE**	This indicates SATA Flash Module Write Protect (WP) Enable status. 0 = Disable (default). 1 = Enable.
4	RW	**MICROCONTROLLER ISP ENABLE**	This indicates PCIe Redriver Configuration disable status 0 = Disable (default). 1 = Enable.
3	RO	**BOARD STATUS**	This indicates operating mode status of the board in VME chassis. 0 = Board works as peripheral card. 1 = Board works as a System Controller card.
2	RW	**UNIVERSE II IRQ SELECT**	This bit is used to set the connection path for Universe™ II IRQ to Processor. 0 = IRQ is routed via PCIe-to-PCI bridge (x130) / GPIO of Processor 1 = IRQ routed via SERIRQ
1	RO	**RFU**	Reserved
0	RO	**RFU**	Reserved

9.4 Microcontroller Sub-System Interface Registers

The VP E2x/msd board includes a low-power microcontroller sub-system which implements a number of board-specific features. The SoC communicates with the microcontroller via a set of registers through the SMIC interface. The following sections outline the contents of the registers used by that interface.

NOTE: A full description of the operation of this interface is not provided here, but Concurrent Technologies Board Support Package (BSP) software includes drivers to support the board features using this interface.

9.4.1 SMIC Data Register

This register is used to pass data between the SoC and microcontroller sub-system.

Register		**SMIC Data Register**	
Address		**0x0CA9**	
Bit	Type	Name	Description
7	RW	**D7**	This indicates SMIC Data Value.
6	RW	**D6**	
5	RW	**D5**	
4	RW	**D4**	
3	RW	**D3**	
2	RW	**D2**	
1	RW	**D1**	
0	RW	**D0**	

9.4.2 SMIC Control/Status Register

This register is used to pass status information between the SoC and microcontroller sub-system.

Register		**SMIC Status and Control Register**	
Address		**0x0CAA**	
Bit	Type	Name	Description
7	RW	**CS7**	This indicates SMIC Control/Status Value.
6	RW	**CS6**	
5	RW	**CS5**	
4	RW	**CS4**	
3	RW	**CS3**	
2	RW	**CS2**	
1	RW	**CS1**	
0	RW	**CS0**	

9.4.3 SMIC Flags Register

This register is used to handshake data transfers between the SoC and microcontroller sub-system.

Register		**SMIC Flags Register**	
Address		**0x0CAB**	
Bit	Type	Name	Description
7	RO	**RX_Data_RDY**	This indicates microcontroller has data ready for processor.
6	RO	**TX_Data_RDY**	This indicates microcontroller is ready to accept data from processor.
5	RO	**RFU**	Reserved
4	RO	**SMI**	Not used.
3	RO	**EVT_ATN**	This indicates microcontroller has an event message for processor.
2	RO	**SMS_ATN**	This indicates microcontroller has an event for processor.
1	RO	**RFU**	Reserved
0	R/SET	**Busy**	This indicates processor has a command for the microcontroller.

9.5 VMEbus Error Address Registers

The VP E2x/msd provides hardware that captures the VME address when a VMEbus error occurs. The captured data consists of the A31-A1, DS1-0, AM5-0, LWord and WR signal states.

Registers at I/O address 0x0320 to 0x0325 control this function. The register provides access to the captured information as explained in Section 9.5.2 to Section 9.5.6.

The bus error event may be detected by means of the bus error Interrupt or by polling the VME BERR Flag bit in 0x0320. When using the bus error Interrupt with the VME Address Capture, these functions must be enabled together.

The VME address information is valid when the Address Capture Status bit at 0x0320 indicates 'Idle', following a VMEbus error event. A read of the VME address at any other time is invalid.

See Section 9.5.7 for an example code to enable the VME Address Capture Function and to retrieve the address information.

9.5.1 VMEbus Address Capture Control Register

Register		**VME Address Capture Control Register**	
Address		**0x0320**	
Bit	**Type**	**Name**	**Description**
7	RO	**Address Capture Status**	This bit indicates the status of VMEbus error address capture. 0 = Address capture is Idle. 1 = Address capture is in Progress.
6	RO	**Type of VME Transaction**	This bit shows the type of VME transaction when bus error address is captured. 0 = Read 1 = Write
5	R/Clr	**BERR Flag**	This bit is used to indicate the status for bus error. 0 = No Bus Error is occured (Default) 1 = Bus Error is occured **NOTE:** Writing ”0” to this bit clears the flag.
4	RW	**BERR IRQ Disable**	This bit is used to disable Interrupt based on VMEbus error. 0 = Interrupt is disabled (Default) 1 = Interrupt is enabled
3	RO	**RFU**	Reserved
2	RO	**RFU**	Reserved
1	RO	**RFU**	Reserved
0	RW	**Address Capture Enable**	This bit is used to enable VME address capture in register (0x321 to 0x325) 0 = VME address capture is disabled (Default) 1 = VME address capture is enabled

9.5.2 VMEbus Error Address Capture Register 1

Register		**VMEbus Error Address Capture Register 1**	
Address		**0x0321**	
Bit	**Type**	**Name**	**Description**
7	RO	**A31**	This register stores VME address [31: 24] when VMEbus error is occurred.
6	RO	**A30**	
5	RO	**A29**	
4	RO	**A28**	
3	RO	**A27**	
2	RO	**A26**	
1	RO	**A25**	
0	RO	**A24**	

9.5.3 VMEbus Error Address Capture Register 2

	Register	VMEbus Error Address Capture Register 2	
	Address	0x0322	
Bit	**Type**	**Name**	**Description**
7	RO	**A23**	This register stores VME address [23: 16] when VMEbus error is occurred.
6	RO	**A22**	
5	RO	**A21**	
4	RO	**A20**	
3	RO	**A19**	
2	RO	**A18**	
1	RO	**A17**	
0	RO	**A16**	

9.5.4 VMEbus Error Address Capture Register 3

	Register	VMEbus Error Address Capture Register 3	
	Address	0x0323	
Bit	**Type**	**Name**	**Description**
7	RO	**A15**	This register stores VME address [15: 8] when VMEbus error is occurred
6	RO	**A14**	
5	RO	**A13**	
4	RO	**A12**	
3	RO	**A11**	
2	RO	**A10**	
1	RO	**A9**	
0	RO	**A8**	

9.5.5 VMEbus Error Address Capture Register 4

	Register	VMEbus Error Address Capture Register 4	
	Address	0x0324	
Bit	**Type**	**Name**	**Description**
7	RO	**A7**	This register stores VME address [7: 1] when VMEbus error is occurred.
6	RO	**A6**	
5	RO	**A5**	
4	RO	**A4**	
3	RO	**A3**	
2	RO	**A2**	
1	RO	**A1**	
0	RO	**LWORD**	This bit shows the status of LWORD signal when VMEbus error is occurred.

9.5.6 VMEbus Error Address Capture Register 5

Register	VMEbus Error Address Capture Register 5		
Address	0x0325		
Bit	**Type**	**Name**	**Description**
7	RO	**DS1**	This register stores the status of VME control signal – Address Modifier (AMx) and Data Strobe (DSx) when VMEbus Error occurs
6	RO	**DS0**	
5	RO	**AM5**	
4	RO	**AM4**	
3	RO	**AM3**	
2	RO	**AM2**	
1	RO	**AM1**	
0	RO	**AM0**	

9.5.7 VMEbus Error Address Capture Example Code

The following code fragments show how the system software can, by using the on-board hardware, detect and handle bus errors occurring in coupled bus cycles on the VMEbus when the Universe™ II peripheral is the VMEbus master. A VMEbus Error is generated when the slave device fails to complete the bus transaction within the nominal bus error timeout period (default value approximately 64ms).

The VMEbus Error Detection control and status flags are held in Status and Control registers and defined thus:

```
#define VME_ADDR_CAP_CTRL    (0x0320)
#define BERR_AC_EN  (0x01) // bit 0 - (R/W) BERR capture enable (1=En)
                           // bit 1 - Reserved
                           // bit 2 - Reserved
                           // bit 3 - Reserved
#define BERR_INT_EN (0x10) // bit 4 - (R/W) BERR INT enable (1=En)
#define BERR_FLAG   (0x20) // bit 5 - (R) BERR status (1=Occurred)
                                     (W) 0 to clear BERR status
#define BERR_RW     (0x40) // bit 6 - (R) Operation (1=Write, 0=Read)
#define BERR_BUSY   (0x80) // bit 7 - (R) BERR capture status (1-in Progress)

#define VME_ADDR_CAP_HH     (0x0321) // address bits[31:24]
#define VME_ADDR_CAP_HL     (0x0322) // address bits[23:16]
#define VME_ADDR_CAP_LH     (0x0323) // address bits[15:8]
#define VME_ADDR_CAP_LL     (0x0324) // address bits[7:1], bit[0]=LWORD
#define VME_ADDR_CAP_MOD    (0x0325) // bits[7:6]=DS[1:0],

                                     // bits[5:0]=AM[5:0]
```

It may be convenient to generate an interrupt when a VMEbus Error occurs and the following code fragment shows how the interrupts and address capture logic are enabled.

```
// Enable BERR IRQ
os_outb((BERR_INT_EN | (os_inb(VME_ADDR_CAP_CTRL))), VME_ADDR_CAP_CTRL);

// Enable BERR Address Capture
os_outb((BERR_AC_EN | (os_inb(VME_ADDR_CAP_CTRL))), VME_ADDR_CAP_CTRL);
```

The following code fragment shows only the basic interrupt handling function to process the VMEbus Error interrupt.

```
// Checks that BERR interrupt is active
reg = os_inb(VME_ADDR_CAP_CTRL);
if (reg & BERR_FLAG)
{
    // Disable BERR IRQ
    reg &= ~BERR_INT_EN;
    os_outb(reg, VME_ADDR_CAP_CTRL);

    // Clear BERR IRQ flag
    reg &= ~BERR_FLAG;
    os_outb(reg, VME_ADDR_CAP_CTRL);

    // Wait for error capture to complete
    timeout = 1000;
    do {
        reg = os_inb(VME_ADDR_CAP_CTRL);
        timeout--;

    } while ((reg & BERR_BUSY) && (timeout));

    // If capture completed, read details of bus error
    if (timeout != 0)
    {
        // Read and assemble the bus error address
        vmeBusErrorAddress = 0;
        vmeBusErrorAddress |= (os_inb(VME_ADDR_CAP_HH) << 24);
        vmeBusErrorAddress |= (os_inb(VME_ADDR_CAP_HL) << 16);
        vmeBusErrorAddress |= (os_inb(VME_ADDR_CAP_LH) << 8);
        vmeBusErrorAddress |= (os_inb(VME_ADDR_CAP_LL) & 0xFE);

        // Read the access modifiers
        vmeBusErrorLword = os_inb(VME_ADDR_CAP_LL) & 0x01;
        vmeBusErrorAttributes = os_inb(VME_ADDR_CAP_MOD);
        reg = os_inb(VME_ADDR_CAP_CTRL);
        vmeBusErrorReadWrite = ((reg & BERR_RW)?0x1:0x0);

        // Re-enable the BERR interrupt
        os_outb( (os_inb(VME_ADDR_CAP_CTRL) | BERR_INT_EN),
                  VME_ADDR_CAP_CTRL);
    }
}
```

9.6 Watchdog Timer

The VP E2x/msd board includes a hardware Watchdog timer which can be used by the operating software to monitor the normal operation of the system. The timer is enabled by a DIP switch (see Figure 9-3) and controlled by software. Once enabled, it must be restarted at regular intervals. If it is not restarted in less than10 seconds, the timer will expire and cause a Non-Maskable Interrupt or reset to the local processor.

Details of how it is used are provided in the following sections, starting with a description of the I/O register provided for this purpose.

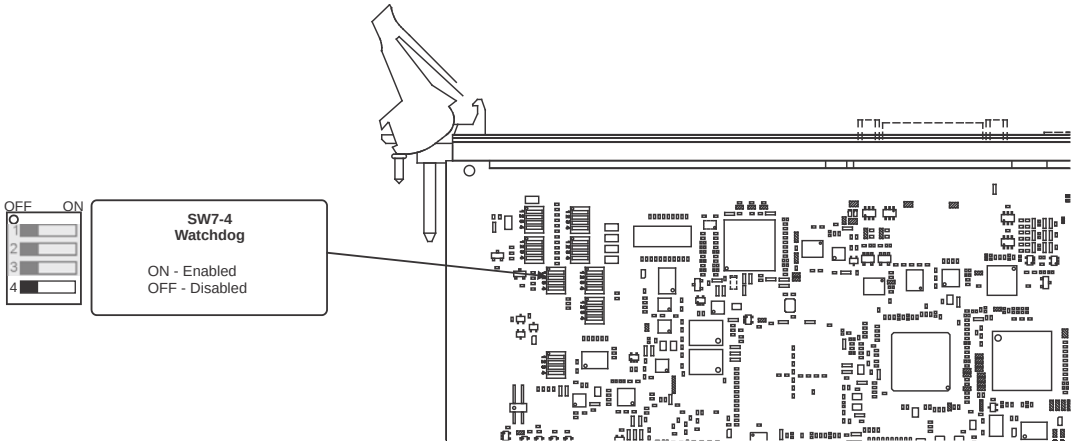

Figure 9-3 Watchdog Switch

9.6.1 Watchdog (board logic) Status & Control Register

	Register	**Watchdog Status & Control Register**	
	Address	**0x0214**	
Bit	Access	Name	Description
7		**RFU**	Reserved
6	RW	**SYSRSTOUT_WD**	This indicates status of Watchdog Time-out based on System RESET# Enable. 0 = Watchdog time-out does not drives System RESET# (default). 1 = Watchdog time-out drives System RESET#.
5	RW	**S/W Enable**	This indicates status of Watchdog Software Enable. 0 = Watchdog disabled (default). 1 = Watchdog enabled.
4	RO	**ENABLE Link**	This indicates status of the Watchdog Configuration switch. See Figure 9-3. 0 = Watchdog is under software control. 1 = Watchdog disabled by the switch.
3	RO	**STATUS**	Watchdog Status bit can be used to determine if the Watchdog was the source of an NMI or reset. A valid Watchdog restart will set this bit to 'watchdog OK' if the Watchdog had previously timed out. 0 = Watchdog timed out. 1 = Watchdog OK (default).
2	RW	**NMI / RESET**	The Select Watchdog Action bit selects the following actions when the Watchdog times out. 0 = generate an NMI (default). 1 = generate a board reset.
1 0	RW	**PATTERN**	Watchdog Restart Pattern Refer to Section 9.6.2 for details of how to use the Watchdog timer.

9.6.2 Enabling and Disabling the Watchdog Timer

The watchdog circuitry contains features to safeguard against accidental use through faulty or unintended software actions.

To enable the watchdog, the following sequence of events needs to be executed:

1. Read the Watchdog Status & Control register. Check the status of the Watchdog Configuration switch in the Watchdog Status & Control Register (0x0214, bit 4), see Section 9.6.1. If it reads 'low', then proceed to step 2. If it reads 'high', then the Watchdog is disabled by the Watchdog switch (SW7-4) (See Figure 9-3), and cannot be enabled in software.
2. Set bits 1 & 0 to the complement of each other (e.g. 0, 1 or 1, 0) and at the same time set bit 5 'high'.
3. Complement bits 1 & 0. Write the new values to the bit 1 & 0 of Watchdog Status & Control register before the timer expires.
4. Repeat step 3.

Once the Watchdog has been enabled, it can be disabled by setting bit 5 'Low' in the Watchdog Status & Control Register (0x0214, bit 5).

9.6.3 Using the Watchdog Timer

Once enabled, the Watchdog timer must be restarted at regular intervals to prevent it expiring. The maximum interval time is fixed at 10 seconds. If the Watchdog timer is not restarted within this time, it will time out and cause a reset or generate an NMI depending on the state of bit 2 of the Watchdog Status & Control Register. To restart the Watchdog the complement of the lower two bits needs to be written into the Watchdog Status & Control register. These two bits must also be the complement of each other i.e. 0, 1 or 1, 0. Writing any other value or the same value will not restart the Watchdog. If the Watchdog time-out is configured to generate a board reset and a time-out occurs, the Watchdog circuit will also be reset. The Watchdog must be enabled again after a reset has occurred. This allows operating systems software to boot after a reset without having to keep the Watchdog from timing out during this period. The Watchdog status bit will not be cleared; so this must be performed by enabling and restarting the Watchdog. This is to preserve the status of the Watchdog timeout, whereby allowing the software to determine the source of the NMI or reset was caused by the watchdog.

9.7 Long Duration Timer / Periodic Interrupt Timer

The Long Duration Timer (LDT) consists of a 32-bit free running counter with a 32-bit holding register and a status and control register. It may be used by user software to timestamp events to a resolution of 1 microsecond. The counter bytes are laid out in little-endian format to permit multi-byte read/write operations. The status & control register controls the operation of the LDT. A 32-bit holding register is provided to ensure stable count values are read. Read operations return the holding register byte values. A read operation on the low byte of the counter causes the count value to be transferred to the holding register. Hence, the low byte should be read first to ensure a stable count value.

The counter may be preset by writing to the registers. The counter bytes may be written independently. The counter should be stopped before writing to it or the outcome may be indeterminate. The counter registers are cleared at power-on, but not by subsequent reset operations. If necessary, the LDT can be cleared by writing zero to all four counter bytes. An interrupt may be generated when the counter rolls over (from 0xFFFFFFFF to zero). This occurs approximately every 72 minutes (1 MHz clock).

The LDT doubles as a simple Periodic Interrupt Timer (PIT). It offers 7 fixed interrupt rates, namely: 100, 200, 500, 1,000, 2,000, 5,000 and 10,000Hz (1 MHz clock). The mode / interrupt rate is set by three bits in the LDT status & control register.

NOTE: If the LDT clock frequency is not 1 MHz, the above rates should be scaled accordingly.

In PIT mode, the counter counts up to a pre-determined maximum value and then goes back to zero. To ensure a full first interval, the low and mid-low bytes of the counter should be cleared before the counter is started.

9.7.1 Long Duration Timer / Periodic Interrupt Timer Low Byte

	Register	Long Duration Timer / Periodic Interrupt Timer Low Byte	
	Address	0x0218	
Bit	**Access**	**Name**	**Description**
7 6 5 4 3 2 1 0	RW	**LDT_PIT LOW_BYTE**	Low byte of LDT / PIT (Bits 7 – 0) Reading this register causes the current value of the LDT to be transferred to a holding register. This allows a stable 4 byte count to be read. The low byte of the holding register is returned by the read. Writing to this register loads a value into the low byte of the LDT / PIT counter. The counter should be stopped when writing or the result will be indeterminate.

9.7.2 Long Duration Timer / Periodic Interrupt Timer Mid-low Byte

	Register	Long Duration Timer / Periodic Interrupt Timer Mid-low Byte	
	Address	0x0219	
Bit	**Access**	**Name**	**Description**
7 6 5 4 3 2 1 0	RW	**LDT_PIT MID_LOW_BYTE**	Mid-low byte of LDT / PIT (Bits 15 – 8) Reading this register returns the mid-low byte of the holding register. Writing to this register loads a value into the mid-low byte of the LDT / PIT counter. The counter should be stopped when writing or the result will be indeterminate.

9.7.3 Long Duration Timer Mid-High Byte

	Register	Long Duration Timer Mid-high Byte	
	Address	0x021A	
Bit	**Access**	**Name**	**Description**
7 6 5 4 3 2 1 0	RW	**LDT MID_HIGH_BYTE**	Mid-high byte of LDT (Bits 23 – 16) Reading this register returns the mid-high byte of the holding register. Writing to this register loads a value into the mid-high byte of the LDT counter. The counter should be stopped when writing or the result will be indeterminate.

9.7.4 Long Duration Timer High Byte

	Register	Long Duration Timer High Byte	
	Address	0x021B	
Bit	**Access**	**Name**	**Description**
7 6 5 4 3 2 1 0	RW	**LDT HIGH_BYTE**	High byte of LDT (Bits 31 – 24) Reading this register returns the high byte of the holding register. Writing to this register loads a value into the mid-high byte of the LDT counter. The counter should be stopped when writing or the result will be indeterminate.

9.7.5 Long Duration Timer / Periodic Interrupt Timer Status & Control Register

The default LDT / PIT clock signal is generated by the board logic at 1.0 MHz

	Register	**LDT / PIT Status and Control Register**	
	Address	**0x021C**	
Bit	**Access**	**Name**	**Description**
7	RW	**LDT INT EN**	This indicates LDT interrupt is enabled or not. 0 = Interrupt is disabled (Default). 1 = Interrupt is enabled.
6		**RFU**	Reserved
5	RW	**CLOCK Select**	This controls the LDT / PIT clock source. 0 = 1 MHz 1 = 32.768 kHz
4	RC	**LDT/PIT Interrupt**	This indicates the status of the LDT / PIT interrupt flag, which is set if the RUN bit is set and either the LDT rolls over or the PIT interval expires. It can be cleared by writing to the register with a zero in its bit position. This should be done in the LDT / PIT interrupt service routine. 0 = LDT / PIT interrupt has not occurred 1 = LDT / PIT interrupt has occurred
3 2 1	RW	**MODE**	This indicates status of the LDT / PIT mode. If the Bit 5(Clock Select) is set to 0, below PIT rates are available. 0 0 0 = LDT 0 0 1 = PIT 100Hz 0 1 0 = PIT 200Hz 0 1 1 = PIT 500Hz 1 0 0 = PIT 1,000Hz 1 0 1 = PIT 2,000Hz 1 1 0 = PIT 5,000Hz 1 1 1 = PIT 10,000Hz If the Bit 5(Clock Select) is set to 1, below PIT rates are available. 0 0 0 = LDT 0 0 1 = PIT 3.2768Hz 0 1 0 = PIT 6.5536Hz 0 1 1 = PIT 16.384Hz 1 0 0 = PIT 32.768Hz 1 0 1 = PIT 65.536Hz 1 1 0 = PIT 163.84Hz 1 1 1 = PIT 327.68Hz
0	RW	**RUN**	This bit controls whether the LDT / PIT runs or is stopped. 0 = stop (default). 1 = run.

The LDT clock signal is obtained from a fixed rate crystal oscillator which is divided down in the board logic to provide two selectable clock rates of 1 MHz or 32.768 kHz.

9.7.6 Programming the LDT/PIT

The following code fragments illustrate how the system software, by using the on-board hardware, creates accurate time delays and measure elapsed times, accurate to 1µs, irrespective of the SoC's operating frequency.

The LDT and PIT control registers and operational modes are defined thus:

```
#define TIMER_BYTE_0                (0x0218U)
#define TIMER_BYTE_1                (0x0219U)
#define TIMER_BYTE_2                (0x021AU)
#define TIMER_BYTE_3                (0x021BU)
#define CONTROL_STATUS              (0x021CU)

#define INTERRUPT_MASK              (0x10U)
#define INTERRUPT_ENABLE            (0x10U)
#define INTERRUPT_DISABLE           (0x00U)
#define INTERRUPT_SET               (0x10U)
#define INTERRUPT_RESET             (0x00U)

#define TIMER_ROLLOVER              (0x10U)

#define MODE_MASK                   (0x0EU)
#define MODE_PIT_10000Hz            (0x0EU)
#define MODE_PIT_5000Hz             (0x0CU)
#define MODE_PIT_2000Hz             (0x0AU)
#define MODE_PIT_1000Hz             (0x08U)
#define MODE_PIT_500Hz              (0x06U)
#define MODE_PIT_200Hz              (0x04U)
#define MODE_PIT_100Hz              (0x02U)
#define MODE_LDT                    (0x00U)

#define MODE_RUN_MASK               (0x01U)
#define MODE_RUN_GO                 (0x01U)
#define MODE_RUN_STOP               (0x00U)
```

The following code fragment illustrates how a simple delay of 10ms is implemented.

```
outbyte (CONTROL_STATUS, MODE_RUN_STOP);
outbyte (TIMER_BYTE_0, 0);
outbyte (TIMER_BYTE_1, 0);
outbyte (TIMER_BYTE_2, 0);
outbyte (TIMER_BYTE_3, 0);
outbyte (CONTROL_STATUS, MODE_PIT_100Hz | MODE_RUN_GO);

/* wait until the PIT rolls over ...  */

while (inbyte (CONTROL_STATUS) & TIMER_ROLLOVER) == 0)
    ; /* do nothing ...  */

/* reset the PIT "rollover" flag ...  */

outbyte (CONTROL_STATUS, MODE_RUN_STOP);
```

It is possible to implement delays of 5ms, 2ms, 1ms, 500µs, 200µs and 100µs by utilizing other PIT modes.

The PIT can generate an interrupt whenever the PIT rolls over. The system programmer must initialize the interrupt vector, enable PIC interrupts, etc. The following code fragment shows the basic interrupt handling function.

```
static volatile signed long int dCounter;

#pragma interrupt (vInterruptHandler)
static void far vInterruptHandler (void)
{
  /*
   * clear the source of the interrupt by resetting the rollover
   * flag, thus:
   */

   outbyte (CONTROL_STATUS, inbyte (CONTROL_STATUS) & ~INTERRUPT_MASK);

   /*
   * perform the relevant actions to acknowledge the interrupt
   * in the PIC, etc. ...
   */

   dCounter--;
}
```

The following code fragment used in conjunction with the previous code fragment illustrates another method of implementing a timed delay. The **dCounter** variable is declared volatile, which prevents any ANSI standard compatible C compilers from optimizing accesses to the **dCounter** variable.

```
outbyte (CONTROL_STATUS, MODE_RUN_STOP);
outbyte (TIMER_BYTE_0, 0);
outbyte (TIMER_BYTE_1, 0);
outbyte (TIMER_BYTE_2, 0);
outbyte (TIMER_BYTE_3, 0);
outbyte (CONTROL_STATUS, MODE_PIT_100Hz | MODE_RUN_GO);
dCounter = 500; /* 500 * (1 / 100) == 5 seconds */

/*
 * install the interrupt for the PIT counter, modify the
 * PIC settings, etc.  And ensure interrupts are enabled.
 */

while (dCounter > 0)
    ; /* do nothing ...  */

outbyte (CONTROL_STATUS, MODE_RUN_STOP);
```

The following code fragment uses the LDT to measure the elapsed time to a resolution of 1ms. In this example, the LDT is zeroed at the start of the test and so there is no need to subtract the LDT's initial value from its final value.

```
static UINT32 dElapsedTime;

outbyte (CONTROL_STATUS, MODE_RUN_STOP);
outbyte (TIMER_BYTE_0, 0);
outbyte (TIMER_BYTE_1, 0);
outbyte (TIMER_BYTE_2, 0);
outbyte (TIMER_BYTE_3, 0);
outbyte (CONTROL_STATUS, MODE_LDT | MODE_RUN_GO);

/*
 * perform action to be timed ...
 */

outbyte (CONTROL_STATUS, MODE_STOP);
dElapsedTime  =  (UINT32) inbyte (TIMER_BYTE_0);
dElapsedTime |= ((UINT32) inbyte (TIMER_BYTE_1)) << 8;
dElapsedTime |= ((UINT32) inbyte (TIMER_BYTE_2)) << 16;
dElapsedTime |= ((UINT32) inbyte (TIMER_BYTE_3)) << 24;
printf ("Elapsed time = %u.%06u seconds\n",
         dElapsedTime / 1000000U, dElapsedTime % 1000000U);
```

The TIMER_BYTE_0, TIMER_BYTE_1, TIMER_BYTE_2 and TIMER_BYTE_3 control registers are at successive addresses and form a 32-bit register in "little endian" format. It is possible to read and write the timer's value in a single 32-bit I/O operation. For example, to read the timer's value, use the following C statement.

```
CounterValue = inlong (TIMER_BYTE_0);
```

This page is intentionally unused

10 BIOS

The VP E2x/msd is fitted with BIOS firmware that performs many of the functions of a standard desktop PC. It also includes additional features specifically tailored for the VMEbus environment. In addition to the core BIOS firmware, the board is fitted with BIOS Extensions for remote boot-load capability via any of the on-board Ethernet channels.

To improve the flexibility of the board, some of these features may be selectively enabled or disabled by an operator using BIOS setup menus. Many of the features provided by the BIOS are unlikely to be adjusted by the user, but there are several options that many users will find helpful. Some of these are already referenced in earlier sections of this manual and this chapter describes some other commonly used options.

More information about each of the options available is provided in the Help box of the BIOS setup menus. For a detailed description of the BIOS features, see the Technical Reference Manual for the VP E2x/msd BIOS (document number 550 8049).

10.1 Entering the BIOS

The startup mode for the board is selected using the Boot Mode switch (SW8-2) and can be set to either:

- SW8-2 OFF (BIOS mode – the factory default setting) this mode generally follows the behavior of a desktop PC, or;
- SW8-2 ON (CUTE mode – (Concurrent Technologies Unified Test Environment) a flexible testing mode primarily for use at the factory) this mode can be used for system or board testing

CUTE mode operation and features are beyond the scope of this manual. Figure 10-1 shows the location and setting options for the Boot Mode switch.

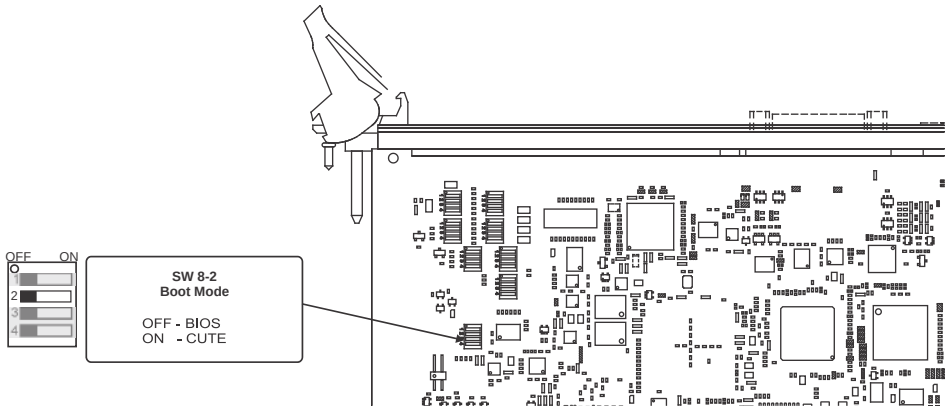

Figure 10-1 Boot Mode Switch

A reset caused by a keyboard <**CTRL-ALT-DEL**> keystroke combination, or by a programmed reset using one of several different I/O access sequences, will only result in a BIOS restart. A complete board or system reset (using the front panel switch) will cause the board to restart in the mode selected by the Boot Mode switch.

Operator communication with the BIOS is usually through a DVI-D or optional DVI-I display and a separate keyboard. This can be reconfigured with on-board switches to use a serial terminal connected to the COM ports as described in Section 7.1. A VT100-compatible serial terminal or an emulator program should be used. By default the serial line is programmed to operate at 115,200 Baud with 8 data bits, 1 stop bit and no parity (8N1). There is no flow control. For slow terminals, the baud rate can be reduced via the Baud Rate field of the **`Advanced | Console Redirection`** menu.

10.2 BIOS Startup Sequence

When the board starts up without operator intervention, it runs a basic Power On Self-Test (POST) sequence, including DRAM initialization and a DRAM test. The full DRAM test is omitted on subsequent restarts if the BIOS configuration settings have not been changed. Once the DRAM test is completed, the board tries to boot-load application software from any attached mass-storage medium or through one of the Ethernet interfaces.

Pressing <**F2**> at any time during the BIOS startup sequence results in the BIOS Setup menu being entered. The Setup menu is extensive and supplied with context-sensitive help information, displayed on screen, in the right-hand side of the panel.

NOTE: When <**F2**> is pressed, a few seconds may elapse before the BIOS Setup menu appears. The BIOS will always run BIOS Extensions for any PMC/XMC modules it detects before responding to a key press.

If changes made through the BIOS Setup menu prevent the board booting, it can be returned to the factory default settings using the Force Optimal Defaults switch. See Section 10.5 for further details.

10.3 Boot Device Selection

10.3.1 Setup Boot Menu

The order in which the BIOS search for a bootable medium is pre-configured, but may be altered by the operator using the **Boot | Legacy** setup sub-menu. When the order is changed using this menu it will be retained in a non-volatile memory so that the order is maintained after a restart.

The boot order menu has two configuration modes: Normal and Advanced. This can be selected via the **Boot | Legacy | Normal Boot Menu** setup sub-menu.

10.3.1.1 Normal

In Normal mode, the user specifies the boot order using device categories.

The **Boot Type Order** sub-menu specifies the relative ordering for Hard Disk, CD/DVD-ROM and Others device categories. The <**+**> and <**–**> keys can be used to raise or lower the relative priority of each device category.

For each category where a physical device is attached an additional sub-menu will be created. Through this menu, the relative boot order of devices within that category can be further configured, again using the <**+**> and <**–**> keys.

10.3.1.2 Advanced

In Advanced mode, the user specifies the boot order for all attached devices through a unified device list. The <**+**> and <**–**> keys can be used to raise or lower the relative priority of each device.

This mode provides complete control over the boot order; however, the user requires a greater understanding of the attached boot devices.

10.3.2 One-time Boot Override

It is also possible to specify a one-time override of the boot device when the board starts, by pressing <**F12**>. This will result in the BIOS entering the Boot Manager. From here, the required boot device may be selected from a list using the cursor keys and by pressing <**Enter**>. However, this selection is not retained in non-volatile memory, so the correct device must be re-selected if necessary at a subsequent restarts.

> **NOTE:** When <**F12**> is pressed, a few seconds may elapse before the boot device selection menu appears. The BIOS will always run BIOS Extensions for any PMC/XMC modules it detects before responding to a key press.

Alternatively, the Boot Manager can be quit by pressing <**Esc**>, which offers the options to enter Setup or Continue and boot using the order previously configured through Setup.

10.3.3 PXE Network Boot

The on-board Ethernet channels require their PXE Firmware to be enabled before they can be used as boot devices. A BIOS setup option controls whether PXE Firmware runs for the front or rear Ethernet channels. This can be found under **Main** | **Boot Features | PXE Boot**.

The Ethernet boot firmware allows remote booting using the Pre-Boot Execution (PXE) protocols. Further information on the capabilities of this software is available from the Intel® web site at: http://developer.intel.com

> **NOTE:** The BIOS has limited space available for Extension ROMs. If a PMC/XMC module containing extension firmware is fitted to the board, it may be necessary to disable one or more of the on-board firmware extensions before the PMC/XMC firmware can be loaded.

10.4 PCI Bus Resource Management

The bus structure of the VP E2x/msd is complex. It has two PCI buses. One 32-bit bus is used for the Universe™ II VMEbus bridge and is derived from a PCIe-to-PCI-X bridge connected to the PCIe switch. It runs at 33 MHz. The PCI bus to both PMC sites is derived from the SoC's PCIe port through a PCIe-to-PCI bridge. This 64-bit bus normally operates with 3.3V signaling levels but is 5V tolerant. It runs at up to 100 MHz in PCI-X Bus mode or up to 66 MHz in PCI Bus mode. Actual bus speed is determined by the PMC(s) fitted and by setting certain board switches (see Section 2.7.2).

10.4.1 PCIe Port Configuration

The SoC provides four x1 PCIe ports. One x1 PCIe port connects directly to the quad port Gigabit Ethernet controller (Intel® i350-AM4), one x1 PCIe port connects to a quad port PCIe-to-PCIe switch (Pericom PI7C9X2G404) for XMC sites, one x1 PCIe port is connected to a quad port PCIe-to-SATA controller for SATA ports and one x1 PCIe port is connected to a PCIe-to-PCI-X bridge which connects to the PMC Sites.

Downstream ports of the PCIe-to-PCIe switch are extended to XMC sites and Universe™ II VME Bridge (through a PCIe-to-PCI-X bridge).

10.4.2 PCI Resource Allocation

The BIOS initializes all devices on the local PCI bus and allocates appropriate memory address ranges, I/O address ranges and interrupt routings for all these devices. This process is automatic as part of the BIOS "Plug-and-play" setup. The chipset allows for a flexible allocation of many PCI bus interrupts to the available interrupt inputs on the PC-compatible interrupt controllers provided on the board. The BIOS uses this feature to program default settings that it considers appropriate for the combination of on-board devices and any device fitted to the XMC or PMC sites.

10.4.3 PCI Interrupt Allocation

The interrupt controller in the SoC can operate in two basic modes, namely PIC (or Non-APIC) mode and APIC mode. PIC mode corresponds to the legacy PC interrupt structure. APIC mode provides additional interrupts and several functional improvements.

Table 10-1 lists the typical interrupt structure in PIC mode. A total of 16 usable interrupts are available. The actual allocation of PCI bus interrupts to available interrupt controller inputs will depend on both the default "Plug-and-play" settings programmed by the BIOS, and the way in which the user has overridden them using the Setup screens. When more than one PCI bus interrupt is routed to the same interrupt controller input, that input will remain active while any of the sources connected to it are active.

Interrupt	Device(s)
IRQ0	Timer 0
IRQ1	Keyboard
IRQ2	Slave PIC
IRQ3	Serial Port COM2
IRQ4	Serial Port COM1
IRQ5	Board Logic Interrupt (LDT, SMIC, PIT)
IRQ6	Reserved
IRQ7	PCI device interrupt
IRQ8	Real Time Clock
IRQ9	PCI device interrupt
IRQ10	PCI device interrupt
IRQ11	Serial Port COM3
IRQ12	Mouse
IRQ13	Floating Point Error
IRQ14	SATA Controller
IRQ15	SATA Controller

Table 10-1 Interrupt Structure in PIC Mode

Table 10-2 lists the typical interrupt structure in APIC mode. A total of 24 interrupts are available. The SoC interrupt inputs PIRQA – PIRQH are mapped to IRQ16 – IRQ23 respectively.

Interrupt	Device(s)
IRQ0	Legacy PIC Interrupt
IRQ1	Keyboard
IRQ2	Timer 0
IRQ3	Serial Port COM2
IRQ4	Serial Port COM1
IRQ5	Board Logic Interrupt (LDT, SMIC, PIT)
IRQ6	Reserved
IRQ7	-
IRQ8	Real Time Clock
IRQ9	-
IRQ10	-
IRQ11	Serial Port COM3
IRQ12	Mouse
IRQ13	Floating Point Error
IRQ14	Primary IDE via SATA controller in Legacy mode
IRQ15	Secondary IDE via SATA controller in Legacy mode
IRQ16	PIRQA
IRQ17	PIRQB
IRQ18	PIRQC
IRQ19	PIRQD
IRQ20	PIRQE
IRQ21	PIRQF
IRQ22	PIRQG
IRQ23	PIRQH

Table 10-2 Interrupt Structure in APIC Mode

NOTE: IRQ16 to IRQ23 can be used for PCI internal devices.

10.4.4 PCI Device IDs

Each PCI bus and each device on an individual PCI bus has a unique ID. Table 10-3 lists the Device ID and vendor IDs for the components used in VP E2x/msd.

Device (Controller)	Vendor ID (in Hex)	Device ID (in Hex)	Remarks
SoC Transaction Router (Host Bridge)	8086	0F00	B:0, F:0, D:0
Graphics and Display	8086	0F31	B:0, F:0, D:2
SATA Controller	8086	0F20, 0F21 for IDE mode 0F22, 0F23 for AHCI mode	B:0, F:0/1, D:19
Inter HD Audio Controller	8086	0F04	B:0, F:0, D:27
PCIe Root port1	8086	0F48	B:0, F:0, D:28
PCIe Root port2	8086	0F4A	B:0, F:1, D:28
PCIe Root port3	8086	0F4C	B:0, F:2, D:28
PCIe Root port4	8086	0F4E	B:0, F:3, D:28
USB EHCI Controller	8086	0F34	B:0, F:0, D:29
USB2 xHCI Controller	8086	0F35	B:0, F:0, D:20
LPC Controller	8086	0F1C	B:0, F:0, D:31
SMBus controller	8086	0F12	B:0, F:3, D:31
PI7C9X2G404SL	12D8	2404	4 Port 4 Lane Gen2 PCIe switch
PI7C9X130	12D8	E130	PCIe-to-PCI-X Bridge
88SE9235	1B4B	9235	PCIe-to-SATA Controller
I350-AM4	8086	1521	Quad Port Ethernet controller
Universe™ II	10E3	0000	PCI-to-VME Bridge

Table 10-3 PCI Device Numbers

10.4.5 Universe II Outbound Image Allocation

The boards fitted with 4 Gbytes or more of DRAM do not have a convenient 'hole' in the address map where Universe™ II Local Outbound Slave Images can be mapped. Therefore the BIOS must reserve a block of address space for this purpose.

The **`Vme | Outbound Reserved Size`** setup option is used to specify the size of the reserved memory block. As required the VME Outbound Images 0 and 1 can be configured using the **`Vme | Outbound Images`** sub-menu, however, the total of the two image sizes must not exceed the reserved size.

The BIOS reserves memory by increasing the size of the block used by PCI devices, as a result the size of DRAM available below 4GB will be reduced by a corresponding amount (for 64-bit operating systems this DRAM is remapped above 4GB and the total memory size is unaffected).

The BIOS creates a data-structure in DRAM that defines details of the reserved memory. This data structure is described below.

10.4.6 Universe II Inbound Image Allocation

Some operating systems wishing to map Universe™ II VME Slave (Inbound) Images into DRAM can encounter problems allocating the required buffers. To overcome this, the BIOS can reserve a block of DRAM (below 4 Gbytes) that is hidden from the operating system memory-manager.

The size of the reserved block is specified through the **`Vme | Inbound Reserved Size`** option. The BIOS allocates this memory by marking the specified block of memory as reserved, thus preventing the operating system memory-manager from utilizing it.

Details of the data structure are described in Section 10.4.7.

10.4.7 VME Reserved Memory Data Structure

The details of the Outbound and Inbound memory reservations are provided by the VME Reserved Memory data structure which the BIOS constructs in DRAM.

Software requiring details of this reserved memory block can locate this structure by searching for the signature bytes between addresses 0xE0000 and 0xFFFFF.

```
/* Header part */

UINT32          vmeLsi_header      = 'EMV$';     /* signature, '$' in LSB */
UINT8           vmeLsi_version     = 0x02;       /* version of structure */
UINT8           vmeLsi_length;                   /* total length of structure */
UINT16          vmeLsi_reserved    = 0;

/* Version 1 payload */

UINT32          vmeLsi_mem_base;          /* physical address of reserved block */
UINT32          vmeLsi_mem_size;          /* size (in bytes) of reserved block */
UINT32          vmeLsi_image_0_base;      /* base address of enabled LSI images */
UINT32          vmeLsi_image_1_base;
UINT32          vmeLsi_image_2_base;
UINT32          vmeLsi_image_3_base;
UINT32          vmeLsi_image_4_base;
UINT32          vmeLsi_image_5_base;
UINT32          vmeLsi_image_6_base;
UINT32          vmeLsi_image_7_base;

/* Version 2 payload */

UINT32          vmeVsi_mem_base;          /* physical address of reserved block */
UINT32          vmeVsi_mem_size;          /* size (in bytes) of reserved block */
UINT32          vmeVsi_image_0_base;      /* base address of enabled VSI images */
UINT32          vmeVsi_image_1_base;
UINT32          vmeVsi_image_2_base;
UINT32          vmeVsi_image_3_base;
UINT32          vmeVsi_image_4_base;
UINT32          vmeVsi_image_5_base;
UINT32          vmeVsi_image_6_base;
UINT32          vmeVsi_image_7_base;
```

10.5 BIOS Defaults

The BIOS provided with the VP E2x/msd stores configuration data in Flash memory, rather than battery-backed CMOS RAM so that settings are not lost if the board is powered-off and the battery removed.

The BIOS contains three sets of configuration data: a Working Set, a set of Optimal Defaults, and a set of Custom Defaults. When the board is shipped from the factory, the Working Set will contain the Optimal Defaults. The Optimal Defaults are pre-configured in the factory and cannot be changed by the user. The user can restore the board to these factory default settings at any time using the **`Exit | Load Optimal Defaults`** option.

When the board is powered-on, configuration settings will always get loaded from the Working Set. When settings are modified and saved via the **`Exit | Exit Saving Changes`** option, only the Working Set will be updated with these changes.

If desired, the user can save their preferred settings as Custom Defaults via the **`Exit | Save Custom Defaults`** option; this will also save the selected configuration to the Working Set. Later, if the settings are subsequently changed, the user can quickly return to their preferred configuration using the **`Exit | Load Custom Defaults`** option.

If the board ever fails to boot due to changes made via Setup, the board can be forced back to the factory configured settings using SW7-2 (Force Optimal Defaults) as shown in Figure 10-2. Once the board has been booted with the switch in the 'Enabled' position, it should be powered off and the switch should be returned to the 'Disabled' position, otherwise changes made via Setup will be lost each time the board is power cycled.

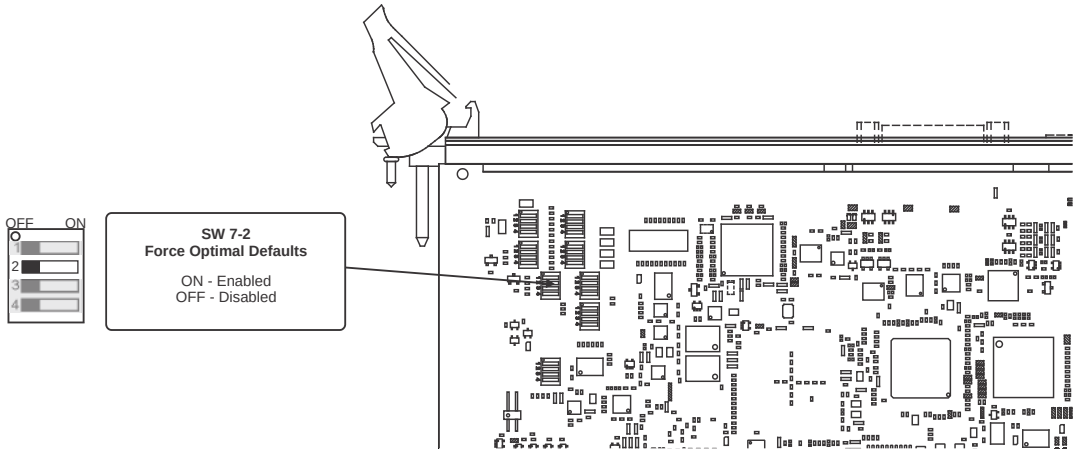

Figure 10-2 Force Optimal Defaults Switch

NOTE: If the board is returned for repair, the saved settings may be changed or invalidated during the repair process.

10.6 Recovery BIOS

In the unlikely event that the board's BIOS ROM contents become corrupted and it is not possible to perform the normal BIOS update procedure, the VP E2x/msd has a minimal Recovery BIOS that will allow the board to boot from a disk and restore a known-good BIOS image.

The BIOS recovery process can be forced using SW5-3 (Boot Type switch) as shown in Figure 10-3.

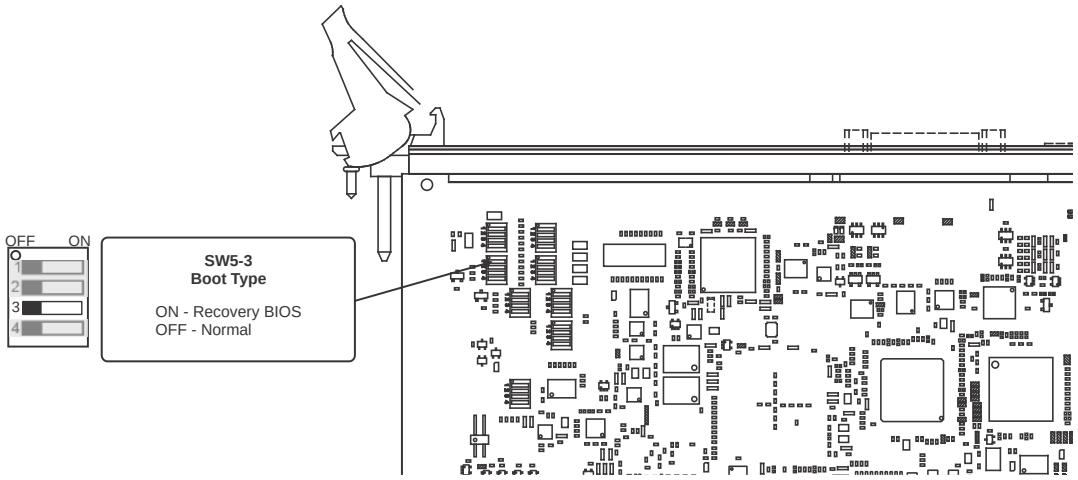

Figure 10-3 Boot Type Switch

The Recovery BIOS requires a suitable firmware image which can be obtained from Concurrent Technologies, if required.

The VP E2x/msd also supports two BIOS devices for recovery. In case the content of one BIOS devices is corrupted, the second BIOS device can be used.

11 BOARD MANAGEMENT

11.1 Thermal Management

The maximum power dissipation of the Intel® Atom™ processor on this board is very low. It is 10W for the 4-core processor (E3845) and 5W for the 1-core processor (E3815) variants. Under most normal conditions, the heatsink (and cooling airflow) keeps the processor die temperature within specification. However, if the board is running compute-intensive or other high stress software and the airflow is inadequate, the heatsink alone may not be able to prevent the processor overheating in some variants.

Some variants can operate without forced airflow (so-called “fanless” configurations, 0LFM); see Section A.3 for more details.

The processor includes several thermal management and protection functions to ensure that the processor always operates within its thermal specifications. Each function is described below. Use the BIOS setup options to select which functions are to be enabled. See Section 11.1.2 for further details.

11.1.1 SoC Thermal Trip

The processor chip also contains a thermal trip circuit. This is intended to protect the processor in the event of a catastrophic cooling failure. If the die temperature reaches approximately 125°C, catastrophic trip signals from all the temperature sensors in the SoC are combined to generate the THERMTRIP signal, which, when activated, will shut off all the PLLs and power rails to prevent an SoC breakdown. To prevent glitches from triggering shutdown events, catastrophic trips from the temperature sensors are registered before being sent out.

11.1.2 BIOS Setup Options

The BIOS Setup Menu provides control over the thermal management functions, using the setting for the **`Advanced | Thermal Configuration | Thermal Configuration Parameters`** option. It offers four choices, namely:

- Critical Trip Point
- Passive Trip Point
- Active Trip Point
- DPTF Feature

It is desirable that some form of thermal management is enabled to handle operation at very high load and high temperature. Under normal conditions, even with high loads, the standard heatsink and specified forced or natural air-cooling are adequate to keep the processor operating within its limits even with the Thermal Management option set to Disabled. The BIOS setup option provides a means to enable additional protection if there is any concern about heat dissipation in the particular system being used.

11.2 Processor Thermal Status Indication

The User/PROCHOT LED may be programmed to indicate if the processor die has reached the critical temperature at which thermal management is activated, using SW7-1 (User/PROCHOT LED Mode switch). Figure 11-1 shows the location of this switch on the board, its settings and default position.

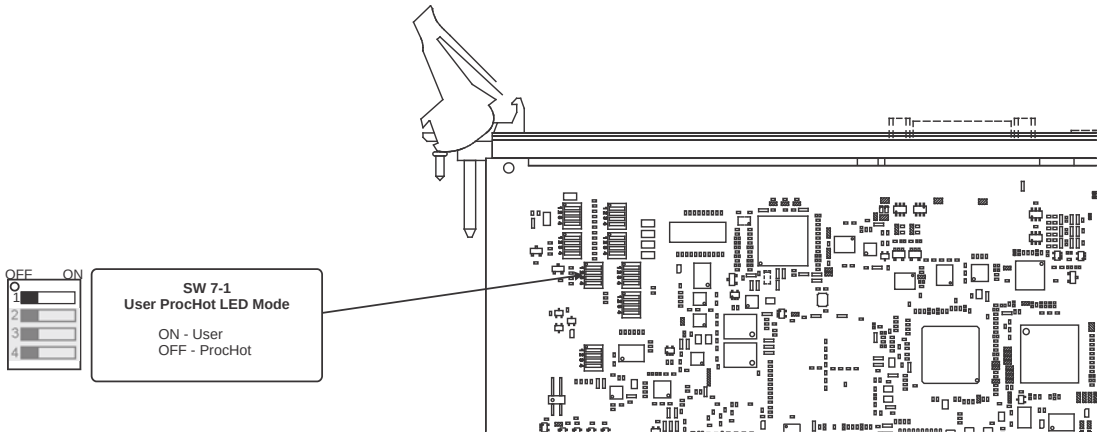

Figure 11-1 User/PROCHOT LED Mode Switch

A SPECIFICATIONS

A.1 Functional Specification

Processor:	• 4-core 1.91 GHz Intel® Atom™ processor E3845 (DDR3L-1333). • 1-core 1.46 GHz Intel® Atom™ processor E3815 (DDR3L-1066).
Level 1 Cache:	• 32 Kbytes instruction cache and 24 Kbytes data cache.
Level 2 Cache:	• 2 Mbytes (E3845) or 512 Kbytes (E3815) on-die RAM operating at core frequency.
Memory:	• Two 8 Mbyte Flash Serial EEPROM for BIOS and factory test firmware. • 4 Gbytes DDR3L single channel DRAM with ECC or 8 Gbytes DDR3L dual channel DRAM without ECC (4-core processor only). • Two 8 Kbytes Serial I^2C user EEPROM.
Interfaces:	• 64-bit VME interface utilizing IDT®'s Universe™ II VME-to-PCI bridge. • One RS232 serial channel via front panel connector using 16550 compatible UART. Limited set of signals. • One RS232/RS422/RS485 serial channel via rear P2 connector using 16550 compatible UART. Full set of signals in RS232 mode. • One RS232 interface via rear P2 connector (in selected board configurations only). • Two SATA interfaces via P2 connector and one SATA interface via rear P0 connector (in selected board configurations only) and on-board mass storage interfaces (HDD/SSD, CFast and SATA Flash Module). • Up to 3 x USB 2.0 interfaces, 1 via front panel connector (selected variants) and 2 via rear P2 connector - 1.5, 12 and 480 Mbps interfaces supported. • 1x USB 3.0 interface via front panel connector • Two single-width PMC/XMC sites supporting a 32/64-bit PCI interface up to 66 MHz or a PCI-X interface up to 100 MHz with 3.3V or 5.0V signaling. Each XMC site supports x1 PCIe, Gen2 interface. • PS/2 compatible keyboard / mouse interface via rear P2 connector (in selected board configurations only). • 2 x 10/100/1000 Mbps Ethernet interfaces via rear P0 connector. • 2 x 10/100/1000 Mbps Ethernet interfaces via front panel connectors. • DVI-D interface via rear P2 connector; resolutions up to 1600 x 1200 with up to 16 million colors. • DVI-I interface via front panel connector (in selected board configurations) DVI-D resolutions up to 1600 x 1200 with up to 16 million colors and VGA resolutions up to 2048 x 1536 with up to 16 million colors. • High definition audio via P2 connector (in selected board configurations only). • 4 General Purpose I/Os via rear P2 connector. • Push Button/LK1 Header Reset input via front panel (in selected board configurations) and/or via rear P2 connector.
Peripherals:	• Intel® SoC provides standard PC-AT architecture peripherals. • PC-AT Real Time Clock. • 32-bit Long Duration Timer with processor interrupt capability. • Watchdog Timer. • Trusted Platform Module (TPM, a factory build option).

SPECIFICATIONS

A.2 Environmental Specifications

	Standard Temperature, All Variants, N-Series	Extended Temperature, All variants, E-Series	Extended Temperature, All variants, K-Series	Rugged Conduction-Cooled, All Variants, RC-Series
Temperature Range (operating)	0°C to +70°C	-25°C to +70°C	-40°C to +85°C	-40°C to +85°C
Temperature Range (non-operating)	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	-55°C to +105°C
Temperature Rate of Change	1°C / min	2°C / min	3°C / min	3°C / min
Required Airflow (linear feet per minute)	Refer to Section A.3 for the graph showing the typical airflow for each processor and the temperature-series			Conduction Cooled
Relative Humidity (operating)	5% to 95%	5% to 95%	5% to 95%	5% to 95%
Relative Humidity (non-operating)	5% to 95%	5% to 95%	5% to 95%	5% to 95%
Humidity Protection	Optional	Optional	Yes	Yes
Altitude (operating)	0 to 15,000 ft (0 to 4,572m)	0 to 15,000 ft (0 to 4,572m)	0 to 15,000 ft (0 to 4,572m)	-1,000 to 50,000 ft (-305 to 15,240m)
Altitude (non-operating)	0 to 50,000 ft (0 to 15,240m)	0 to 50,000 ft (0 to 15,240m)	0 to 50,000 ft (0 to 15,240m)	-1,000 to 50,000 ft (-305 to 15,240m)

Table A-1 Environmental Specifications

NOTE: If the battery is fitted, the non-operating temperature range will be restricted to -20°C to +70ºC. This is because the SoC is partially operational when the battery is connected. The battery life will be reduced by storing at high temperatures due to increased self-discharge. It is therefore recommended that the battery be removed during storage.

NOTE: The RC-Series operating temperature range refers to the temperature at the board edge.

A.3 Airflow Requirements

The graph below illustrate the airflow levels required for various SoC configurations and operating temperatures using the loading conditions summarized for Activity Level C in Section A.7.1.

A.3.1 Airflow Requirements Graph (N-Series E-Series and K-Series)

The graph below illustrates the operating temperature versus airflow required for the 1-core and the 4-core processor configurations.

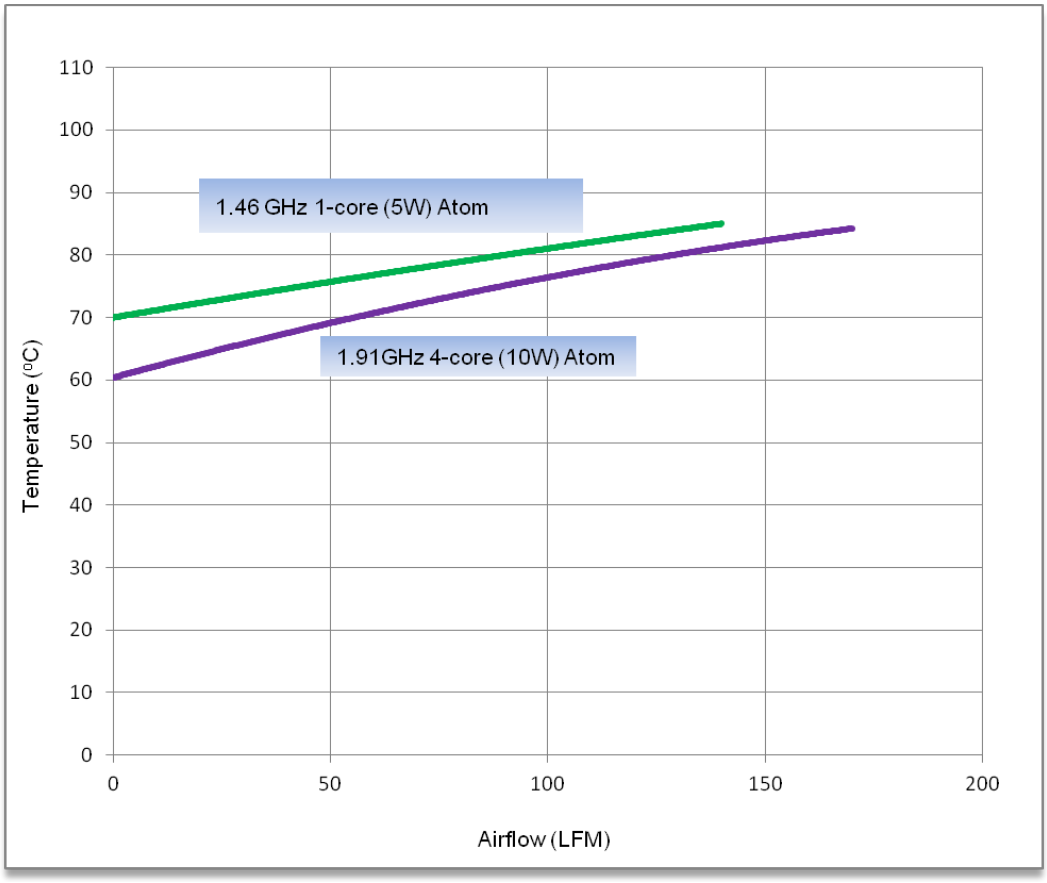

Figure A-1 Airflow Graph (N-Series, E-Series and K-Series)

A.4 Shock and Vibration Specification

	Standard Temperature, N-Series	Extended Temperature, E-Series	Extended Temperature, K-Series	Rugged Conduction-cooled, RC-Series
Shock	20g, 11ms, ½ sine	20g, 11ms, ½ sine	20g, 11ms, ½ sine	40g, 11ms, ½ sine
Sinusoidal Vibration	0.38mm pk at 5Hz to 36Hz 2g at 36Hz to 2kHz	0.38mm pk at 5Hz to 36Hz 2g at 36Hz to 2kHz	0.38mm pk at 5Hz to 36Hz 2g at 36Hz to 2kHz	N/A
Random Vibration	N/A	N/A	N/A	0.1 g^2/Hz (Note 1) VITA 47 V3

Table A-2 Shock and Vibration Specifications (Operating)

Note 1: VITA 47 Class V3: 5 Hz to 100 Hz, PSD increasing at 3dB/octave.
100 Hz to 1000 Hz, PSD = 0.1 g^2/Hz.
1000 Hz to 2000 Hz, PSD decreasing at 6dB/octave.

NOTE: All the above figures are for boards without an on-board mass storage option.

A.5 MTBF Values

Board Variant	Test used	Temperature	Environment	MTBF
VP E24/012	Telcordia	50°C	Ground Fixed	110600 hrs

Table A-3 MTBF Values

A.6 Dimensions

Height.....23.3cm
Depth.....16.0cm
Width.....2.0cm

Weight.....514g – N, E and K-Series

.....TBD - RC Series

NOTE: The above weights are without the mass storage kits and PMC/XMC modules.

A.7 Electrical Specification

A.7.1 Board Current Requirements

Variant	Processor Speed	Maximum Current	Typical Power (W)
VP E24/m1d-yz	1.91 GHz	4.8A	21.5W
VP E21/m1d-yz	1.46 GHz	3.9A	18W

Table A-4 Voltage and Current Requirements

1. These figures are for a board with 4 Gbytes DRAM. The 4-core processor variant with 8 Gbytes DRAM (VP E24/m16-yz) consumes 3 Watts (typical power) additionally.
2. These figures are for a board without on board SSD/HDD, PMC/XMC Module(s) or SATA Flash Module (AD 231/10x) fitted.
3. Typical power figures are the average board requirement while maintaining a 50% program execution load on all processor cores and an additional 60% load on the graphics core with the board operating at an ambient temperature of 25°C.
4. Maximum figures are the worst-case power dissipation that may occur for periods of at least 100ms duration with maximum processor activity and for maximum graphics activity with the board at the maximum operating temperature.
5. The maximum power figures include activity on four 1 Gbps Ethernet ports, four SATA ports and three USB ports.
6. The additional current for each rear Ethernet port running at 1 Gbps is approximately 0.2A at 3.3V.
7. Since all these components interact and are controlled by the Intel® Atom™ processor, the peak currents for all the interfaces will not occur simultaneously.
8. The figures in the table are those for the nominal voltage of +5V. The tolerance on this supply rail is +5% and -2.5%.
9. The +3.3V backplane power supply is not required.
10. ±12V supplies are provided for the PMC/XMC interface. These supplies do not need to be present if the XMC module does not require them. Current requirements are those of the fitted XMC module.
11. VCC_STDBY (P1 pin B31) Requirement: +5V +5%/-2.5%, current drawn does not exceed 10 µA.
12. There are no sequencing requirements for the VP E2x/msd between any of the supply rails during power up and power down, but any fitted PMC or XMC modules may have its own restrictions on voltage sequencing.

A.7.2 Power Supply Capability for PMC/XMC Modules

Variant	Max power dissipation per PMC/XMC module	Max current @ 3.3V per PMC/XMC module	Max current @ 5V per PMC/XMC module	Max current @ +12V per PMC/XMC module	Max current @ -12V per PMC/XMC module
VP E2x/msd (all variants)	25W	5A	5A	0.5A	0.5A

Table A-5 Current Supply Capability for PMC/XMC modules

A.8 Connectors - all variants except RC-Series

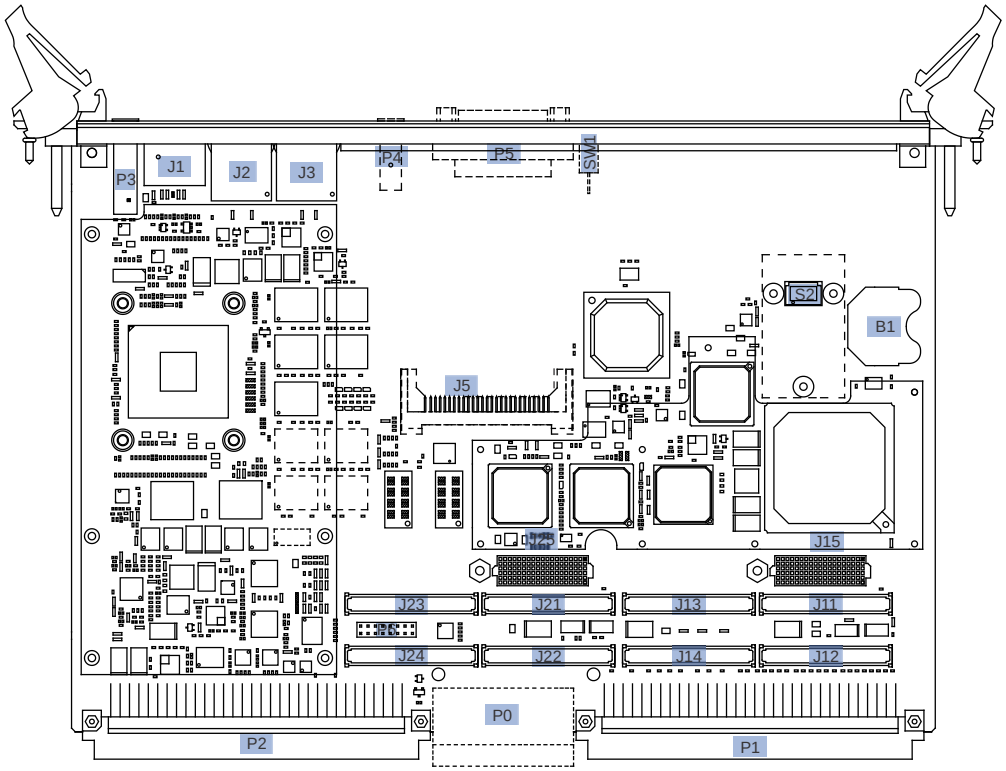

Figure A-2 Connector Layout – Top

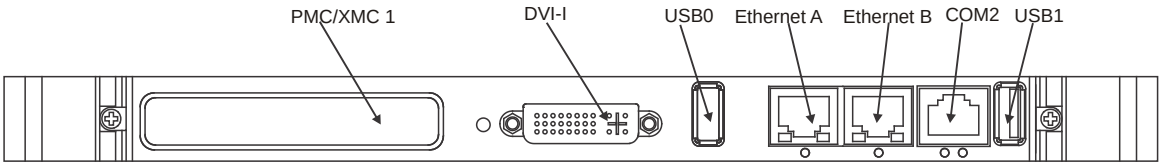

Figure A-3 Connector Layout – Front Panel for Single PMC/XMC site variants

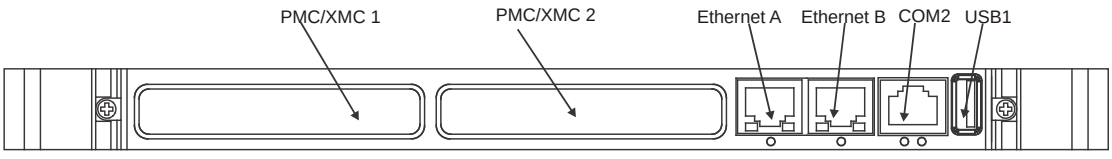

Figure A-4 Connector Layout – Front Panel for Dual PMC/XMC site variants

A.8.1 VME Interface P1 Pin-out

The VME interface P1 consists of a 160-pin connector with signals assigned as follows:

Pin	Row Z	Row A	Row B	Row C	Row D
1	-	D00	BBSY#	D08	+5V
2	GND	D01	BCLR#	D09	GND
3	-	D02	ACFAIL#	D10	-
4	GND	D03	BG0IN#	D11	-
5	-	D04	BG0OUT#	D12	-
6	GND	D05	BG1IN#	D13	-
7	-	D06	BG1OUT	D14	-
8	GND	D07	BG2IN#	D15	-
9	-	GND	BG2OUT#	GND	GAP#
10	GND	SYSCLK	BG3IN#	SYSFAIL#	GA0#
11	-	GND	BG3OUT#	BERR#	GA1#
12	GND	DS1#	BR0#	VME_SYSRST#	-
13	-	DS0#	BR1#	LWORD#	GA2#
14	GND	WRITE#	BR2#	AM5	-
15	-	GND	BR3#	A23	GA3#
16	GND	DTACK#	AM0	A22	-
17	-	GND	AM1	A21	GA4#
18	GND	AS#	AM2	A20	-
19	-	GND	AM3	A19	SMB_SCL††
20	GND	IACK#	GND	A18	-
21	-	IACKIN#	IPMB_SCL††	A17	SMB_SDA††
22	GND	IACKOUT#	IPMB_SDA††	A16	-
23	-	AM4	GND	A15	SMB_ALERT#††
24	GND	A07	IRQ7#	A14	-
25	-	A06	IRQ6#	A13	-
26	GND	A05	IRQ5#	A12	-
27	-	A04	IRQ4#	A11	-
28	GND	A03	IRQ3#	A10	-
29	-	A02	IRQ2#	A09	-
30	GND	A01	IRQ1#	A08	-
31	-	-12V	VCC_STDBY	+12V	GND
32	GND	+5V	+5V	+5V	+5V

Table A-6 VME Interface P1 Pin-out

NOTE: †† signals are optional

A.9 P2 and P0 Pin-outs - VP A45/01x compatible variants

This section defines the P2 (Section A.9.1) and P0 (Section A.9.2) connector pin-outs for the VP E2x/0sd-y1 variant compatible with the VP A45/01x (a legacy Concurrent Technologies processor board).

NOTE: Highlighted pins in the tables show functional differences between this build variant and other VP E2x/msd P2/P0 build connector variants.

A.9.1 P2 Pin-out - VP A45/01x compatible variants

NOTE: This P2 pin-out is compatible with the legacy VP A45/01x-5y (without P0) and VP A45/01x-6y (with P0).

Two build options support the P2 pin-out specified in Table A-7 below:

- VP E2x/0sd-11 (without P0)
- VP E2x/0sd-21 (with P0, Section A.9.2)

The auxiliary interface P2 consists of a 160-pin connector: PMC site 1 rear I/O is mapped to this connector, where the pin assignments conform to the mapping defined in ANSI/VITA 35 P4V2-64ac.

NOTE: The highlighted pins (MS, KBD, NC) show functional differences compared with Table A-9 (an alternative VP E2x/0sd P2 pin-out, dual PMC/XMC sites).

Pin	Column Z	Column A	Column B	Column C	Column D
1	GPIO0	PMC1_IO(2)	+5V	PMC1_IO(1)	DVI_TX0+
2	GND	PMC1_IO(4)	GND	PMC1_IO(3)	DVI_TX0-
3	GPIO2	PMC1_IO(6)	VME_RETRY#	PMC1_IO(5)	DVI_TX1+
4	GND	PMC1_IO(8)	VME_A(24)	PMC1_IO(7)	DVI_TX1-
5	GPIO1	PMC1_IO(10)	VME_A(25)	PMC1_IO(9)	DVI_TX2+
6	GND	PMC1_IO(12)	VME_A(26)	PMC1_IO(11)	DVI_TX2-
7	GPIO3	PMC1_IO(14)	VME_A(27)	PMC1_IO(13)	DVI_TXC+
8	GND	PMC1_IO(16)	VME_A(28)	PMC1_IO(15)	DVI_TXC-
9	COM1_DCD	PMC1_IO(18)	VME_A(29)	PMC1_IO(17)	VCC_USBC
10	GND	PMC1_IO(20)	VME_A(30)	PMC1_IO(19)	USBC_D-
11	COM1_TXD	PMC1_IO(22)	VME_A(31)	PMC1_IO(21)	USBC_D+
12	GND	PMC1_IO(24)	GND	PMC1_IO(23)	VCC_USBD
13	COM1_DTR	PMC1_IO(26)	+5V	PMC1_IO(25)	USBD_D+
14	GND	PMC1_IO(28)	VME_D(16)	PMC1_IO(27)	USBD_D-
15	COM1_RXD	PMC1_IO(30)	VME_D(17)	PMC1_IO(29)	MS_CLK#
16	GND	PMC1_IO(32)	VME_D(18)	PMC1_IO(31)	MS_DATA#
17	COM_RTN	PMC1_IO(34)	VME_D(19)	PMC1_IO(33)	SATA0_TX+
18	GND	PMC1_IO(36)	VME_D(20)	PMC1_IO(35)	SATA0_TX-
19	COM1_RTS	PMC1_IO(38)	VME_D(21)	PMC1_IO(37)	SATA0_RX+
20	GND	PMC1_IO(40)	VME_D(22)	PMC1_IO(39)	SATA0_RX-
21	COM1_DSR	PMC1_IO(42)	VME_D(23)	PMC1_IO(41)	SATA1_TX+
22	GND	PMC1_IO(44)	GND	PMC1_IO(43)	SATA1_TX-
23	COM1_CTS	PMC1_IO(46)	VME_D(24)	PMC1_IO(45)	SATA1_RX+
24	GND	PMC1_IO(48)	VME_D(25)	PMC1_IO(47)	SATA1_RX-
25	COM1_RI	PMC1_IO(50)	VME_D(26)	PMC1_IO(49)	DVI_DDCCLK
26	GND	PMC1_IO(52)	VME_D(27)	PMC1_IO(51)	DVI_DDCDATA
27	KBD_VCC	PMC1_IO(54)	VME_D(28)	PMC1_IO(53)	EXT_RESET#
28	GND	PMC1_IO(56)	VME_D(29)	PMC1_IO(55)	HOT_PLUG#
29	KBD_DATA#	PMC1_IO(58)	VME_D(30)	PMC1_IO(57)	NC
30	GND	PMC1_IO(60)	VME_D(31)	PMC1_IO(59)	NC
31	KBD_CLK#	PMC1_IO(62)	GND	PMC1_IO(61)	GND
32	GND	PMC1_IO(64)	+5V	PMC1_IO(63)	+5V

Table A-7 P2 Pin-out - VP A45/01x compatible variant

NOTE: The P2 pin-out in Table A-7 is defined for compatibility with the legacy VP A45/01x processor board, it is not recommended for new projects due to the legacy keyboard and mouse interfaces. For new projects see Section A.10 and Section A.11.

A.9.2 P0 Pin-out - VP A45/01x compatible variants

NOTE: This P0 pin-out is compatible with the legacy VP A45/01x-6y.

A single build option supports the P0 pin-out specified in Table A-8 below:

- VP E2x/0sd-21

(See Section A.9.1 for the P2 pin-out.)

The P0 connector consists of a 105-way IEC 61076-4-101 2 mm pitch connector: PMC site 2 rear I/O is mapped to this connector, where the pin assignments conform to the mapping defined in ANSI/VITA 35 P4V0-64.

Only the pin-out for Ethernet port C (ETHC) is compliant with ANSI/VITA 31.1.

NOTE: The highlighted pins (ETHC and ETHD LED signaling) show functional differences compared with Table A-10 (an alternative VP E2x/0sd P0 pin-out, dual PMC/XMC sites).

Pin	Row F	Row E	Row D	Row C	Row B	Row A
1	GND	-	-	-	-	-
2	GND	ETHC_DC-	ETHC_DC+	GND	ETHC_DA-	ETHC_DA+
3	GND	ETHC_DD-	ETHC_DD+	GND	ETHC_DB-	ETHC_DB+
4	GND	PMC2_IO(1)	PMC2_IO(2)	PMC2_IO(3)	PMC2_IO(4)	PMC2_IO(5)
5	GND	PMC2_IO(6)	PMC2_IO(7)	PMC2_IO(8)	PMC2_IO(9)	PMC2_IO(10)
6	GND	PMC2_IO(11)	PMC2_IO(12)	PMC2_IO(13)	PMC2_IO(14)	PMC2_IO(15)
7	GND	PMC2_IO(16)	PMC2_IO(17)	PMC2_IO(18)	PMC2_IO(19)	PMC2_IO(20)
8	GND	PMC2_IO(21)	PMC2_IO(22)	PMC2_IO(23)	PMC2_IO(24)	PMC2_IO(25)
9	GND	ETHD_DC-	ETHD_DC+	GND	ETHD_DA-	ETHD_DA+
10	GND	ETHD_DD-	ETHD_DD+	GND	ETHD+DB-	ETHD_DB+
11	GND	ETHD_ACT#	ETHC_ACT#	-	ETHD_SPD#	ETHC_SPD#
12	GND	PMC2_IO(26)	PMC2_IO(27)	PMC2_IO(28)	PMC2_IO(29)	PMC2_IO(30)
13	GND	PMC2_IO(31)	PMC2_IO(32)	PMC2_IO(33)	PMC2_IO(34)	PMC2_IO(35)
14	GND	PMC2_IO(36)	PMC2_IO(37)	PMC2_IO(38)	PMC2_IO(39)	PMC2_IO(40)
15	GND	PMC2_IO(41)	PMC2_IO(42)	PMC2_IO(43)	PMC2_IO(44)	PMC2_IO(45)
16	GND	PMC2_IO(46)	PMC2_IO(47)	PMC2_IO(48)	PMC2_IO(49)	PMC2_IO(50)
17	GND	PMC2_IO(51)	PMC2_IO(52)	PMC2_IO(53)	PMC2_IO(54)	PMC2_IO(55)
18	GND	PMC2_IO(56)	PMC2_IO(57)	PMC2_IO(58)	PMC2_IO(59)	PMC2_IO(60)
19	GND	PMC2_IO(61)	PMC2_IO(62)	PMC2_IO(63)	PMC2_IO(64)	-

Table A-8 P0 Pin-out - VP A45/01x compatible variant

NOTE: The P0 pin-out in Table A-8 is defined for compatibility with the legacy VP A45/01x processor board, it is not recommended for new projects due to the legacy keyboard and mouse interfaces on the P2 connector (Table A-7). For new projects see Section A.10 and Section A.11.

NOTE: The P0 connector is a factory build option and is not available on all variants.

A.10 P2 and P0 Pin-outs - Dual PMC/XMC sites variants

This section defines the P2 (Section A.10.1) and P0 (Section A.10.2) connector pin-outs for the VP E2x/0sd-y2 dual PMC/XMC sites variant

NOTE: Highlighted pins in the tables show functional differences between this build variant and other VP E2x/msd P2/P0 connector build variants.

A.10.1 P2 Pin-out - Dual PMC/XMC sites variants

Two build options support the P2 pin-out specified in Table A-9:

- VP E2x/0sd-12 (without P0)
- VP E2x/0sd-22 (with P0, Section A.10.2)

The auxiliary interface P2 consists of a 160-pin connector: PMC site 1 rear I/O is mapped to this connector, where the pin assignments conform to the mapping defined in ANSI/VITA 35 P4V2-64ac.

NOTE: The highlighted pins (COM3, LINEIN, LINEOUT) show functional differences compared with Table A-7 (the legacy VP A45/01x variant).

Pin	Column Z	Column A	Column B	Column C	Column D
1	GPIO0	PMC1_IO(2)	+5V	PMC1_IO(1)	DVI_TX0+
2	GND	PMC1_IO(4)	GND	PMC1_IO(3)	DVI_TX0-
3	GPIO2	PMC1_IO(6)	VME_RETRY#	PMC1_IO(5)	DVI_TX1+
4	GND	PMC1_IO(8)	VME_A(24)	PMC1_IO(7)	DVI_TX1-
5	GPIO1	PMC1_IO(10)	VME_A(25)	PMC1_IO(9)	DVI_TX2+
6	GND	PMC1_IO(12)	VME_A(26)	PMC1_IO(11)	DVI_TX2-
7	GPIO3	PMC1_IO(14)	VME_A(27)	PMC1_IO(13)	DVI_TXC+
8	GND	PMC1_IO(16)	VME_A(28)	PMC1_IO(15)	DVI_TXC-
9	COM1_DCD	PMC1_IO(18)	VME_A(29)	PMC1_IO(17)	VCC_USBC
10	GND	PMC1_IO(20)	VME_A(30)	PMC1_IO(19)	USBC_D-
11	COM1_TXD	PMC1_IO(22)	VME_A(31)	PMC1_IO(21)	USBC_D+
12	GND	PMC1_IO(24)	GND	PMC1_IO(23)	VCC_USBD
13	COM1_DTR	PMC1_IO(26)	+5V	PMC1_IO(25)	USBD_D+
14	GND	PMC1_IO(28)	VME_D(16)	PMC1_IO(27)	USBD_D-
15	COM1_RXD	PMC1_IO(30)	VME_D(17)	PMC1_IO(29)	COM3_TXD
16	GND	PMC1_IO(32)	VME_D(18)	PMC1_IO(31)	COM3_RXD
17	COM_RTN	PMC1_IO(34)	VME_D(19)	PMC1_IO(33)	SATA0_TX+
18	GND	PMC1_IO(36)	VME_D(20)	PMC1_IO(35)	SATA0_TX-
19	COM1_RTS	PMC1_IO(38)	VME_D(21)	PMC1_IO(37)	SATA0_RX+
20	GND	PMC1_IO(40)	VME_D(22)	PMC1_IO(39)	SATA0_RX-
21	COM1_DSR	PMC1_IO(42)	VME_D(23)	PMC1_IO(41)	SATA1_TX+
22	GND	PMC1_IO(44)	GND	PMC1_IO(43)	SATA1_TX-
23	COM1_CTS	PMC1_IO(46)	VME_D(24)	PMC1_IO(45)	SATA1_RX+
24	GND	PMC1_IO(48)	VME_D(25)	PMC1_IO(47)	SATA1_RX-
25	COM1_RI	PMC1_IO(50)	VME_D(26)	PMC1_IO(49)	DVI_DDCCLK
26	GND	PMC1_IO(52)	VME_D(27)	PMC1_IO(51)	DVI_DDCDATA
27	KBD_VCC	PMC1_IO(54)	VME_D(28)	PMC1_IO(53)	EXT_RESET#
28	GND	PMC1_IO(56)	VME_D(29)	PMC1_IO(55)	HOT_PLUG#
29	LINEIN_R	PMC1_IO(58)	VME_D(30)	PMC1_IO(57)	LINEOUT_R
30	GND	PMC1_IO(60)	VME_D(31)	PMC1_IO(59)	LINEOUT_L
31	LINEIN_L	PMC1_IO(62)	GND	PMC1_IO(61)	GND
32	GND	PMC1_IO(64)	+5V	PMC1_IO(63)	+5V

Table A-9 P2 Pin-out - Dual PMC/XMC sites variant

CAUTION: This pin-out table is NOT compatible with the legacy VP A45/01x processor board. See Section A.9.

A.10.2 P0 Pin-out - Dual PMC/XMC sites variants

A single build option supports the P0 pin-out specified in Table A-10:

- VP E2x/0sd-22

(See Section A.10.1 for the P2 pin-out.)

The P0 connector consists of a 105-way IEC 61076-4-101 2 mm pitch connector: PMC site 2 rear I/O is mapped to this connector, where the pin assignments conform to the mapping defined in ANSI/VITA 35 P4V0-64.

Only the pin-out for Ethernet port C (ETHC) is compliant with ANSI/VITA 31.1.

NOTE: The highlighted pins (SATA2) show functional differences compared with Table A-8 (legacy VP A45/01x variant).

The highlighted pins (PMC2_IO) show functional differences compared with Table A-12 (the single PMC/XMC site variant).

Pin	Row F	Row E	Row D	Row C	Row B	Row A
1	GND	-	-	-	-	-
2	GND	ETHC_DC-	ETHC_DC+	GND	ETHC_DA-	ETHC_DA+
3	GND	ETHC_DD-	ETHC_DD+	GND	ETHC_DB-	ETHC_DB+
4	GND	PMC2_IO(1)	PMC2_IO(2)	PMC2_IO(3)	PMC2_IO(4)	PMC2_IO(5)
5	GND	PMC2_IO(6)	PMC2_IO(7)	PMC2_IO(8)	PMC2_IO(9)	PMC2_IO(10)
6	GND	PMC2_IO(11)	PMC2_IO(12)	PMC2_IO(13)	PMC2_IO(14)	PMC2_IO(15)
7	GND	PMC2_IO(16)	PMC2_IO(17)	PMC2_IO(18)	PMC2_IO(19)	PMC2_IO(20)
8	GND	PMC2_IO(21)	PMC2_IO(22)	PMC2_IO(23)	PMC2_IO(24)	PMC2_IO(25)
9	GND	ETHD_DC-	ETHD_DC+	GND	ETHD_DA-	ETHD_DA+
10	GND	ETHD_DD-	ETHD_DD+	GND	ETHD+DB-	ETHD_DB+
11	GND	SATA2_TX-	SATA2_TX+	-	SATA2_RX-	SATA2_RX+
12	GND	PMC2_IO(26)	PMC2_IO(27)	PMC2_IO(28)	PMC2_IO(29)	PMC2_IO(30)
13	GND	PMC2_IO(31)	PMC2_IO(32)	PMC2_IO(33)	PMC2_IO(34)	PMC2_IO(35)
14	GND	PMC2_IO(36)	PMC2_IO(37)	PMC2_IO(38)	PMC2_IO(39)	PMC2_IO(40)
15	GND	PMC2_IO(41)	PMC2_IO(42)	PMC2_IO(43)	PMC2_IO(44)	PMC2_IO(45)
16	GND	PMC2_IO(46)	PMC2_IO(47)	PMC2_IO(48)	PMC2_IO(49)	PMC2_IO(50)
17	GND	PMC2_IO(51)	PMC2_IO(52)	PMC2_IO(53)	PMC2_IO(54)	PMC2_IO(55)
18	GND	PMC2_IO(56)	PMC2_IO(57)	PMC2_IO(58)	PMC2_IO(59)	PMC2_IO(60)
19	GND	PMC2_IO(61)	PMC2_IO(62)	PMC2_IO(63)	PMC2_IO(64)	-

Table A-10 P0 Pin-out - Dual PMC/XMC sites variant

NOTE: The P0 connector is a factory build option and is not available on all variants.

CAUTION: This pin-out table is NOT compatible with the legacy VP A45/01x processor board. See Section A.9.

A.11 P2 and P0 Pin-outs - Single PMC/XMC site variants

This section defines the P2 (Section A.11.1) and P0 (Section A.11.2) connector pin-outs for the VP E2x/4sd-y2 (single PMC/XMC site variant).

NOTE: Highlighted pins in the tables show functional differences between this build variant and other VP E2x/msd P2/P0 connector build variants.

A.11.1 P2 Pin-out - Single PMC/XMC site variants

Two build options support the P2 pin-out specified in Table A-11:

- VP E2x/4sd-12 (without P0)
- VP E2x/4sd-22 (with P0, Section A.11.2).

The auxiliary interface P2 consists of a 160-pin connector: PMC site 1 rear I/O is mapped to this connector, where the pin assignments conform to the mapping defined in ANSI/VITA 35 P4V2-64ac.

NOTE: There are no functional differences compared with Table A-9 (the dual PMC/XMC sites variant).

Pin	Column Z	Column A	Column B	Column C	Column D
1	GPIO0	PMC1_IO(2)	+5V	PMC1_IO(1)	DVI_TX0+
2	GND	PMC1_IO(4)	GND	PMC1_IO(3)	DVI_TX0-
3	GPIO2	PMC1_IO(6)	VME_RETRY#	PMC1_IO(5)	DVI_TX1+
4	GND	PMC1_IO(8)	VME_A(24)	PMC1_IO(7)	DVI_TX1-
5	GPIO1	PMC1_IO(10)	VME_A(25)	PMC1_IO(9)	DVI_TX2+
6	GND	PMC1_IO(12)	VME_A(26)	PMC1_IO(11)	DVI_TX2-
7	GPIO3	PMC1_IO(14)	VME_A(27)	PMC1_IO(13)	DVI_TXC+
8	GND	PMC1_IO(16)	VME_A(28)	PMC1_IO(15)	DVI_TXC-
9	COM1_DCD	PMC1_IO(18)	VME_A(29)	PMC1_IO(17)	VCC_USBC
10	GND	PMC1_IO(20)	VME_A(30)	PMC1_IO(19)	USBC_D-
11	COM1_TXD	PMC1_IO(22)	VME_A(31)	PMC1_IO(21)	USBC_D+
12	GND	PMC1_IO(24)	GND	PMC1_IO(23)	VCC_USBD
13	COM1_DTR	PMC1_IO(26)	+5V	PMC1_IO(25)	USBD_D+
14	GND	PMC1_IO(28)	VME_D(16)	PMC1_IO(27)	USBD_D-
15	COM1_RXD	PMC1_IO(30)	VME_D(17)	PMC1_IO(29)	COM3_TXD
16	GND	PMC1_IO(32)	VME_D(18)	PMC1_IO(31)	COM3_RXD
17	COM_RTN	PMC1_IO(34)	VME_D(19)	PMC1_IO(33)	SATA0_TX+
18	GND	PMC1_IO(36)	VME_D(20)	PMC1_IO(35)	SATA0_TX-
19	COM1_RTS	PMC1_IO(38)	VME_D(21)	PMC1_IO(37)	SATA0_RX+
20	GND	PMC1_IO(40)	VME_D(22)	PMC1_IO(39)	SATA0_RX-
21	COM1_DSR	PMC1_IO(42)	VME_D(23)	PMC1_IO(41)	SATA1_TX+
22	GND	PMC1_IO(44)	GND	PMC1_IO(43)	SATA1_TX-
23	COM1_CTS	PMC1_IO(46)	VME_D(24)	PMC1_IO(45)	SATA1_RX+
24	GND	PMC1_IO(48)	VME_D(25)	PMC1_IO(47)	SATA1_RX-
25	COM1_RI	PMC1_IO(50)	VME_D(26)	PMC1_IO(49)	DVI_DDCCLK
26	GND	PMC1_IO(52)	VME_D(27)	PMC1_IO(51)	DVI_DDCDATA
27	KBD_VCC	PMC1_IO(54)	VME_D(28)	PMC1_IO(53)	EXT_RESET#
28	GND	PMC1_IO(56)	VME_D(29)	PMC1_IO(55)	HOT_PLUG#
29	LINEIN_R	PMC1_IO(58)	VME_D(30)	PMC1_IO(57)	LINEOUT_R
30	GND	PMC1_IO(60)	VME_D(31)	PMC1_IO(59)	LINEOUT_L
31	LINEIN_L	PMC1_IO(62)	GND	PMC1_IO(61)	GND
32	GND	PMC1_IO(64)	+5V	PMC1_IO(63)	+5V

Table A-11 P2 Pin-out - Single PMC/XMC site variant

CAUTION: This pin-out table is NOT compatible with the legacy VP A45/01x processor board.

A.11.2 P0 Pin-out - Single PMC/XMC site variants

A single build option supports the P0 pin-out specified in Table A-12:

- VP E2x/4sd-22

(See Section A.11.1 for the P2 pin-out.)

The P0 connector consists of a 105-way IEC 61076-4-101 2 mm pitch connector.

Only the pin-out for Ethernet port C (ETHC) is compliant with ANSI/VITA 31.1.

NOTE: The highlighted pins (not used by the VP E2x/4sd-22 variant) show functional differences compared with Table A-10 (the dual PMC/XMC sites variant).

Pin	Row F	Row E	Row D	Row C	Row B	Row A
1	GND	-	-	-	-	-
2	GND	ETHC_DC-	ETHC_DC+	GND	ETHC_DA-	ETHC_DA+
3	GND	ETHC_DD-	ETHC_DD+	GND	ETHC_DB-	ETHC_DB+
4	GND	-	-	-	-	-
5	GND	-	-	-	-	-
6	GND	-	-	-	-	-
7	GND	-	-	-	-	-
8	GND	-	-	-	-	-
9	GND	ETHD_DC-	ETHD_DC+	GND	ETHD_DA-	ETHD_DA+
10	GND	ETHD_DD-	ETHD_DD+	GND	ETHD+DB-	ETHD_DB+
11	GND	SATA2_TX-	SATA2_TX+	-	SATA2_RX-	SATA2_RX+
12	GND	-	-	-	-	-
13	GND	-	-	-	-	-
14	GND	-	-	-	-	-
15	GND	-	-	-	-	-
16	GND	-	-	-	-	-
17	GND	-	-	-	-	-
18	GND	-	-	-	-	-
19	GND	-	-	-	-	-

Table A-12 P0 Pin-out - Single PMC/XMC site variant

NOTE: The P0 connector is a factory build option and is not available on all variants.

CAUTION: This pin-out table is NOT compatible with the legacy VP A45/01x processor board.

A.12 PMC Site Connector Pin-outs

The Signal assignments on the PMC connectors are shown in Table A-13, Table A-14, Table A-15 and Table A-16.

Pin	Signal	Pin	Signal
1	-	2	-12V
3	GND	4	INTA#
5	INTB#	6	INTC#
7	BUSMODE1#	8	+5V
9	INTD#	10	-
11	GND	12	+3.3V††
13	CLK	14	GND
15	GND	16	GNT#
17	REQ#	18	+5V
19	V (I/O)	20	AD(31)
21	AD(28)	22	AD(27)
23	AD(25)	24	GND
25	GND	26	C/BE(3)#
27	AD(22)	28	AD(21)
29	AD(19)	30	+5V
31	V (I/O)	32	AD(17)
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5V
39	GND	40	LOCK#
41	SDONE#	42	SBO#
43	PAR	44	GND
45	V (I/O)	46	AD(15)
47	AD(12)	48	AD(11)
49	AD(09)	50	+5V
51	GND	52	C/BE(0)#
53	AD(06)	54	AD(05)
55	AD(04)	56	GND
57	V (I/O)	58	AD(03)
59	AD(02)	60	AD(01)
61	AD(00)	62	+5V
63	GND	64	REQ64#

V (I/O) can be +5V or +3.3 V depending on-board configuration
†† pulled high via 10KΩ resistor.
NOTE: 3.3V is generated in VP E2x/msd and other voltages +5V and -12V are backplane voltages.

Table A-13 PMC Connector J11 and J21 Pin-outs

Pin	Signal	Pin	Signal
1	+12V	2	-
3	-	4	-
5	-	6	GND
7	GND	8	-
9	-	10	-
11	+3.3V††	12	+3.3V
13	RST#	14	GND
15	+3.3V	16	GND
17	-	18	GND
19	AD(30)	20	AD(29)
21	GND	22	AD(26)
23	AD(24)	24	+3.3V
25	IDSEL	26	AD(23)
27	+3.3V	28	AD(20)
29	AD(18)	30	GND
31	AD(16)	32	C/BE(2)#
33	GND	34	IDSEL B
35	TRDY#	36	+3.3V
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3V	42	SERR#
43	C/BE(1)#	44	GND
45	AD(14)	46	AD(13)
47	M66EN	48	AD(10)
49	AD(08)	50	+3.3V
51	AD(07)	52	REQ B#
53	+3.3V	54	GNT B#
55	PMC-RSVD	56	GND
57	PMC-RSVD	58	EREADY††
59	GND	60	-
61	ACK64#	62	+3.3V
63	GND	64	+3.3V††

†† pulled high via 10KΩ resistor.

NOTE: 3.3V is generated in VP E2x/msd and other voltage of +12V is backplane voltage.

Table A-14 PMC Connector J12 and J22 Pin-outs

Pin	Signal	Pin	Signal
1	-	2	GND
3	GND	4	C/BE(7)#
5	C/BE(6)#	6	C/BE(5)#
7	C/BE(4)#	8	GND
9	V(I/O)	10	PAR64
11	AD(63)	12	AD(62)
13	AD(61)	14	GND
15	GND	16	AD(60)
17	AD(59)	18	AD(58)
19	AD(57)	20	GND
21	V(I/O)	22	AD(56)
23	AD(55)	24	AD(54)
25	AD(53)	26	GND
27	GND	28	AD(52)
29	AD(51)	30	AD(50)
31	AD(49)	32	GND
33	GND	34	AD(48)
35	AD(47)	36	AD(46)
37	AD(45)	38	GND
39	V(I/O)	40	AD(44)
41	AD(43)	42	AD(42)
43	AD(41)	44	GND
45	GND	46	AD(40)
47	AD(39)	48	AD(38)
49	AD(37)	50	GND
51	GND	52	AD(36)
53	AD(35)	54	AD(34)
55	AD(33)	56	GND
57	V(I/O)	58	AD(32)
59	-	60	-
61	-	62	GND
63	GND	64	-

Table A-15 PMC Connector J13 and J23 Pin-out

Pin	Signal	Pin	Signal
1	I/O 1	2	I/O 2
3	I/O 3	4	I/O 4
5	I/O 5	6	I/O 6
7	I/O 7	8	I/O 8
9	I/O 9	10	I/O 10
11	I/O 11	12	I/O 12
13	I/O 13	14	I/O 14
15	I/O 15	16	I/O 16
17	I/O 17	18	I/O 18
19	I/O 19	20	I/O 20
21	I/O 21	22	I/O 22
23	I/O 23	24	I/O 24
25	I/O 25	26	I/O 26
27	I/O 27	28	I/O 28
29	I/O 29	30	I/O 30
31	I/O 31	32	I/O 32
33	I/O 33	34	I/O 34
35	I/O 35	36	I/O 36
37	I/O 37	38	I/O 38
39	I/O 39	40	I/O 40
41	I/O 41	42	I/O 42
43	I/O 43	44	I/O 44
45	I/O 45	46	I/O 46
47	I/O 47	48	I/O 48
49	I/O 49	50	I/O 50
51	I/O 51	52	I/O 52
53	I/O 53	54	I/O 54
55	I/O 55	56	I/O 56
57	I/O 57	58	I/O 58
59	I/O 59	60	I/O 60
61	I/O 61	62	I/O 62
63	I/O 63	64	I/O 64

Table A-16 PMC Connector J14 and J24 Pin-outs

A.13 XMC Site Connector Pin-out

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	PET0p0	PET0n0	+3.3V	-	-	+5V
2	GND	GND	PULL DOWN	GND	GND	RESET#
3	-	-	+3.3V	-	-	+5V
4	GND	GND	PULL DOWN	GND	GND	PULL UP
5	-	-	+3.3V	-	-	+5V
6	GND	GND	PULL UP	GND	GND	+12V
7	-	-	+3.3V	-	-	+5V
8	GND	GND	PULL UP	GND	GND	-12V
9	-	-	-	-	-	+5V
10	GND	GND	-	GND	GND	GA0
11	PER0p0	PER0n0	MBIST#	-	-	+5V
12	GND	GND	GA1	GND	GND	PRSNT#
13	-	-	+3.3V	-	-	+5V
14	GND	GND	GA2	GND	GND	MSDA
15	-	-	-	-	-	+5V
16	GND	GND	PULL UP	GND	GND	MSCL
17	-	-	-	-	-	-
18	GND	GND	-	GND	GND	-
19	REFCLK+	REFCLK-	-	WAKE#	-	-

Table A-17 XMC Site Connector J15 and J25 Pin-out

NOTE: The terminology in the above table matches that used in the XMC specification, VITA 42.3. The PET0x0 signals are used to receive data from the XMC module (i.e. they are the XMC module's transmit signals). The PER0x0 signals are used to send data to the XMC module (i.e. they are the XMC module's receive signals).

NOTE: 3.3V is generated in VP E2x/msd and other voltages +5V, +12V and -12V are backplane voltages.

A.14 Other I/O Interface Connectors

A.14.1 Serial Interface - J1

The COM2 RS232 serial interface uses a RJ45 connector with signals assigned as follows:

Pin	Signal	Direction
1	RTS - Request To Send	Output from board
2	DTR - Data Terminal Ready	Output from board
3	RETURN (GND)	-
4	TX - Tx Data	Output from board
5	RX - Rx Data	Input to board
6	DCD – Data Carrier Detect	Input to board
7	DSR - Data Set Ready	Input to board
8	CTS - Clear To Send	Input to board

Table A-18 Serial Interface (J1) Pin-out

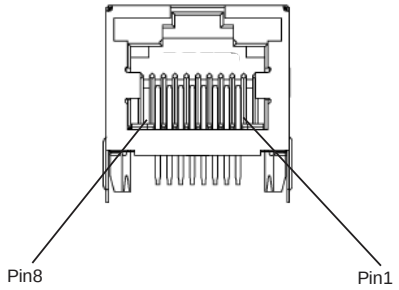

Figure A-5 Serial Interface J1 - Pin Map

A.14.2 USB3.0/2.0 Interface - P3

The USB3.0 Interface uses 9-way USB3.0 connectors with USB3.0/2.0 signals assigned as follows:

Pin	Signal
1	USBA_PWR (+5V)
2	USBA_D-
3	USBA_D+
4	GND
5	USBE_Rx-
6	USBE_Rx+
7	GND
8	USBE_Tx-
9	USBE_Tx+

Table A-19 USB 3.0/2.0 Connector P3 - Pin-out

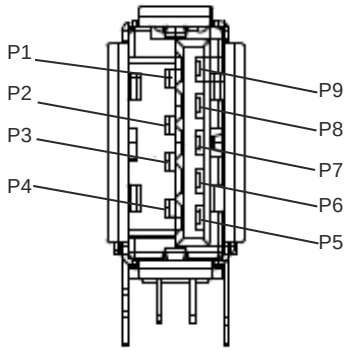

Figure A-6 USB 3.0/2.0 Connector P3 - Pin Map

A.14.3 Ethernet Interface - J2 and J3

The front panel Ethernet interface J2 and J3 uses an 8-way RJ45 connector with signals assigned as follows:

Pin	Signal
1	DA+
2	DA-
3	DB+
4	DC+
5	DC-
6	DB-
7	DD+
8	DD-

Table A-20 Ethernet Interface - J2 and J3 Pin-out

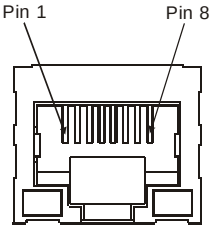

Figure A-7 Ethernet Interface - J2 and J3 Pin Map

A.14.4 DVI-I Interface - P5

The DVI-I interface comprises of both DVI-D and VGA interfaces on a single connector. Both VGA and DVI-D signals are available, but not simultaneously.

NOTE: This option is available only with the VP E2x/4sd Single XMC site variants.

Pin	Signal	Pin	Signal
1	DVI_TX2-	2	DVI_TX2+
3	GND	4	NC
5	NC	6	DVI_DDCCLK
7	DVI_DDCDATA	8	VGA_VSYNC
9	DVI_TX1-	10	DVI_TX1+
11	GND	12	NC
13	NC	14	VCC
15	GND	16	HOT_PLUG#
17	DVI_TX0-	18	DVI_TX0+
19	GND	20	NC
21	NC	22	GND
23	DVI_TXC+	24	DVI_TXC-
C1	VGA_RED	C2	VGA_GREEN
C3	VGA_BLUE	C4	VGA_HSYNC
C5A	VGA_GND		
C5B	VGA_GND		

Table A-21 DVI-I connector - P5 Pin-out

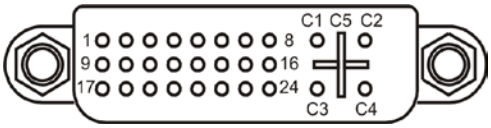

Figure A-8 DVI-I Connector - P3 Pin Map

A.14.5 USB Interface - P4

The front panel USB Interface P4 uses a 4-way USB 2.0 connector with signals assigned as follows:

Pin	Signal
1	USBB_VPWR
2	USBB_D-
3	USBB_D+
4	USB GND

Table A-22 USB Interface - P4 Pin-out

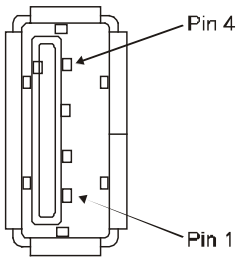

Figure A-9 USB Interface - P4 Pin Map

A.14.6 On-Board SATA Flash Module Option Interface - S2

Pin	Signal	Pin	Signal
1	GND	2	GND
3	SATA_TX+	4	+3.3V
5	SATA_TX-	6	+3.3V
7	GND	8	+3.3V
9	-	10	GND
11	-	12	NC
13	GND	14	GND
15	SATA_RX+	16	WRITE_PROT#
17	SATA_RX-	18	RESET#
19	GND	20	PRESENT#

Table A-23 On-Board SATA Flash Module Option Interface - S2 Pin-out

NOTE: This connector forms part of the SATA on-board AD 231/10x SATA Flash Module option. Contact your distributor or Concurrent Technologies for details.

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B REAR TRANSITION MODULES

B.1 Introduction

This section details all the Rear Transition Modules (RTMs) available for use with the VP E2x/msd. Each RTM provides a means of connecting interface cables to the rear I/O of the VP E2x/msd.

All RTMs utilize a 5-row P2 connector for rear I/O.

An overview of each RTM is given with a reference to a pin-out table for each of the connectors identified.

REAR TRANSITION MODULES

B.2 RTM List

The following RTMs are suitable for use with the VP E2x/msd:

Sales Part No.	Board Number (as marked on PCB)
AD VP2/020-10	721-6249-10
AD VP2/020-30	721-6249-11
AD VP2/033-10	TBD
AD VP2/033-30	721-6330-11
AD VP2/433-30	721-6330-10

Table B-1 Rear Transition Module List

B.3 AD VP2/020-10

The AD VP2/020-10 is a 160-way P2 backplane RTM for the VP E2x/msd. It provides one 68-way SCSI-3 style socket for PMC1 I/O, a PS/2 keyboard and mouse connector, Push Button, DVI-D connector, two USB and two SATA connectors with additional headers for other miscellaneous I/O functions.

This RTM requires one slot width and a minimum of 115 mm behind the backplane.

B.3.1 Layout

The Figure B-1 shows the locations of the connectors, jumpers and switches. The following sections describe the switch and jumper options.

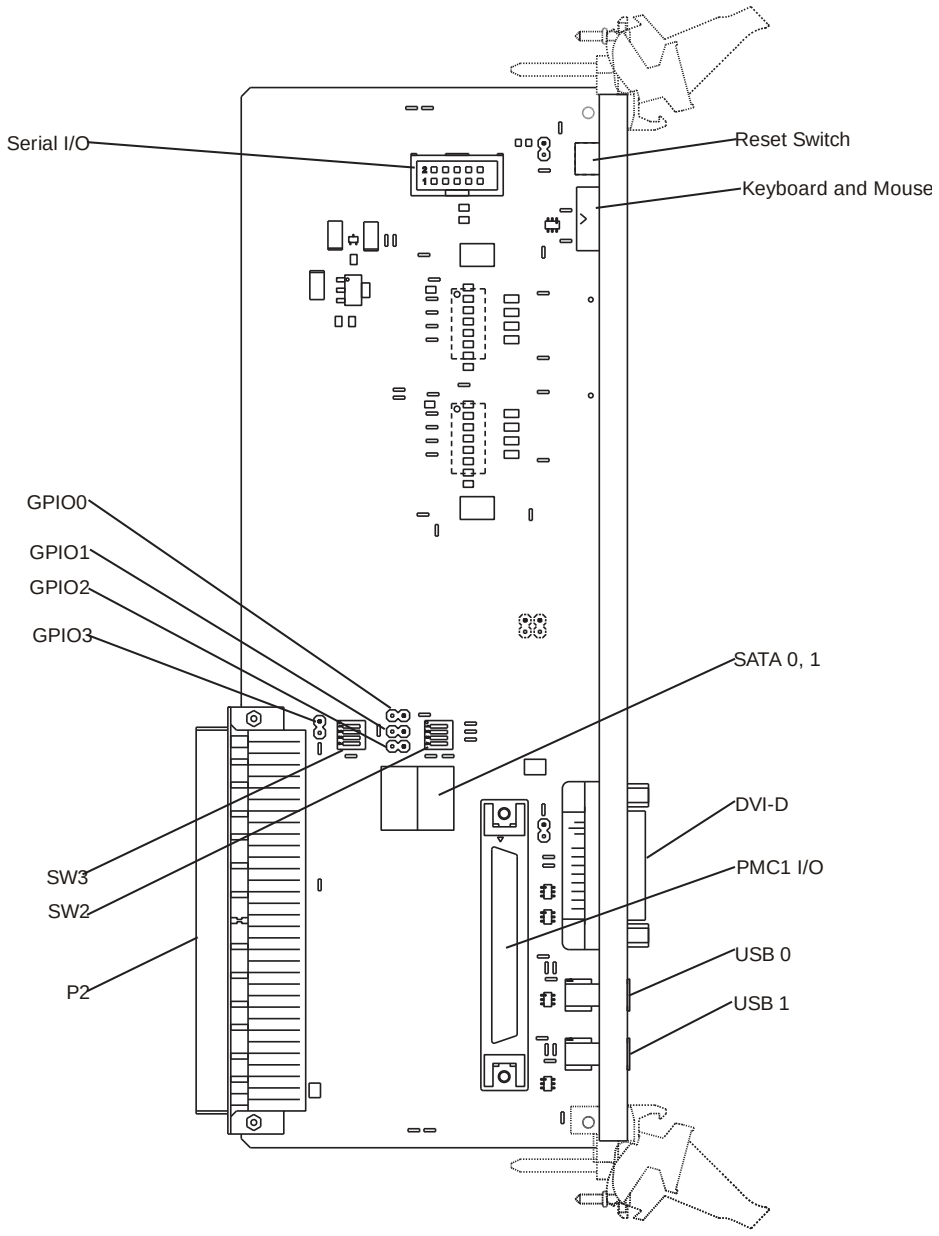

Figure B-1 AD VP2/020-10 RTM Connectors and Switches

B.3.2 Pin-out Tables

Signal Name	Details
USB0 and USB1	Table B-6
Keyboard and Mouse	Table B-7
Serial I/O	Table B-9
PMC1 I/O	Table B-11
DVI-D	Table B-14
SATA 0 and 1	Table B-13
GPIO0-2	Figure B-2
GPIO3	Figure B-2

Table B-2 AD VP2/020-10 Connector List

B.3.3 GPIO Interface

The GPIO connections on this RTM provide a few different options for the I/O interface.

Figure B-2 shows a simplified schematic diagram of the functions provided.

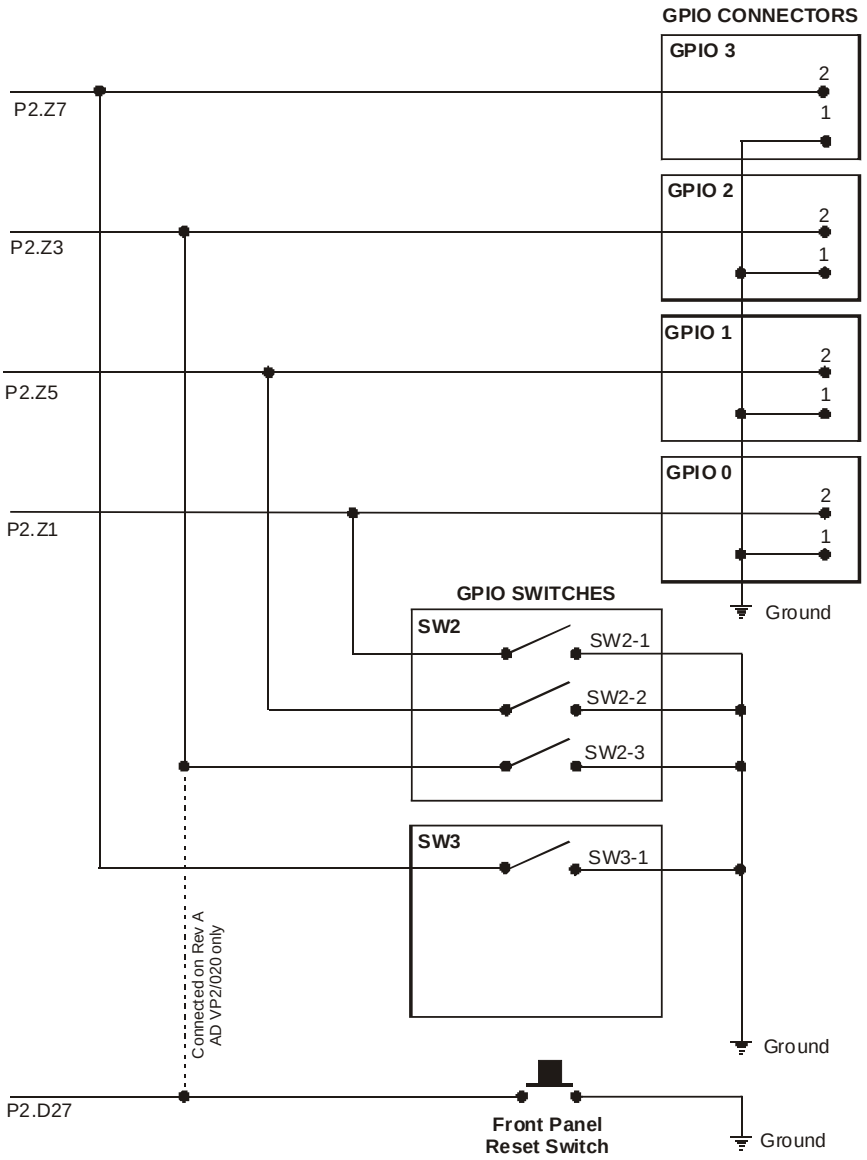

Figure B-2 AD VP2/020 GPIO Interface

The location and settings of the GPIO switches are outlined in Figure B-2. The switch settings allow each GPIO signal to be driven to a logic 0 state when the corresponding switch is set to ON, or to be controlled by an external device when the switch is set to OFF. When the switch is in the OFF position, the corresponding input pin will read as logic 1 and the signal is pulled up by a 10kΩ resistor. When the GPIO signal is set as an output, the corresponding switch must be set to OFF.

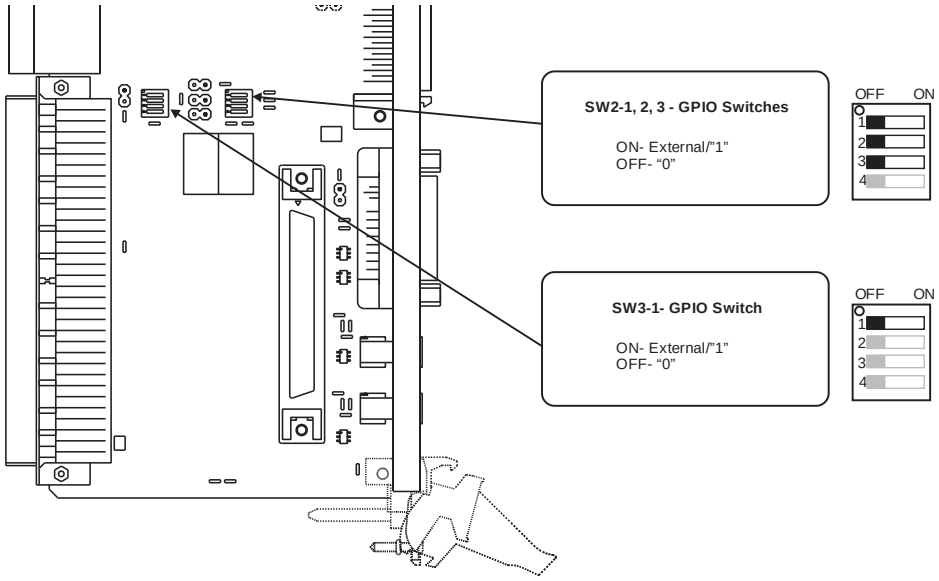

Figure B-3 AD VP2/020 GPIO Switch Settings

B.4 AD VP2/020-30

The AD VP2/020-30 is a 160-way P2 plus P0 backplane RTM for the VP E2x/msd. It provides two RJ45 connectors for 10/100/1000 Mbps Ethernet, two 68-way SCSI-3 style sockets for PMC I/O, PS/2 keyboard and mouse connector, Push Button switch, DVI-D, two USB and two SATA connectors and additional headers for other miscellaneous I/O functions. Additional switches are provided for Ethernet signal routing.

This RTM requires one slot width and a minimum of 115 mm behind the backplane.

B.4.1 Layout

The Figure B-4 shows the locations of the connectors, jumpers and switches. The following sections describe the switch and jumper options.

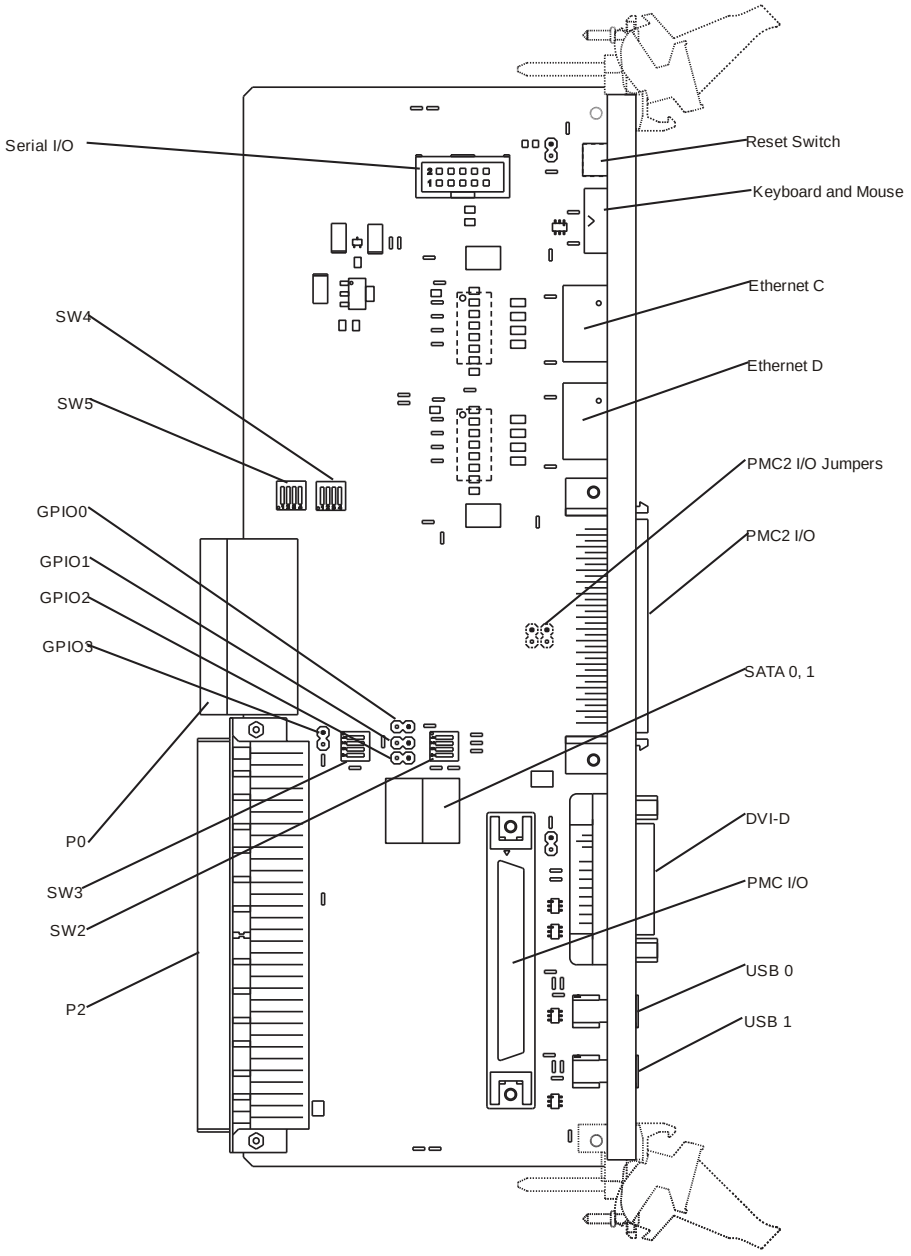

Figure B-4 AD VP2/020-30 RTM Connectors and Switches

B.4.2 Pin-out Tables

Signal Name	Details
USB	Table B-6
Keyboard and Mouse	Table B-7
Serial I/O	Table B-9
Ethernet	Table B-8
PMC1 I/O	Table B-11
PMC2 I/O	Table B-11
DVI-D	Table B-14
SATA 0 and 1	Table B-13
GPIO0-2	Figure B-2
GPIO3	Figure B-2

Table B-3 AD VP2/020-30 Connector List

B.4.3 PMC I/O Switch and Jumper Settings

The pins 18, 19, 52 and 53 of the PMC2 I/O connector have no function on this board and are not connected. However, to improve signal quality on the connecting cable it may be preferable to connect these pins to ground, using SW2-4 as shown in Figure B-5.

When using the PMC2 I/O with a parallel SCSI I/O module, SW2-4 should be set to connect ground on pins 19 and 53 of the PMC2 I/O connector. In addition, pins 18 and 52 of the PMC2 I/O connector should also be configured to provide additional ground connections for the SCSI interface. This is done by bridging pins 1-2 of each of the PMC2 I/O Ground Jumpers (see Figure B-5).

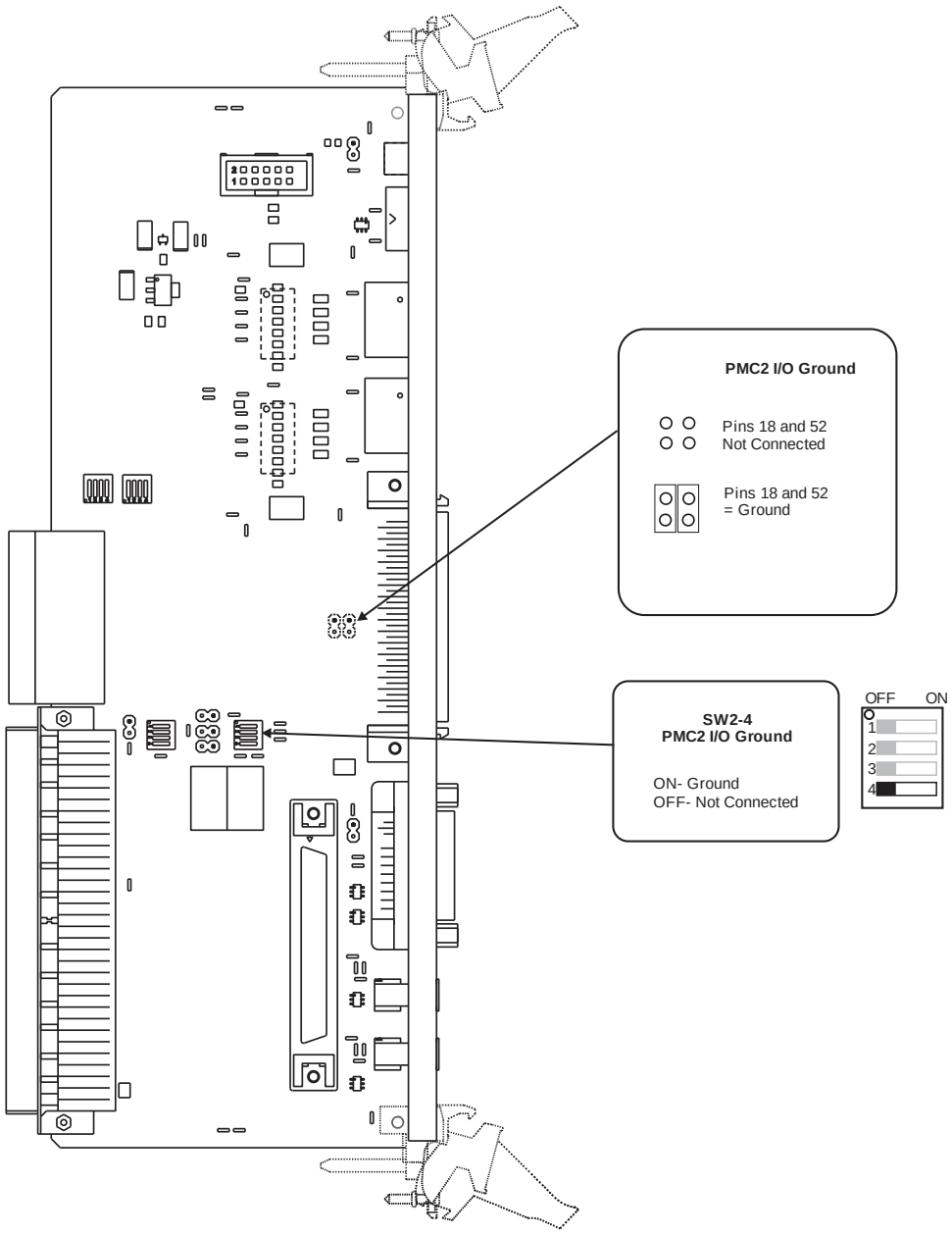

Figure B-5 AD VP2/020-30 PMC2 I/O Switch and Jumper Settings

B.4.4 Ethernet Switch Settings

This RTM also supports Ethernet connections via the P0 connector. These connections may be configured on the VP E2x/msd board to provide either a single port packet-switched backplane interface compliant with ANSI/VITA 31.1 (Ethernet port C) and a single external interface via the RTM (Ethernet port D), or two external interfaces via the RTM. Two sets of 4 DIP switches must be correctly configured to match the VP E2x/msd configuration, as shown in Figure B-6. All eight individual switches must always be set to the same position i.e. all OFF or all ON.

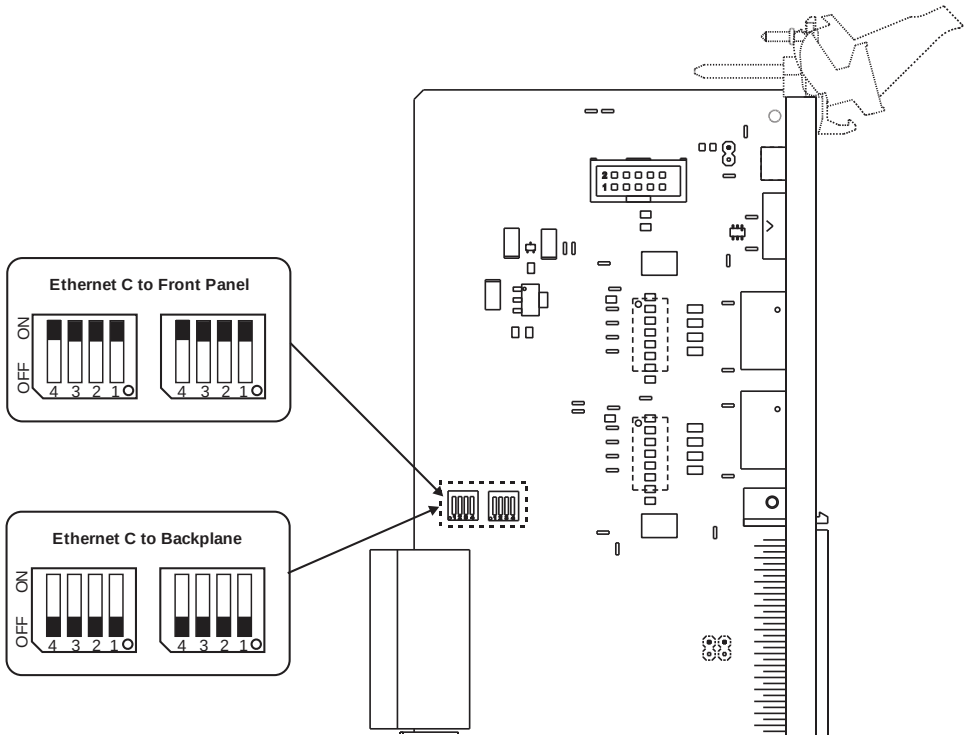

Figure B-6 AD VP2/020-30 Ethernet Switch Settings

B.4.5 GPIO Interface

See Section B.3.3 for details of the GPIO interface, switch settings and jumper settings for this RTM.

B.5 AD VP2/033-10

The AD VP2/033-10 is a 160-way P2 backplane RTM for the VP E2x/msd. It provides one 68-way SCSI-3 style socket for PMC1 I/O, HD Audio, Push Button switch, DVI-D, two USB and two SATA connectors, with additional headers for other miscellaneous I/O functions.

This RTM requires one slot width and a minimum of 115 mm behind the backplane.

B.5.1 Layout

The Figure B-7 shows the locations of the connectors, jumpers and switches. The following sections describe the switch and jumper options.

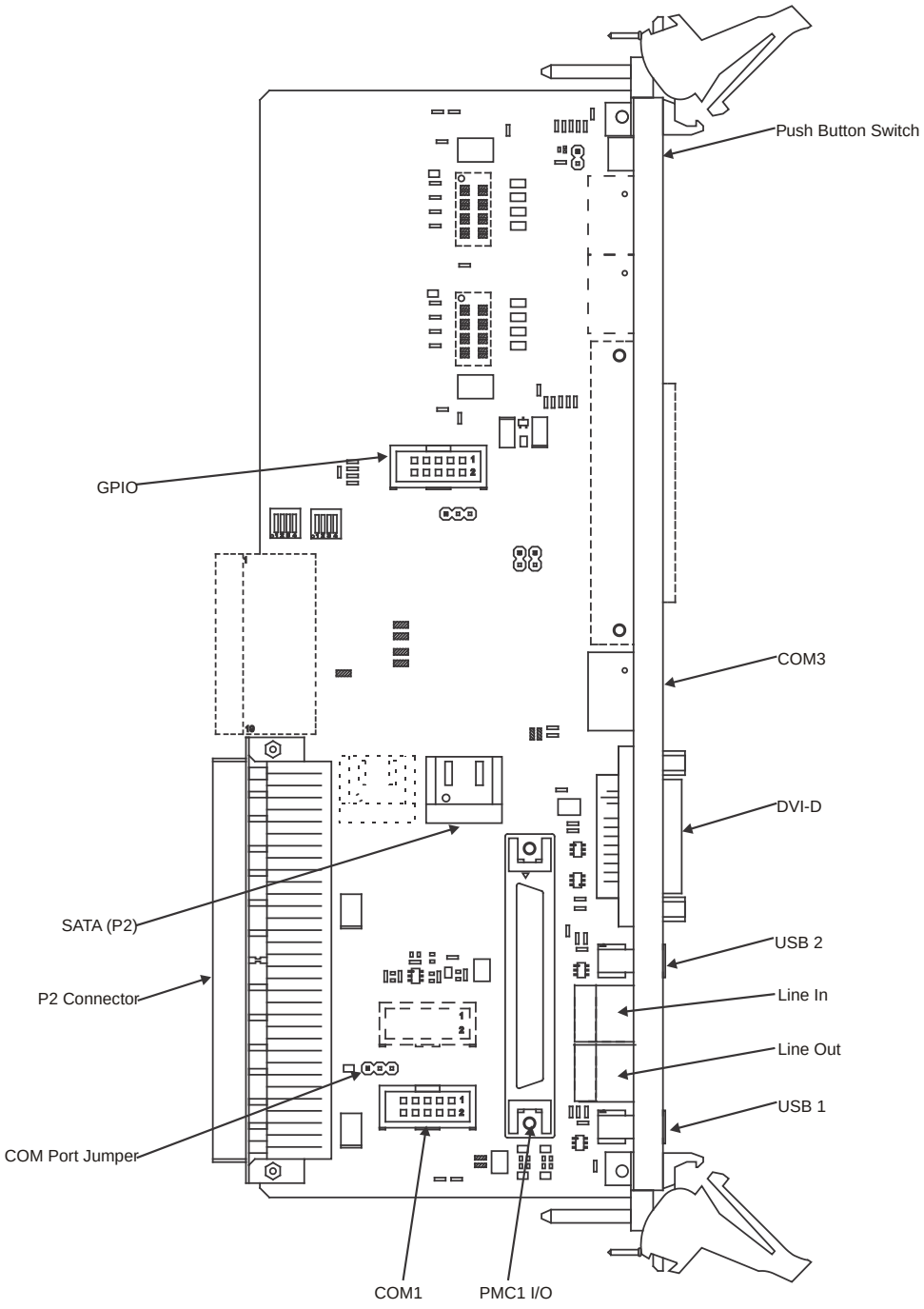

Figure B-7 AD VP2/033-10 RTM Connectors and Switches

B.5.2 Pin-out Tables

Signal Name	Details
USB Connector	Table B-6
Serial Port Header	Table B-9
PMC1 I/O	Table B-11
DVI-D	Table B-14
SATA 0 and 1	Table B-13
GPIO Header	Table B-10
HD Audio	Table B-15
COM3	Table B-16

Table B-4 AD VP2/033-10 Connector List

B.6 AD VP2/033-30 and AD VP2/433-30

The AD VP2/033-30 is a 160-way P2 plus P0 backplane RTM for the VP E2x/msd. It provides two RJ45 connectors for 10/100/1000 Mbps Ethernet, two 68-way SCSI-3 style sockets for PMC I/O, HD audio connectors, Push Button switch, a DVI-D connector, two USB and three SATA connectors, and additional headers for other miscellaneous I/O functions. Additional switches are provided for Ethernet signal routing.

This RTM requires one slot width and a minimum of 115 mm behind the backplane.

NOTE: The AD VP2/433-30 has the same functionality except that it does not support the PMC2 I/O connector.

B.6.1 Layout

The Figure B-8 shows the locations of the connectors, jumpers and switches. The following sections describe the switch and jumper options.

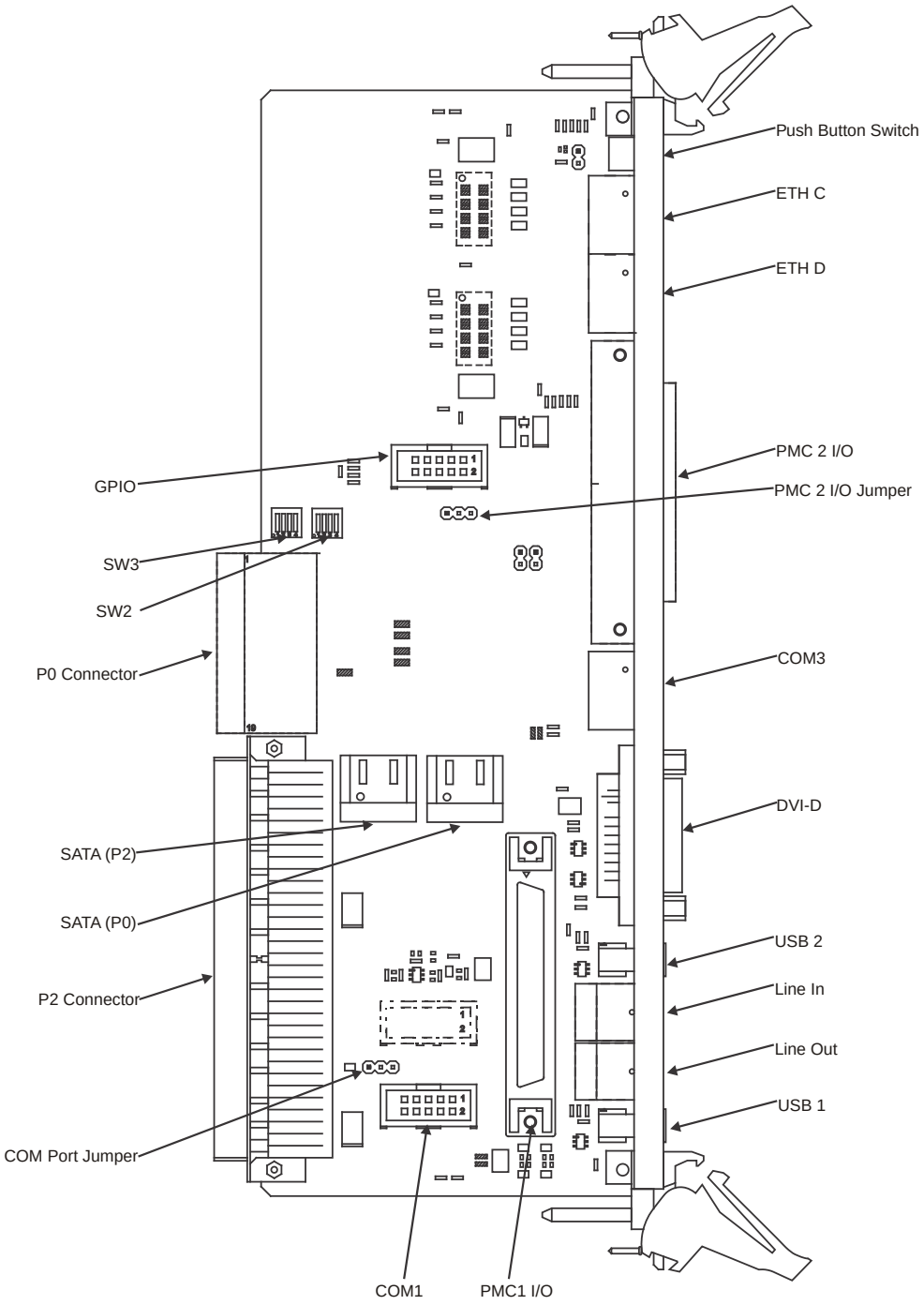

Figure B-8 AD VP2/033-30 RTM Connectors and Switches

NOTE: The AD VP2/433-30 has the same connectors and switches except that it does not support the PMC2 I/O connector.

B.6.2 Pin-out Tables

Signal Name	Details
USB Connector	Table B-6
Serial Port Header	Table B-9
PMC1 I/O	Table B-11
PMC2 I/O	Table B-11
DVI-D	Table B-14
SATA 0 and 1	Table B-13
SATA 2	Table B-12
GPIO Header	Table B-10
HD Audio	Table B-15
High Speed Serial Port	Table B-16
Ethernet Connector	Table B-8

Table B-5 AD VP2/033-30 Connector List

NOTE: The AD VP2/433-30 has the same functionality except that it does not support the PMC2 I/O connector.

B.6.3 PMC2 I/O Switch and Jumper Settings

The pins 19 and 53 of the PMC2 I/O connector have no function on this board and are normally not connected. However, to improve signal quality on the connecting cable it may be preferable to connect these pins to ground using the PMC2 I/O Ground jumpers as shown in Figure B-9. This section is not applicable for AD VP2/433-30 variants.

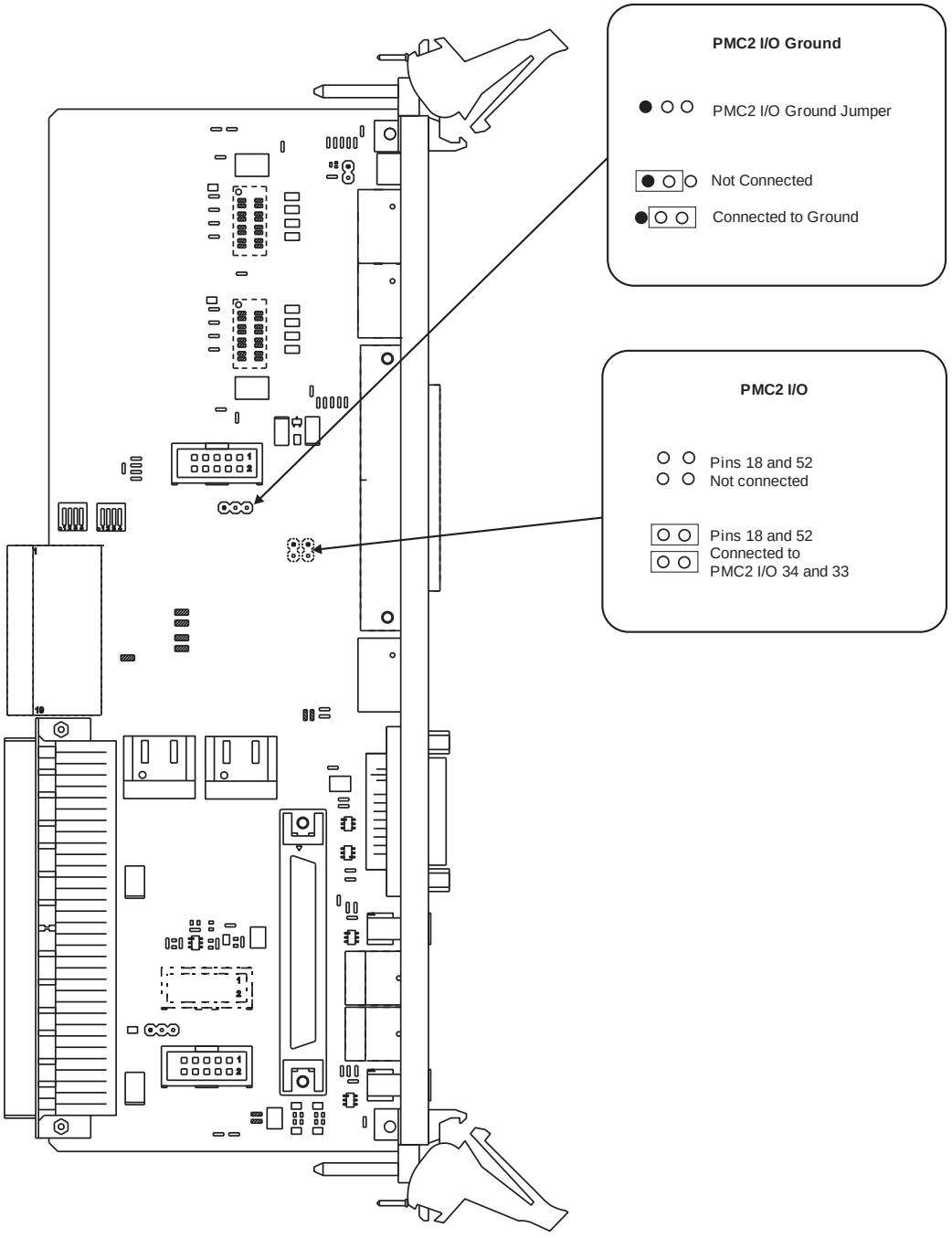

Figure B-9 AD VP2/033-30 PMC2 I/O Switch and Jumper Settings

B.6.4 Ethernet Switch Settings

The RTM also supports Ethernet connections via the P0 connector. These connections may be configured on the VP E2x/msd board to provide either a single port packet-switched backplane interface compliant with ANSI/VITA 31.1 (Ethernet port C) and a single external interface via the RTM (Ethernet port D), or two external interfaces via the RTM. Two sets of four DIP switches must be correctly configured to match the VP E2x/msd configuration as shown in Figure B-10. All eight individual switches must always be set to the same position, i.e. all OFF or all ON.

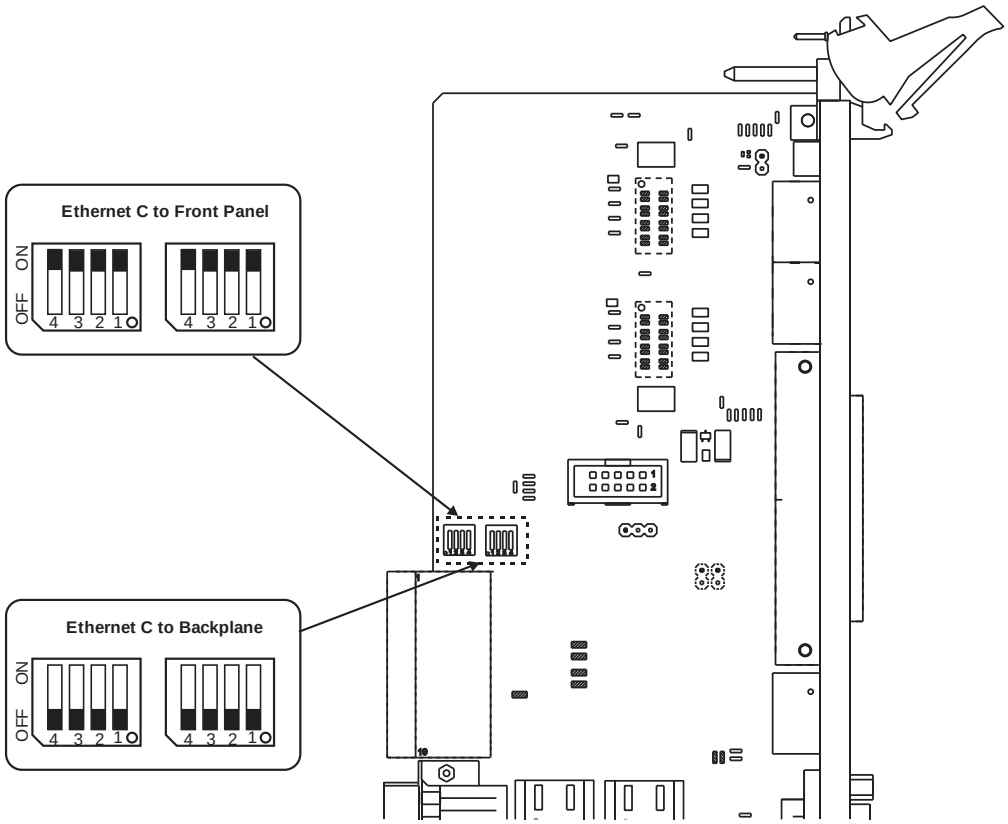

Figure B-10 AD VP2/033-30 Ethernet Switch Settings

B.7 Header/Connector Configuration Tables

The headers and connectors are designed to enable the use of standard PC interface cables wherever possible. Detailed below are the pin-outs of the headers and connectors used on the breakout modules.

B.7.1 USB Connector

Pin	Signal
1	USB_VCC
2	USBD-
3	USBD+
4	USB GND
SHIELD	CHASSIS GND

Table B-6 USB Connector - Pin-out

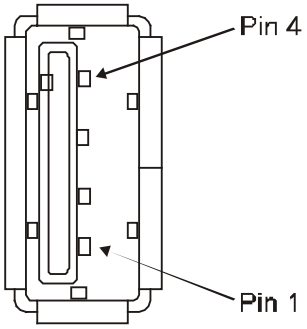

Figure B-11 USB Connector - Pin Map

B.7.2 Keyboard and Mouse Connector

Pin	Signal
1	KBD_DATA
2	MS_DATA
3	GND
4	KBD_PWR
5	KBD_CLOCK
6	MS_CLOCK
SHELL	CHASSIS GND

Table B-7 Keyboard and Mouse Connector - Pin-out

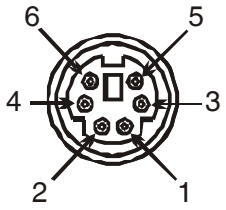

Figure B-12 Keyboard and Mouse Connector - Pin Map

B.7.3 Ethernet RJ45 Connector

Pin	Signal
1	DA+
2	DA-
3	DB+
4	DC+
5	DC-
6	DB-
7	DD+
8	DD-

Table B-8 Ethernet RJ-45 Connector - Pin-out

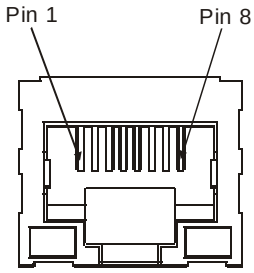

Figure B-13 Ethernet RJ-45 Connector - Pin Map

B.7.4 Serial I/O IDC Header

Pin	Signal	Pin	Signal
1	DCD	2	DSR
3	RX (RXA)	4	RTS (TXB)
5	TX (TXA)	6	CTS (RXB)
7	DTR (DIR)	8	NC
9	RETURN	10	RETURN

Table B-9 Serial I/O IDC Header - Pin-out

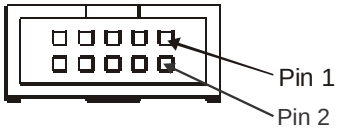

Figure B-14 Serial I/O IDC Header - Pin Map

B.7.5 GPIO Header

Pin	Signal	Pin	Signal
1	GPIO1	2	GPIO0
3	GPIO3	4	GPIO2
5	GND	6	GND
7	EXT_RESET	8	NC
9	+5V	10	+5V

Table B-10 GPIO Header - Pin-out

B.7.6 PMC 1 and PMC 2 (64-bit) I/O Connector (68-way D-type)

Pin	Signal	Pin	Signal
1	I/O 1	35	I/O 2
2	I/O 3	36	I/O 4
3	I/O 5	37	I/O 6
4	I/O 7	38	I/O 8
5	I/O 9	39	I/O 10
6	I/O 11	40	I/O 12
7	I/O 13	41	I/O 14
8	I/O 15	42	I/O 16
9	I/O 17	43	I/O 18
10	I/O 19	44	I/O 20
11	I/O 21	45	I/O 22
12	I/O 23	46	I/O 24
13	I/O 25	47	I/O 26
14	I/O 27	48	I/O 28
15	I/O 29	49	I/O 30
16	I/O 31	50	I/O 32
17	I/O 33	51	I/O 34
18	NC	52	NC
19	GND†	53	GND†
20	I/O 35	54	I/O 36
21	I/O 37	55	I/O 38
22	I/O 39	56	I/O 40
23	I/O 41	57	I/O 42
24	I/O 43	58	I/O 44
25	I/O 45	59	I/O 46
26	I/O 47	60	I/O 48
27	I/O 49	61	I/O 50
28	I/O 51	62	I/O 52
29	I/O 53	63	I/O 54
30	I/O 55	64	I/O 56
31	I/O 57	65	I/O 58
32	I/O 59	66	I/O 60
33	I/O 61	67	I/O 62
34	I/O 63	68	I/O 64

† In some cases, jumpers are provided to either leave these pins disconnected or to connect them to ground. See Sections B.4.3 and B.6.3.

Table B-11 PMC I/O Connector (68-way D-Type) Pin-out

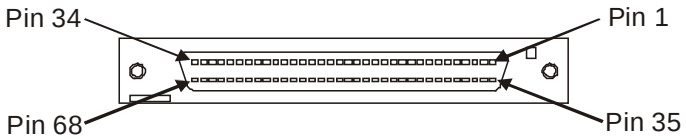

Figure B-15 PMC I/O Connector (68-way D-Type) Pin Map

B.7.7 Single SATA Connector

Pin	Signal
1	GND
2	SATA2_TX+
3	SATA2_TX-
4	GND
5	SATA2_RX-
6	SATA2_RX+
7	GND

Table B-12 SATA Connector - Pin-out

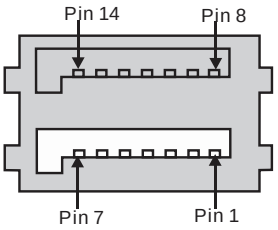

Figure B-16 SATA Connector - Pin Map

NOTE: Top part of the dual SATA socket has no connections

B.7.8 Dual-SATA Connector

Pin	Signal
1	GND
2	SATA1_TX+
3	SATA1_TX-
4	GND
5	SATA1_RX-
6	SATA1_RX+
7	GND
8	GND
9	SATA2_TX+
10	SATA2_TX-
11	GND
12	SATA2_RX-
13	SATA2_RX+
14	GND

Table B-13 SATA Connector - Pin-out

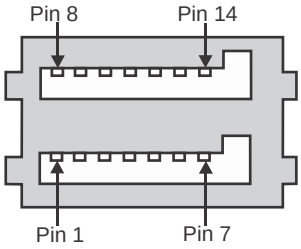

Figure B-17 SATA Connector - Pin Map for AD VP2/020

NOTE: The orientation of the SATA connector in the AD VP2/033 is changed as shown in Figure B-18

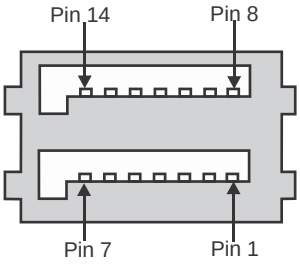

Figure B-18 SATA Connector – Pin Map for AD VP2/033

B.7.9 DVI-D Connector

Pin	Signal	Pin	Signal
1	DVI_TX2-	2	DVI_TX2+
3	GND	4	NC
5	NC	6	DVI_DDCCLK
7	DVI_DDCDATA	8	NC
9	DVI_TX1-	10	DVI_TX1+
11	GND	12	NC
13	NC	14	VCC
15	GND	16	HOT_PLUG#
17	DVI_TX0-	18	DVI_TX0+
19	GND	20	NC
21	NC	22	GND
23	DVI_TXC+	24	DVI_TXC-
C1	NC	C2	NC
C3	NC	C4	NC
C5A	GND	-	-
C5B	GND	-	-

Table B-14 DVI-D connector - Pin-out

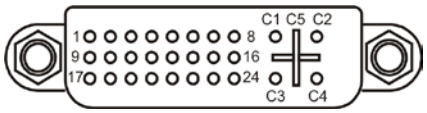

Figure B-19 DVI-D Connector - Pin Map

B.7.10 Audio Jacks

To use the High Definition stereo audio capability of the VP E2x/msd, the RTM variant AD VP2/033 that supports the audio jacks has to be used.

Jack	Used for
1	Line Out
2	Line In

Table B-15 AD VP2/033 Audio Jack Numbering

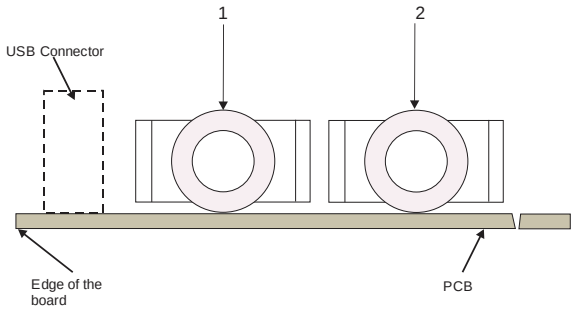

Figure B-20 AD VP2/033 Audio Jack Position

B.7.11 COM3 Interface

The COM3 interface uses an RJ45 connector with signals assigned as follows:

Pin	Signal	Direction
1	-	-
2	-	-
3	RETURN (GND)	-
4	TX - Tx Data	Output from board
5	RX - Rx Data	Input to board
6	-	-
7	-	-
8	-	-

Table B-16 COM3 Interface Pin-out

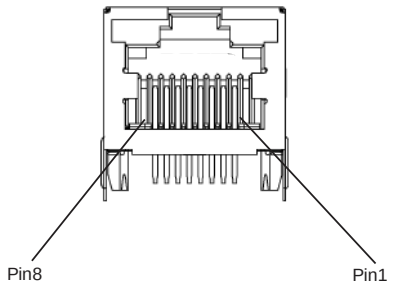

Figure B-21 COM3 Interface - Pin Map

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