technical information manual

NIM 621 SERIES

Quad Discriminators

(621AL, 621BL, 621BLP, 621CL)

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
West Nyack, New York

NOTE TO THE USER

LeCroy Research Systems is committed to providing unique, reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, and in response to information received from the users of our equipment, the Engineering Department at LeCroy is continually seeking to refine and improve the performance of our products.

While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

If you have any questions about the performance or operation of this unit, rapid assistance may be obtained from our Engineering Services Department in Spring Valley, NY, telephone 914-425-2000, or from your local distributor in countries other than the U.S.A.

LeCROY RESEARCH SYSTEMS

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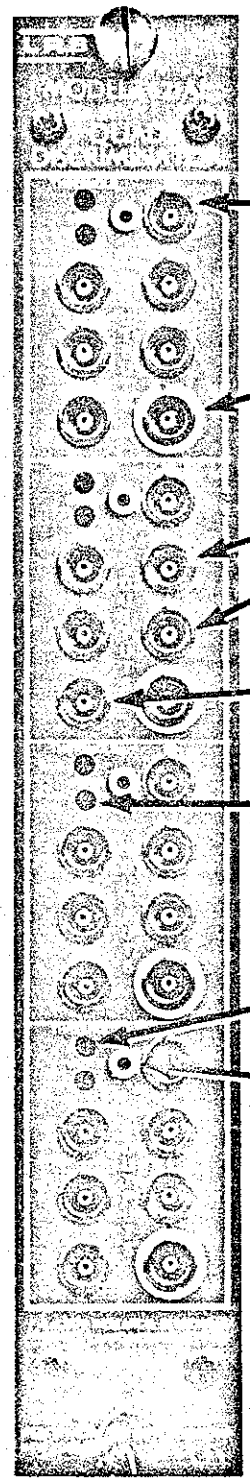
NIM Model 621AL
Quad Discriminator



50 Ω input, <2% reflections.

1 complementary 50 Ω output; quiescently, -16 mA; logical 1, 0 mA.

2 pairs bridged 50 Ω outputs; quiescently, 0 mA; logical 1, -32 mA per pair.

1 normal 50 Ω output (quiescently, 0 mA, logical 1, -16 mA.

Continuous width adjust, 5 nsec to 1 usec.

Threshold adjust, -30 mV to -1 volt; stability, <0.2%/°C.

Threshold monitor point; reads 10X actual threshold.

Standard AEC/NIM packaging, in conformance with AEC Report TID-20898; #1 width module.

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621 SERIES DISCRIMINATORS Date of Last Update:

Addenda To General Description And/Or Specifications

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INPUT CHARACTERISTICS

Threshold Range: The threshold range of 621 Series Quad Discriminators is -30 mV to -1 volt. Because the front-panel screwdriver-adjustable potentiometer gets more and more sensitive as the threshold is increased, it eventually reaches a point (approximately -600 mV) beyond which it becomes difficult to set. Thus, beyond the -600 mV level it should be assumed that the discriminator will attain its maximum threshold setting of -1 volt with almost negligible additional turning of the pot.

The low minimum threshold of the 621 Series units makes it possible to use lower gain photomultipliers, lower high voltage in the phototubes, and to drive PM signals over longer cable lengths than would be possible with higher thresholds. Compared with a -50 mV discriminator, for instance, utilizing RG-58 cable, the -30 mV discriminator would permit cable runs 66.7 feet longer than those permitted by a -50 mV discriminator for equal amplitude pulses. In addition, the low minimum threshold helps make it possible for one to back-terminate at the photomultiplier to absorb reflections and high amplitude noise. (In this case, the PM drives 25 ohms, the tube current is shared, and the amplitude is half that of the unterminated system).

Threshold Uncertainty: While most people consider the threshold of a discriminator to be that value which is written on a spec sheet or determined by a front-panel pot, in reality the actual value not only varies from channel to channel, but can be a strong function of other environmental conditions. The external factors with the strongest effect upon the threshold value are the temperature coefficient of threshold and the power supply coefficient of threshold. Combining these, the actual threshold value V_T is given by:

V_T = Threshold according to front-panel control setting ± dc offset ± temperature coefficient X temperature change from calibration temperature ± supply coefficient X voltage change from calibration voltage.

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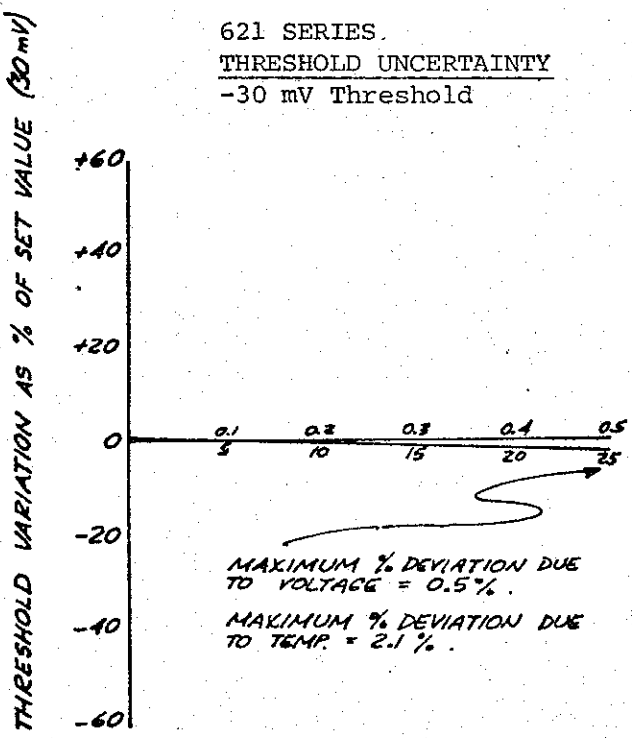
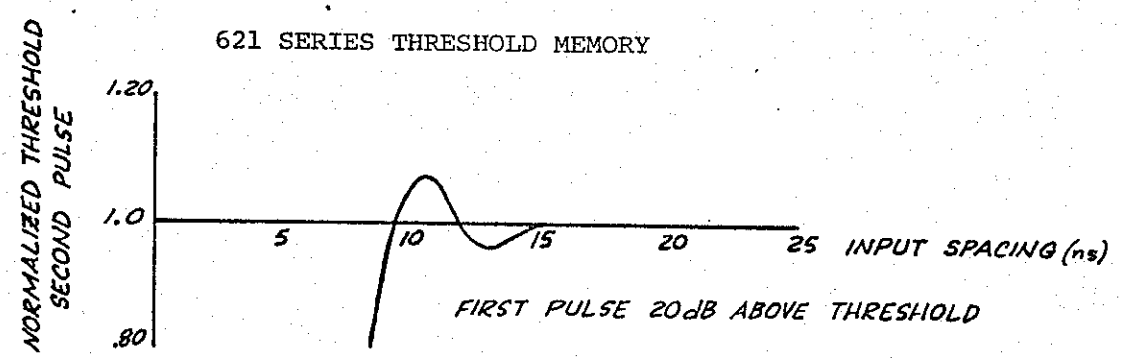
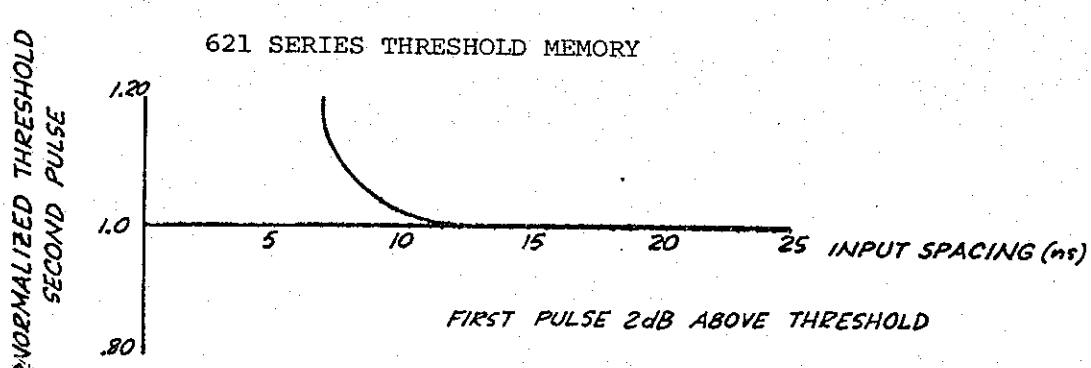
The figure below indicates the total threshold uncertainty of the 621 Series Discriminators.



Threshold Memory: In order for an experimenter to be assured of a well defined threshold value, it must be independent of the typical conditions encountered in its use. While one does not expect large changes in basic pulse shape, etc., a discriminator does experience all varieties of pulse pair separation. If a discriminator's threshold is affected by previous events, it is said to have threshold memory. To the experimental physicist, this is additional threshold uncertainty, since the discriminator's threshold for any given event depends upon the elapsed time from the preceding threshold crossing. In most discriminators, threshold memory (or second pulse sensitivity) becomes much larger as the pulse separations are reduced. The effect can be further aggravated by the amplitude of the preceding signal, so much so with some circuits, that an overload or noise pulse can effectively paralyze the discriminator for threshold level signals for 10's of nanoseconds following the overload.

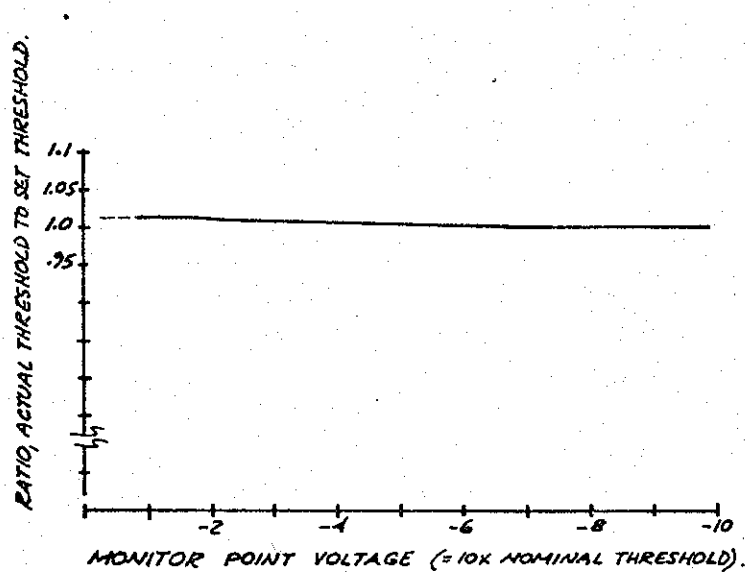
The figure below shows the threshold memory of the 621 Series Discriminators, where the first signal is 20 dB over threshold. The subsequent figure depicts threshold memory characteristics for the first input just slightly above threshold.





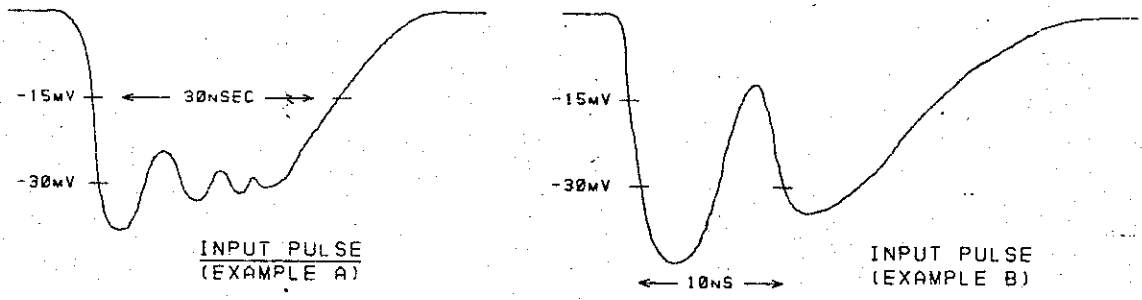
Note that in both cases the threshold for the second pulse is 6% for all spacing wider than 9 nsec. The second graph (i.e., the one more favorable to the discriminator) shows exceptionally clear response with virtually no effect in evidence above 10.5 nsec.

Threshold Calibration: Determination of the input threshold set by the front-panel control has typically required the experimenter to calibrate each change in setting with an external pulse source and oscilloscope. Newer discriminators offer a front-panel test point whose dc level is proportional to the actual discriminator threshold. Not only does this allow rapid and simple determination of threshold, but it also allows the experimenter to easily return the threshold level to a previously recorded setting. The convenience, and therefore the usefulness, of this feature is strongly dependent upon the characteristics of this monitor voltage, particularly its linear proportionality with the threshold setting. The figure below indicates the characteristic curve for the LRS 621 Series Discriminators.



621 Series Threshold Hysteresis

In standard 621 or 620 Series Discriminators, hysteresis is built into the front end, such that every threshold crossing will not trigger the discriminator unless the previous signal has returned to below approximately -15 mV. This avoids multiple pulsing due to, say, fine structure riding on a flat-topped pulse that may bring the pulse above and below threshold. Note the examples below.



In Example A, the pulse shape variations of the input pulse will not retrigger the discriminator even though they cross the threshold level at a time exceeding the DPR of the unit. In Example B, since the input signal does go back through -15 mV and then once again rises to exceed the -30 mV threshold level, two discriminator outputs would result. Since LRS discriminators are most often used with photomultipliers and plastic scintillators, and since the characteristic pulses out of this type detector are typically smooth for each individual event, multiple outputs should only occur when they represent multiple events.

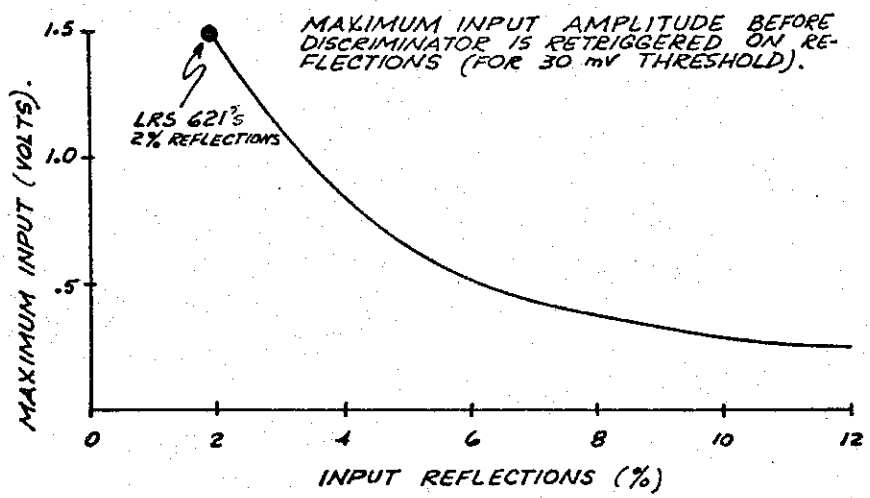
-10 mV Minimum Threshold Option: By special request and at added cost, LRS can provide any 621 Series Discriminator (or 620 Series Octal Discriminator) with its minimum threshold set at -10 mV instead of -30 mV. Extreme care must be taken in the use of these modified units. The hysteresis level (described above) is only 5 mV for the -10 mV unit, such that any pulse entering with variation on it exceeding 5 mV may cause the discriminator to retrigger. Care should be taken that the discriminator is not fed by any circuit with any small DC level on it, and the less noisy the environment, the better. It is actually recommended that AC coupling be used if the input rates are low enough to permit it.

OPERATION

Input Relections: Input reflections probably account for the majority of multiple-pulsing problems encountered in an experiment. As discriminator thresholds have become lower, the amount of reflected signal required to retrigger the unit has decreased accordingly. Unless the percentage of input reflections is reduced along with the minimum threshold value, the experimenter finds himself in the situation where multiple-pulsing negates the usefulness of lower threshold. The input reflections of a discriminator effectively determine the allowable dynamic range of event or noise input signals.

On the experimental floor, a limited dynamic range may mean that minimum threshold values will have to be set higher to prevent multiple-pulsing on noise or large (shower) event signals. In addition, high input reflections also limit the ability of a discriminator to be used to restandardize logic signals which have been degraded by long cables.

The figure below shows the maximum input voltage and allowable dynamic range as a function of discriminator input reflections.



OPERATION

As is evident, the 621 Series Discriminators offer a dramatic improvement in input reflection suppression over previously available discriminators. Because of the extremely low reflection coefficient of the 621's (i.e., <2% for inputs of risetime ≥2 nsec), maximum input signal is more than a volt larger than it would be for a unit exhibiting the typical 10% reflections, offering five times increase in the discriminators' dynamic range.

Input Protection: The inputs of 621 Series Discriminators are protected to 5 A for 0.5 A for 0.5 usec., clamping at +1 and -7 volts.

The DC protection is limited by the 0.25 watt dissipation limit of the input resistor, which can be assumed to offer protection against DC signals between -5 volts and +5 volts.

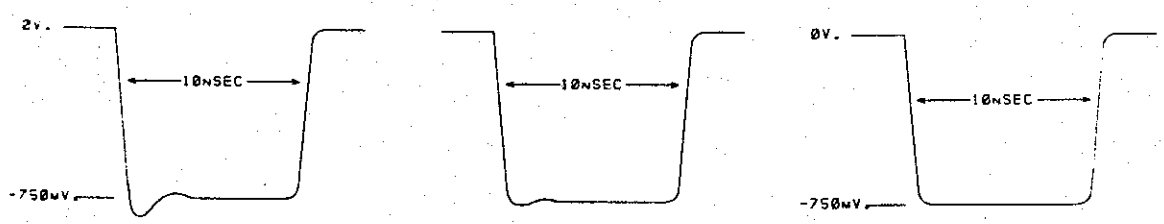
Bridged High Impedance Input Option: Certain 621 Series modules are offered with bridged high impedance input options. These units are the Models 621BL and 621BLP. Although other models have been supplied occasionally with this option in the past by special request. The bridged high impedance inputs permit a user to drive one cable only from the photomultiplier to the discriminator to permit subsequent fast logic decision and pattern recognition to be performed. A popular method in the absence of this discriminator input option is to run two cables, one of which is from the dynode, which then must be inverted before the ADC or discriminator could accept it.

For this bridged input option, the top output connector of the right-hand output pair is generally sacrificed. The wire normally feeding this cable is tied to 50Ω to permit normal operation of the other half of the output. A silver-colored ring is placed around this connector (as well as around the original input connector) when the unit is modified for this option to signify the fact that there are now two input connectors. In standard usage, the silver-colored ring usually specifies complementary output.

OUTPUT CHARACTERISTICS

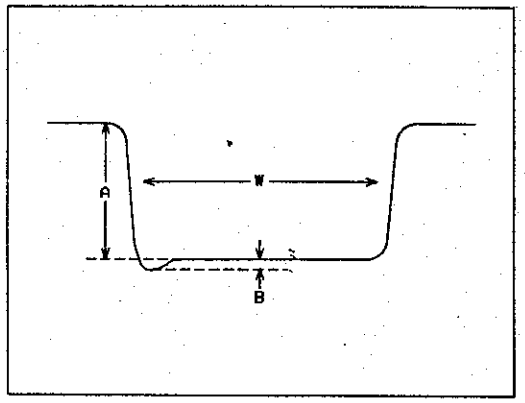
Bridged Negative Outputs: The 621 Series Discriminators all have two pairs of current source 50 Ω outputs, delivering -32 mA of current during the output and 0 mA quiescently. The 621, 621AL, 621BL, and 621BLP all have switched current outputs, requiring no quiescent current and permitting extremely low power dissipation in the total circuit. These bridged outputs on the 621CL and 621S, however, are full differential type current outputs requiring quiescent current and dissipating significantly more power than the switched outputs. The benefit of the 621CL-type outputs is faster risetime and a generally cleaner output pulse shape, but the additional current used is quite substantial. The standard switched current outputs nevertheless maintain a risetime of <2.5 nsec and a reasonably clean shape, as long as care is taken to terminate at least one half of the other bridged output in that channel.

The actual shape of typical outputs from the 621 Series Discriminators is approximated below.



OPERATION

Using the typical output pulse shape shown below as a visual reference, LRS output shapes for switched current outputs (such as on Models 621L, 621AL, 621BL, 621BLP) are set up to adhere to the following restrictions when one output from the adjacent pair is terminated.



AMPLITUDE: -700mV≤A≤-800mV.

OVERSHOOT: B≤10% OF A

RISETIME:TYPICALLY ≤2.0 NSEC.

FALLTIME:TYPICALLY ≤2.5 NSEC. AT MINIMUM WIDTH.

MINIMUM WIDTH: WMIN (FWHM) ≤5.0 NSEC.

MAXIMUM WIDTH: WMAX (FWHM) ≈ 1 USEC.

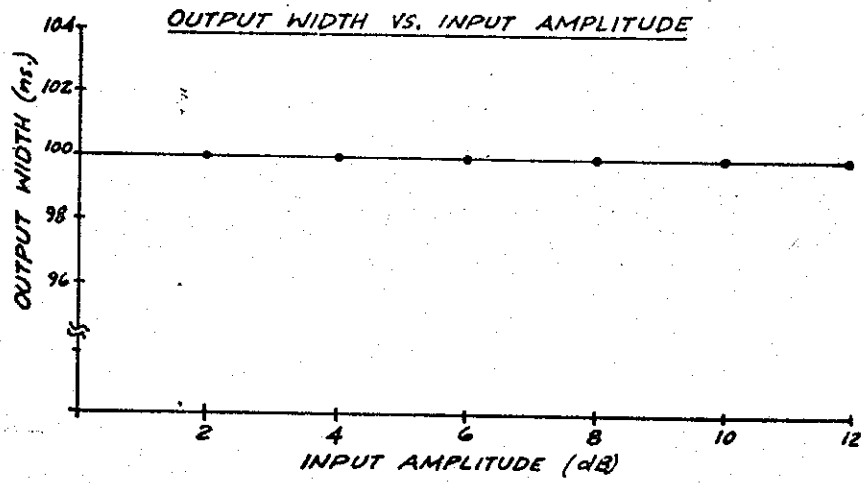
Fast Negative Timing Output: The fast negative timing output on all 621 Series Discriminators is a full differential type current source output. Its name originates from the contrast in risetime (1.3 nsec vs 2.5 nsec) between it and the other 4 negative outputs on all 621's except for the 621CL and 621S. Because the risetime is much faster, there is less timing inaccuracy that would be created by the nominal "threshold" levels of subsequent time measuring circuits.

Complementary Output: The single complementary output is actually the output from the collector of the other half of the differential pair supplying current to the fast negative timing output. It is a 50Ω output with quiescent level at -16 mA, and logical 1 at 0 mA. Risetime and other characteristics are similar to that of the fast negative timing output.

Output Width: The output range of LRS Series 621 Discriminators in standard updating mode is 5.0 nsec to 1 usec, continuously adjustable via front-panel potentiometer. Output characteristics for units possessing a Burst Guard mode are described below.

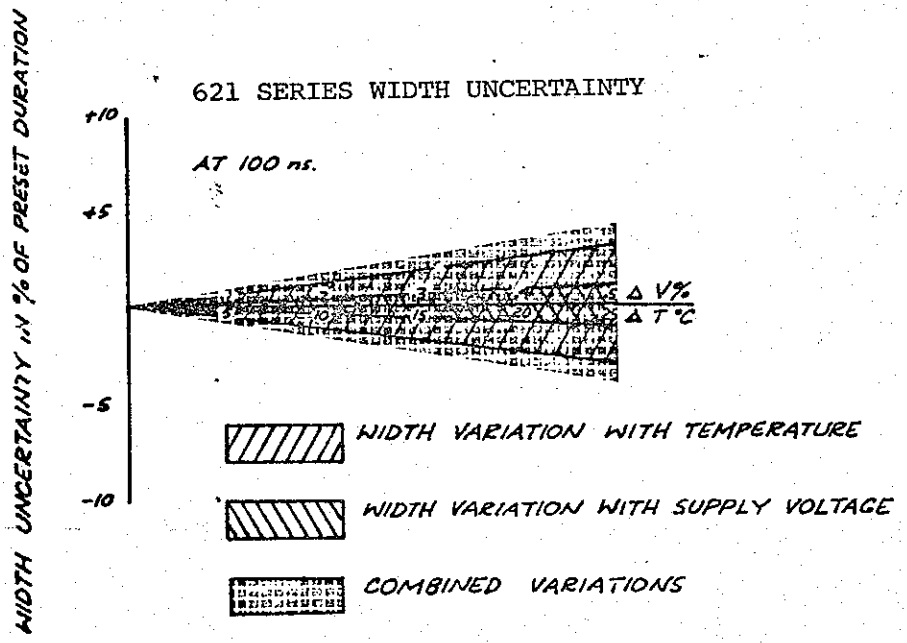
Because the potentiometer is very sensitive beyond 600 nsec, it is actually almost impossible to set the width between 600 nsec and 1 usec. As a result the specifications indicate continuous adjustment up to 600 nsec, with a ≈ 1 μsec setting at the far end of the pot.

Output Width Uncertainty: The output width of most discriminators is a nominal value determined by the front-panel potentiometer. Dispersion caused by variation in the discriminator input amplitude (jitter) results in a broadening of the skirts on the timing curve. In the LRS 621 Series Discriminators, this contribution is virtually non-existent as indicated by the figure below.



The other main contributions to output width uncertainty are a function of external conditions in a manner similar to threshold uncertainty. Variations in both temperature and voltage can cause significant changes in output width with undesirable consequences identical to dispersion caused by input amplitude.

The figure below indicates the uncertainty in output width of the 621 Series Discriminators as a function of reasonable variations in temperature and supply voltage.



Updating: The LRS 621 Series Discriminators are all updating (unless the Burst Guard mode is chosen, such as is available on the Models 621BL, 621BLP, and 621CL). In an updating discriminator the output is extended if a second pulse comes in before the first output returns to zero, as long as the second pulse arrives at a time later than the double-pulse resolution of the unit. Thus, the second pulse will be seen by the front end even though an output pulse is still present from the first signal, and that second pulse will cause a new output to be generated and added (in time) to the portion of the original output already occurred.

OPERATION

Burst Guard: LRS Models 621BL, 621BLP, and 621CL offer a Burst Guard mode of operation in addition to the normal Update Only mode. In this Burst Guard mode, the output of the front end is ORed with the conventional mode output. Thus, for input pulses arriving at a rate which exceeds the double-pulse resolution of the unit, the discriminator output duration will be equal to the time interval between the first leading edge threshold crossing and the last trailing edge threshold recrossing, or the preset output width, whichever is greater. This feature is expecially important in veto applications, where it is desired to keep the discriminator output on when the detector is being hit by unwanted and unmeasurable high rates. A discriminator without Burst Guard would see the first pulse and generate the preset output width, but would be paralyzed at quiescent level or would trigger only randomly for subsequent pulses separated by less time than the DPR of the unit. Burst Guard assures a logical 1 output level during these high rate bursts.

It is important to note that propagation delay through the discriminator is approximately 1 nsec less in the Burst Guard mode. The output width in this mode will be then correspondingly longer, since the output leading edge appears sooner.

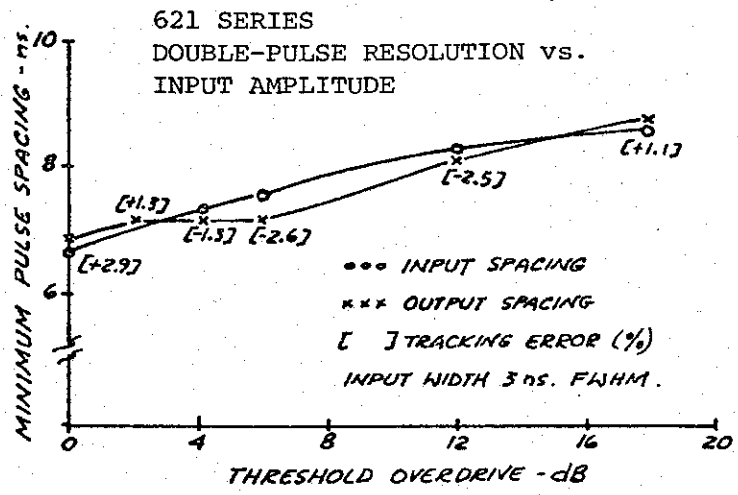
Usage of Bridged Negative Outputs Driving a Single Cable: In applications where it is necessary to drive very long cable lengths from a discriminator output, it is common to use only one half of the bridged 32 mA output and to leave the other half unterminated. This effectively channels all 32 mA into the one cable, giving a double amplitude output. It is important to know that 621 Series Discriminators all have clamp diodes that limit the output amplitude so as not to saturate the output transistors. This limit is approximately -1.4 volts. It cannot be assumed, therefore, that the -32 mA into one 50 Ω cable will give a -1.6 volt output signal.

TIMING CHARACTERISTICS

Maximum Rate: Maximum CW rate capability of the 621 Series Discriminators is guaranteed at 100 MHz. Typically, the maximum rate is 110 MHz, with some units being capable of operation up to 120 MHz for small bursts of input pulses.

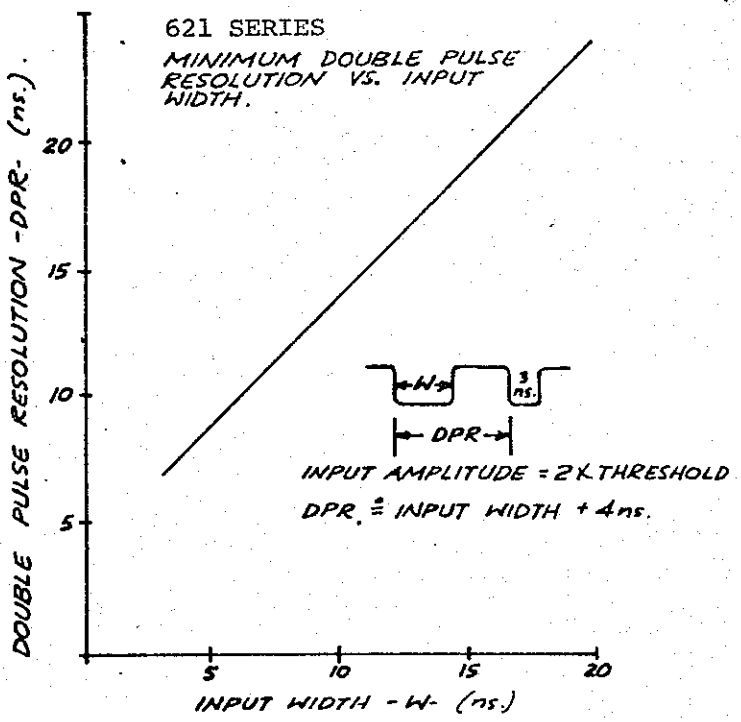
Double-Pulse Resolution: The speed of a discriminator is practically defined by its double-pulse resolution or the time between the leading edges of the most closely spaced pulse pair for which the discriminator produces two distinct output pulses. Although simple in concept, this specification can be misleading unless the input conditions are precisely defined and ambiguities in performance are disclosed. Characteristic curves which more adequately describe double-pulse resolution are indicated and discussed below.

Double-Pulse Resolution vs Input Amplitude: The double-pulse resolution of some discriminators is a strong function of the amount of overdrive. Typical anomalies include substantial increases in amplitude to achieve minimum pulse pair resolution (which is an effective threshold increase as a function of rate) and/or limited input dynamic range over which the discriminator adheres to specifications. A third effect is equivalent to tracking error. Does a discriminator have 8 nsec DPR if it never produces output pulses spaced more closely than 10 nsec apart? In some cases, this effective timing error can be much larger than time shift due to intrinsic slewing or risetime dependent slewing. The figure below shows the minimum double-pulse resolution of the LRS621 Series Discriminators as a function of input amplitude from threshold to 10X threshold.



It is worth noting that the 621's maintain a DPR of under 9 nsec for all inputs over the 10:1 dynamic range. Although not featured as part of the general specifications, the double-pulse resolution is much better than specified over most of the measured dynamic range. Also significant is the absence of tracking error at the limit of the discriminator's input performance. Throughout the measured range, the time shift of the output averages 2.54% or approximately 200 ps.

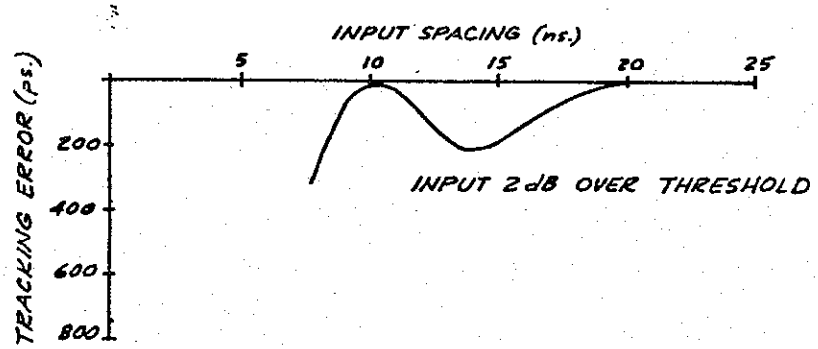
Double-Pulse Resolution vs Input Width: The DPR of a discriminator is a strong function of the duration of the first pulse in an input pair, since this width affects the recovery time allowed the discriminator input stage between the two pulses. If the double-pulse resolution is not linear with input width, it may mean that the discriminator may not respond to the second pulse following an overload photomultiplier signal. The double-pulse resolution vs input width of the 621 Series Discriminators is shown below:

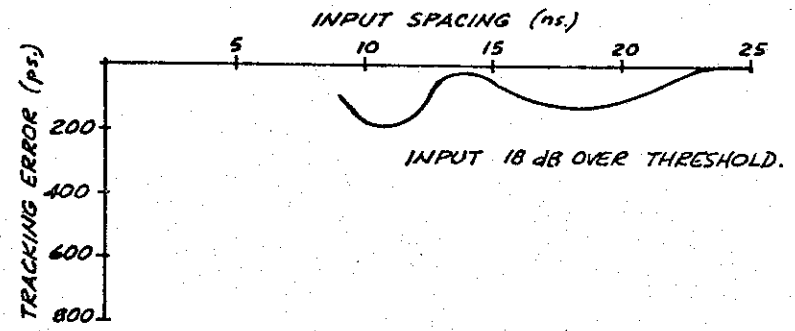


The above characteristic indicates that the discriminator's response is linear with input width and has a fixed recovery time of 4 nsec following an input of any duration.

Tracking Error: The ability of a discriminator to be used for precise timing (coincidence or TOF) in an environment which encounters narrow pulse pair separations is demonstrated by considering the time shift (or tracking error) introduced as the time interval between successive inputs is reduced. In an experiment, tracking error is equivalent to time dispersion as a function of input rate. For many experiments, this can be critical, since it is often in high rate situations that the best timing resolution is required.

Tracking error of the 621 Series Discriminators as a function of input pulse spacing is indicated in the figures below.





Note that the tracking error assumes the shape of a damped oscillation which decays to zero at several times the unit's minimum double-pulse resolution.

Slewing

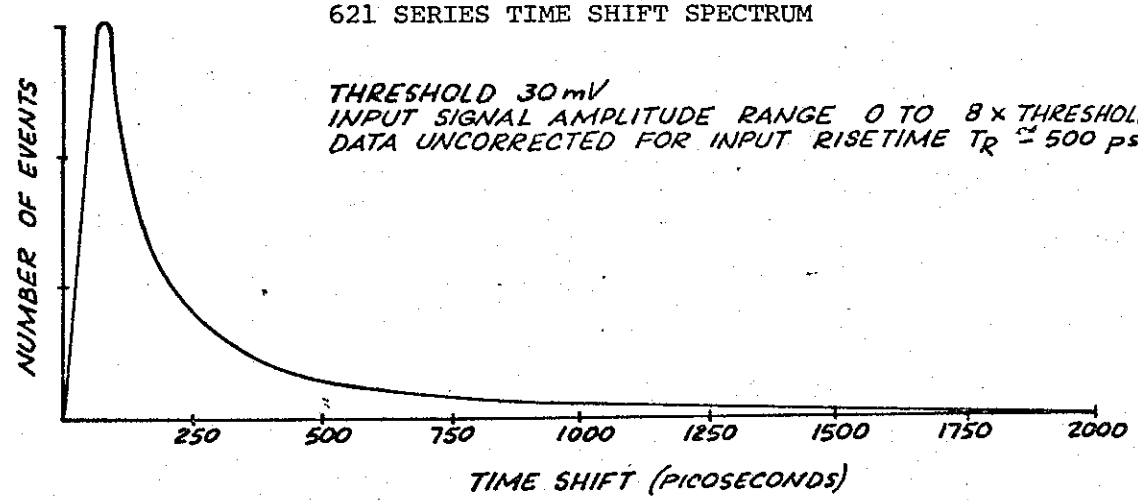
At less than maximum input rates which do not tax the double-pulse resolution of the discriminator, a class of characteristics comes into play which defines the fidelity of the discriminator output to the time information in the input signal. The most important of these, and the most difficult to strictly define and to measure, is time slewing or walk. This is variation in the input-to-output time delay of a discriminator with input amplitude. The net measured slewing yielded by a discriminator has two components, one contributed by the discriminator itself (intrinsic slewing) and the other dependent upon the input risetime.

Instrinsic slewing might be defined as the slewing measured with a delta function input. Risetime-dependent slewing arises from the fact that the discriminator fires earlier on the leading edge of a large pulse of finite risetime than on one of smaller amplitude. For an extreme range of pulse heights, the maximum contribution is equal to the 0 to 100% risetime of the pulse.

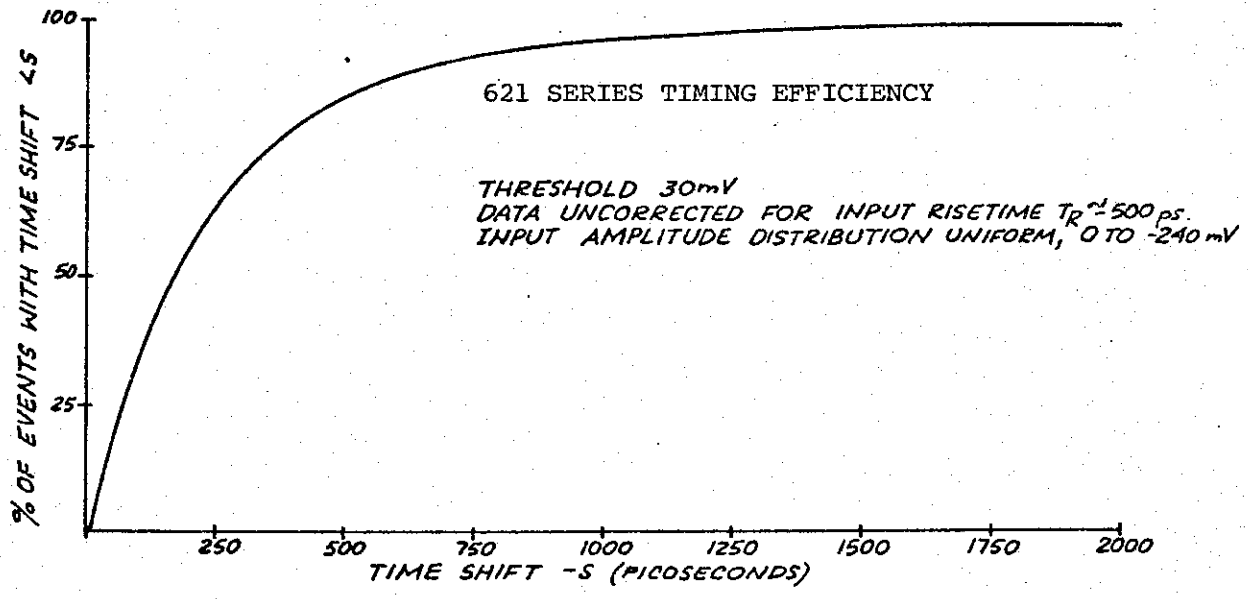
With most discriminators, by far the largest portion of the slewing occurs in the amplitude region just above threshold, threshold being defined as the input amplitude that produces 50% triggering. Slewing specifications are frequently given over an input amplitude range from threshold to a specified overload factor (such as 10X threshold).

No commonly accepted standard exists for measuring the slewing characteristics of discriminators. One technique which LRS considers relevant to describing a discriminator's timing characteristics is to obtain a time spectrum of shift in input-output delay when a uniform spectrum of pulse heights from belowthreshold to many times threshold is used to drive the discriminator. Such an input spectrum constitutes a relatively severe test of the discriminator's timing performance for it contains a relatively higher proportion of near threshold pulses than does a usual beam-derived photomultiplier spectrum. It takes into account all aspects of discriminator slewing performance and presents their combined effect in terms of a time dispersion curve such as indicated below.

621 SERIES TIME SHIFT SPECTRUM



From this curve, an integral curve such as shown below may be plotted indicating the percentage of the linearly distributed input events encompassed within any given time interval.



The above figures were plotted from computer-generated runs on several Model 621AL channels using a linear input amplitude distribution from 0 to -240 mV. System time resolution was <25 ps. Data in both curves was not corrected for input risetime of 500 ps. The F W H M of the time dispersion curve under these conditions is 125 ps.

GENERAL

Packaging: The 621 Series Discriminators are all packaged in a #1 NIM module with Lemo-type connectors. Due to front panel space limitations, the 621's are not offered with BNC's.

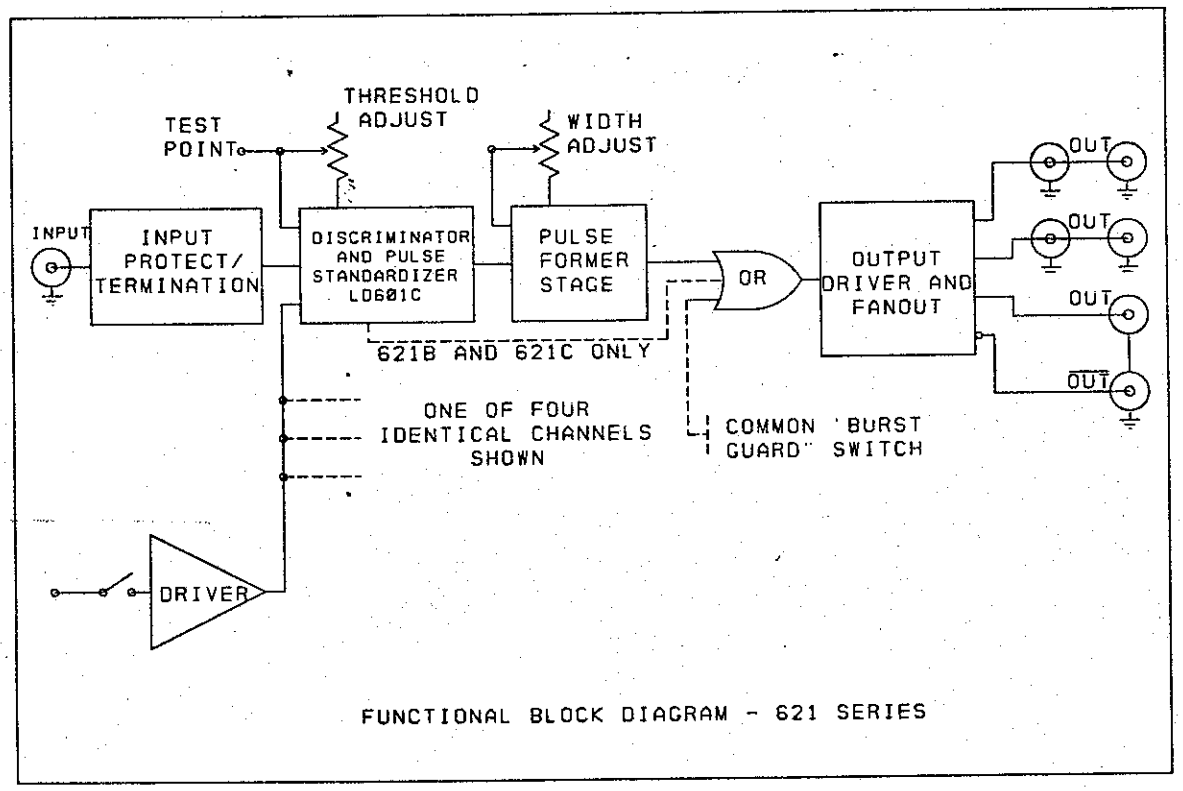
Current Requirements: The current usage of the 621AL is low enough to permit the use of 12 modules per standard 96-watt NIM bin offering a 5 A of $\pm$-6V, 2 A of $\pm$12 V, and 1 A of $\pm$24 V. Power calculation works out to 7.74 watts, which does not exceed the 8 watts recommended by the NIM standard for maximum power dissipation for a single NIM slot.

The 621BL and 621BLP draw slightly more milliamps of -6V current than does the 621AL, which was necessitated by the addition of the Burst Guard mode. Total power consumption is 7.86 watts, (less than the 8 watt NIM requirement), but the higher drain upon the -6 volt supply means that only 11 modules should be used in a NIM bin that only supplies 5 A of -6V current.

The Model 621CL requires considerably more current than does the 621AL and 621BL to maintain its full differential-type outputs. The current drain upon the -6 volt supply is 750 mA, indicating barely 7 units per bin offering 5 A of -6V, or 11 units per bin for those bins offering 8 A of -6V. Power dissipated by the 621CL is approximately 11 watts, so it is highly recommended to use a NIM bin with higher power dissipation limits, or to take care to carefully choose low power modules for the remaining slots in the bin, or to perhaps leave some NIM slots blank.

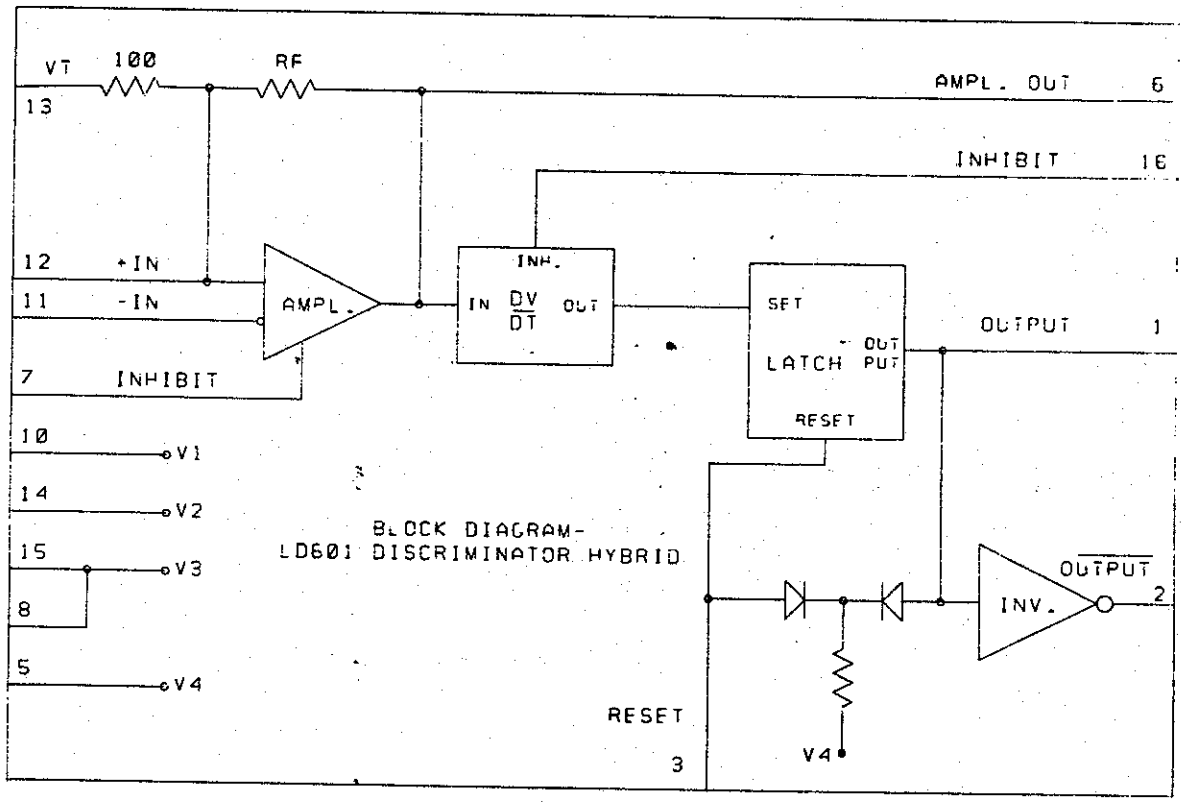
Recommended Use of the NIM Power Bins: It is highly recommended to keep any NIM bin at as constant a temperature as possible, using air conditioning in the trailer or experimental station and definitely using fans to assure an air flow through all modules in every bin. Elimination of large temperature variations removes the worry of temperature drift effects upon modules of any manufacturer, and the forced air flow is good insurance against the potential failure of components in the modules due to excessive heating for extended periods of time. Despite the fact that all components are pre-aged and burned-in before insertion into LRS modules, and the modules themselves are temperature cycled for days under power between initial test and final test, it is recommended to avoid subjecting any modules to adverse operating conditions if it could be avoided.

General: Each of the four channels of the 621 Series models is composed of three basic sections: the input and discriminator stage, the timing or pulse-former stage, and the output stage. A block diagram of the 621 Series models can be seen below, and a complete schematic of the specific model can be found at the end of this manual.



FUNCTIONAL BLOCK DIAGRAM - 621 SERIES

Input and Discriminator: The input and discriminator stage is based on the LRS Model LD601C hybrid. This unit contains all of the circuitry of the discriminator with the exception of the input termination and high voltage protection. The latter two functions are self-explanatory in the schematic enclosed, and the LD601 is functionally presented on the following page. The threshold level is set by changing the voltage bias on a fast differential amplifier which has a small amount of positive feedback to provide regeneration at threshold. In actual operation the V_T input is grounded, and the threshold level is determined by the 10:1 voltage divider (composed of the external 909 Ω and internal 100 Ω resistors) operating from a voltage which is set by a front-panel potentiometer and monitored at the front panel test point.



BLOCK DIAGRAM-
LD601 DISCRIMINATOR HYBRID

The measured voltage will be 10 times the actual threshold voltage. When an input signal applied to -IN is equal to the threshold voltage at +IN, the amplifier output will begin to go positive. This will force +IN closer to 0 volts, which increases the differential input voltage in such a direction that the output locks and then the cycle reverses. The amplifier output thus provides a time-over-threshold pulse with fixed amplitude. This pulse can be monitored at the AMPL. OUT point (Pin 6) and is used to do the Burst Guard mode in the 621B and 621C. The quiescent level should be nominally -2.4 volts going to -1.6 volts during the pulse. The leading edge of this output sets the latch circuit which is used as a pulse width standardizer. Before the amplifier and the latch can be set, the inhibit inputs (used for the bin gate) must be off. The required level at Pins 7 and 16 of the LD601C must be 0 to -1.6 V to enable, and -2.5 to -6.0 to disable. The purpose of the first inhibit is to avoid generating a low level transient at the output associated with the leading edge of an amplified input pulse inhibited at the dV/dt stage only. (The common bin gate driver shifts this so that 0 volts at the Bin Gate input will inhibit, greater that +3 volts will enable.) Once the latch is set,

a latch OUTPUT is available to start the 621 Series timing stage. The OUTPUT amplitude and leading edge should be similar in appearance to the AMPL OUT above, but the width of the output will be fixed independent of the input width. Internally, the latch output is fed back to reset the latch after a short time delay, thus generating a short output pulse whose actual width can be set by the proper external selection of RC time constant and voltage levels at Pins 3 and/or 4. It is set at approximately 3 nsec in the 621 Series models.

Two trim resistors T1 and T2 are associated with this stage. (See enclosed schematic.) T1 sets the minimum threshold. T2 calibrates the LD601C threshold to the test point voltage at its respective channel. If the LD 601C is changed, T2 will probably require trimming.

Older 621AL, 621BL, and 621CL units use the LD601B hybrid, while more recent units use LD601C's. These two hybrids are identical and interchangeable. However, LD601's should only be used in the 621L.

Timing Stage: The timing or pulse-forming stage of the 621 Series utilize three stages of MC1692 MECL receivers for amplifying and shaping. The timing is done by first charging a 33 pf capacitor with the pulse from the LD601C (via one MC1692 stage and the differential stage, composed of two A430 transistors) until it is clamped by the FD777 diode to a voltage set indirectly by the front-panel width potentiometer (via two stages of 747). The discharge rate is set by the current source stage composed of the width potentiometer, one stage of 747, the current source transistor, and its associated 604 Ω emitter resistor. The actual current is varied from near zero (for the 1 μsec maximum width) to about 10 mA (for the 5 nsec minimum width). Thus, simultaneously, as the width is increased, the clamp voltage is increased (allowing more initial charge to be stored on the timing capacitor) and the current is decreased (reducing the rate of discharge), thus multiplying the effect of the width control. An internal trim resistor, Tw, sets the minimum width to 5 nsec. The effect of the 2N5962 and the diodes associated with it are to provide fast recovery of the timing capacitor. The 1692 ECL amplifiers are interconnected in a manner to provide stable leading edge timing and fast risetimes and falltimes of the output pulse. The first amplifier (output pin 3) provides final shaping and standardization of the pulse from the LD601C to the timing stage, as well as driving the output stage directly via a second 1962 amplifier (output pin 14). This provides a prompt output pulse

for the duration of the 601C output, independent of the delay encountered in initializing the timing stage. Before the 601C output is over, the timing capacitor is charged, causing the third 1692 amplifier (output pin 15) to now maintain the pulse level to the output stage (using emitter ORing) until the timing capacitor subsequently discharges to a sufficiently low level (approximately -2.0 volts). At this point (because of regeneration) the third amplifier promptly switches back to its quiescent off condition, terminating the output pulse.

The Models 621B and 621C both have an optional Burst Guard mode. This mode is activated by a front-panel switch which enables a fourth stage of the 1692 (present, but not used in the 621A). When enabled, it receives its input from the AMPL OUT of the LD601C. When the input rate exceeds the DPR capability of the LD601, this point begins to "pump up" such that it does not fall below the ON level of the 1692. Its output level is wire-ORed with the feedback input of the 1692 which is driven from the timing stage to appear finally to the output stage as an "ON" level for the duration of the "Burst" at the front panel input.

Output Stage: The output stages of all but the 621C utilize two different types of circuits. The single normal and complementary outputs use a conventional differential stage. This stage requires a continuous 16 mA of current which is quiescently available at the complementary output connector. During an output pulse, the MC1692 will switch from the quiescent level of -2.4 volts to a higher level of -1.6 volts, causing the differential stage to switch the 16 mA current from the complementary to the normal output connector for the duration of the pulse. The other two pairs of outputs each supply 32 mA of current during the pulse, because at this time the bases of the two A430 transistors are at -1.6 volts. The emitters are therefore at about -2.4 volts. This places about 600 mV across each 18 Ω emitter resistor, and the resulting 32 mA will be available at each output connector pair for the duration of the pulse. Quiescently, the bases of these transistors are at -2.4 volts; therefore, there is only -600 mV drop available for V_{BE} so the transistors are off, resulting in a substantial power saving. All outputs are diode clamped so they will provide proper operation even without output loads. Without the diode path for the current during the pulse, even on a single output stage, the current would have to be supplied via the transistor base, which would severely load the driver and not allow proper drive to the remaining stages.

The 621C output stage utilizes the same fully switched differential-type current source for all outputs as is used above for the single output. The only differences are that the dual output stages must stand and switch 32 mA each, and the complementary collectors are tied to ground instead of the output connectors. The slight advantage of this circuit is that the output pulses from the dual bridged output are aesthetically cleaner (i.e., it has less overshooting and a flatter top) than the switched single transistor current source used in the outputs of the other 621 Series.

Internal Power Supplies: Four internal power supplies are used to generate the -0.8, -2.2, -3.0, and -11.5 V which are special bias voltages used by the four channels. These stages provide voltage regulation and tracking and provide proper temperature compensation for the other sections, particularly the width and threshold circuits. They depend to some degree on uniform heating of the entire circuit board. Heating local areas of the board may cause drifting, but during operation in a normal bin environment these supplies compensate to stabilize operation. In all cases, the power supply uses a LM301 operational amplifier to maintain the output voltage of a series-pass transistor equal to an input reference voltage. The reference voltages are adjusted via individual potentiometers or trimmed resistors.

If the -6 voltage is sequenced on before the +6 voltage, the LD601 may be forced into a DC latched condition. To prevent this, a relay contact does not supply the -6 VDC until the relay coil, operating from the +6 VDC is energized. This insures that the +6 is up before the -6 in any power-on sequence.

Programming in the 621BLP: The Model 621BLP is a standard 621BL which has the critical threshold and width control voltages brought directly out to an added rear panel 20-pin connector. Internal high frequency filtering is provided (i.e., T_{RC} + 0.01 seconds) on each input.

The remote programming voltage source must be low impedance (ideally less than 100 Ω). When using the front panel potentiometers, the rear panel programming should be removed.

This Test and Calibration Section has been included to familiarize the service technician with the areas that should be checked when searching for sources of failures and after replacing components, especially front end hybrids (LD601's). The trouble-shooting section is by no means exhaustive, but it does provide insight into some of the problems that have occurred at LRS during the initial testing of the 621L's. The technician should follow the "Trouble-Shooting Guide" for ease in determining the defective component. Replacement of critical components will require some recalibration.

Trouble-Shooting

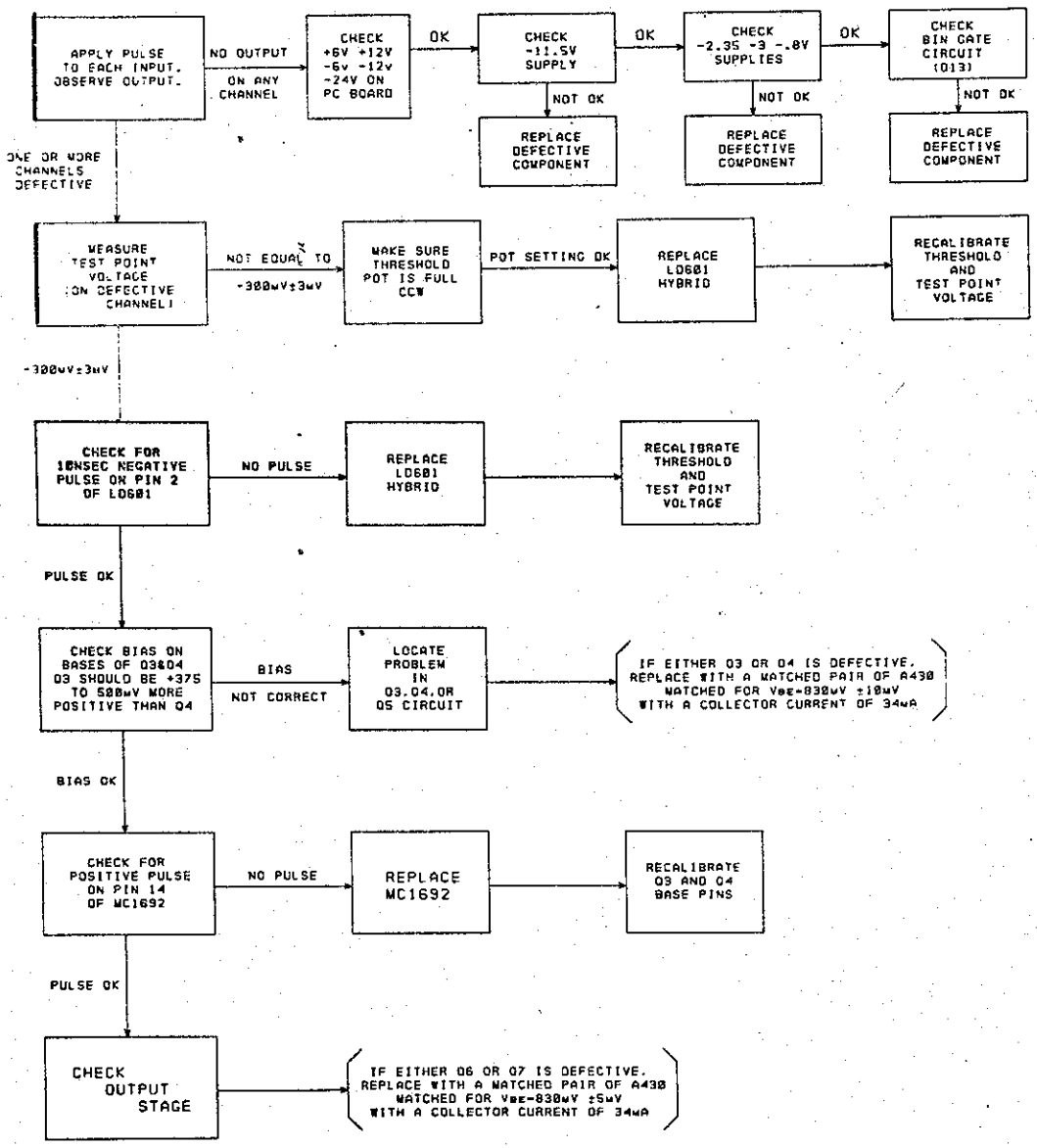
Equipment Required:

1. Digital voltmeter.
2. Sampling scope; 50 Ω input impedance.
3. High impedance real time scope with bandwidth of 150 MHz or greater (Tektronix 454, 475, or equivalent).
4. Pulse generator or signal source capable of producing 10 nsec-50 mV pulse into 50 Ω.

Initial Setup:

1. Use NIM power extended cable to power the 621 under test.
2. Set all threshold and width pots to their full counterclockwise position (threshold equal to -30 mV and width equal to less than 5 nsec).
3. Apply a 10 nsec negative pulse (approximately equal to -50 mV) in turn to each input. Check output on sampling scope.
4. Follow the "Trouble-Shooting Guide", next page.

TROUBLE-SHOOTING GUIDE



Field Replacement of LD601

Pin 7/Pin 16 Jumper Consideration

In late 1973, it was determined that for optimum performance of the discriminator front end, (LD601 hybrid), pin 7 of the LD601 should be externally jumpered to pin 16. This external jumper is provided on the circuit boards themselves of the following discriminators:

Model 621AL, 621BL, 621BLP, 621CL, 621S, Quad

Model 620AL, 620BL, 620BLP, 620CL, 623, Octal

For the Model 621L, Quad, only units produced after November 28, 1973, have the jumper included.* For the 620L Octal, only units produced after October 10, 1973, have the jumper included.

Therefore, for proper installation of replacements LD601's or LD601C's, we can summarize as follows:

(See next page.)

*Approximate production dates can be determined by the dates written on the rear panel Test and Calibration stickers.

TEST & CALIBRATION

Model	LD601C	LD601D	LD601E
621L	Make sure pins 7 and 16 are jumpered.	Make sure pins 7 and 16 are jumpered. Add 3.2 -18 pf trimmer from pin 3 to Gnd. Adjust for optimum output shape.	Cannot be used in 621L.
621AL	Direct replacement.	Add 3.2 -18 pf trimmer from pin 3 to Gnd. Adjust for optimum output shape.	Cannot be used in 621AL.
621BL	Direct replacement.	Add 3.2 -18 pf trimmer from pin 3 to Gnd. Adjust for optimum output shape.	Direct replacement, but only in units originally containing LD601E.
621BLP	Direct replacement.	Add 3.2 -18 pf trimmer from pin 3 to Gnd. Adjust for optimum output shape.	Direct replacement, but only in units originally containing LD601E.
621CL	Direct replacement.	Add 3.2 -18 pf trimmer from pin 3 to Gnd. Adjust for optimum output shape.	Direct replacement, but only in units originally containing LD601E.
621S	Direct replacement.	Add 3.2 -18 pf trimmer from pin 3 to Gnd. Adjust for optimum output shape.	Direct replacement, but only in units originally containing LD601E.
620L	Make sure pins 7 and 16 are jumpered.	Make sure pins 7 and 16 are jumpered. Add 3.2 -18 pf trimmer from pin 3 to Gnd. Adjust for optimum output shape;	Cannot be used in 620L.
620AL	Direct replacement.	Add 3.2 -18 pf trimmer from pin 3 to Gnd. Adjust for optimum output shape. Also remove Min. and Max. trims. Adjust front panel width control to max.(CMW).Adjust trimmer for 22.5 nsec output width.	Cannot be used in 620AL.

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TEST & CALIBRATION

Model	LD601C	LD601D	LD601E
620BL	Direct replacement.	Add 3.2 -18 pf trimmer from pin 3 to Gnd. Adjust for optimum output shape. Also remove Min. and Max. trims. Adjust front panel width control to max. (CMW). Adjust front panel width control to max. (CMW). Adjust trimmer for 22.5 nsec output width.	Direct replacement, but only in units originally containing LD601E.
620BLP	Direct replacement.	Add 3.2 -18 pf trimmer from pin 3 to Gnd. Adjust for optimum output shape. Also remove Min. and Max. trims. Adjust front panel with control to max. (CMW). Adjust front panel width control to max. (CMW). Adjust trimmer for 22.5 nsec output width.	Direct replacement, but only in units originally containing LD601E.
620CL	Direct replacement.	Add 3.2 -18 pf trimmer from pin 3 to Gnd. Adjust for optimum output shape. Also remove Min. and Max. trims. Adjust front panel with control to max. (CMW). Adjust front panel width control to max. (CMW). Adjust trimmer for 22.5 nsec output width.	Direct replacement, but only in units originally containing LD601E.
623	Direct replacement.	Cannot be used in 623.	Cannot be used in 623.
623A	Cannot be used in 623A.	Direct replacement.	Direct replacement, but only in units originally containing LD601E.

January, 1977

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

REQUIRED RECALIBRATION IF LD601, MC1692, OR TIMING STAGE COMPONENTS WERE REPLACED

Replacement of LD601: If any LD601 was found to be defective and required replacement, the Threshold and Test Point voltage should be recalibrated.

Procedure:

1. Set front panel Threshold pot to minimum (counterclockwise).

2. Measure Test Point voltage. If not equal to -300 ±5 MV, replace existing trim resistor T_1 (across 50 KΩ pot) with proper resistance to bring Test Point voltage into required range. (See trim resistor chart to aid in selecting correct value.)

3. Check Threshold level with a 5 nsec wide pulse; if it is not -30 mV, replace existing trim resistor T_2 (across 12.4 KΩ resistor) with proper resistance. (See trim resistor chart to aid in selecting correct value.)

Replacement of MC1692 IC "C": If the MC1692 was found to be defective and required replacement, the base bias of Q3 and Q4 should be recalibrated.

Procedure:

1. Measure the base voltage of Q4 with respect to the base voltage of Q3. This voltage should be between +375 and +500 mV.

2. Select proper trim resistor to obtain above voltage. (This trim resistor is connected from the base of Q5 to the -11.5 volt supply.)

3. Observe output width if less than 1 μsec with front panel width pot set to its full clockwise position. Retrimming will be required. (See Calibration (9) Maximum Width.)

4. Output Amplitude Adjustment: With one output terminated, the output amplitude of the bridged outputs should be greater than -750 mV. If less than 750 mV, the -3 V supply should be readjusted. Wide channel-to-channel variation of output amplitude indicates poorly matched MC1692 and/or output A430's. In order to reduce the channel-to channel output amplitude

variation without replacing any active devices, the emitter resistor of Q6 or Q7 (16 Ω) can be changed. (To increase the output amplitude, the value of this resistor should be decreased.)

Replacement of Q3 and Q4:

1. Observe output width of less than 1 μ sec with front panel width pot set to its full clockwise position. Retrimming will be required. (See Calibration (9) Maximum Width.)

CALIBRATION

The following is a detailed step-by-step calibration procedure for the 621L (and 621AL) Discriminator. The sequence should be followed to avoid extraneous labor.

Important Notes:

a. When actual trim and calibration adjustments are performed, be sure the unit had at least 5 minutes of warmup time. (Calibration may be off if warmup time is too short.

b. If for any reason long periods of time between trimming occur, be sure to double-check periodically the bin voltages (Step 3). (Power supply voltage may change and calibration may be off when performed to the new changed voltage.)

c. A "Voltage vs Resistance graph" is attached to the end of this procedure and can be utilized to ease the selection of the correct value resistor for some of the trim requirements.

d. If at any check or calibration step problems occur, refer to the Trouble-Shooting Guide.

Procedure:

1. Check (on board) the presence and verify the following correct voltages: -12.00 V, -6.00 V, and +6.00 V, and -24.00 V. These voltage points are clearly marked on the rear of the PC board.

2. -11.5 volt regulator (new units only)--Measure the voltage on the -11.5 V bus. Readjust pot (wiper connected to Pin 2 IC "H") if voltage is not -11.5 V ±50 mV.

3. -2.35 volt regulator--Measure voltage on the -2.34 V bus (or 2.2 V bus for 621AL). If voltage is not -2.35 V ±2% (or -2.2 V ± 2% for 621AL), retrimming will be necessary. The existing trim resistor across the 6.98 KΩ resistor (from Pin 3 or IC "E" to the -11.5 V supply) should be removed and replaced by one of proper value.

4. -0.8 volt regulator--Measure voltage on the -0.8 volt bus. If voltage is not -0.8 V ±2%, retrimming will be necessary. The existing trim resistor across the 909 Ω resistor (from Pin 3 or IC "F" to ground) should be removed and replaced by one of proper value.

5. -3 volt regulator--The -3 V regulator should only be adjusted if the output amplitudes of the bridged outputs are less than -750 mV when driving a total load impedance of 25 Ω. An adjustment pot is provided to adjust the -3 V regulator.

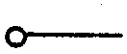
6. Q3 and Q4 bias--Measure the voltage on the base of Q4 with respect to Q3 base. If voltage is not between 270 mV and 330 mV, retrimming will be necessary. The existing trim resistor across the 8.2 KΩ or 7.5 KΩ resistor (from the base of Q5 to the -11.5 V supply) should be removed and replaced by one of proper value.

7. Test point voltage--Turn front panel Threshold pot to its full counter-closkwise position (30 mV threshold). Measure voltage at front panel test point with respect to ground. If voltage is not equal to -300 ±5 mV (10 times threshold), retrimming will be required. The existing trim resistor T_1 (across the 50 KΩ pot) should be removed and replaced by one of proper value. A trim resistor chart to aid in selecting correct value is included on last page of this section.

8. Threshold--Make sure front panel Threshold pot is turned to its full counterclockwise position (-30 mV threshold). Apply a 5 nsec wide -30 mV pulse to the input. The output should be present approximately 50% of the time. If it does not trigger at all, or if it always triggers, remove the existing trim resistor T_2 and replace it with one of the proper value to insure 50% triggering level.

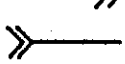
9. Maximum width--Turn front width pot to its full clockwise position. Apply input with amplitude large enough to trigger 621. Check output width. If it is less than 1 μsec, retrimming will be required. The existing trim resistor across the 220 Ω resistor (from one end of the width pot to the +6 supply) should be removed and replaced by one of proper value.

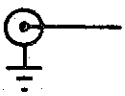
STANDARD DRAFTING SYMBOLS, ELECTRONIC


Connection to any given voltage.

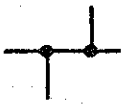
Line ending at the edge of the sheet indicates continuance on another sheet.


Male pin or card edge contact.


Female pin, socket or card edge connector.


Coaxial connector.


No connection.


Connection.

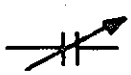

Resistor, 1/4 W, ±5%, value in ohms (unless specified otherwise).

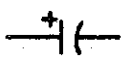
Resistor, 1/4W, ±1%, value in ohms (unless specified otherwise).

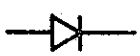

Resistor, variable, any type.

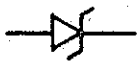

Resistor, variable, any type.


Capacitor, ceramic disc. Value in microfarads (unless specified otherwise).


Capacitor, variable. Values in Picofarads (unless specified otherwise).


Capacitor, polarized. Values in microfarads/volts (unless specified otherwise).


Diode, signal or rectifier.


Diode, zener.

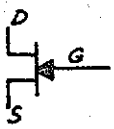

Diode, tunnel.


Diode, snap.

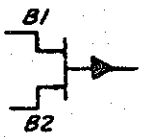

Light emitting diode (LED).

NPN Transistor.

PNP Transistor.



Field effect transistor, P Channel.



Field effect transistor, N.


Air choke.


Ferrite bead.


Ferrite core choke, Z 500 ohms when f ≥ 60 MHz (unless otherwise indicated).


Ferrite core choke, 40 uH, (unless otherwise indicated).

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

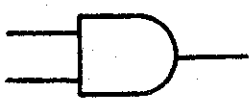
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL).

The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

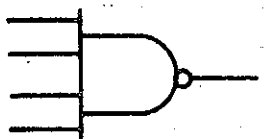
Positive logic notation is used. Logical "0" is nominally zero Volts and logical "1" is nominally 2.5 Volts.

Supply voltages of IC's are shown in a table on each schematic.

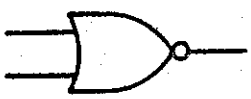
2-Input Positive NAND Gate



2-Input Positive AND Gate

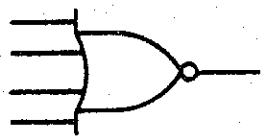


4-Input Positive NAND Gate

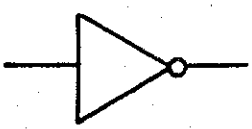


2- Input Positive NOR Gate

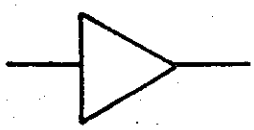
2-Input Positive OR Gate



4-Input Positive NOR Gate



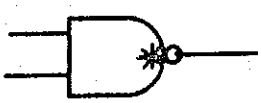
Inverter or Inverting Buffer



Non-Inverting Buffer

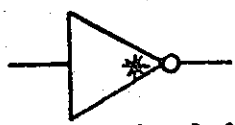
Exclusive OR Gate

Open collector outputs are identified by an asterisk (*) on the output connection.



2-Input Positive NAND Gate W/Open Collector

2-Input Positive OR Gate W/Open Collector



Non Inverting Buffer W/Open Collector

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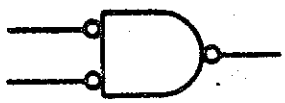
LeCroy Research Systems Corp.
Spring Valley, New York

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS EMITTER - COUPLED LOGIC (ECL)

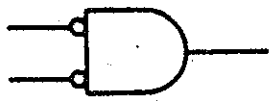
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Logical "0" is nominally -0.8 Volts and logical "1" is nominally -1.6 Volts.

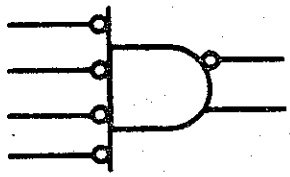
Supply voltages of IC's are shown in a table on each schematic.



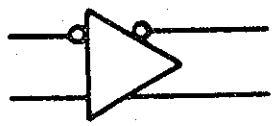
2 - Input Gate.
Negative AND (Positive OR) Gate.



2 - Input Gate.
Negative NAND (Positive NOR) Gate.

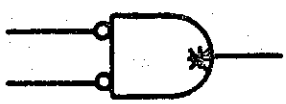


4 - Input Gate.
Negative AND/NAND (Positive OR/NOR) Gate.

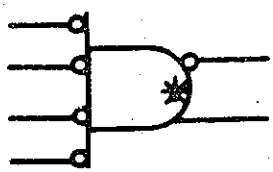


Differential
Amplifier.

Open emitter outputs are identified by an asterisk (*) on the output connection.



2 - Input Negative NAND Gate.
With Open Emitter.



A - Input Gate.
Negative AND/NAND (Positive
OR/NOR) Gate.

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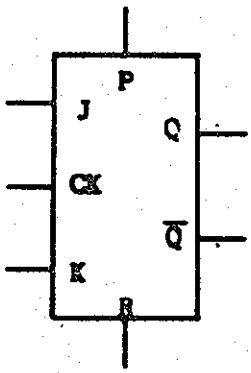
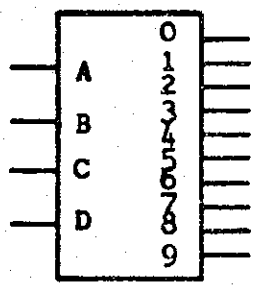
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL) OR EMITTER COUPLED LOGIC (ECL).

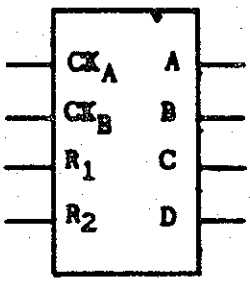
Flip-Flops and other MSI integrated circuits are generally drawn as a rectangular box with connections marked inside the outline. Some abbreviations are: R - Reset (or Clear), P - Preset (or Set), CK or CLK - Clock, etc. Some typical examples are shown below. See the manufacturer's specification for additional information.



J-K Master-Slave Flip-Flop

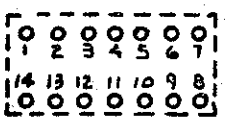


BCD-To-Decimal Decoder-Driver



Binary Counter

Orientation of pin numbers of any DIP (Dual-In-Line-Package) is shown below. Pin 1 will normally be identified on the printed circuit board.



Bottom View

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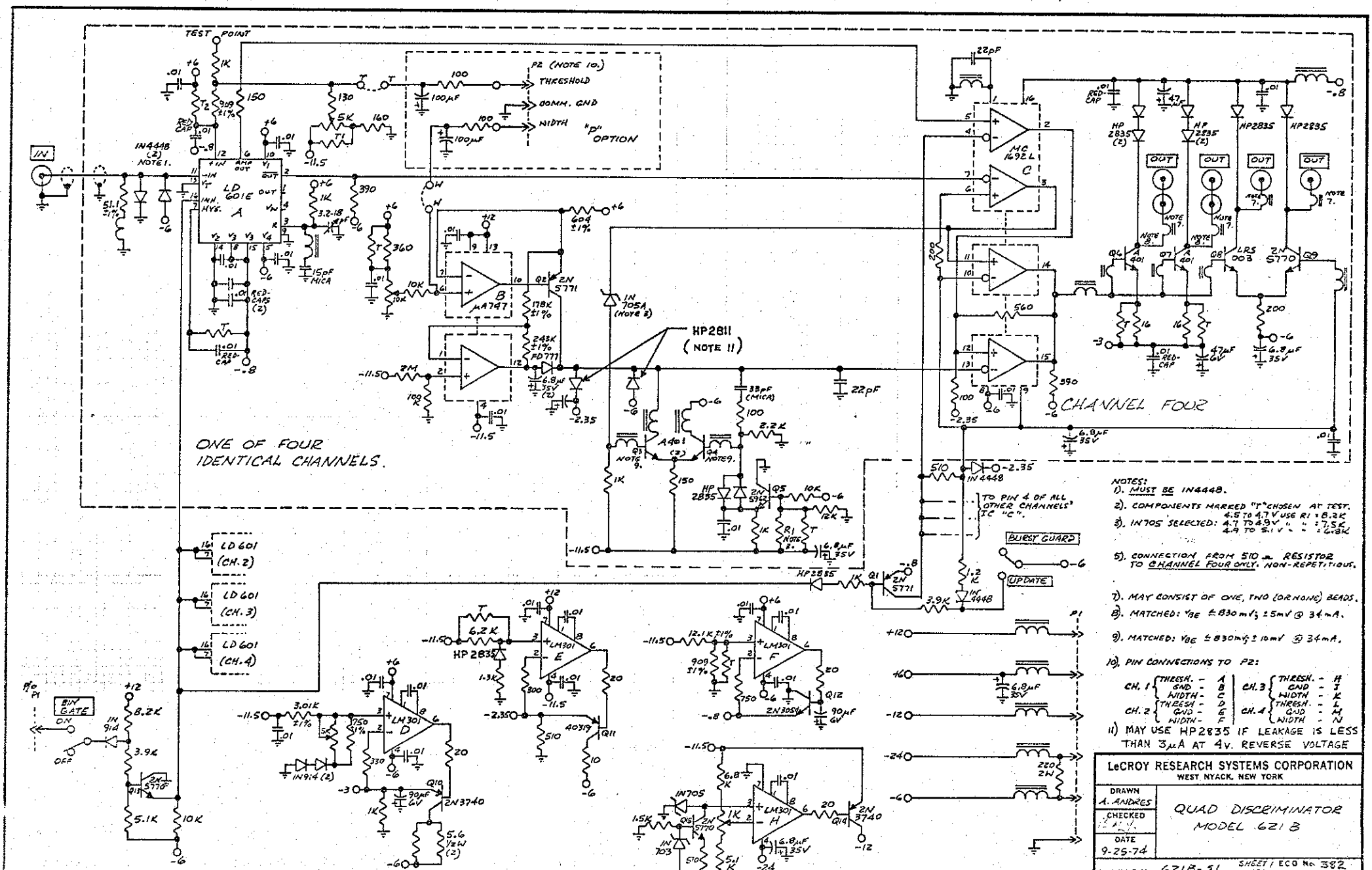

NOTES:
1). MUST BE IN4448.
2). COMPONENTS MARKED "T" CHOSEN AT TEST.
4.5 TO 4.7 V USE R1 = 8.2K
4.7 TO 4.9 V " " = 7.5K
4.9 TO 5.1 V " " = 6.8K
3). IN705 SELECTED: 4.7 TO 4.9 V
4.9 TO 5.1 V
5). CONNECTION FROM 510 Ω RESISTOR TO CHANNEL FOUR ONLY. NON-REPETITIOUS.
7). MAY CONSIST OF ONE, TWO (OR NONE) BEADS.
8). MATCHED: V_{BE} ± 830 mV; ± 5mV @ 34 mA.
9). MATCHED: V_{BE} ± 830 mV; ± 10mV @ 34 mA.
10). PIN CONNECTIONS TO P2:

CH. 1	THRESH. - A	CH. 3	THRESH. - H
	GND - B		GND - J
	WIDTH - C		WIDTH - K
CH. 2	THRESH - D	CH. 4	THRESH. - L
	GND - E		GND - M
	WIDTH - F		WIDTH - N

11) MAY USE HP2835 IF LEAKAGE IS LESS THAN 3μA AT 4V. REVERSE VOLTAGE

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN A. ANDRES	QUAD DISCRIMINATOR MODEL 621B
CHECKED	
DATE 9-25-74	

SHEET / ECO No. 382
621B-51

ECO NO.	DATE	DESCRIPTION
806	1-27-75	TAPING CHANGE FROM 621B/A TO 621B/B. CHANGES: 51 OHMS AT INPUT TO 51.1 PREC./ HP2800 AT PIN 12 OF uA747 CHANGED TO FD777/ TWO MBD 101 DIODES AT Q5 EMITTER CH. TO HP2835/ 8.2K FROM BASE OF Q5 CH. TO R1/Q1 WITH 1K RES. & ONE HP 2835 ADDED AT BURST GUARD SWITCH/ALL OUTPUT DIODES CHANGED TO HP2835 (6 PLACES)/ VARIABLE CAP. AT PIN 1 OF MC1692L CHANGED TO 22 pF/ ALL MUCON CAPACITORS CHANGED TO REDCAPS/ "T" RESISTORS ADDED AT EMITTERS OF Q6 AND Q7/ NOTE 6 DELETED/NOTE 3 CHANGED TO READ: IF 1N705 IS 4.6 TO 5.0 V, R1=8.2K. IF 5.0 TO 5.3 V, R1=7.5K/ POTENTIOMETER AT PIN 2 OF IC "H" CHANGED FROM 500 OHMS/
815	2-17-75	AT PIN 6 OF IC "B" - CH. 1 K RES. TO 10K/NOTES 8 & 9 CHANGED TO READ: $V_{BE} \leq 830$ mV; ± 5 mV @ 34mAand $V_{BE} \leq 830$ mV; ± 10 mV @ 34 mA/
837	3-26-75	1N4448 ADDED FROM PINS 6, 9 & 10 OF MC1692 TO -2.35V (ONLY IN CHANNEL WHICH DIRECTLY CONNECTS TO BURST GUARD-UPDATE SWITCH.
840	3-31-75	ALL .05 CAPACITORS CHANGED TO .01 25V.
843	4-3-75	PARTS LIST CORRECTIONS ONLY, TO CONFORM TO WORKING MODEL & SCHEMATIC.
869	6-16-75	ADD: 100 OHM RES. IN SERIES WITH 33pF MICA CAP FROM PIN 13 OF MC1692L
890	7-11-75	BOARD OUTLINE CHANGED TO FIT NEW WRAPAROUND/ THRESHOLD CKT CHANGED.
894	7-22-75	ADDED: 3.2 TO 18 pF CAP FROM PIN 3 OF LD 601D TO GROUND.
953	10-21-75	RELAY REMOVED FROM -6 VOLT LINE. ALSO ASSOCIATED 100 OHM RESISTOR.
965	10-28-75	BURST GUARD MODIFICATION. TAPING CHANGES FROM /E TO /F.
988	12-8-75	Q 3, 4, 8 & 9 CHANGED TO FLRS 003 WITH BEADS ON BASE AND COLLECTOR OF EACH/ Q6 & 7 CH. TO A 401 WITH BEAD ON BASE OF EACH/ BEAD REMOVED AT MC 1692 PINS 14 & 15 AND REPLACED WITH JUMPER/ 22 pF CAPACITORS REMOVED FROM Q6E AND Q7E/ VARIABLE CAP REM. FROM MC 1692 PINS 6 TO 3/ NO TAPING CHANGE.
036	2-9-76	FULL BEADS REMOVED: BASES OF Q6, Q7 & Q 8, ALSO COLL. OF Q8 AND Q9. FULL BEAD ADDED: PIN 14 OF MC1692. HALF-SIZE BEADS ADDED: BASE OF Q6, Q7 AND Q8/ 22pF CERAMIC CAP ADDED ON PIN 13 OF MC1692/ NEAR PIN 6 OF uA747: 220 OHM RES. CH. TO 360 OHMS.
048	2-23-76	PARTS LIST ONLY AFFECTED: SIGNAL RING NUMBER CHANGE.

REMARKS FOR ECO # 126 & UP, SEE SHEET 2.

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN
CHECKED
DATE

ENGINEERING CHANGE ORDERS

MODEL 621B

DRAWING No.

ECO NO.	DATE	DESCRIPTION
126	4-15-76	LD601D CHANGED TO LD601E/ AT PIN 12 OF SAME: 12.4K DELETED AND .01 TO -.8V ADDED. AT PIN 6: 82Ω RES. CHANGED TO 150Ω, 22pF DELETED. AT PIN 7: CONNECTION TO INH. BUS BROKEN, "T" RESISTOR AND .01 REDCAP ADDED TO -.8V.// Q3 AND Q4 CHANGED TO A401/ NOTE 11 ADDED/ SINGLE-LEAD CHOKE ADDED TO-.8V LINE / NOTE 3 CHANGED TO INCLUDE ONE MORE CHOICE OF R1.
205	7-29-76	CIRCUIT CHANGED FROM /F TO /G TO PICK UP CHANGES OCCURRED ON ECO 126 (LD601D REPLACED WITH LD601E).
273	11-8-76	TAPING CHANGED FROM G TO H (22 pF CAPACITOR TAPED IN). Q9 CHANGED TO 2N5770.
380	4-29-77	CORRECTED ASSEMBLY DRAWING.
382	5-3-77	CHANGED ALL MBD101 DIODES TO HP2811 EXCEPT DIODE CONNECTED TO I.C.E. PIN 3 WHICH SHOULD BE HP2835.
492 & 495	10-12-77	SILVER LEMO SIGNAL RING ELIMINATED FROM 621BL AND 621BLP, RESPECTIVELY.

REMARKS FOR ECO # 48 & EARLIER SEE SHEET 1.

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN	ENGINEERING CHANGE ORDERS
CHECKED	MODEL 621 B
DATE	SHEET 2.

DRAWING No.