ASIC design for MPGDs

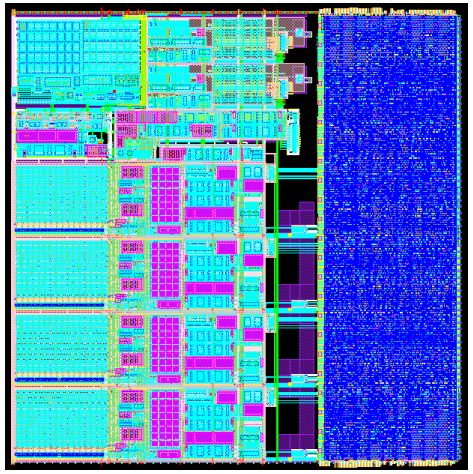
RD51 Topical Workshop on
FE electronics for gas detectors
June 17, 2021

Istituto Nazionale di Fisica Nucleare

Manuel Da Rocha Rolo

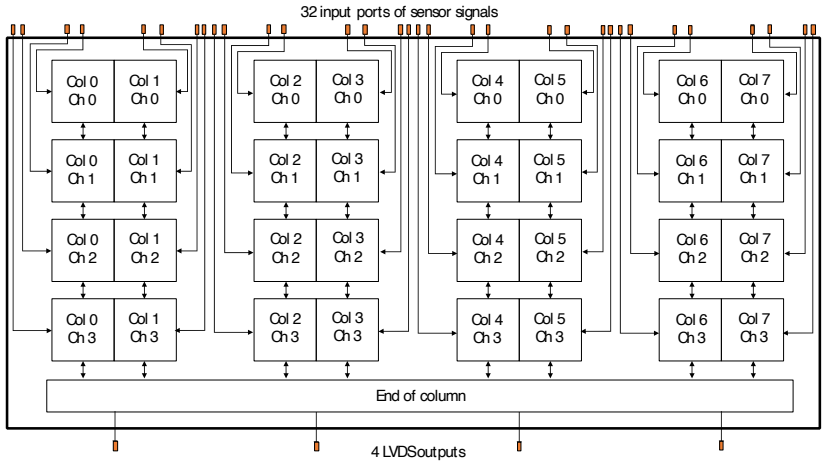
SoCs for next-gen MPGD readout

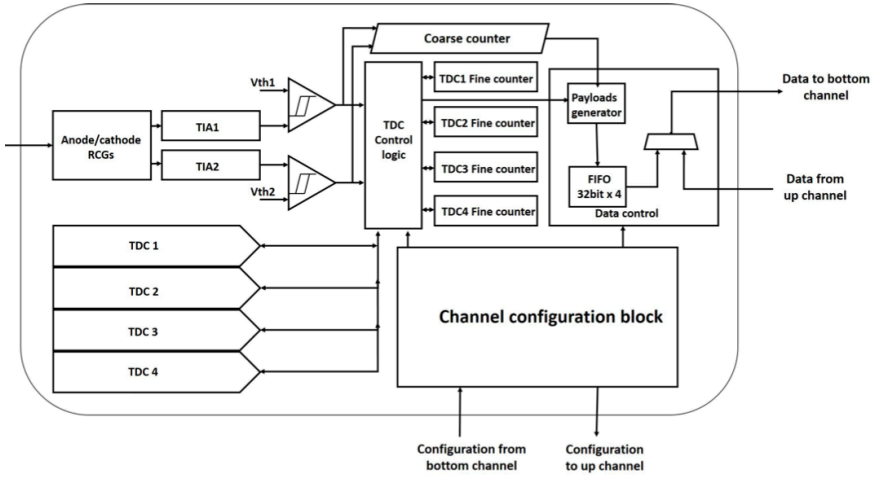
The ALCOR concept: a timing/ToT engine easily adaptable to different kind of detectors



scalable matrix and end-of-column architecture with digital-on-top integration flow

- Pixel pitch below 500 μm, current version 32-pixel matrix
- the chip performs amplification, signal conditioning and event digitisation, and features fully digital I/O.
- Pixel hosts dual-polarity configurable gain VFE+shaper, 2 LE discriminators, 4 TDCs, digital control and interface
- 64-bit (32-bit on time tagging mode) event and status data is generated on-pixel and propagated down the column
- 4 LVDS TX data links, SPI configuration and SEU protection on FSM and configuration registers
- operation up to 320 MHz (TDC binning down to 50 ps and event rate exceeding 500 kHz per channel)





Manuel Da Rocha Rolo (INFN) — darochar@to.infn.it

Thanks for your attention.

Istituto Nazionale di Fisica Nucleare