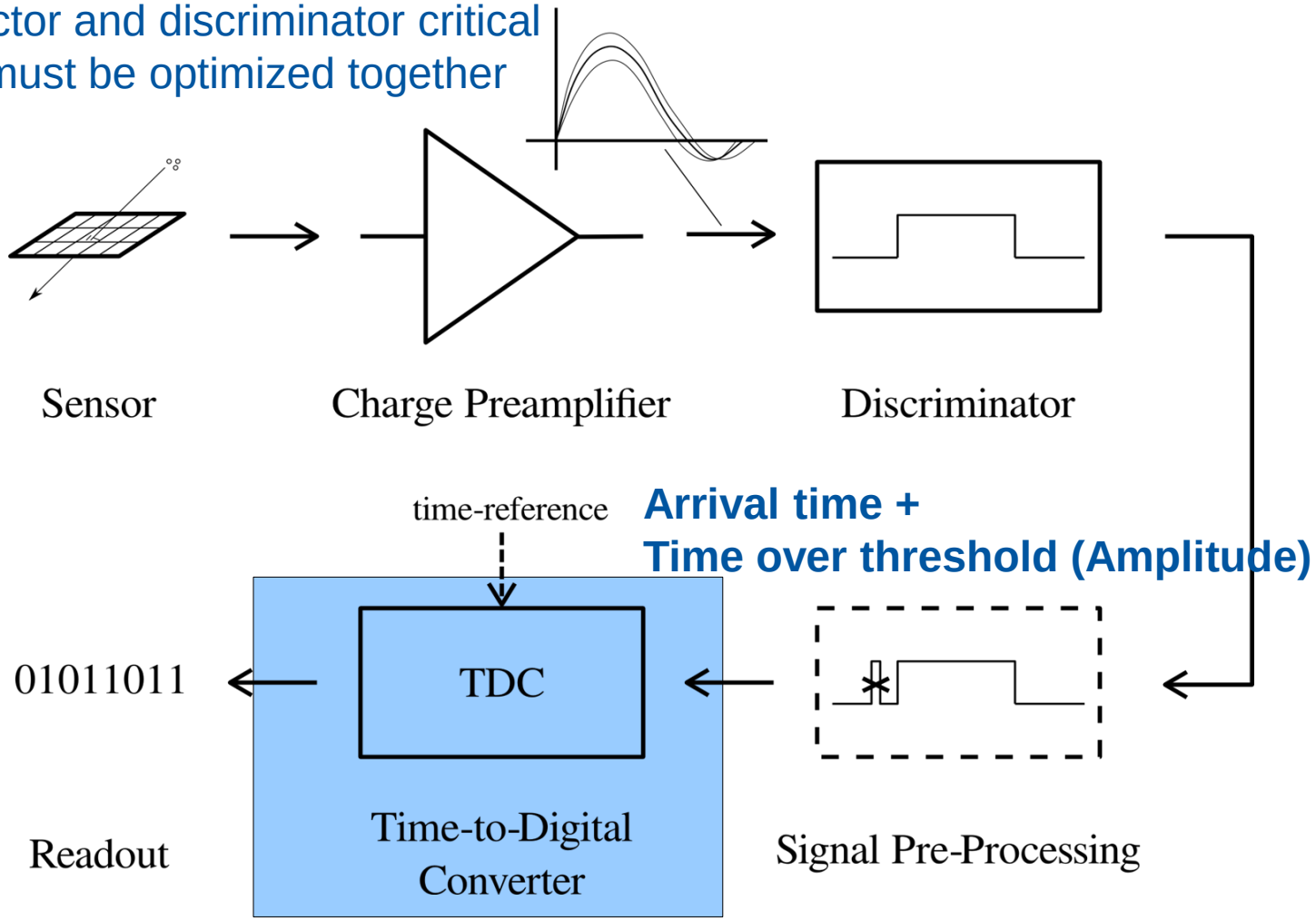

CERN

PicoTDC: General purpose 64 channel 3/12ps TDC

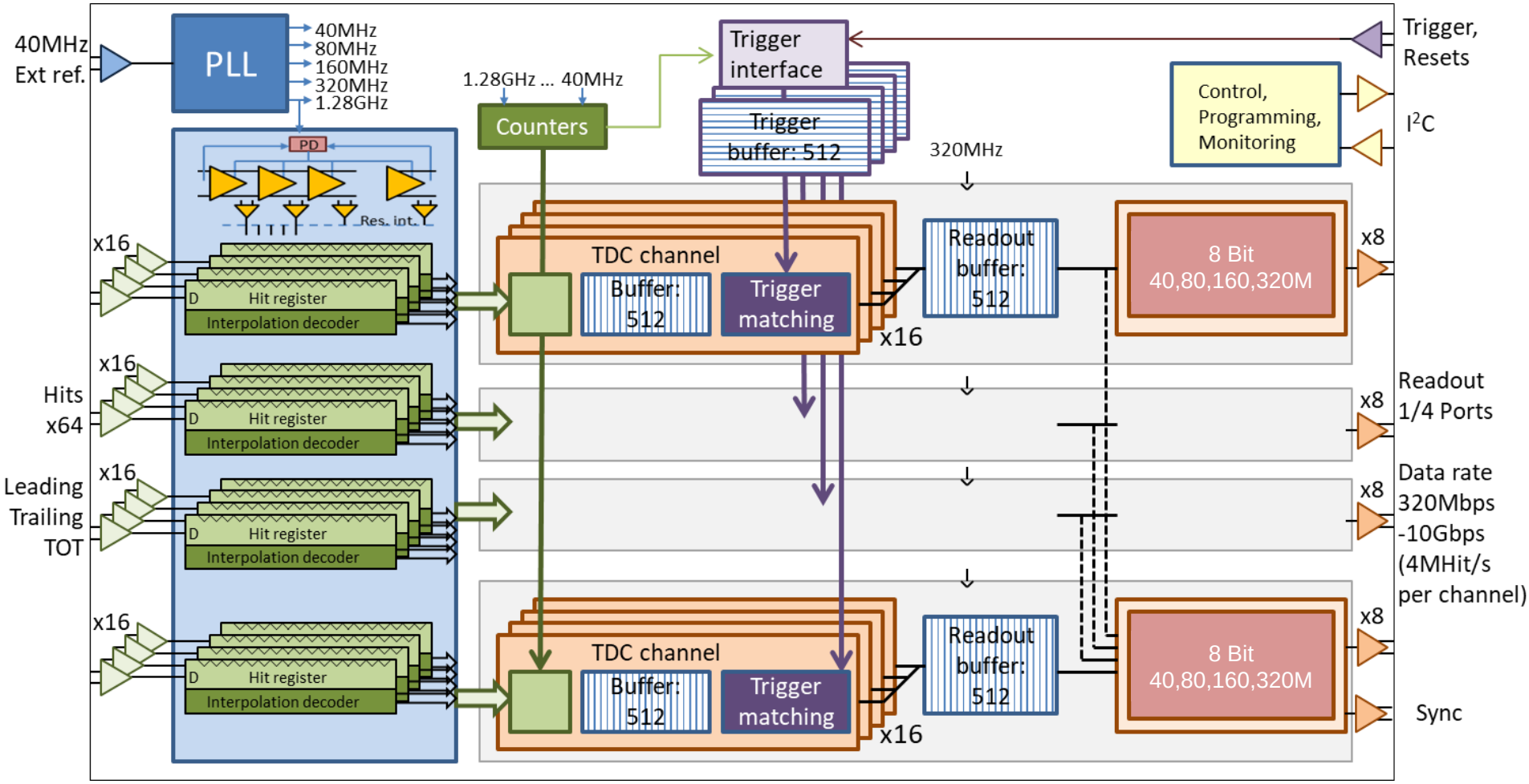
Moritz Horstmann, Samuele Altruda, Jeffrey Prinzie (KU Leuven),
Jorgen Christiansen

TDC in the Measurement Chain

Detector and discriminator critical and must be optimized together

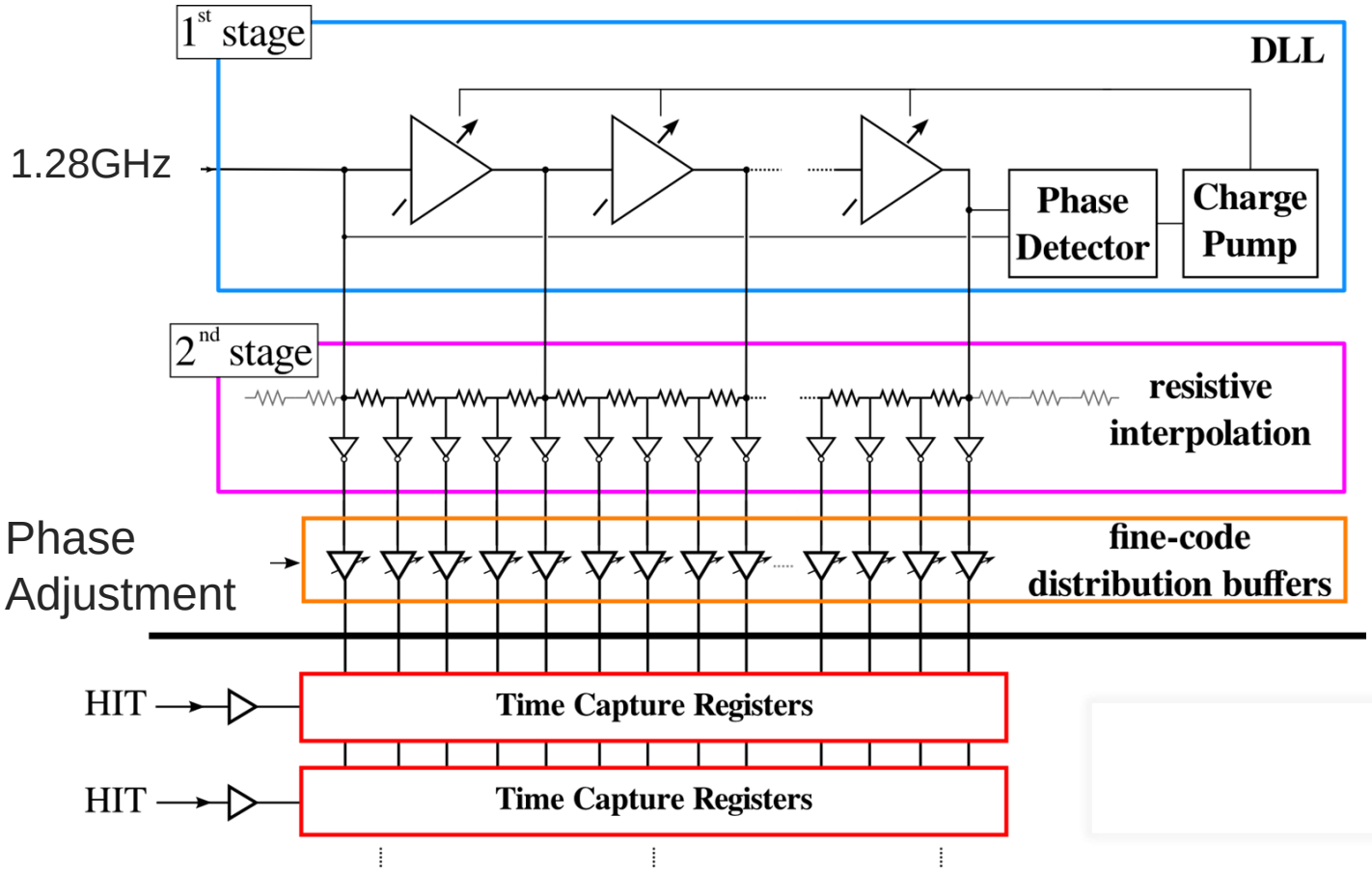


PicoTDC Architecture



64 channels, 3ps or 12ps time binning, 200us dynamic range

Two Stage Time Interpolation



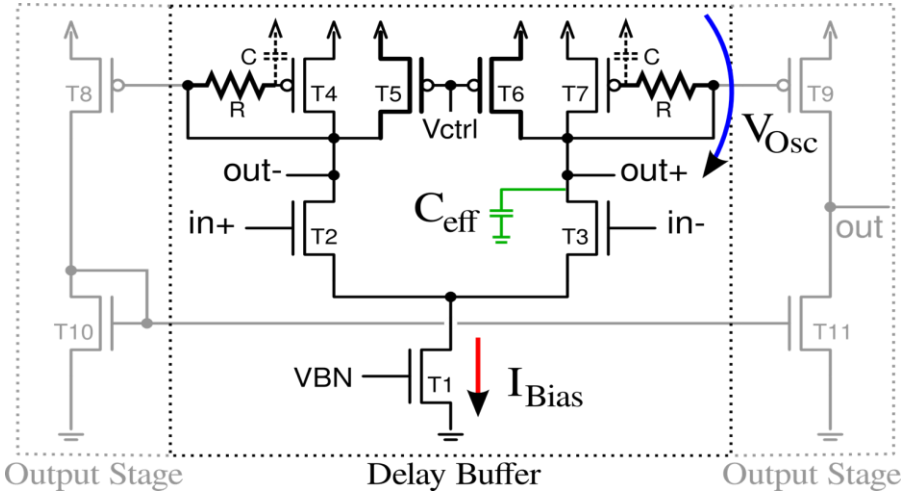
12.2ps delay

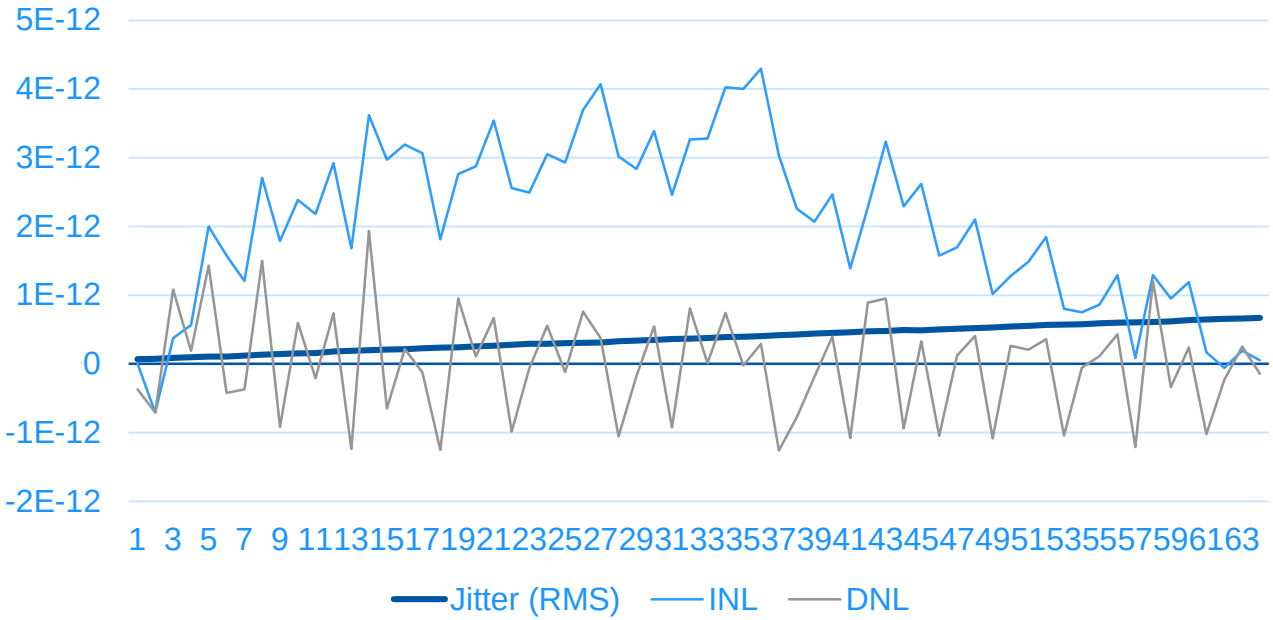
3.05ps delay

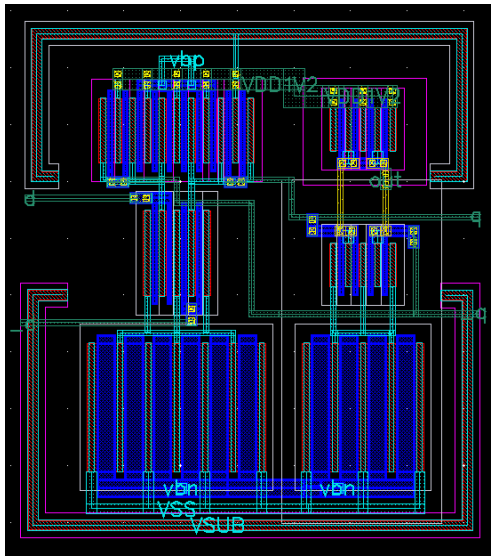
32 steps each with 0.6ps resolution

1st Stage: DLL

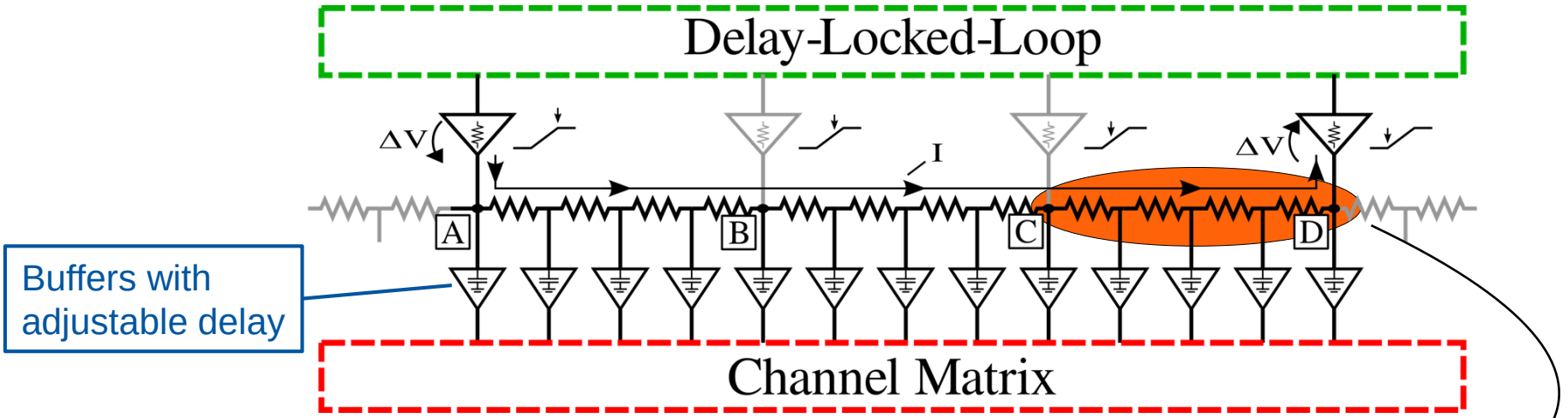
- 64 taps, 12.2ps delay
- Self-Calibrating



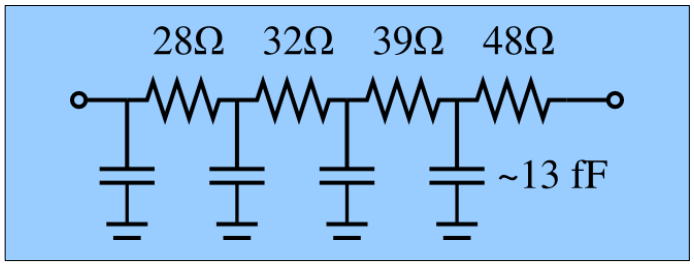


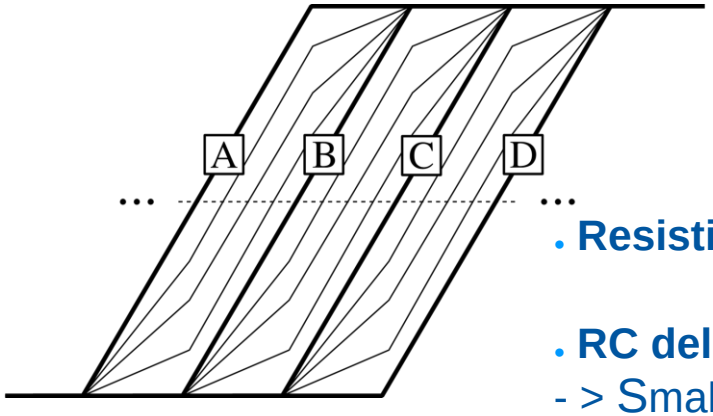


2nd Stage: Resistive Interpolation



Buffers with adjustable delay

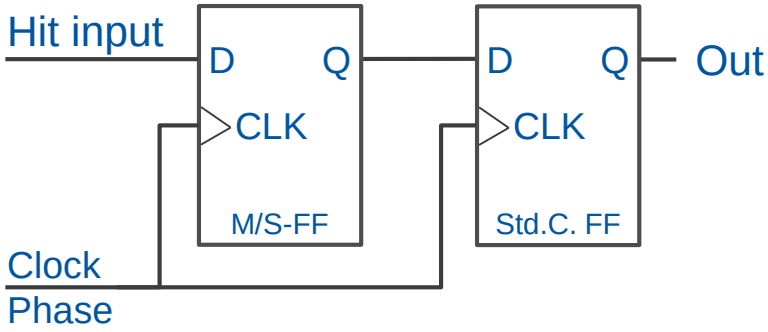


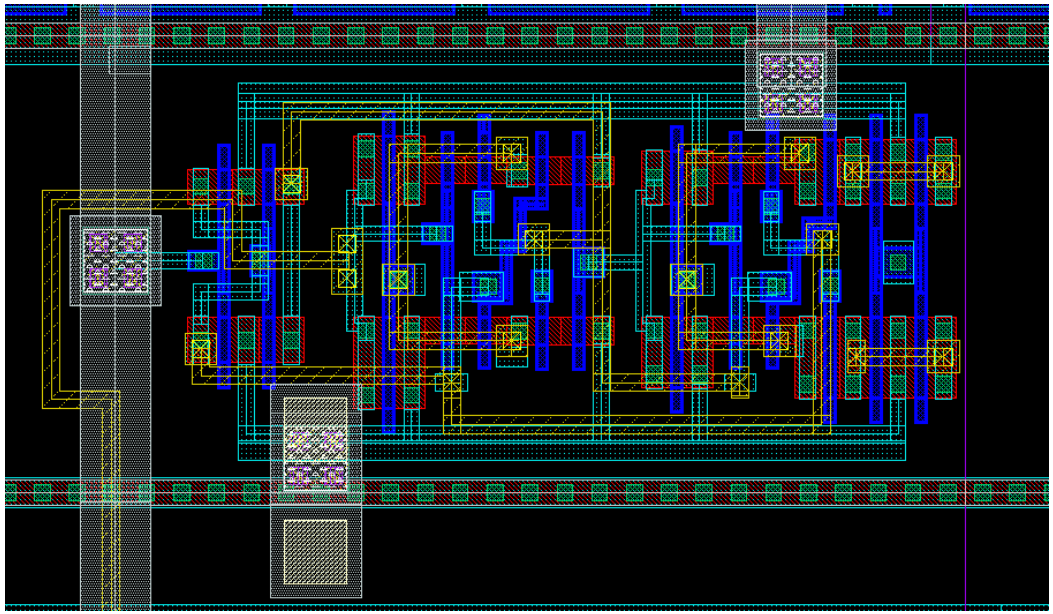


- **Resistive voltage divider**
  -> Signal slopes longer than delay, stabilized by DLL
- **RC delay** (capacitive loading)
  - > Small resistances, small loads
  - > Simulation based optimization of resistor values

Capture Flip Flops

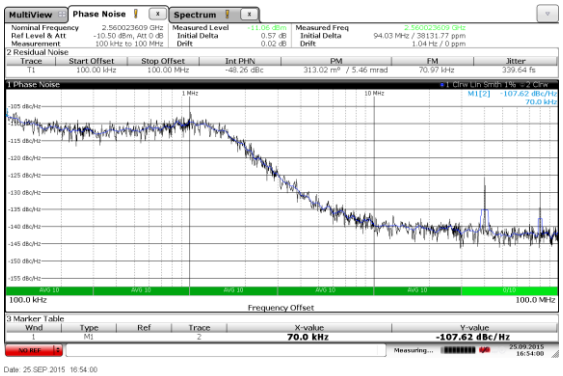
- Revisited design, timing vs. power very critical, 16k capture Flip Flops running @1.28GHz
- Optimized M/S Flip Flop followed by standard cell Flip Flop for metastability resolution
- Monte Carlo simulated mismatch of 800fs RMS, noise influence of 240fs RMS

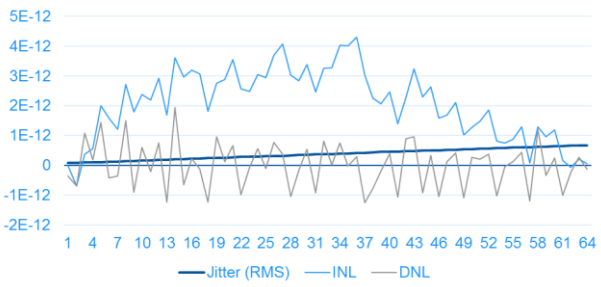


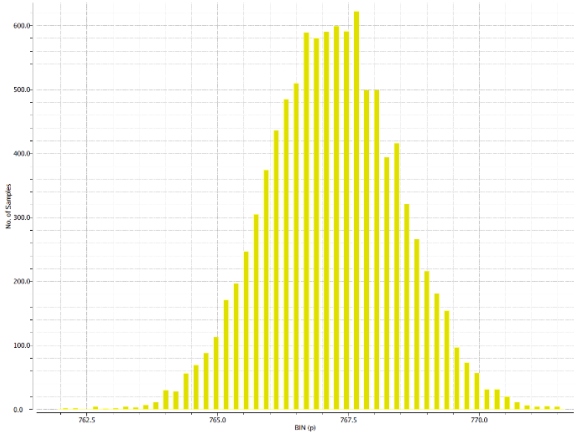


Sources of Measurement Deviation

- Bin size 3ps -> 880fs RMS
- PLL: 350fs RMS phase Jitter
- DLL: 400fs RMS phase Jitter, INL/DNL can be adjusted
- Clock Distribution: <500fs jitter
- Capture FFs: <1ps mismatch (DNL)
- Hit receivers: <1ps jitter
- ➢ ~1.75ps RMS total deviation
- External sources: Clock jitter, hit signal pre-processing

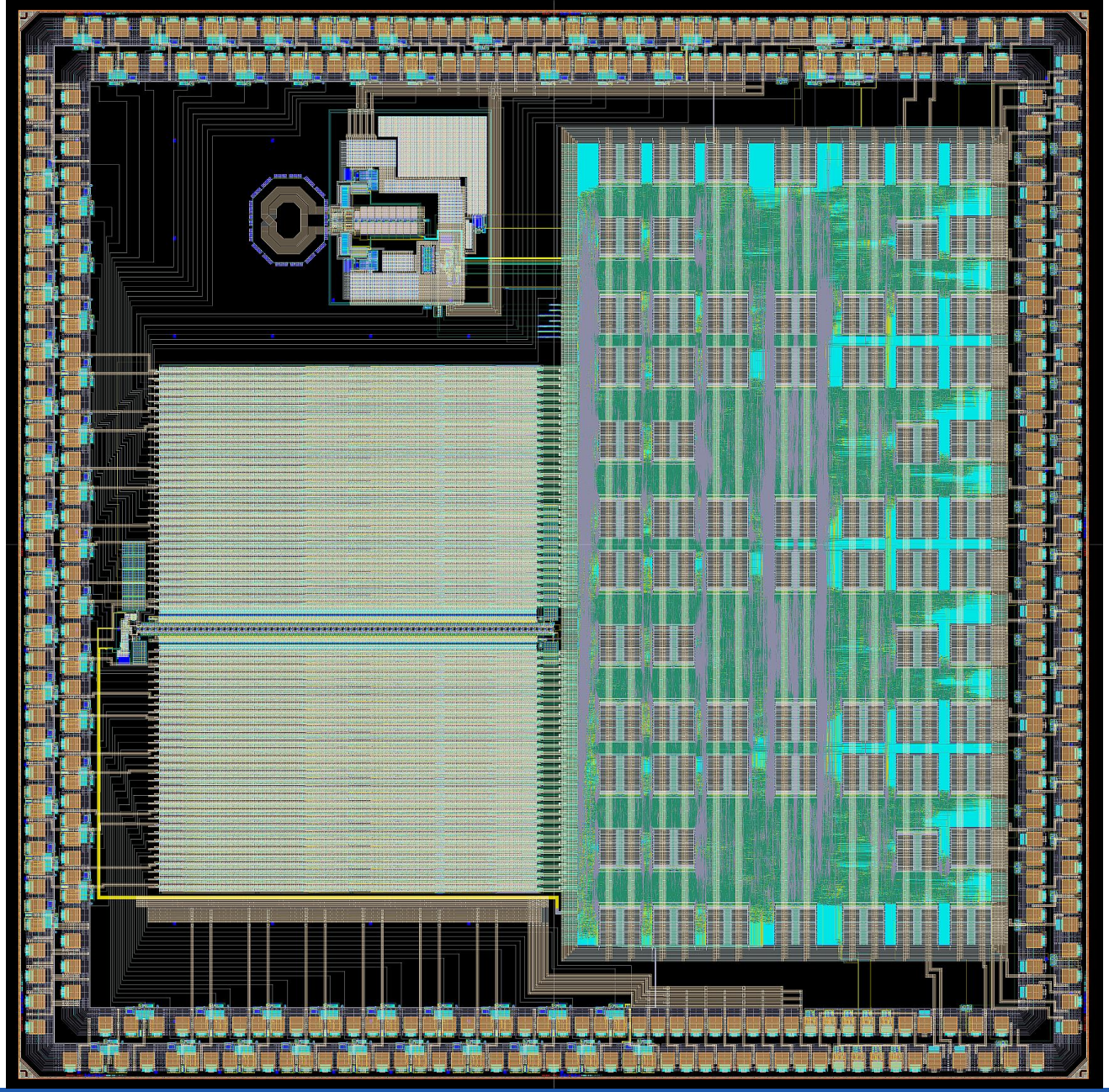




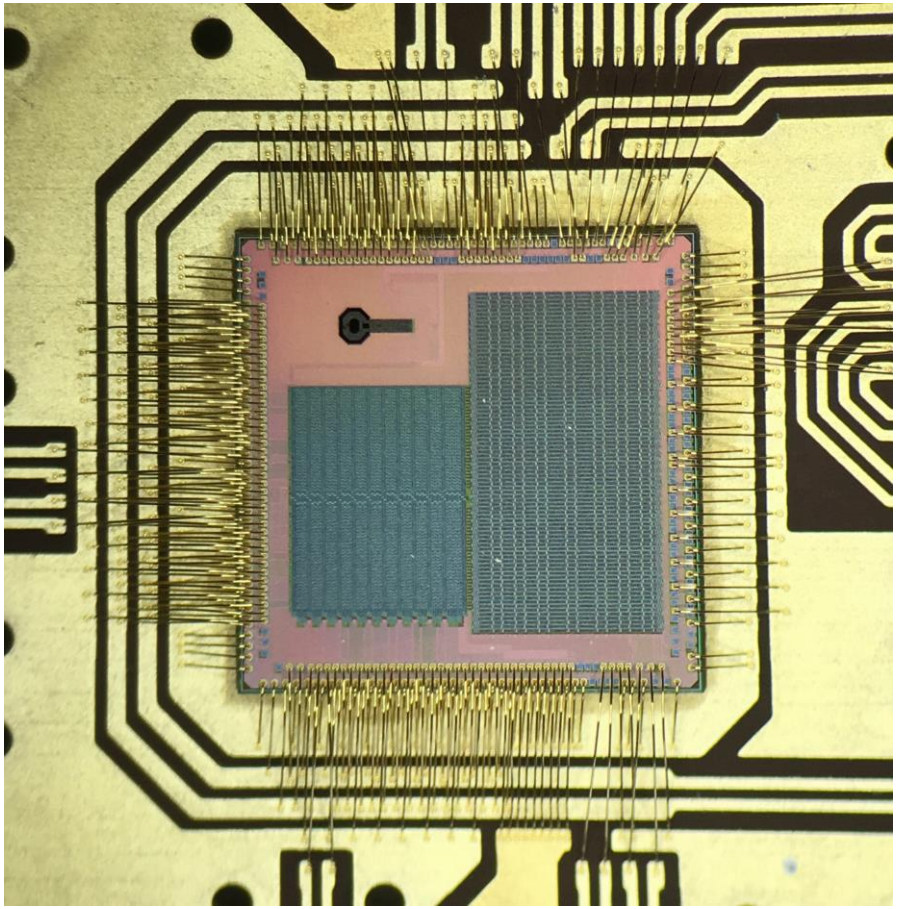


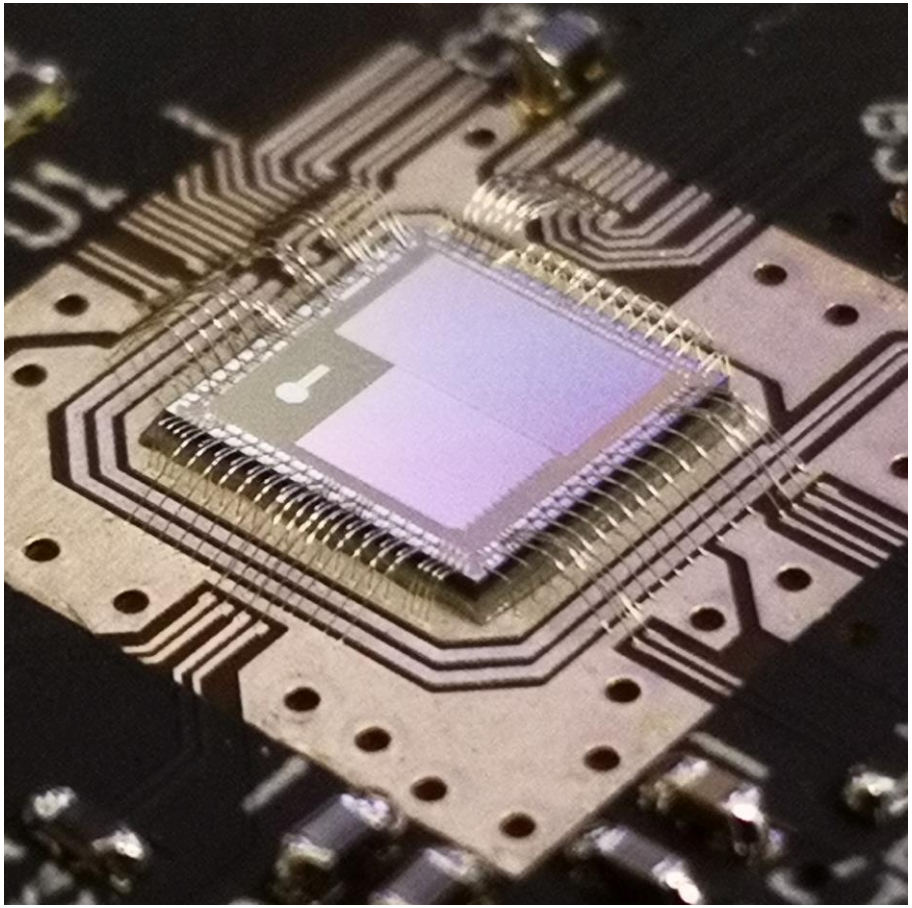
Hit constraints

- One edge per 1.28GHz-Cycle (~0.8ns)
- Internal glitch filter after hit receiver
  - Filter time can be programmed to ensure 0.8ns
  - Or up to 10ns for filtering e.g. oscillations
- Small derandomizer (4 hits) for each channel running @1.28GHz
- Sustainable rate to channel buffer 320MHz, trigger matching running @320MHz for each channel separate

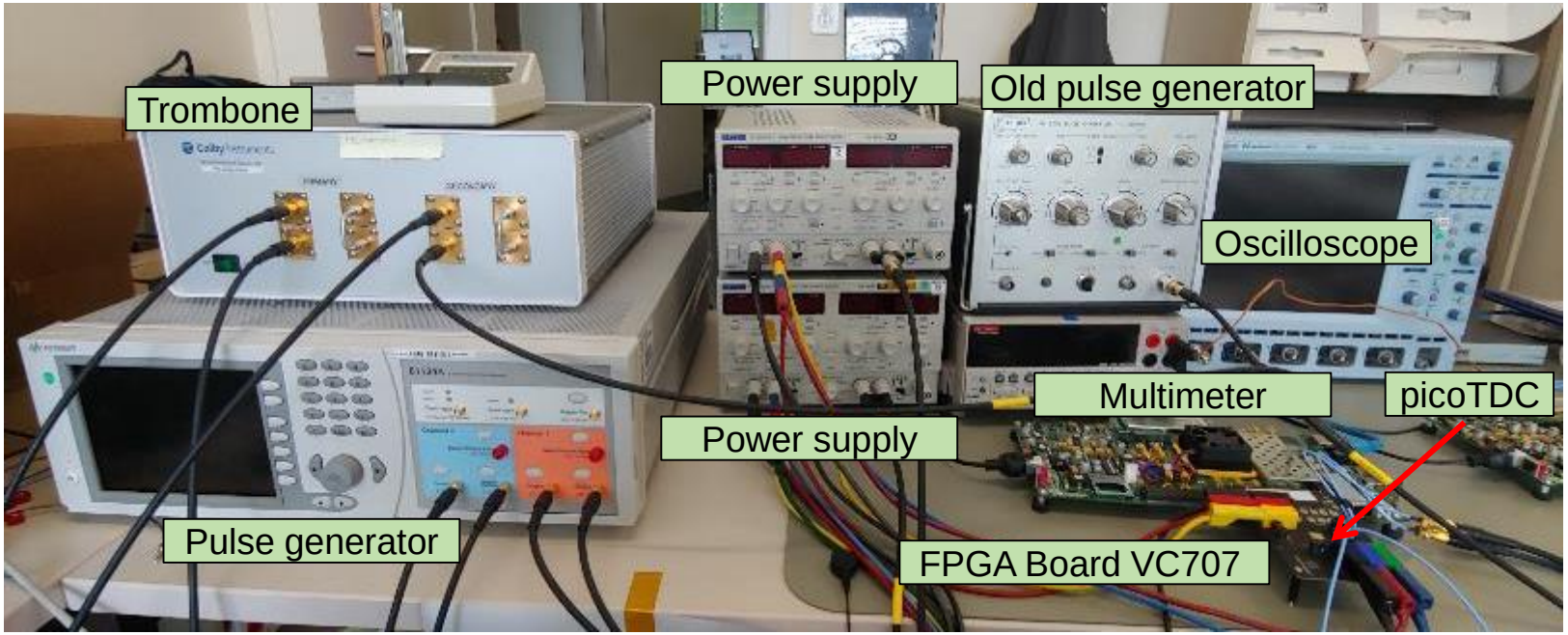


picoTDC on Test Cards





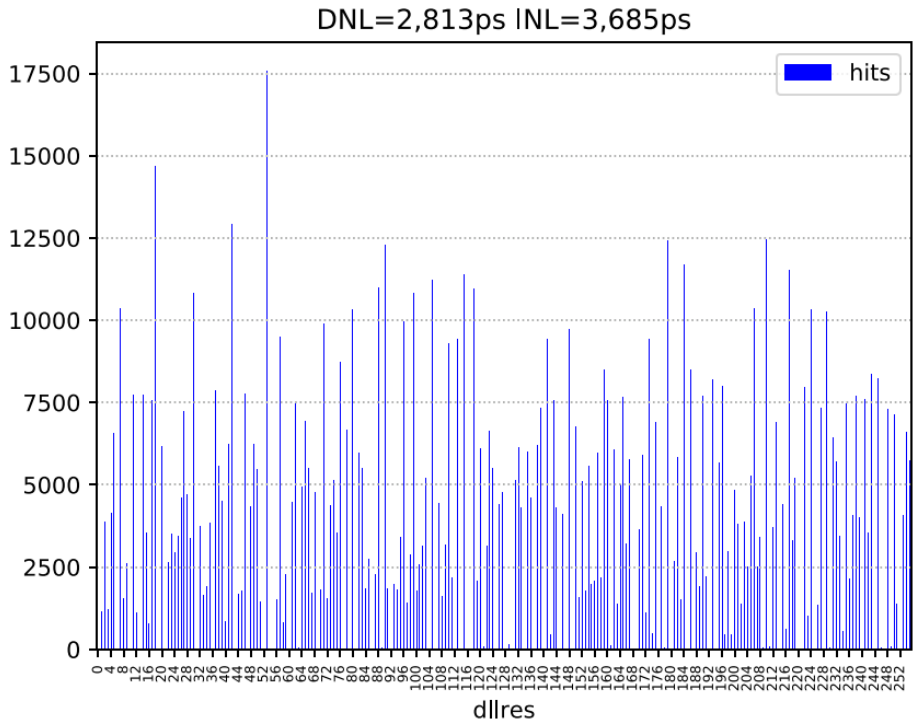
Instrumentation for Testing



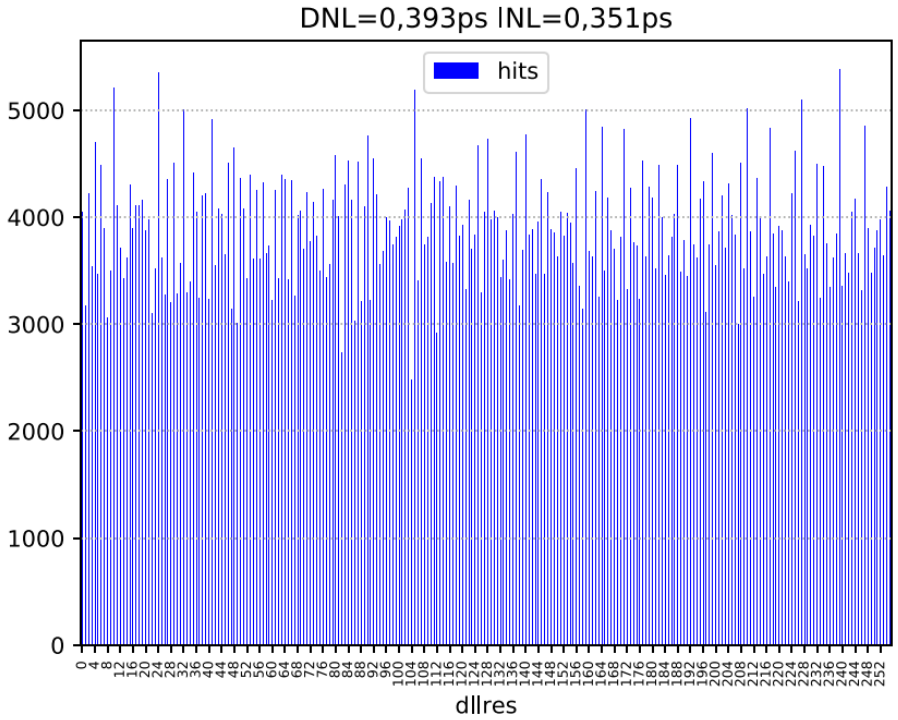
Additional tests with Silicon Labs Si5341 evaluation board for very low jitter measurements

3ps Bin Code Density Test

Not adjusted



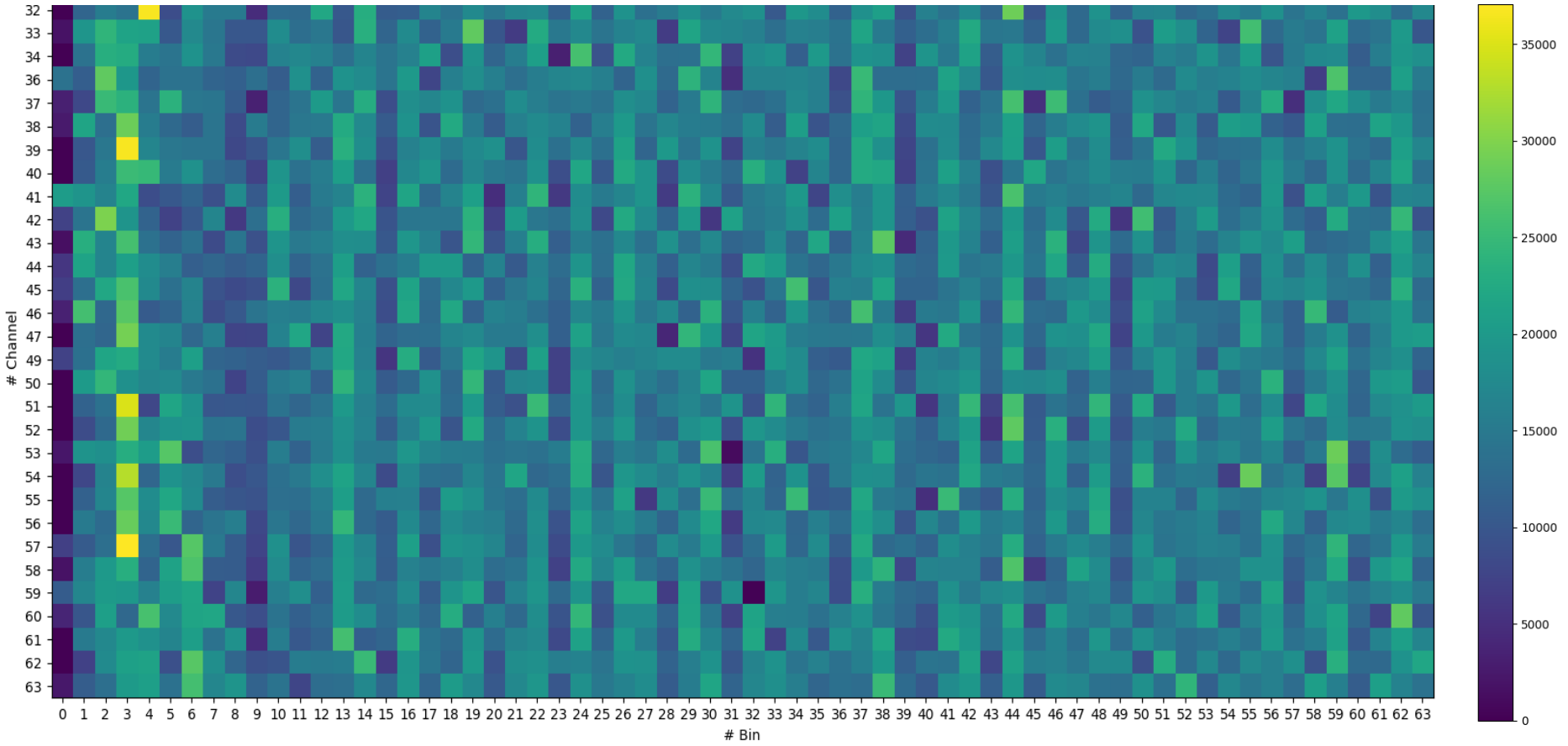
Adjusted



Code Density Test (CDT): Generate random hits uncorrelated to the reference.
-> Number of hits in each bin is equivalent to the bin size.
Adjustment is for single channel only

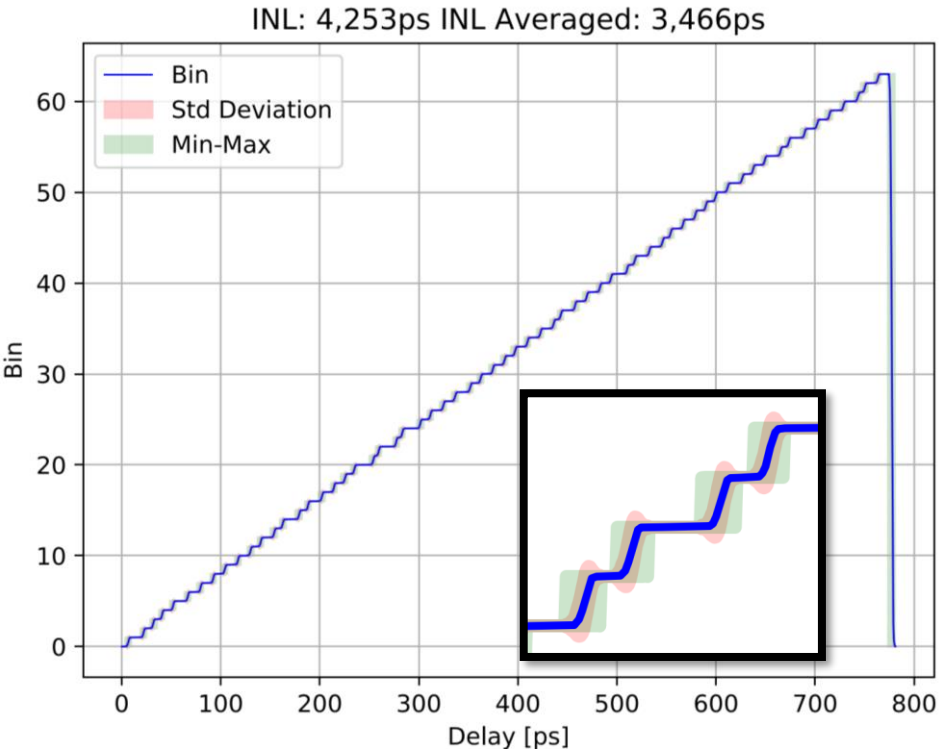
Code Density Test on Multiple Channels

Coarse time, not adjusted, channels 32-64, DNL 3.48ps, Common DNL 1.25ps

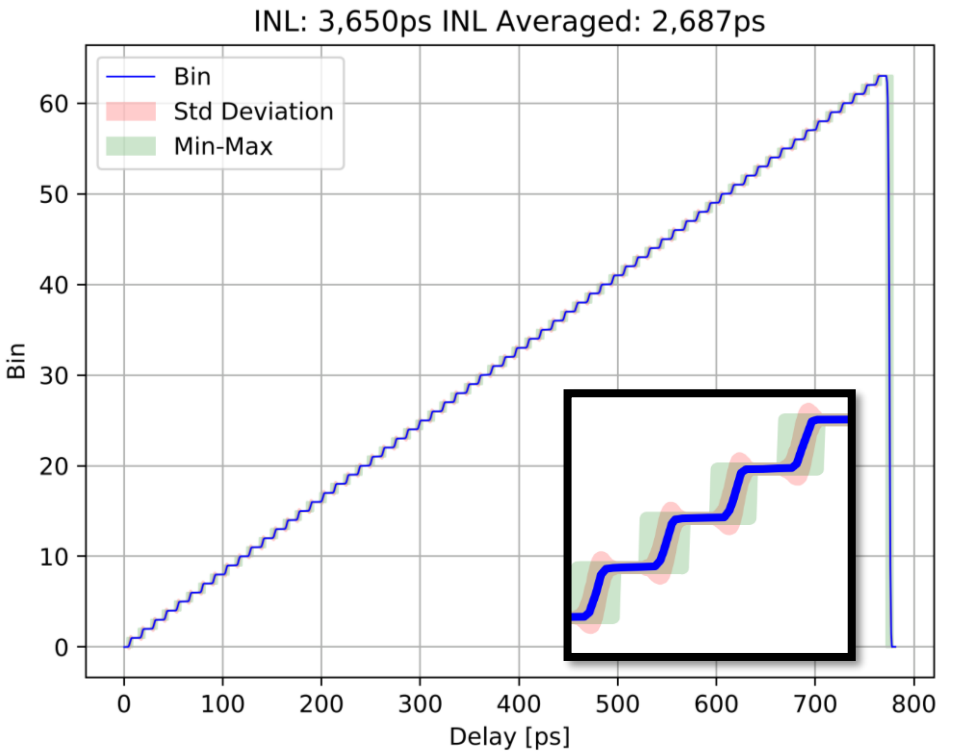


Time Sweep Measurements

Coarse mode, 12ps bin size



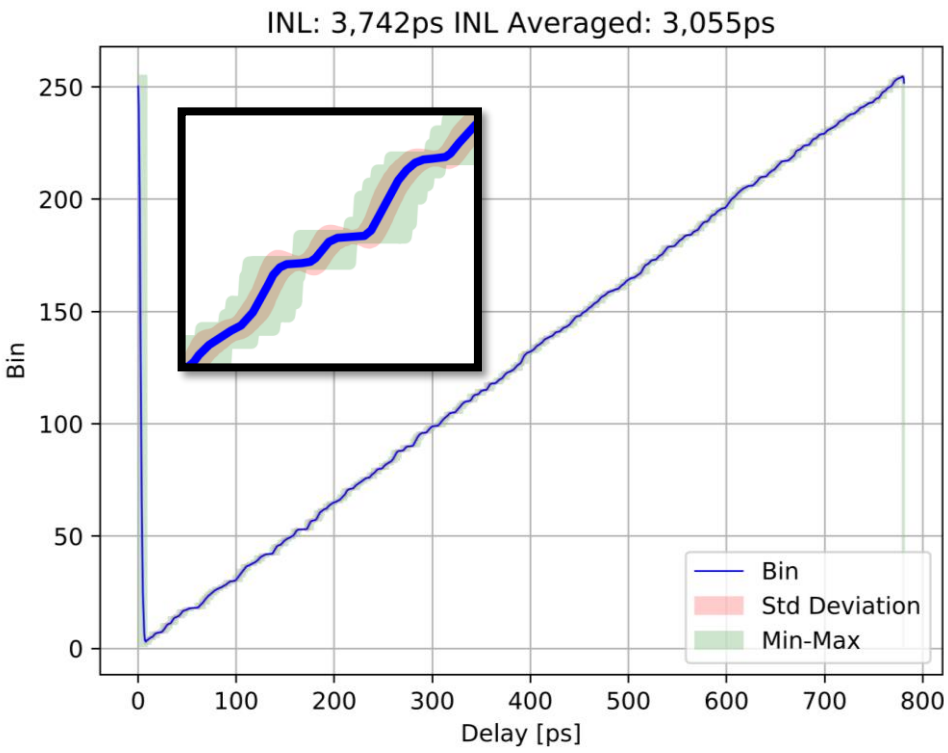
Not adjusted



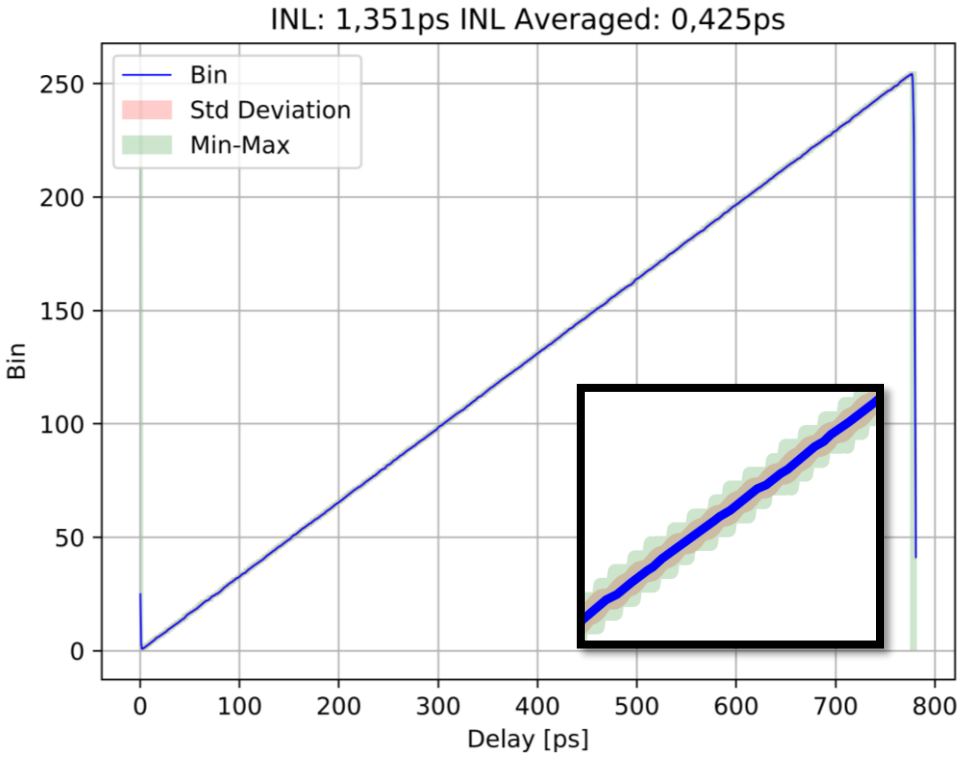
Adjusted

Time Sweep Measurements

Fine mode, 3ps bin size



Not adjusted



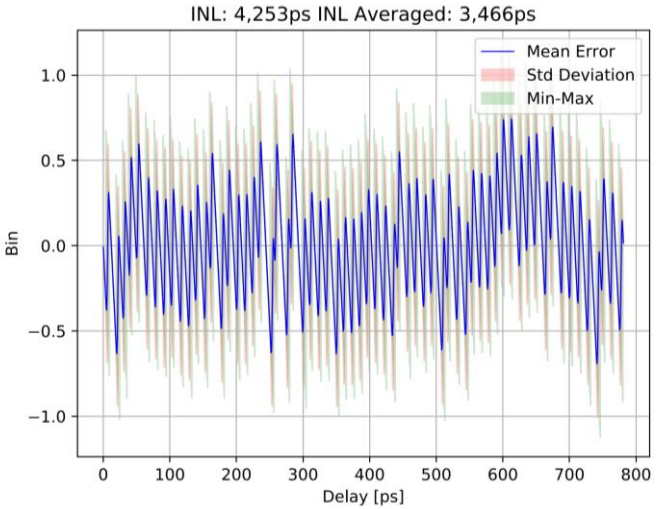
Adjusted

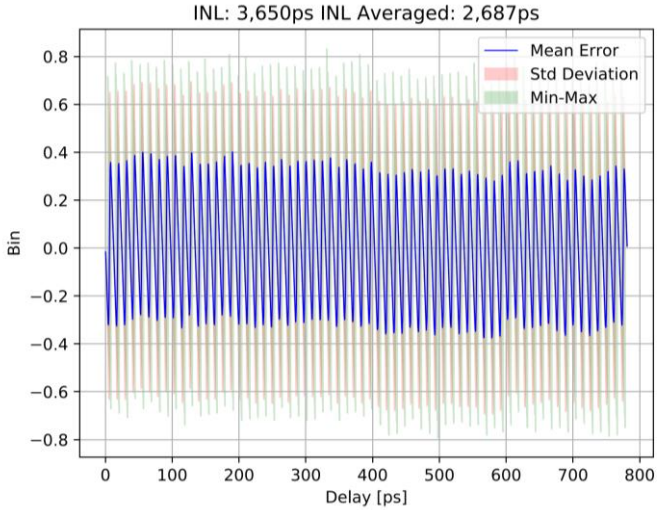
Sweep Measurements Deviation

Not adjusted

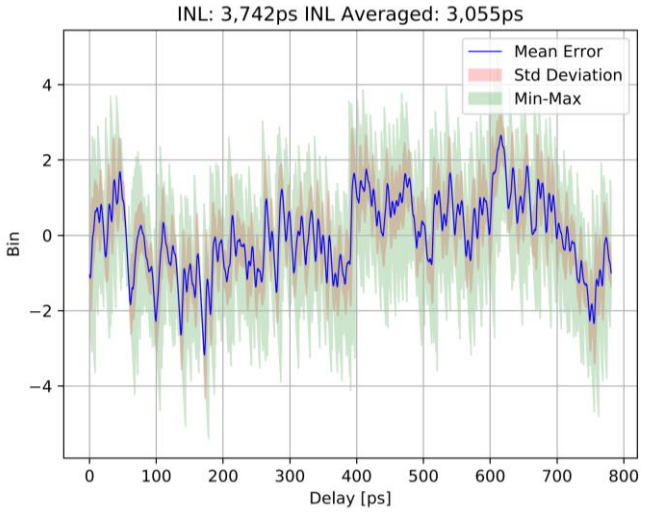
Adjusted

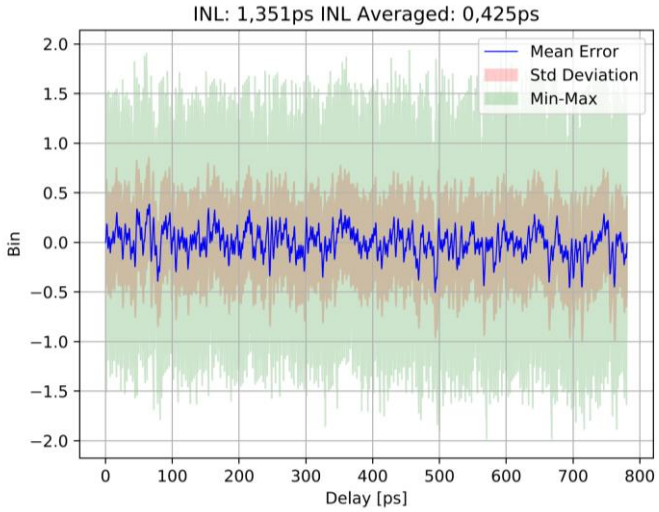
Coarse Mode
12ps Bins





Fine Mode
3ps Bins





Performance Summary

		Code Density Test		Sweep Test	
	Adjusted	DNL	INL	INL(single)	INL avg.
Coarse time 12ps binning	✗	2.75ps	2.12ps	**4.25ps**	3.47ps
	✓	0.36ps	0.45ps	3.66ps	2.69ps
Fine time 3ps binning	✗	2.15ps	3.13ps	**2.90ps**	2.06ps
	✓	0.34ps	0.79ps	**1.35ps**	**0.80ps**

CDT excludes jitter, quantization. Some variation between channels

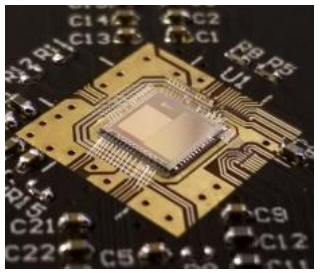
Temperature performance	Variation limited to 1 LSB pp	28 ºC to 42 ºC	<1ps/ºC
Voltage performance	Variation limited to 7 LSB pp	1.10V to 1.30V	<0.5ps/mV
Crosstalk test	Influence limited to 2 LSB Worst case one channel vs. all		

General Features

- 64 (32) channels
- Configurable time digitization:
  - 12ps binning: 4.25ps RMS
  - 3ps binning: 2.90ps RMS (1.35ps adjusted for specific channel, multi shot: 0.80ps)
  - (Optional of time bin adjust per 32 channels to get best possible time resolution on few channels)
- A: Single edge (leading and/or trailing): 32 bit word
- B: Leading edge + pulse width: 32 bit word
  - Programmable dynamic range, resolution
- Digitizer:
  - 1.28GHz digitizer
  - 4 hit buffer
  - 320MHz buffering, triggering and readout
- Un-triggered:
  - Effective sustained hit rate limited by readout. Significant buffering to copy with hit bursts
- Triggered:
  - Configurable latency and window,
  - Overlapping events.
  - Event based readout.
  - (TDC channel 0 can also be used to generate trigger)
- Time counter:
  - Naturally overflowing counter used for calculating trigger matches, TOT etc.
  - (Event header BX-ID Counter with arbitrary overflow and reset for machine cycle, when triggered)
- 1 or 4 readout ports: Byte wise at 320MHz
- I^2C configuration interface
- Configurable pulse generator

Status and more info

- PicoTDC Status:
  - Tested and characterized
  - Wafers produced
  - Few chips packaged in generic packed to test for possible packaging effects (and some design fixes and additions)
  - Huge delay (12+ months) encountered in getting production chips in final package: Packaging company going bust + ASIC crisis affecting seriously final packaging company
  - Availability: After the summer in final package
- Test/evaluation/starter system:
  - FPGA evaluation board, PicoTDC card, FMC to SMA fanout
    - Become available (again) for production version end of year.
  - FPGA firmware, Python based software
  - Will be used for production testing
- More Info on share point: http://cern.ch/PicoTDC (access: needs to be on PicoTDC@cern.ch)



Chip

Generic package

Production package: To come


CERN

Backup Slides

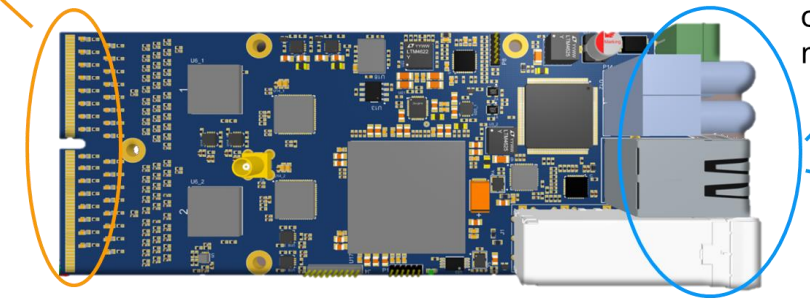
Possible CAEN Modules With picoTDC

The idea of FERS platform

Single card housing Front End ASICs, ADC and/or TDC, FPGA, I/Os, interfaces and, in some cases, detector power supply

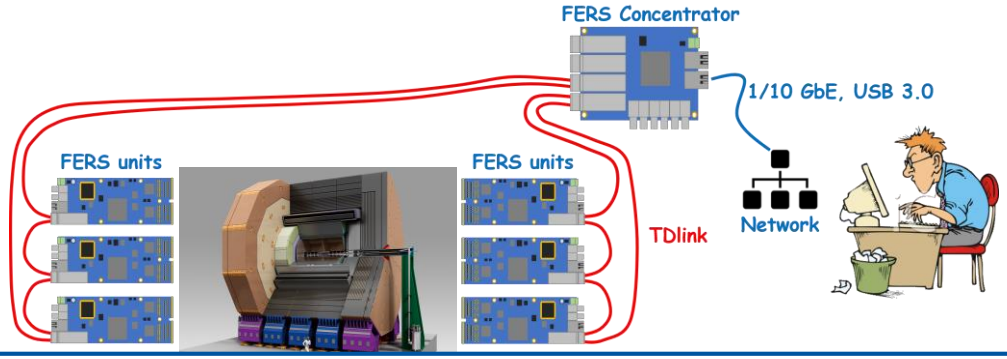
Size of ~15 x 6 cm (for the A5202)

Signals from the detectors come through 0.8 mm edge contacts mating a Samtec **HSEC8-170-01** connector



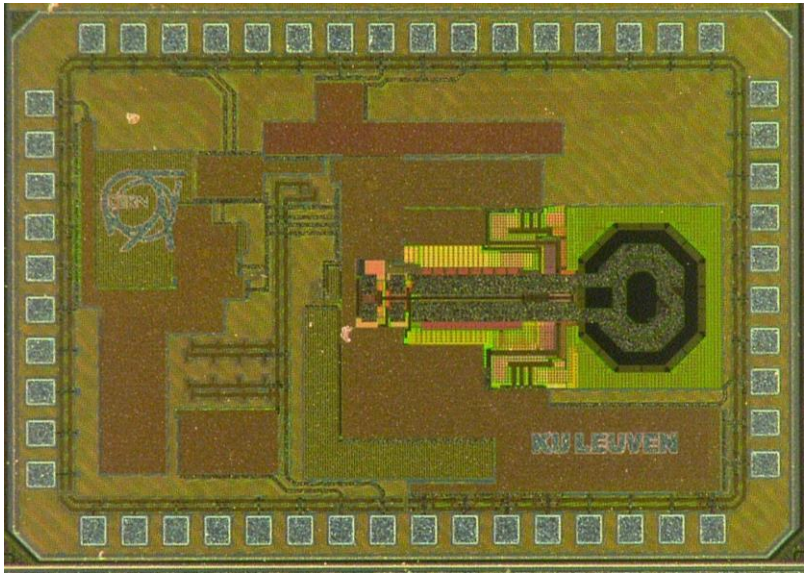
communication interfaces: **TDlink** (sync + commands + data) or **Ethernet**, USB 2.0 (data only, mainly used for evaluation)

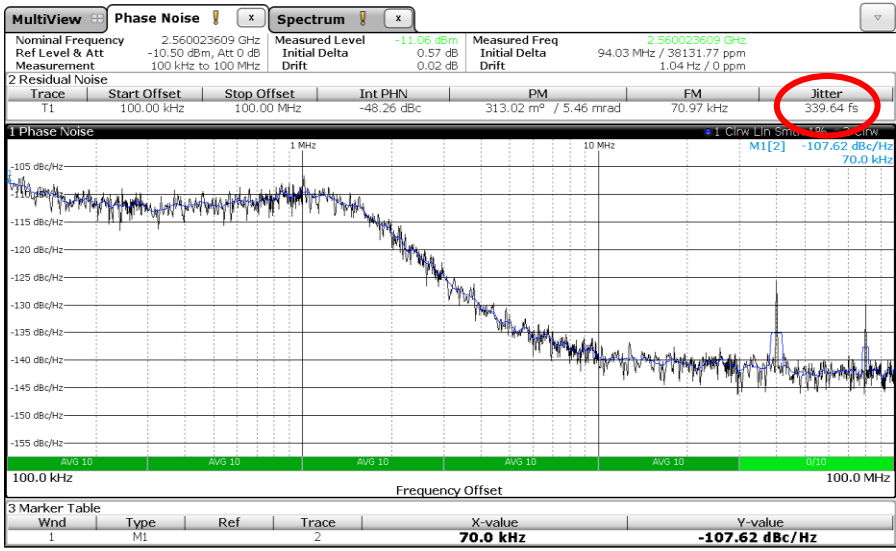
Auxiliary **I/Os** for sub-ns timing and low latency trigger distribution (alternative to TDlink)



Low Jitter PLL

- Clock multiplication from 40MHz to 1.28 (2.56) GHz
  - Low jitter critical
  - Jitter filtering of 40MHz clock to the extent possible
    - 40MHz reference MUST be very clean
  - LC based oscillator
- Prototyped & Tested
- Measurements very promising (340fs RMS jitter)
- Designed by Jeffrey Prinzie, KU Leuven
- Talk at TWEPP 2015:
  A low jitter PLL frequency synthesizer for high resolution TDCs in 65nm CMOS technology

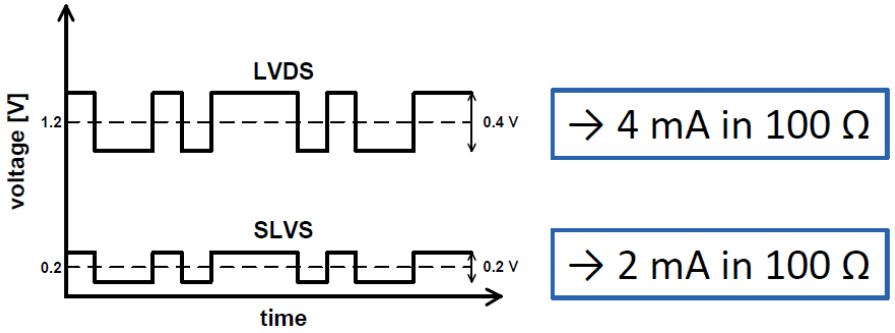




Phase Noise vs. Freq. Offset

Electrical Interfaces

- Hits: Differential (LVDS “compatible”, common mode from 0.2V to 1.2V)
  - Highest speed (resolution) @ ~800mV common mode
- Time reference: 40MHz differential
  - Low jitter reference critical for high time resolution
- Trigger/Event-Rst/BX-Rst/Reset: Sync Yes/No
- Control/monitoring: I^2C at CMOS 1.2V-levels
- Readout: 4 readout ports of 8 differential signals
  - Common mode 0.6V, programmable current 1-5mA
  - Compatible with LpGBT and FPGAs
- Packaging: 400 BGA (1mm pitch)



Config / Control / Status Interface

- I^2C Interface, up to 1MBit/s
- 1.2V CMOS Levels
- 348 Bytes configuration / control
  - Additional 322 bytes delay adjust
- 300 Bytes status

Readout

- 1 or 4 differential readout ports with 8 bits
  - 40 - 320MHz
  - Bandwidth:
    - Min 320Mbits/s (~0.15 Mhits/s per channel)
    - Max 10Gbits/s (~4 Mhits/s per channel)
- Readout data: 32 bit words
  - TDC data, headers, trailers etc.

Power Consumption

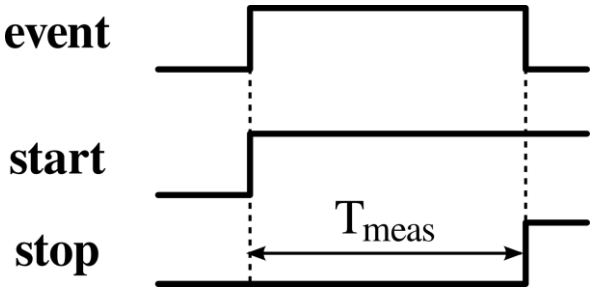
Dependent on hit rate, values based on 1 MHz per channel

- High resolution, 64 channels: 1300mW
- High resolution, 32 channels: 900mW
- Low Resolution, 64 channels: 850mW
- Low Resolution, 32 channels: 550mW

Measurement Scheme

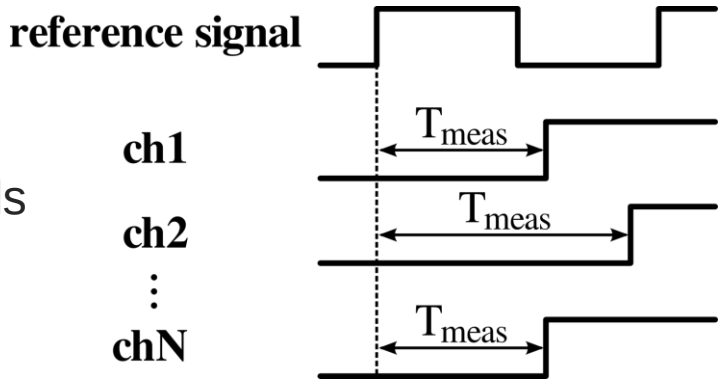
Start - Stop Measurement

- Measure relative time interval between two local events
- Small local systems and low power applications

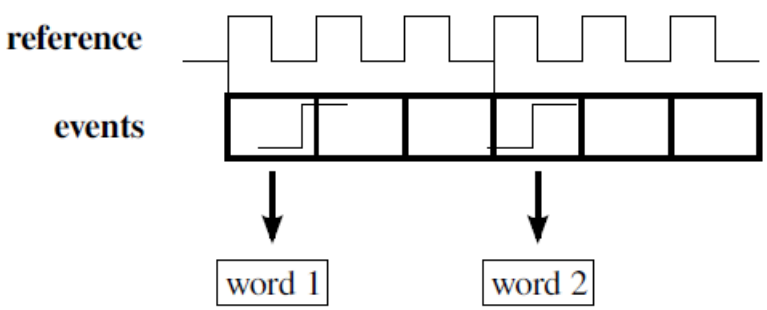


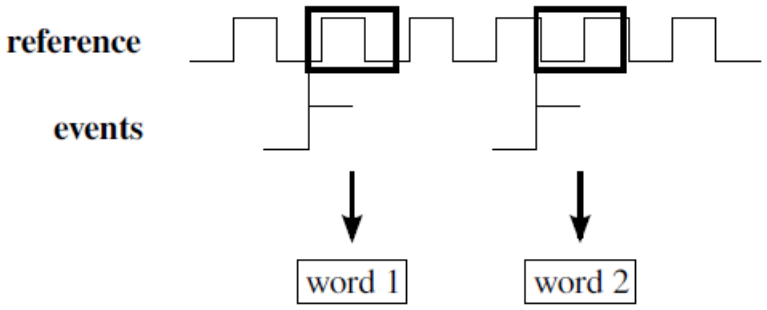
Time Tagging

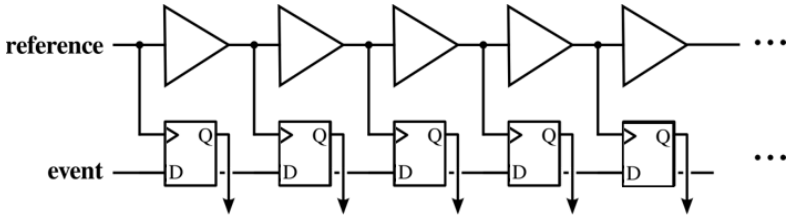
- Measure “absolute” time of an event (Relative to a time reference: clock)
- For large scale systems with many channels all synchronized to the same reference

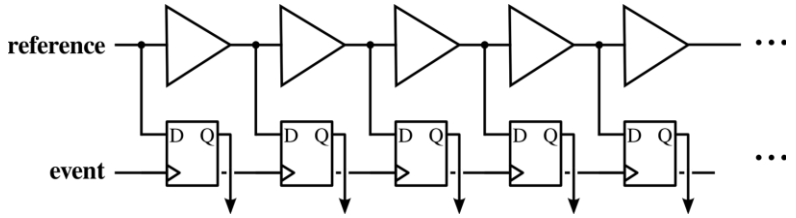


Capture Scheme





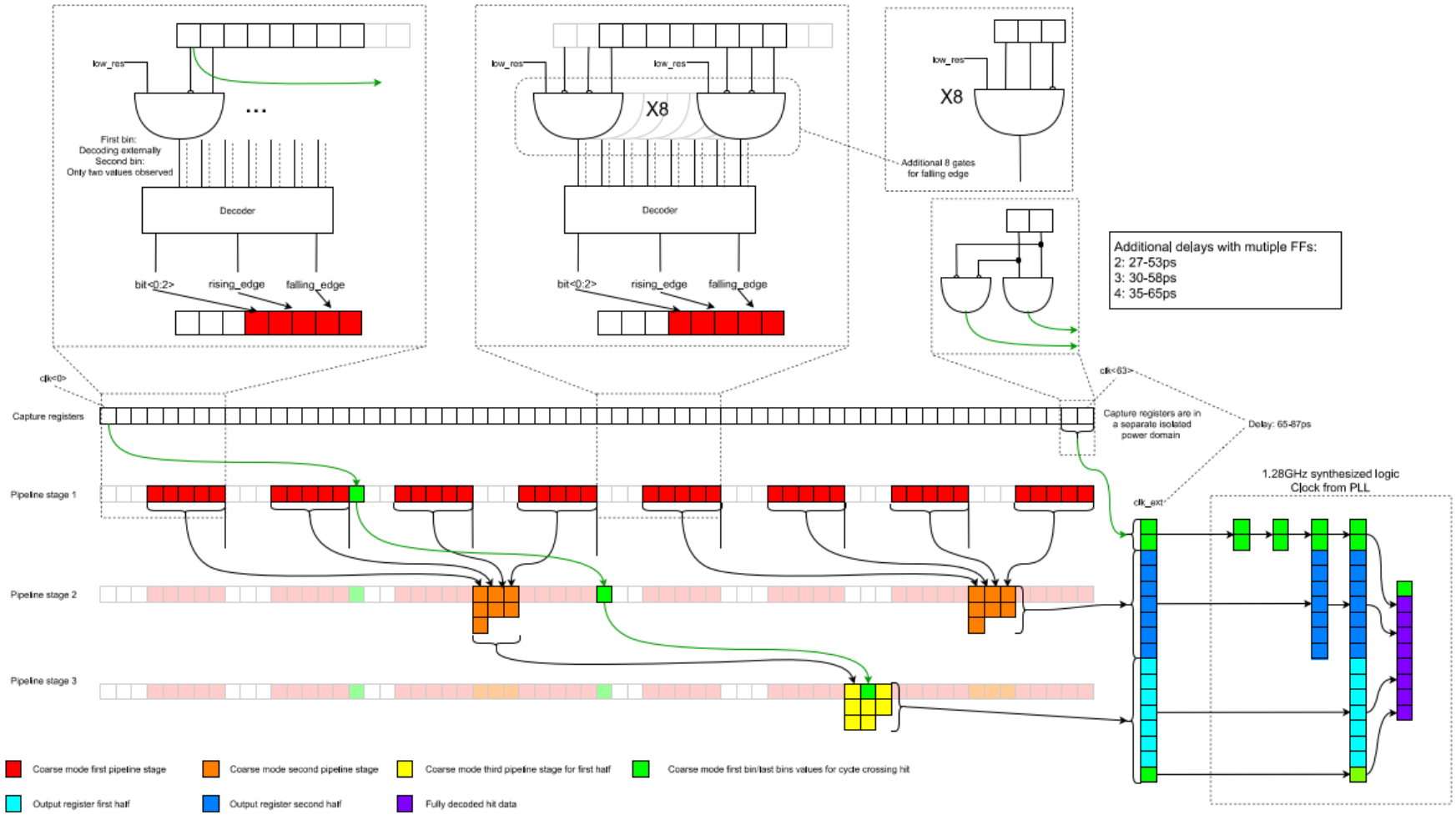




Synchronous

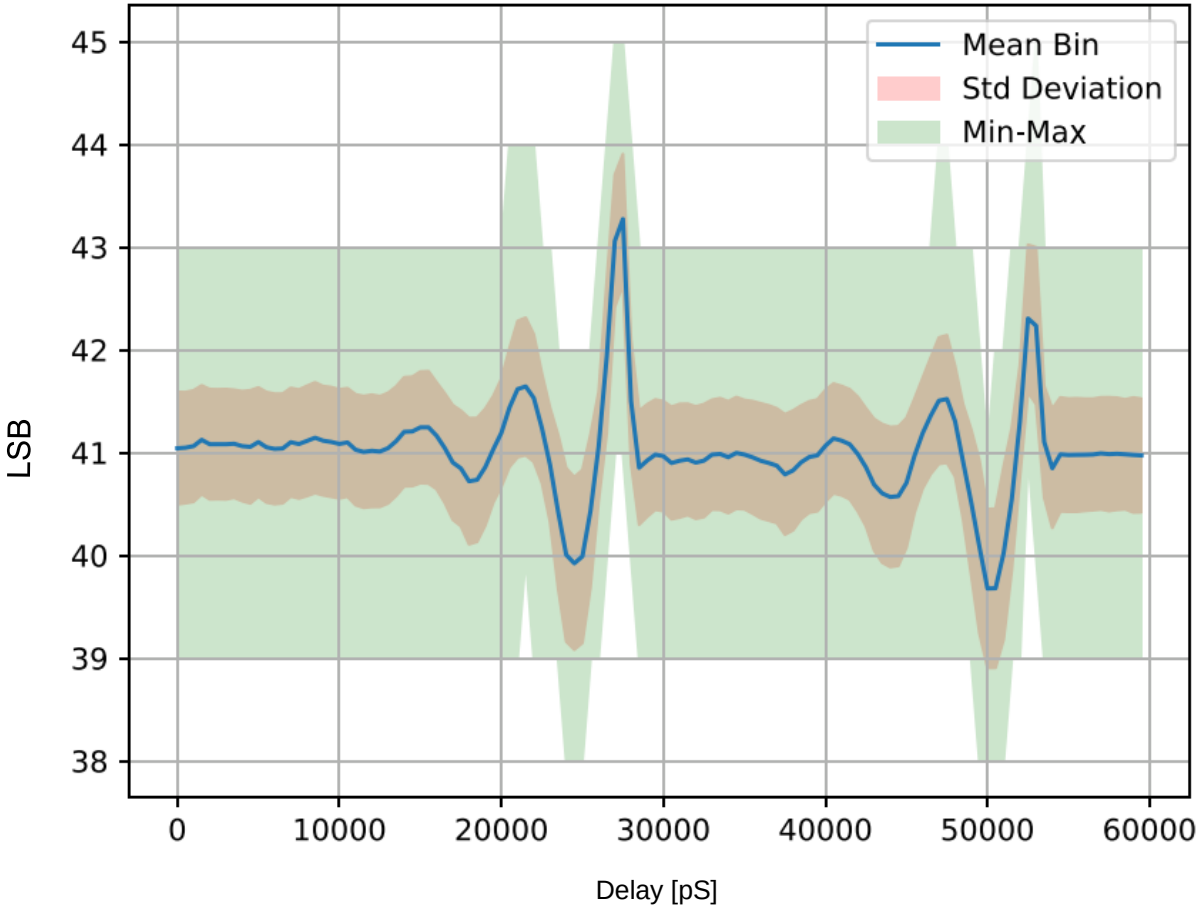
Asynchronous

Coarse Decoding in Timing Macro



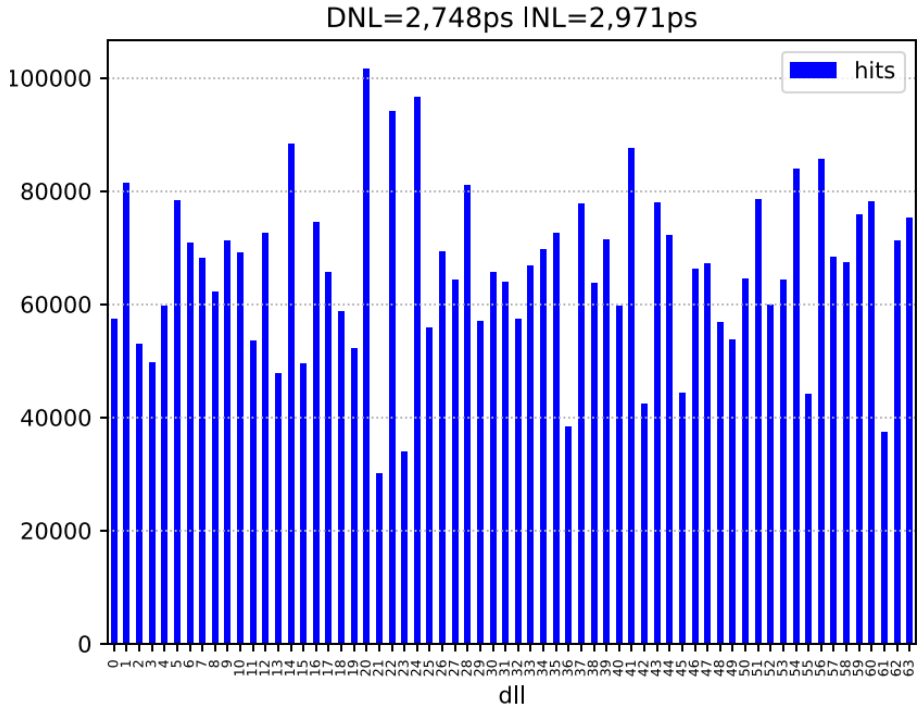
Crosstalk Test

Channel 31 vs. all channels, coarse mode, LSB 12ps

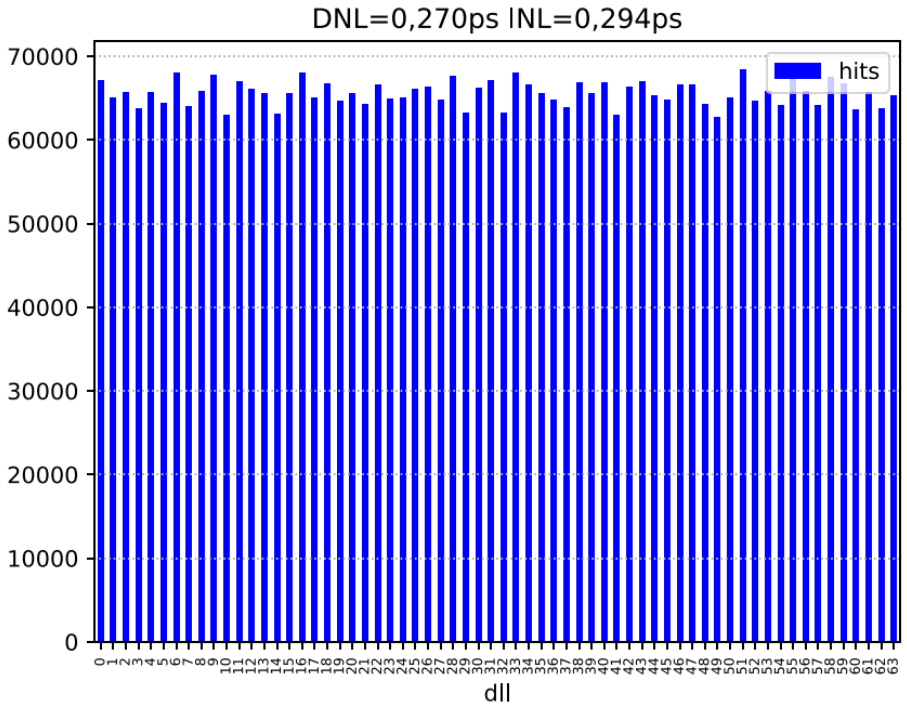


12ps Bin Code Density Test

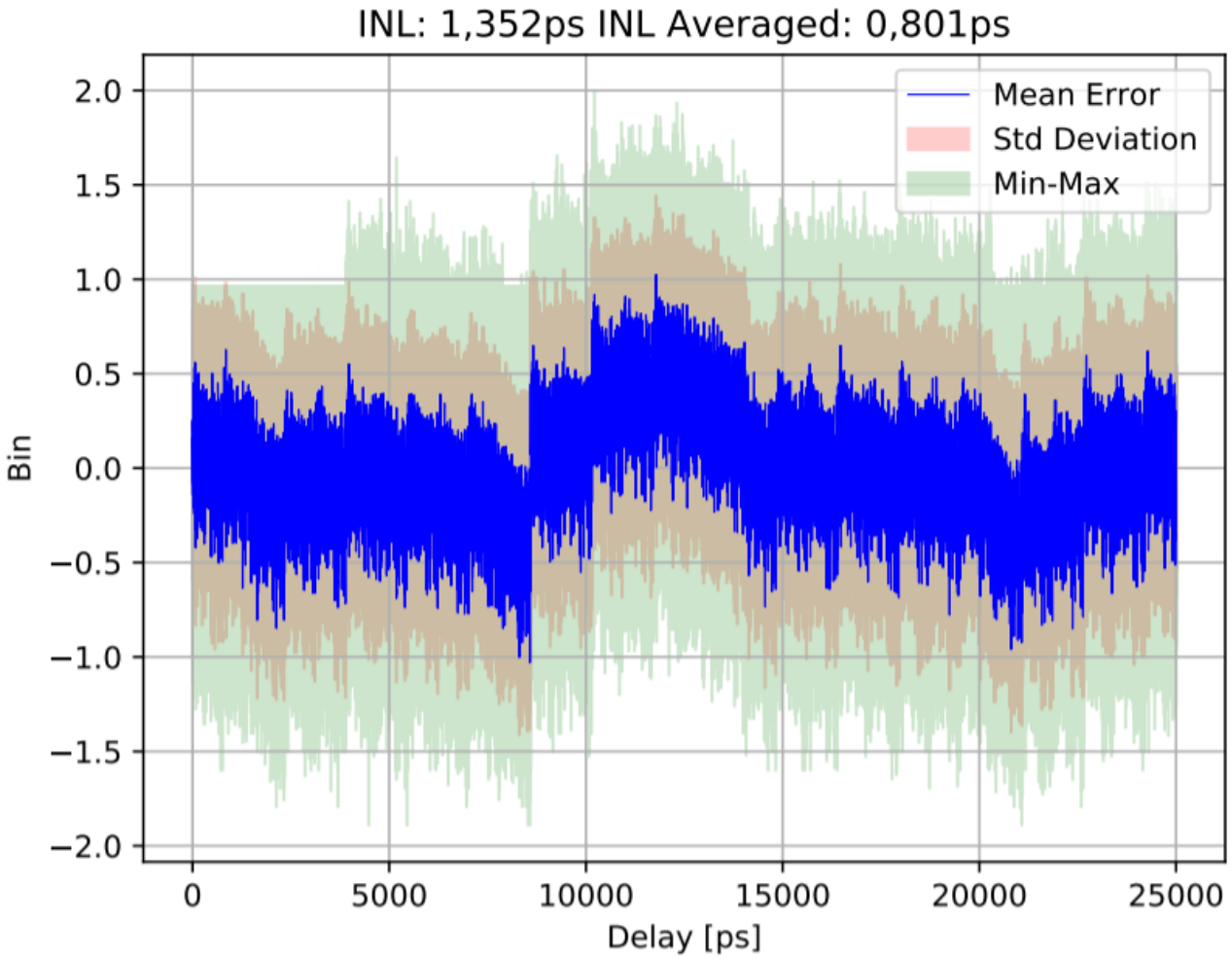
Not adjusted



Adjusted



25ns Sweep Deviation



Readout

- 1 or 4 differential readout ports with 8 bits
  - 40 - 320MHz
  - Bandwidth:
    - Min 320Mbits/s (~0.15 Mhits/s per channel)
    - Max 10Gbits/s (~4 Mhits/s per channel)
- Readout data: 32 bit words
  - TDC data, headers, trailers etc.

32 Bit Frames

TDC measurement

Event headers (up to two)

Possible fields: Event ID, Bx ID, Natural ID

Event trailers

Channel group separator (for single readout port)

Idle frame

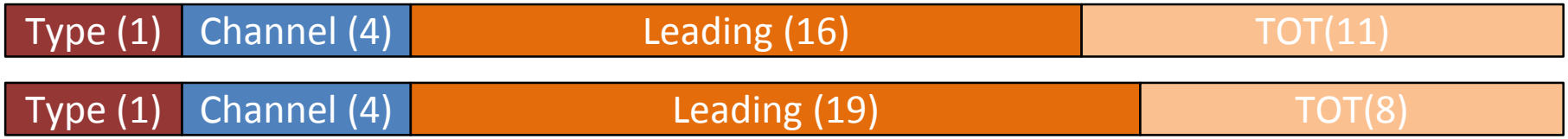
Absolute TDC data

FULL TDC data, **DEFAULT FORMAT**

Relative to Trigger

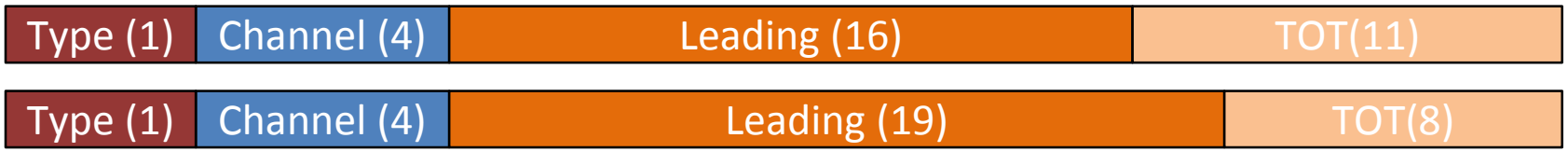
Triggered with relative time: Same as absolute

B: Triggered with relative leading and TOT: Same as absolute Lead. + TOT



Leading + TOT

- Packet Type: 1bit
- Channel ID: 4 bits, for single port readout +2 bit group separator
- Leading: 16/19 bits
  - Large dynamic range
    - 16bit 3ps resolution: 200ns
    - 19bit 3ps resolution: 1600ns
  - **Programmable part of full 25bits leading TDC**
  - (**Relative to trigger to be useable**)
- TOT (Relative to leading): 11/8 bits
  - Short dynamic range:
    - 8bit 3ps resolution: 780ps
    - 11bit 3ps resolution: 6.1ns
  - **Programmable part of full 25bits TOT difference**
    - TOT assumed to be used for offline time-walk correction of leading.
- Alternative: Readout of Individual Leading and Trailing edges with full range/resolution
  - 2x readout bandwidth



Estimated Power Consumption

Highly dependent on hit rate, values based on 1 MHz per channel

- High resolution, 64 channels: 1300mW
- High resolution, 32 channels: 900mW
- Low Resolution, 64 channels: 850mW
- Low Resolution, 32 channels: 550mW