PADI

Mircea Ciobanu for the CBM - ToF group

Outline

- Introduction
- PADI – X
- PADI – XI
- PADI results

Introduction

The planned time-of-flight wall of the CBM experiment at the future FAIR facility requires a full-system time resolution (σ) better than 80 ps – with more than 100,000 channels and event rates of up to 300 kHz per channel. The planned detectors are Resistive-Plate Chambers (RPCs) with electrodes either as strips (read out at both ends) or in pad form.

RPCs deliver very fast pulses when an ionizing particle passes through them. Typical signal parameters of the 50 Ω narrow strip electrodes (2.54 mm pitch) are: rise time ~ 0.3 ns, FWHM ~ 1 - 2 ns, fall time ~ 0.3 ns.

We started the design of a customized ASIC (in UMC 180 nm technology) named PADI after testing and analyzing the first chip specialized in time measurements NINO [1], an 8-channel ASIC amplifier-discriminator chip, developed for the ALICE experiment at CERN. PADI was designed to be coupled with the GET-4 time-to-digital converter (TDC) [2], whose design began at the same time. The evolution of the PADI project from PADI-1 to PADI-8 is described in detail in [3], [4] and [5], with the presentation of the block diagram and the detailed schematic of important cells together with obtained performances both at cell and at whole ensemble level.

[1] F.Anghinolfi et al.," NINO: An Ultrafast Low-Power Front-End Amplifier Discriminator for the Time-of-Flight Detector in the ALICE Experiment", *IEEE Trans. on NS*, Volume 51, Issue 5, pp. 1974 – 1978, Oct. **2004**.

[2] H.Flemming and H.Deppe, "The GSI Event-Driven TDC with 4 Channels GET-4", *IEEE NSS – conference record*, pp. 295-298. Published: **2009**

[3] M.Ciobanu et al.,"PADI, a fast Preamplifier – Discriminator for Time-of-Flight Measurements", *IEEE NSS Conference 2008, IEEE NSS – conference record*, pp. 1293-1299, Published: **2009**.

[4] M.Ciobanu et al., "PADI-2,-3 and -4: The second iteration of the Fast Preamplifier – Discriminator for Time-of-Flight Measurements at CBM", *IEEE NSS Conference 2009 record*, pp: 1300-1303, Published: **2009.**

[5] M.Ciobanu et al., "PADI, an Ultrafast Preamplifier - Discriminator ASIC for Time-of-Flight Measurements", IEEE TNS, Vol.61, No. 2, pp.1015-1023, **2014.**

[6] M.Ciobanu et al., "New Models of PADI, an Ultrafast Preamplifier - Discriminator ASIC for Time-of-Flight Measurements", IEEE TNS, DOI: 10.1109/TNS.2021.3073487, 15 April **2021.**

PADI - X

The PADI-X model is identical with PADI-8 [5] but it is encapsulated in QFN-64 package.

The main parameters are:

- 8 channels per chip, preamplifier (PA)
- PA Bandwidth ~ 411 MHz
- PA voltage gain ~ 250
- PA conversion gain ~ 30 mV/fC
- PA noise ~ 5.5 mVrms
- Threshold dynamics ~ +/- 750 mV
- Input impedance 50 – 400 Ω
- Power consumption ~ 17 mW/channel
- Output LVDS compatible

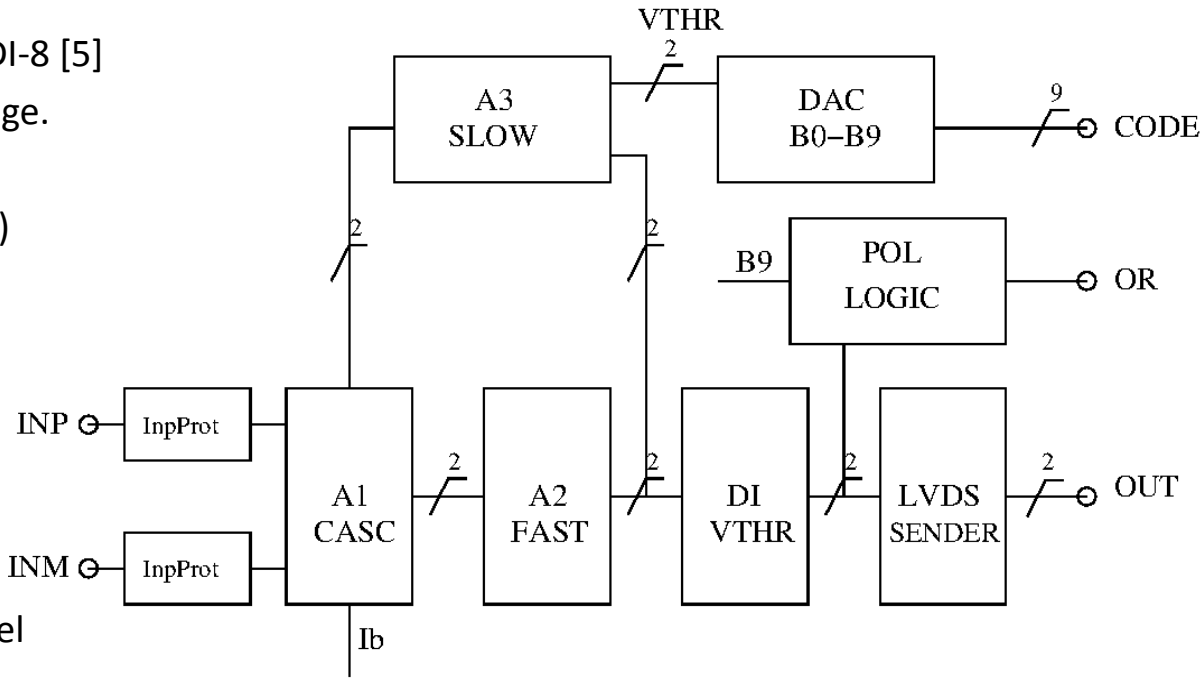


Fig. 1. Simplified block diagram of one PADI-X channel.

PADI – X simulation

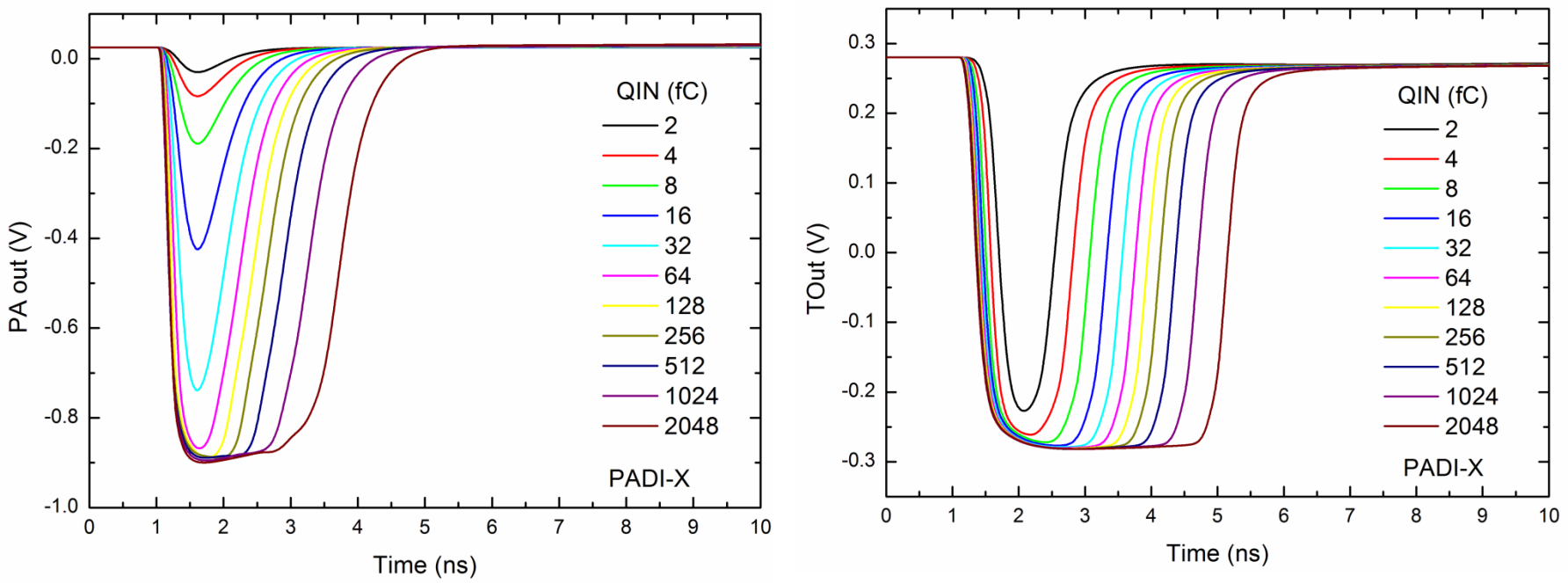


Fig. 3. The PA out and TOut response for input charge QIN swept from 2 fC to 2048 fC, threshold voltage VTHR = 25 mV.

PADI prototypes were used in the development of RPC detectors and very good results were obtained with detectors powered by two high voltage (+/- HV) sources. But economic considerations required the use of a single high voltage source to power the detectors, which led to the "folding" of the detectors. The final detectors have strips with characteristic impedance of around 25 Ohms. To adapt this impedance to the input impedance of the PADI, the FEE had to be placed close to the end of the detection strip, inside the metal box of the detector.

PADI - XI

PADI-XI had to fulfill two new objectives: halving the minimum input impedance (~ 50 Ω differential, for impedance match with the new RPC detectors) and introducing a stretcher to extend the width of the discriminated pulse, to increase the maximum cable length to the TDCs and allow the use of old TDCs.

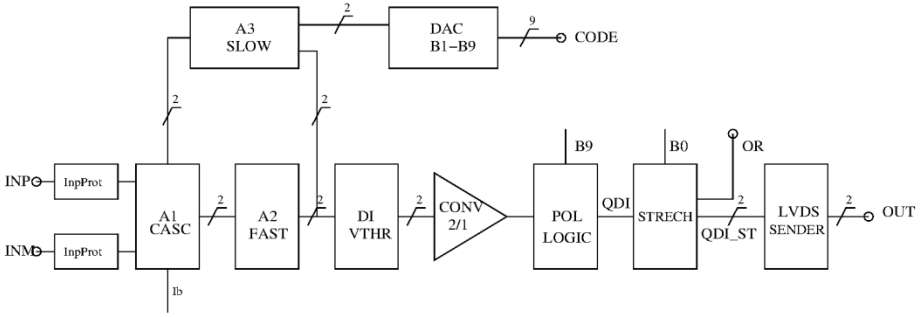
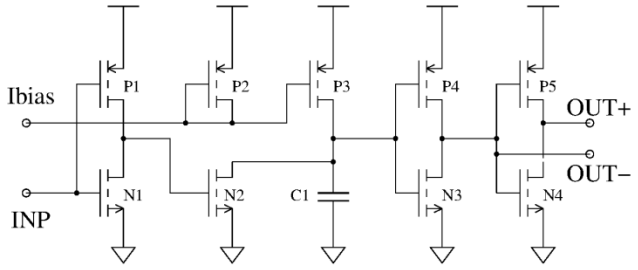


Fig. 3, Simplified block diagram of one PADI-XI channel.



	W (um)	L (um)	fin./val.	II No.
P1,4,5	2.88	0.18	2	1
P2	2.88	0.18	1	10
P3	2.88	0.18	1	1
N1,3,4	1.44	0.18	1	1
N2	1.44	0.18	3	1
C1	4.5	4.5	21.6 fF	1

Fig. 4, The diagram of STRECH cell.

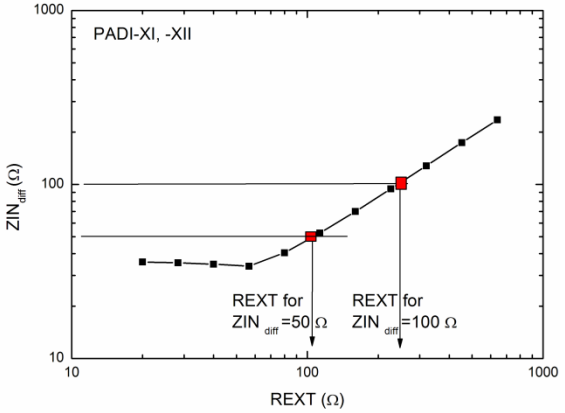


Fig. 5, The input differential impedance versus REXT.

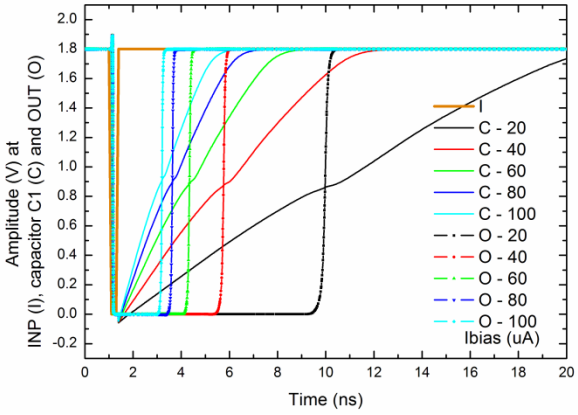
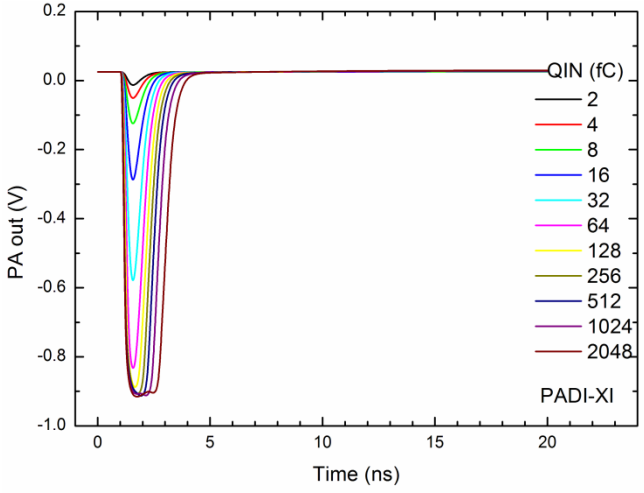


Fig. 6, STRECH cell: simulation.

PADI - XI



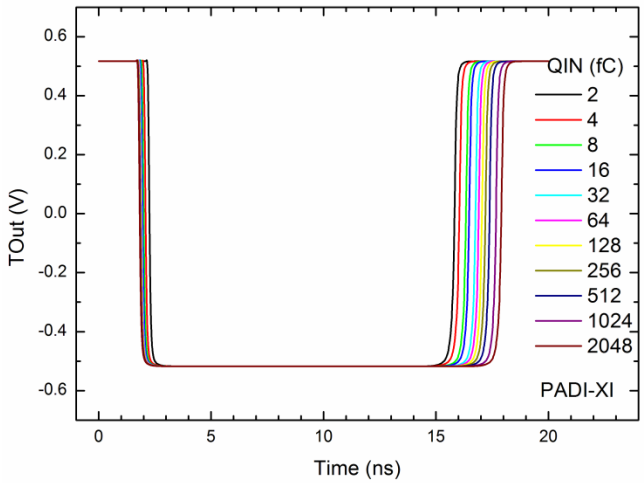


Fig. 7, Simulated response of PA out and Tout for QIN swept from 2 fC to 2048 fC; VTHR=25 mV, the stretched time is set to about 15 ns.

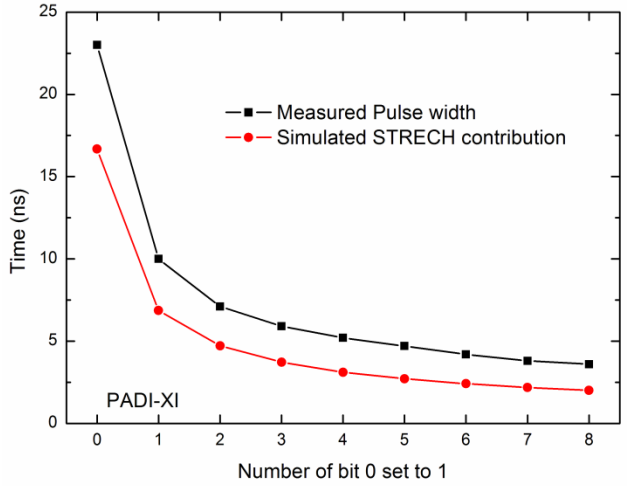


Fig. 8, The output pulse width depends on the number of bits B0 connected to 1 (at VDD).

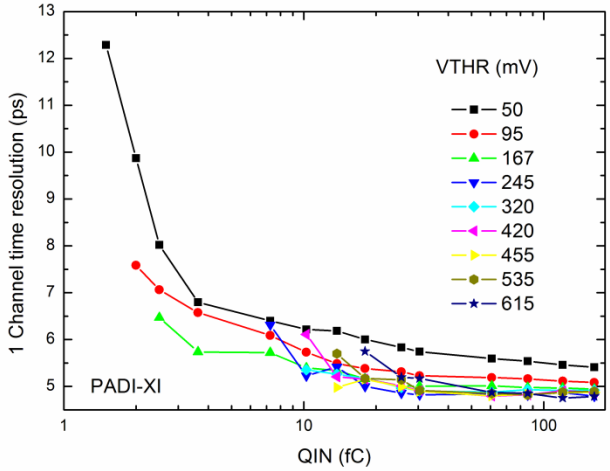
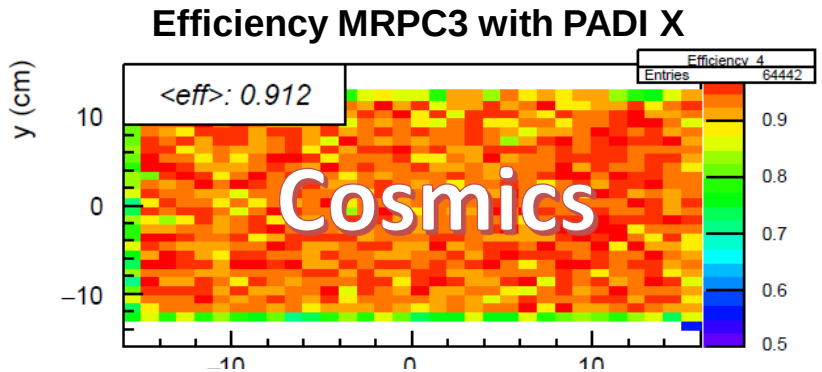
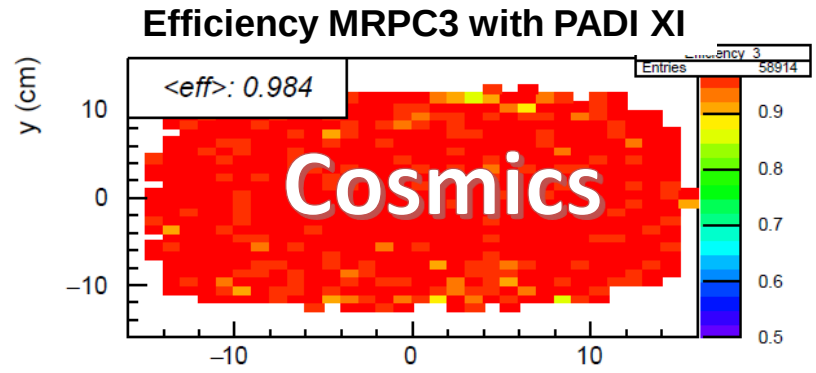
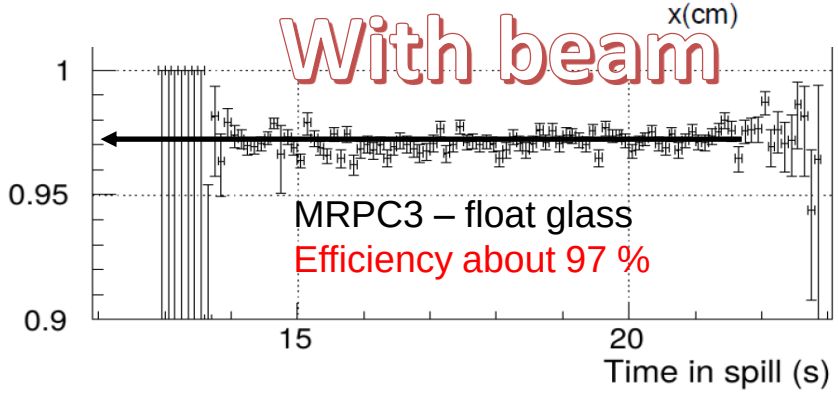
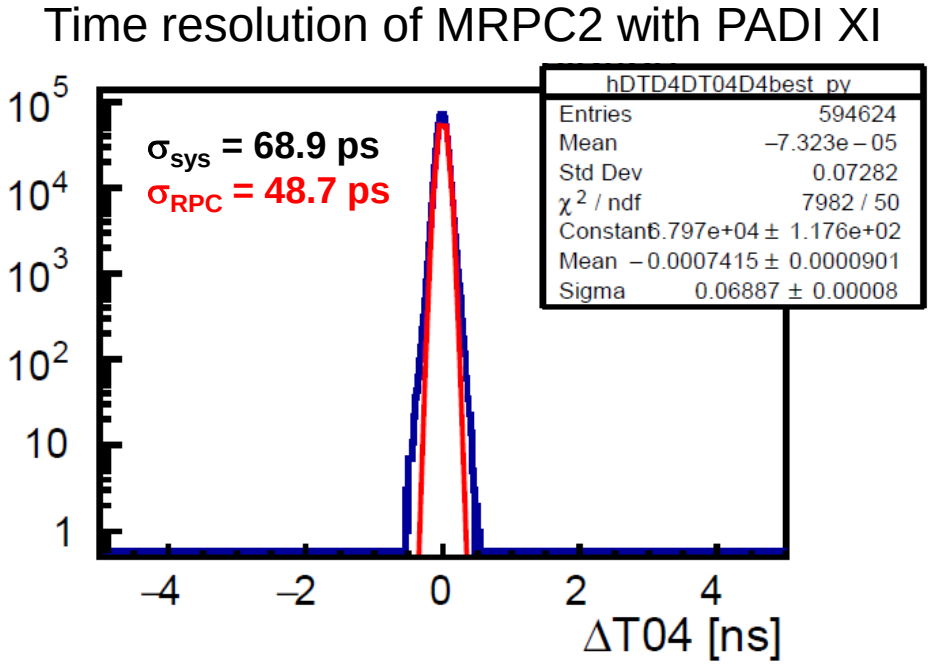


Fig. 9, 1 Channel PADI-XI and TDC time resolution.









Efficiency Bucharest counter

Efficiency	Gap 140 µm	Gap 200 µm
PADI X	81 %	93 %
PAD XI	92 %	98 %

Preliminary