WASA: a Low Power TPC Readout ASIC in 65nm CMOS

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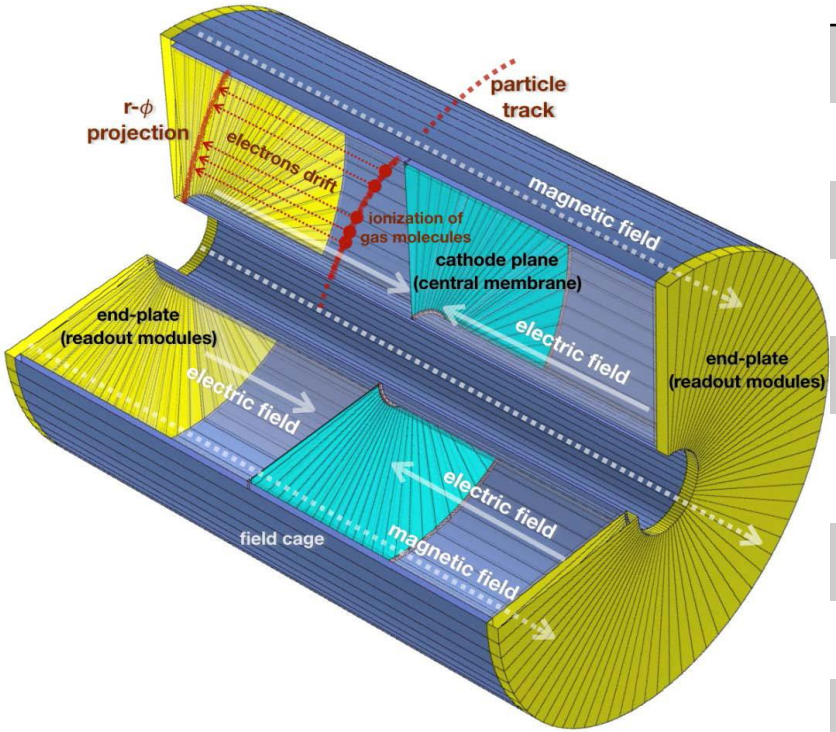
Introduction



Momentum resolution (B=3.5T)	$\delta(1/p_t \approx 10^{-4}/GeV/c)$
δ_{point} in $r\Phi$	<100 μm
δ_{point} in rz	0.4-1.4 mm
Inner radius	329 mm
Outer radius	1800 mm
Drift length	2350 mm
TPC material budget	$\approx 0.05X_0$ incl. field cage $< 0.25X_0$ for readout endcap
Pad pitch/no. padrows	$\approx$ 1 mm × (4~10mm) /$\approx$ 200
2-hit resolution	$\approx$ 2 mm
Efficiency	>97% for TPC only ($p_t > 1GeV$) >99% all tracking ($p_t > 1GeV$)

- TPC can provide large-volume high-precision 3D track measurement with stringent material budget
- In order to achieve high spatial resolution, small pads (e.g. 1 mm x 6mm) are needed, resulting ~1 million channel of readout electronics
- Need low power consumption readout electronics working at continuous mode

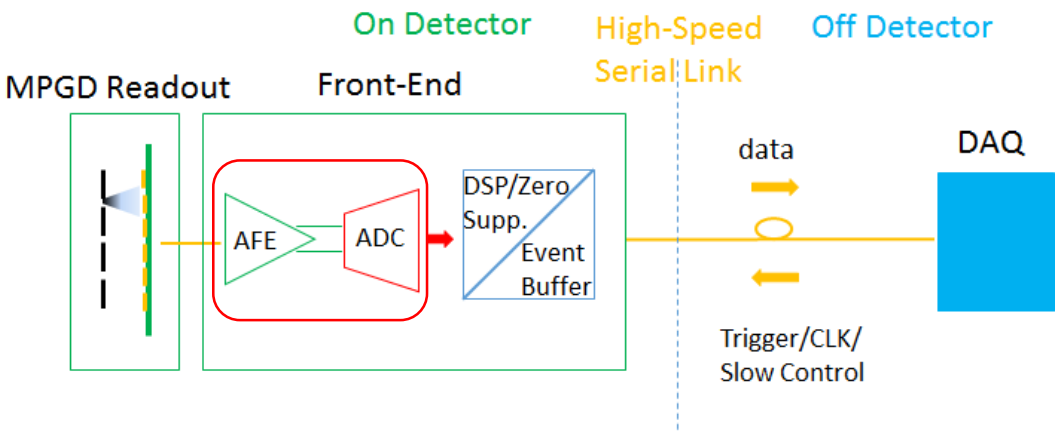
TPC Readout ASICs

- Waveform sampling (8-10 bit, ~10MS/s) is required for TPC signal processing
- Direct ADC sampling is more preferable than SCA for high rate applications
- Lower power consumption → less cooling → less material

	PASA/ALTRO	AGET	Super-ALTRO	SAMPA
TPC	ALICE	T2K	ILC	ALICE upgrade
Pad size	4x7.5 mm^2	6.9x9.7 mm^2	1x6 mm^2	4x7.5 mm^2
Pad channels	5.7 x 10^5	1.25 x 10^5	1-2 x 10^6	5.7 x 10^5
Readout Chamber	MWPC	MicroMegas	GEM/MicroMegas	GEM
Gain	12 mV/fC	0.2-17 mV/fC	12-27 mV/fC	20/30 mV/fC
Shaper	CR-$(RC)^4$	CR-$(RC)^2$	CR-$(RC)^4$	CR-$(RC)^4$
Peaking time	200 ns	50 ns-1us	30-120 ns	80/160 ns
ENC	385 e	850 e @ 200ns	520 e	482 e @ 180ns
Waveform Sampler	ADC	SCA	ADC	ADC
Sampling frequency	10 MSPS	1-100 MSPS	40 MSPS	20 MSPS
Dynamic range	10 bit	12 bit(external)	10 bit	10 bit
Power consumption	32 mW/ch	<10 mW/ch	47.3 mW/ch	17 mW/ch
CMOS Process	250 nm	350 nm	130 nm	130 nm

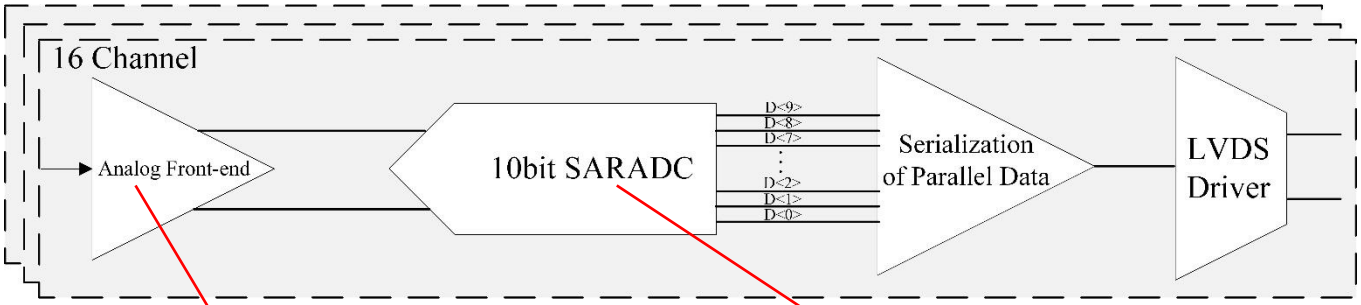
WASA: Waveform Sampling front-end ASIC

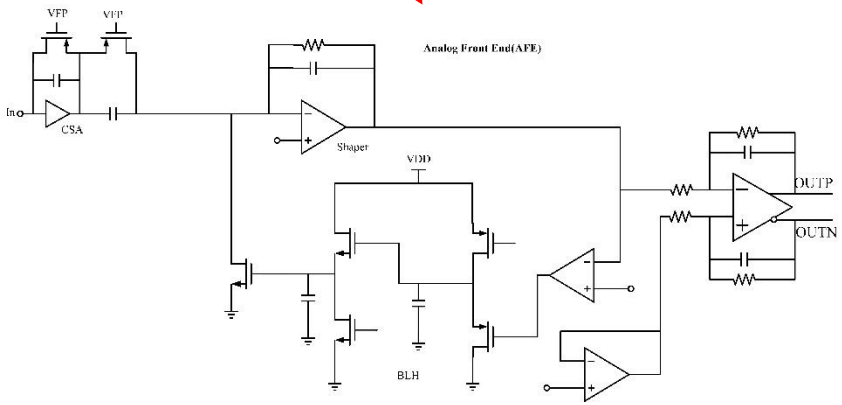
- In order to reduce the power consumption:
  - Using more advanced 65 nm CMOS process favoring digital logics
  - Reducing analog circuits:
    - CR-$(RC)^n$ →CR-RC, moving high order shaping to digital domain
    - ADC structure : pipeline → SAR (Successive Approximation Register)
- So far only the AFE and the ADC parts have been implemented

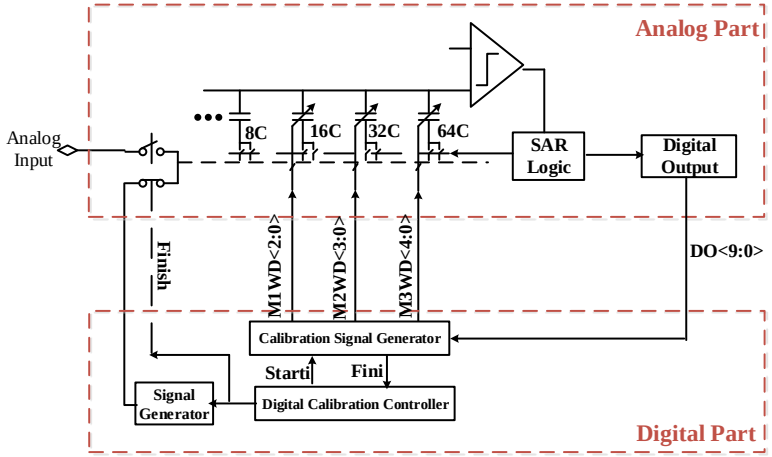


Architecture

- 16 channel prototype chip
  - AFE: CSA+CR-RC shaper
  - SAR-ADC: 10bit, up to 100MSPS
  - Parallel DDR data output

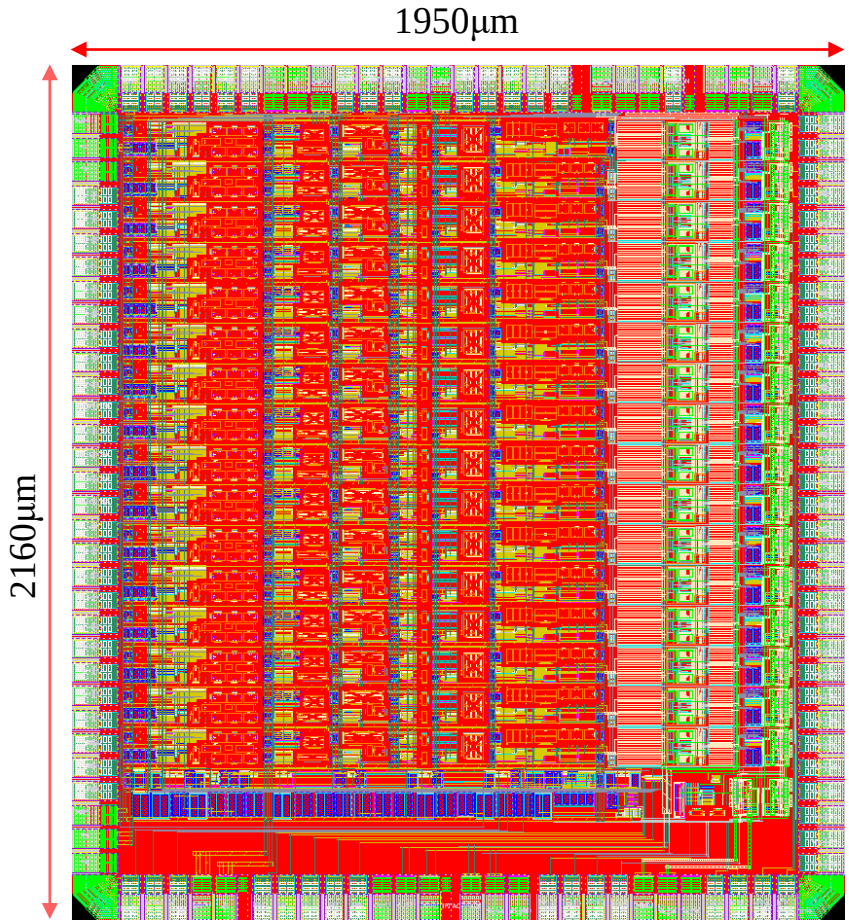






Specifications

- Process: TSMC 65nm LP
- Power supply: 1.2V

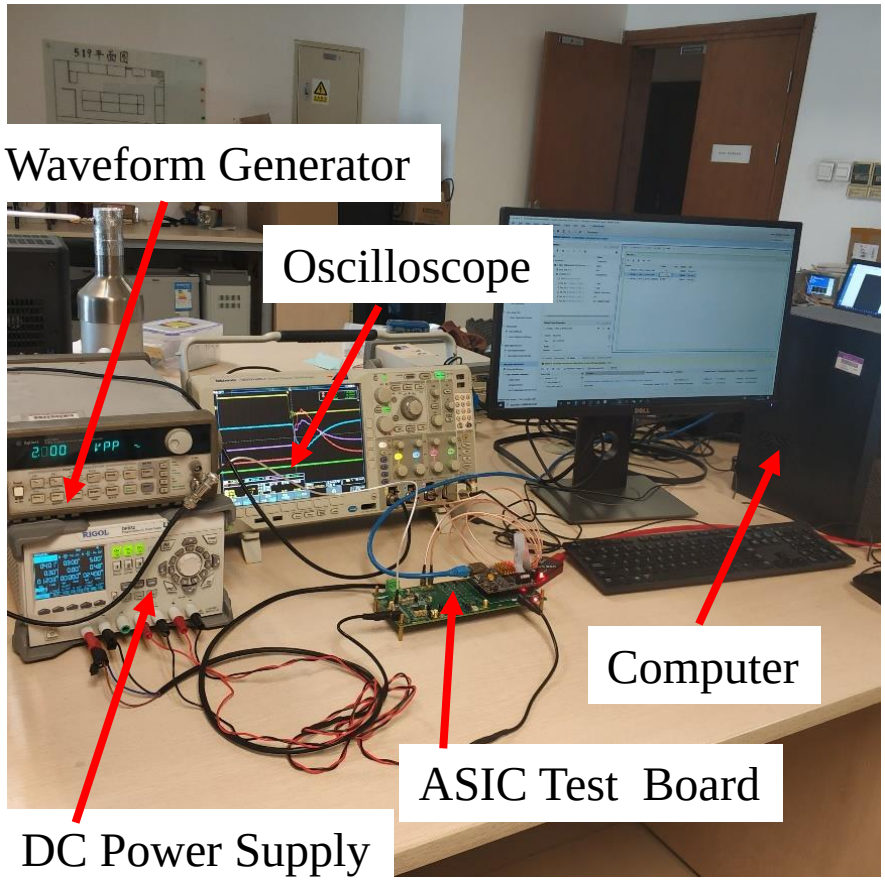


AFE(Analog Front-End)	
Signal Polarity	Negative
Detector Capacitance	5-20 pF
Shaper	CR-RC
Shaping Time	160 ns
ENC (Equivalent Noise Charge)	533e +9.1e/pF
Dynamic Range	120 fC max.
Gain	10-40 mV/fC
INL (Integrated Non-Linearity)	<1%
Crosstalk	<1%
Power Consumption	1.43 mW/ch

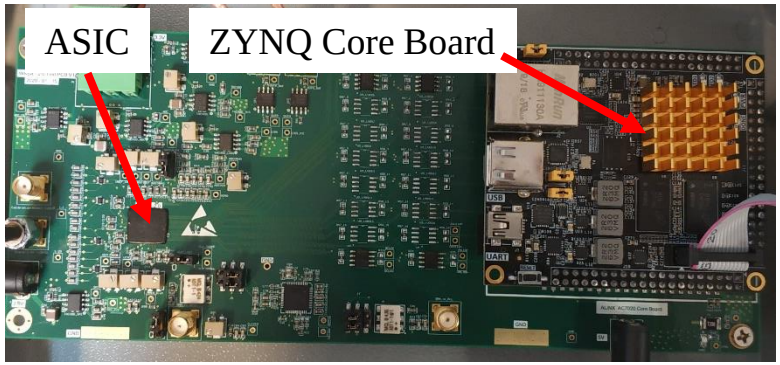
SAR-ADC	
Input Range	-0.6 V ~ 0.6 V diff.
Resolution	10 bit
Sampling Rate	100 MS/s max.
DNL	<0.6 LSB
INL	<0.6 LSB
SFDR @ 2MHz, 40MSPS	68 dBc
SINAD	57 dB
ENOB	>9.2 bit @ 2MHz
Power Consumption	0.9 mW/ch @ 40MS/s

Evaluation System

- Test setup

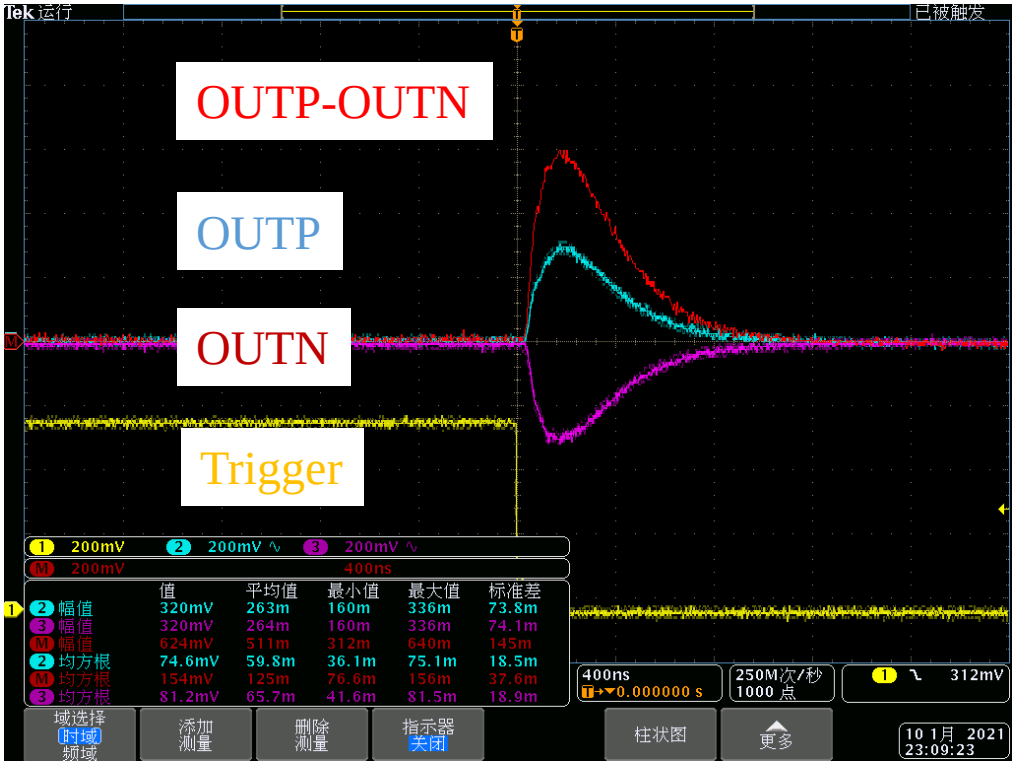


- ASIC Evaluation Board

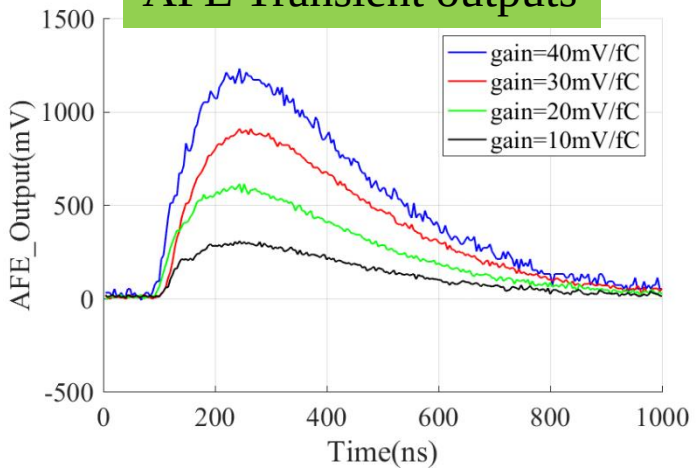


Transient Waveforms

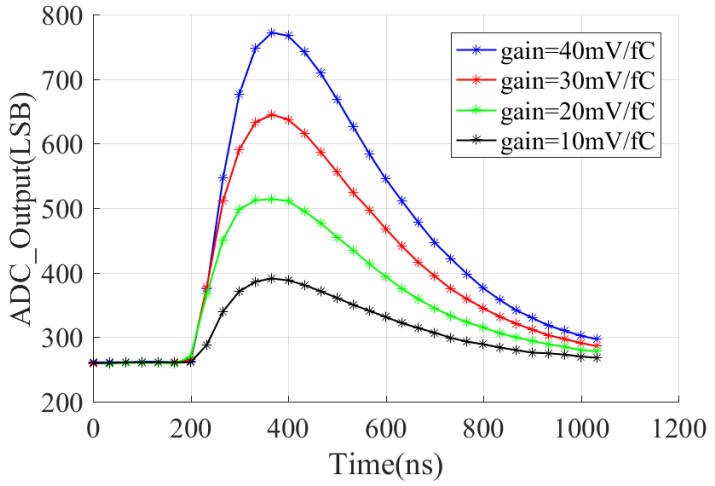
- Transient outputs
  - Differential baseline can be externally adjusted



AFE Transient outputs

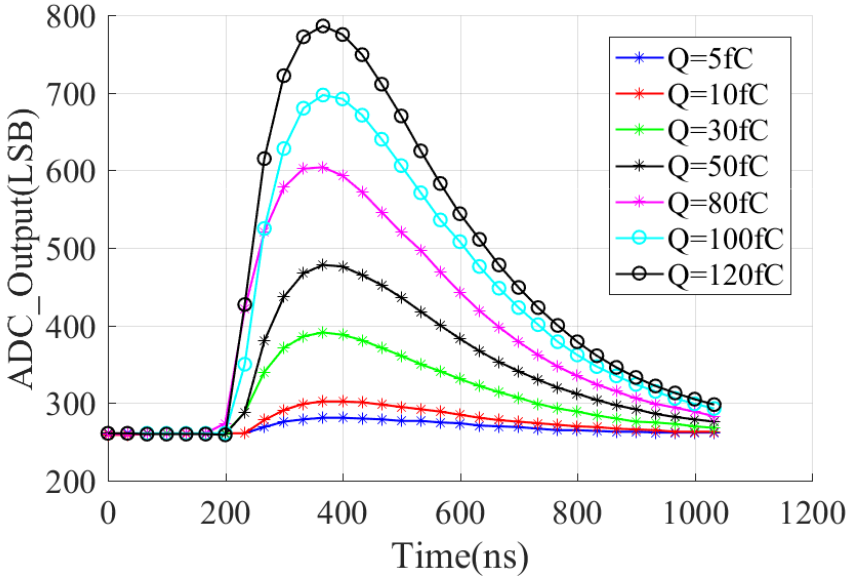


ADC Transient outputs @ 30MSPS

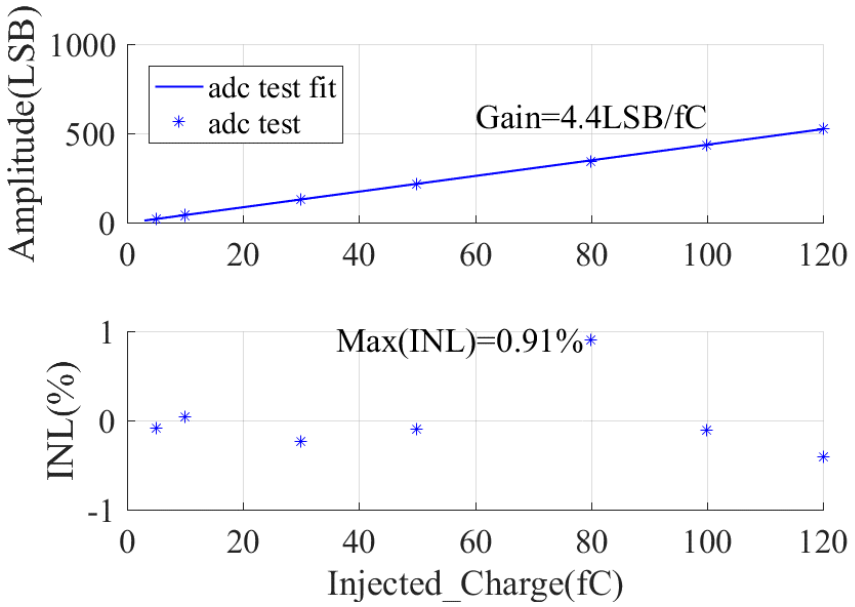


Non-Linearity

- Transient outputs



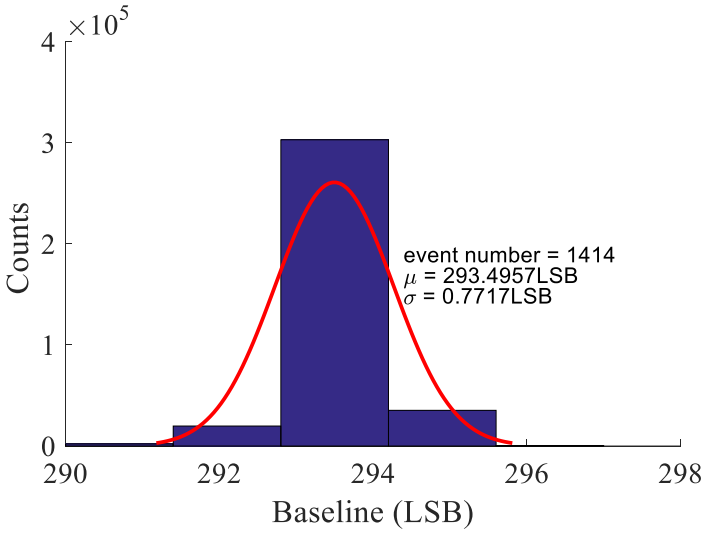
- The linearity @ gain = 10 mV/fC

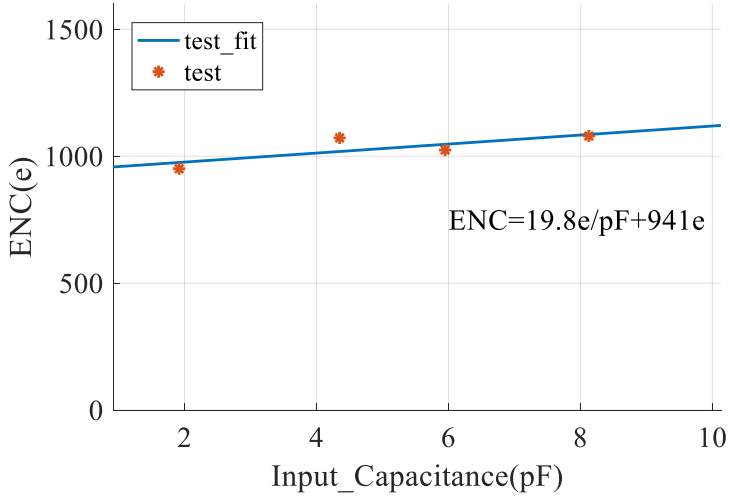


Gain = 4.4 LSB/fC = 4.4 x 2.34 mV/fC = 10.3 mV/fC

Noise Performance

- The baseline fluctuation @ gain = 10 mV/fC
  - Significant contribution from ADC quantization noise
  - Can be reduced using digital filter

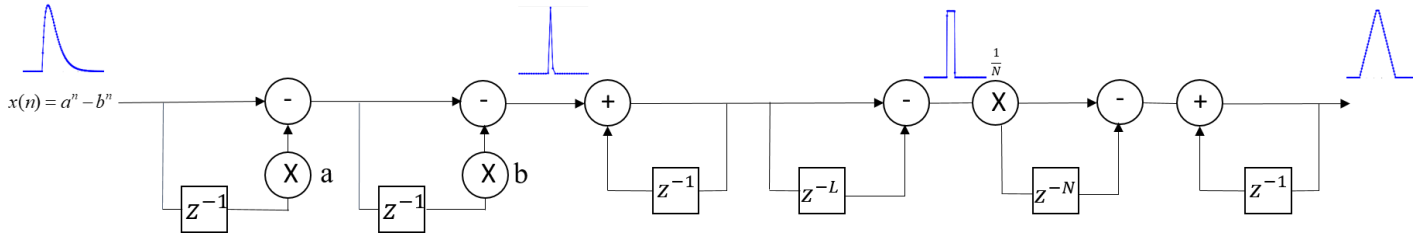


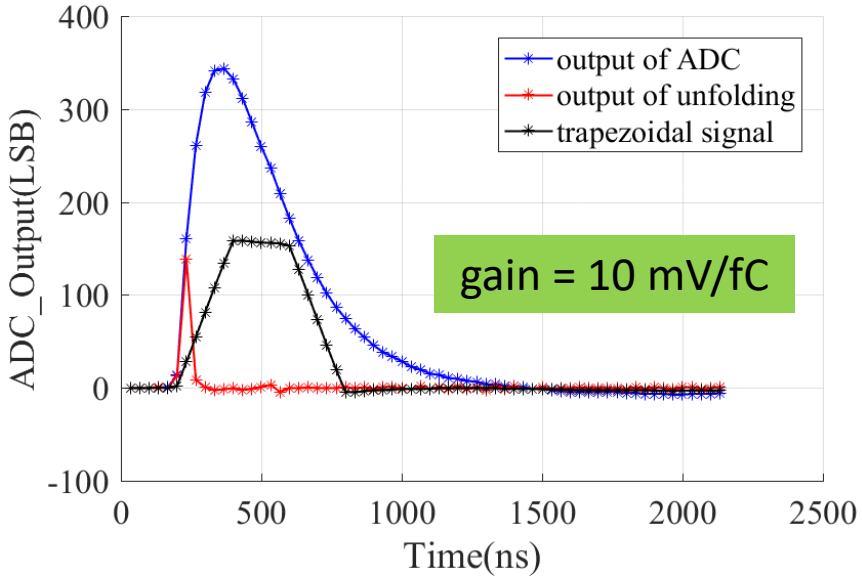


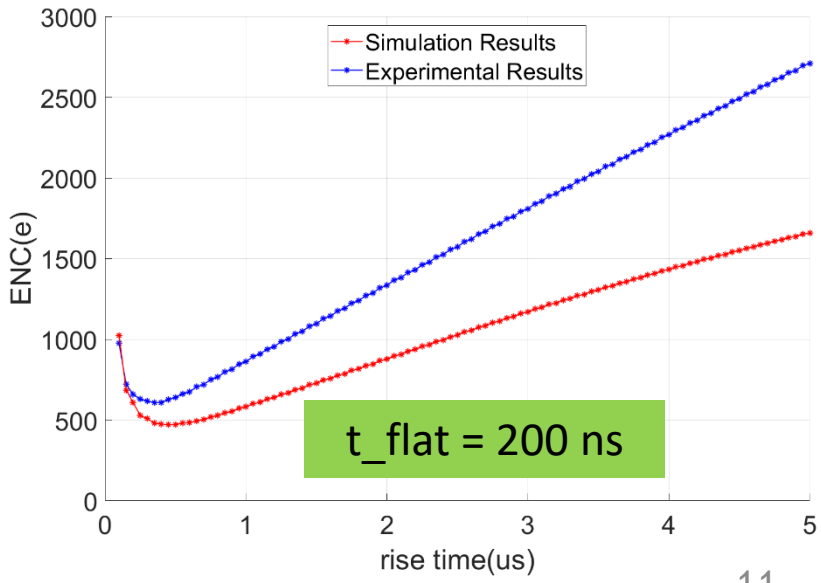
ENC = 980 electron @ Cin = 1.93 pF, gain = 4.4 LSB/fC

Digital Trapezoidal Filter Offline

- Based on unfolding method: 2 MUL, 6 ADD/SUB and SHIFT operations
- More symmetric waveforms
- Original ENC = 980 e reduced to 474 e min. after digital trapezoidal filter



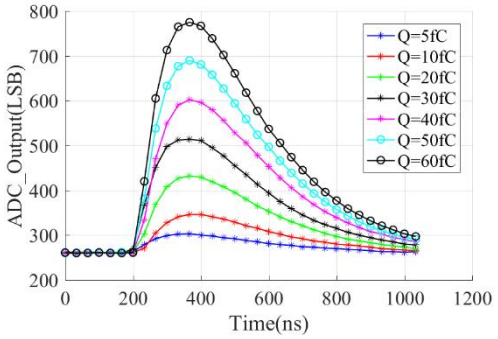


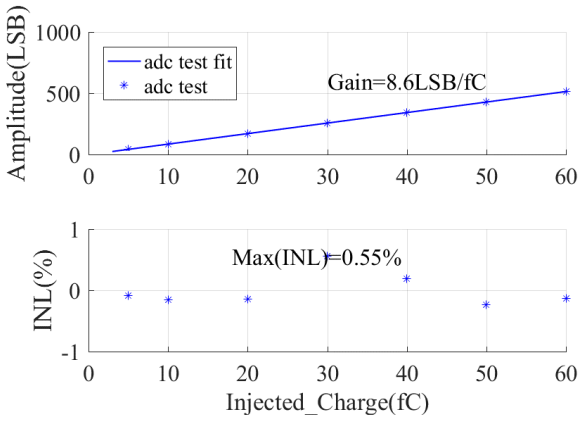


Non-Linearity @ 20-40 mV/fC

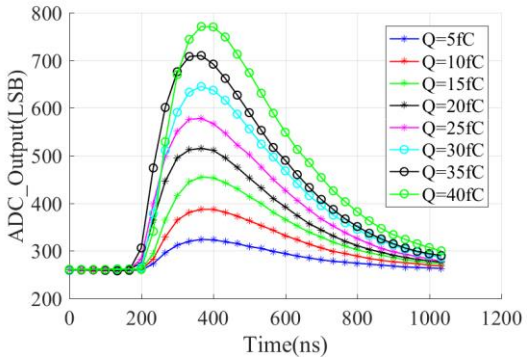
- Non-Linearity performance

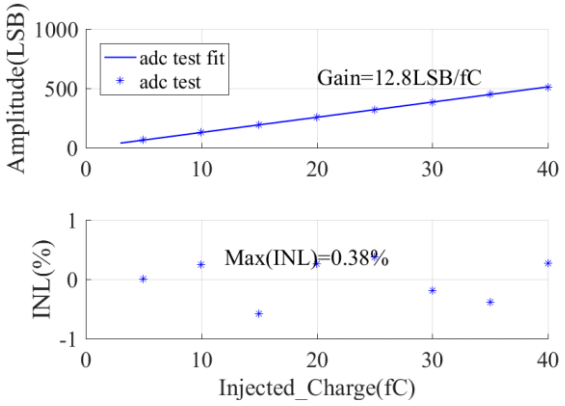
20 mV/fC



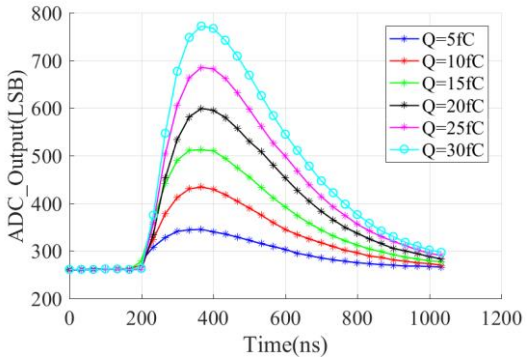


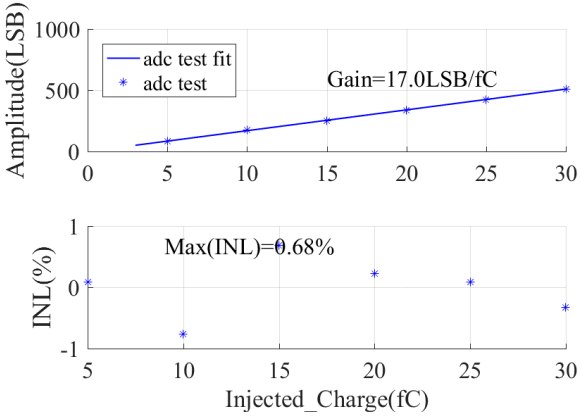
30 mV/fC





40 mV/fC

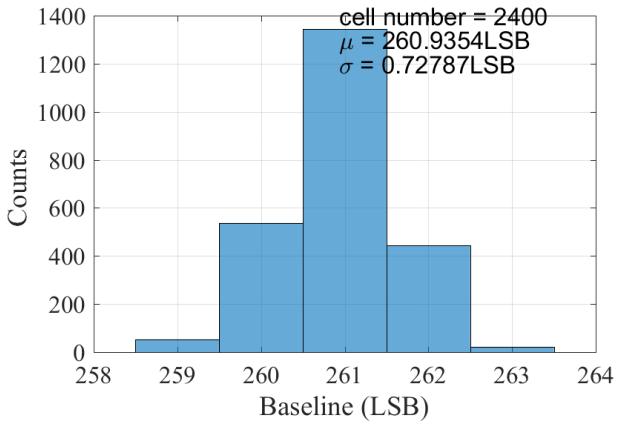




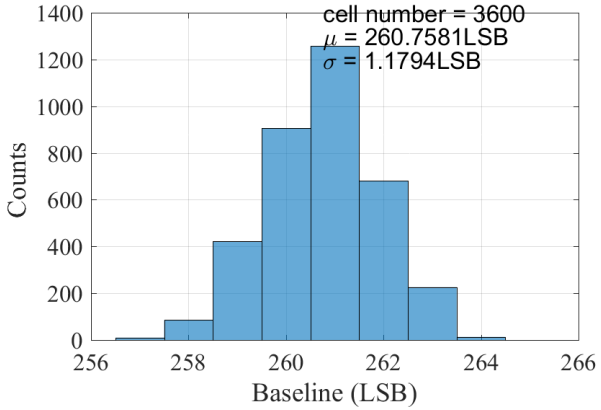
Noises @ 20-30 mV/fC (Preliminary)

- Noise performance @ Cin = 1.93 pF

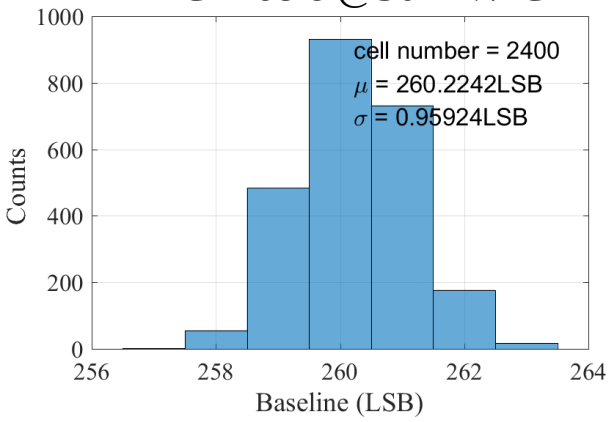
ENC = 529 e @20 mV/fC

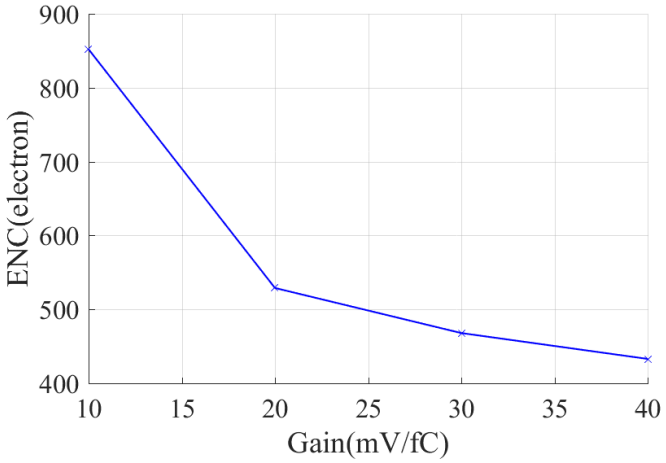


ENC=433 e @40 mV/fC



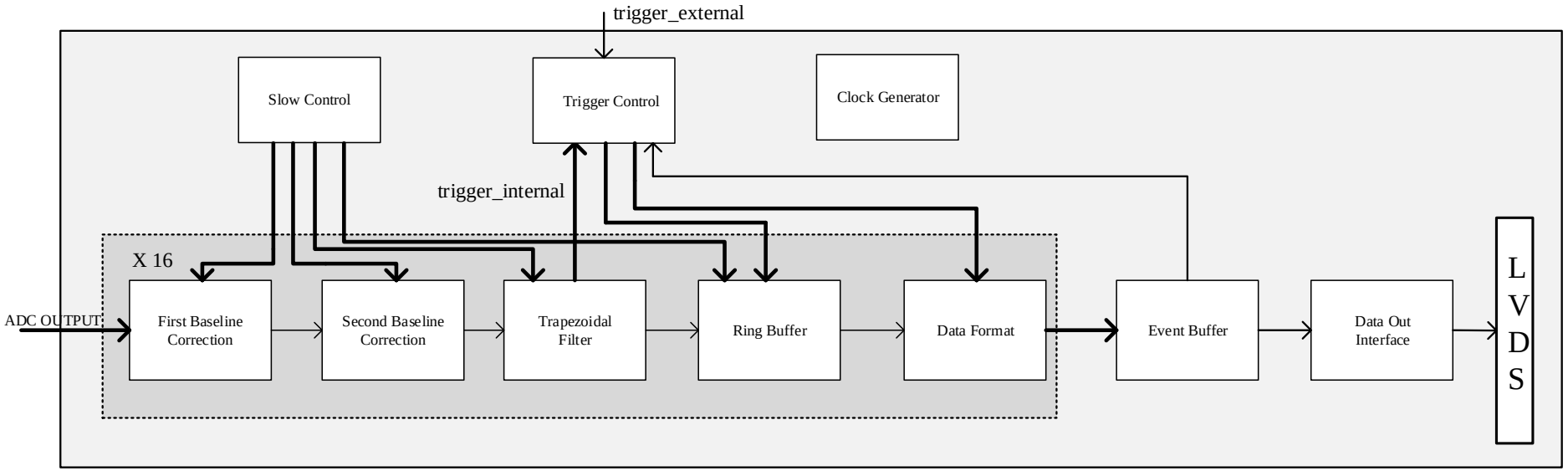
ENC=468 e @30 mV/fC





Future Development

- Integration of digital circuits:
  - Baseline correction filters
  - Trapezoidal filter
  - Two stage buffer with internal/external trigger



Summary

- A 16 channel low power readout ASIC for TPC readout have been developed
  - The power consumption is 2.33 mW/channel:
  - ENC = 980 e @ Cin=2 pF, gain=10 mV/fC and can be reduced to 474 e using digital trapezoidal filter
- Future Plan
  - Test with detectors
  - Low power digital filter and data compression in FPGA/ASIC

W. Liu et al, WASA: a low power front-end ASIC for time projection chambers in 65 nm CMOS 2020 JINST 15 P05005

Thank You