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Project of a new readout chip for MPGDs

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Introduction

Draft chip specifications

Prospects

INTRODUCTION

Motivations of the project

- Versatile readout chip in the framework of the EIC project and beyond
  - adapted to streaming readout DAQ
  - for different kinds of MPGD detectors and beyond
  - production technology available in the future
- Large ranges in term of signal amplitudes, electrode capacitances, peaking times
- Primary goal: readout chip dedicated to most kinds of MPGD detectors
- Optionally: extension to other kinds of detectors (calorimeters ? photon detectors ?) and/or specific constraints (ps-level time resolutions)

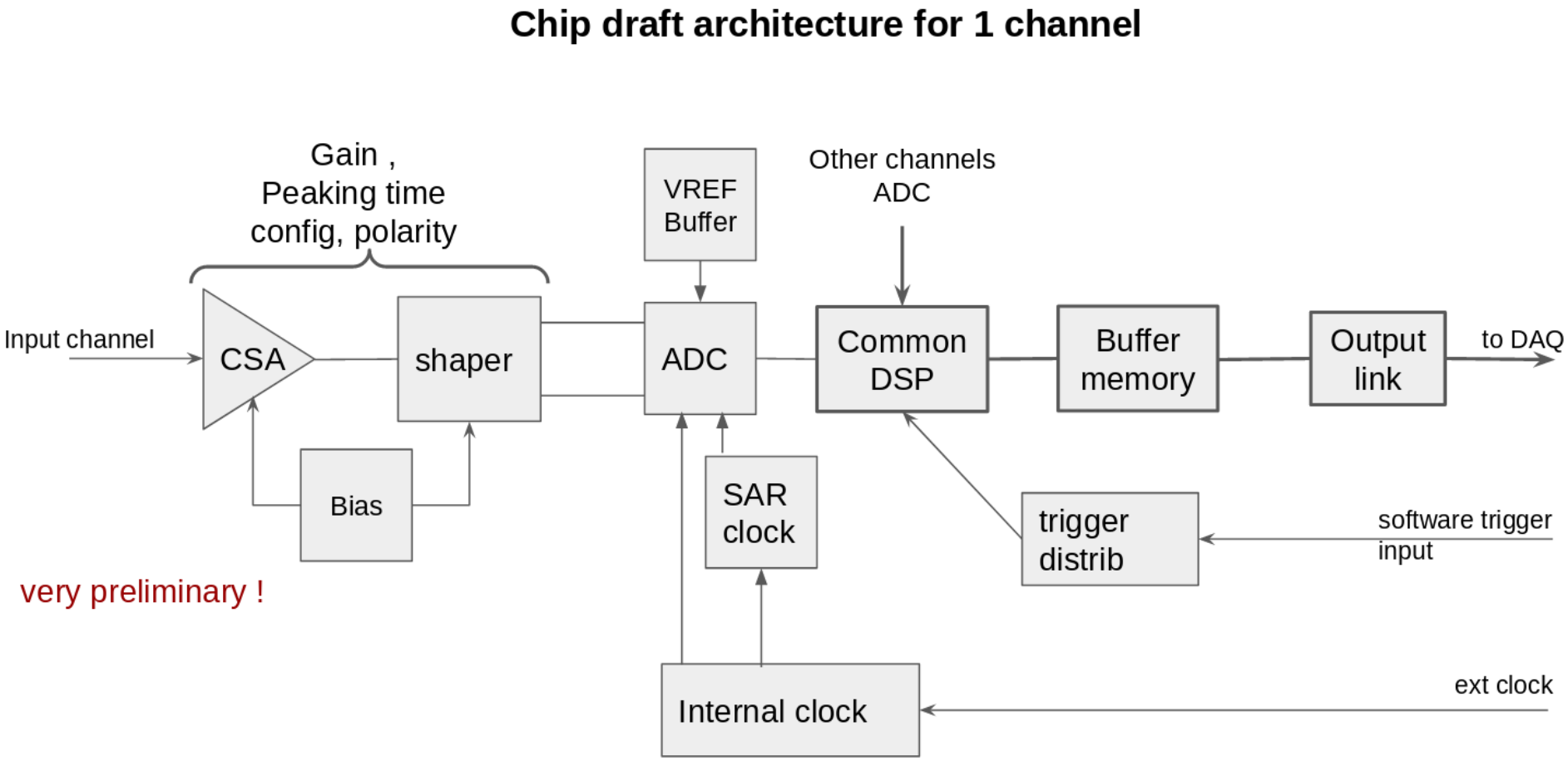
Common initiative of Sao Paulo Universities and CEA Saclay IRFU

- Sao Paulo Universities designed the SAMPA chip (readout chip for ALICE TPC)
- IRFU developed several front-end chips (AFTER, AGET, DREAM,...) and other kinds of chips (SAMPIC TDC,..)
- Large amount of competences on front-end, digitization, and digital treatments

Present status

- Definition of specifications in progress, many open questions
- Preliminary studies on possible architecture, bloc structures, and possible technologies
- Choice of die production technology to be determined soon (130nm or 65nm)

TENTATIVE CHIP ARCHITECTURE



DRAFT SPECIFICATIONS : FRONT-END PART

Front-end characteristics

- Number of channels: 32 or 64, rather low number in order to keep the chip small
- Programmable peaking time: at least in 50-200 ns range, discussions to extend it to shorter values
- Programmable amplitude ranges: from [0-50 fC] to [0-few pC], requirements concerning dynamics to be clarified
- Max input capacitance: 200 pF, extension to larger capacitances asked by some detector groups, to be investigated
- Reversible polarity
- Internal discriminators ? (trigger signal generation, TDC measurements). To be investigated

Chip performances under study

- Noise figures vs detector capacitance, peaking times, gain,...
- Behavior vs hit rate and charge per channel (average and peak), double peak detection
- Time to recover from saturation (for instance after sparks)
- Power consumption per channel

DRAFT SPECIFICATIONS : DIGITAL PART

Digitization characteristics

- ADC sampling frequency range: 10 to 40 MHz, possibility to go to larger value to be investigated (shorter peaking times for better time resolution, larger hit rates and double peak discrimination)
- Dynamics: 12 bits, larger values probably not possible
- Synchronization with external clock (internal PLL if necessary) + common timestamp reset signal or upstream heartbeat packets
- Optionally: additional TDC connected to discriminator, for time resolution better than 1 ns

Data treatment

- Basic treatments: pedestal subtraction, common mode correction, zero suppression
- Optional advanced treatments: clusterization, peak finding, time extraction, energy computation, etc…, possibility to customize data treatment ?
- Both streaming readout and trigger modes possible → external trigger input
- Possibility to emit trigger from digital processing ?
- Output buffer to store data before transfer (+ circular buffer in triggered mode)
- Max output data flux not yet defined, strongly depends on the experimental conditions, to be discussed with detector groups

DRAFT SPECIFICATION : GENERALITIES

General specifications and environment

- Die/package size to be defined, small die size expected, at the level of 1 cm^2, depending on the complexity of the implementation
- Technology (130 or 65nm) to be defined, complex issue depending on several internal and external parameters. We need to chose the technology soon
- Power consumption expected to be around 10-15 mW/ch, also depending on the environment constraints

Open questions

- What are the expectation about the environment ? Temperature ? Max radiation level ?
- Constraints on the chip size ?

PROSPECTS

Chip definition in progress

- Draft specification
- Studies in progress on the possible chip architecture and elements, and on expected performance
- Several questions still open, in particular die production technology

Tentative timeline

- Preliminary studies: ~ 6 months
- Development + prototype production + tests: ~ 2 – 2.5 years
- Preserial production and tests: ~ 1 year
- Full production: 0.5 – 1 year

Collaboration around the chip

- Common initiative of Sao Paulo Universities and CEA Saclay
- Still informal, formalization in progress
- Not funded yet, under investigation
- Other contributors are welcome !