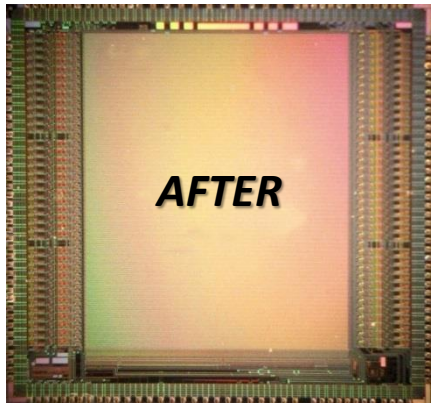
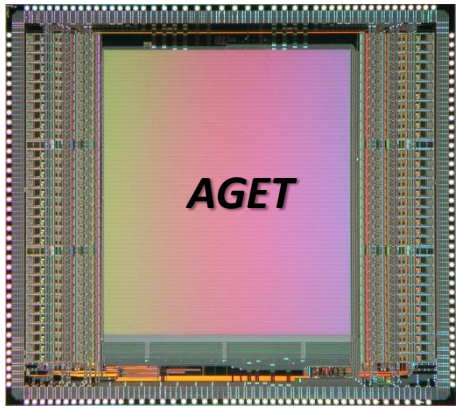
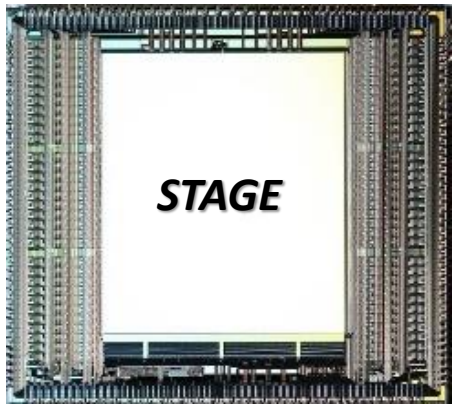
DE LA RECHERCHE À L'INDUSTRIE

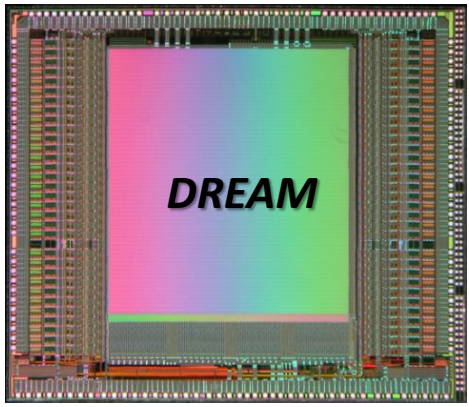
AFTER family

P. Baron; *D. Baudin; E. Delagnes*
IRFU-CEA – Université Paris-Saclay









Topical Workshop on Front End Electronics for Gas Detectors
Developments Session
Linear Chips
Thursday, 17 June 2021

pascal.baron@cea.fr

Outline

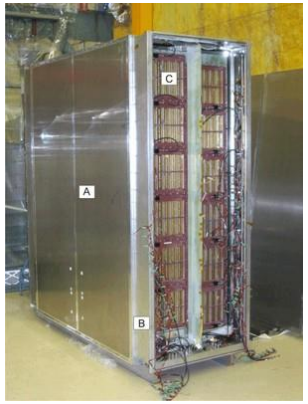
- **AFTER ASIC for T2K project**
  - History, Architecture & Requirements
- **AGET ASIC for GET project & STAGE ASIC**
  - Architecture & Requirements
- **DREAM ASIC for CLAS12 project**
  - Architecture & Requirements
- **SUMMARY**

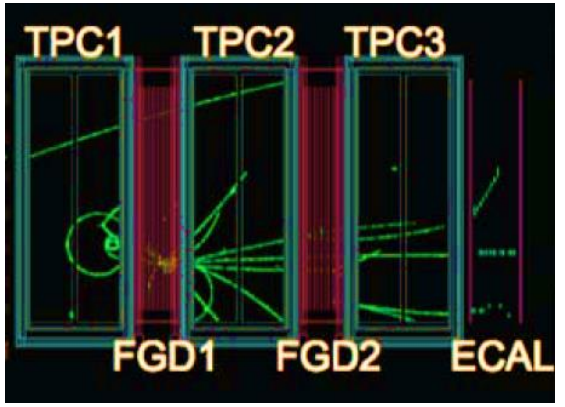
T2K Project: study of neutrino oscillation in J-PARC

- **Electronic**: Must perform a three dimensional space point readout of 3 big TPCs
- **Beginning of the design (Q1 2005)**: End-plate detectors & Gas not defined

=> Electronic must: - support both polarities of detector signal;
- have programmable gain and adaptable time measurement window

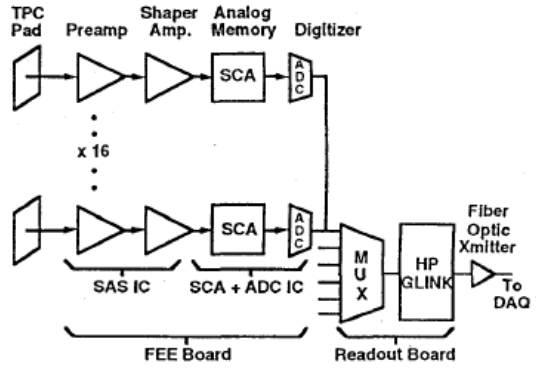
- **Architecture based on STAR TPC electronic: 2 ASICS**
  - Charge: CSA + Filter + Gain (Amplitude of the shaped signal)
  - Drift time: SCA (Time of the peak shaped signal/Trigger)





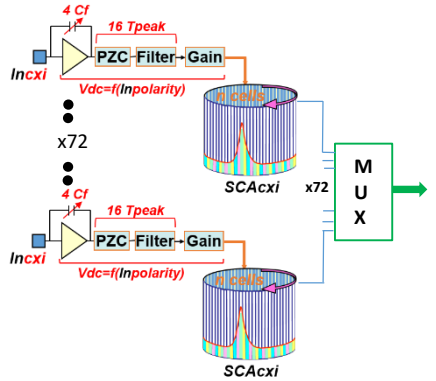
TOKAI : First event (19/12/2009)

STAR electronic



2 ASICs: SAS IC + [SCA+ADC] IC
FEE Board: 2 x 16 channels

T2K ASIC



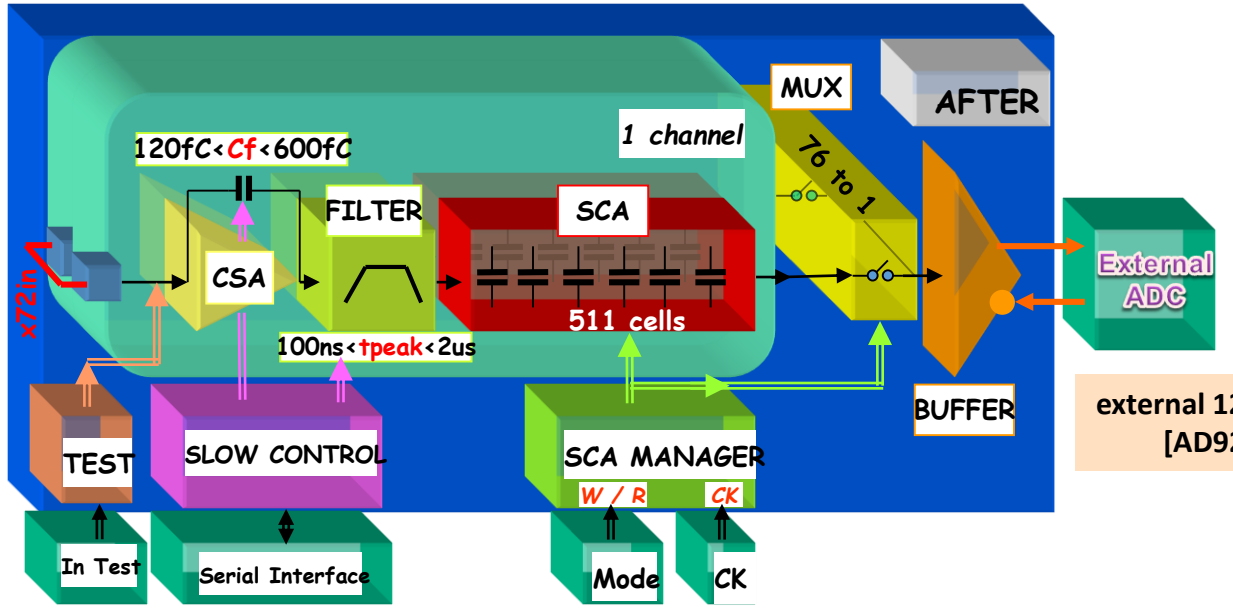
1 ASIC: AFTER + external ADC

- **T2K context:** low event rate (beam rate 0.3 Hz; cosmic 20 Hz) & external trigger available

  => Digitization of the totality of the SCA through commercial ADC; No auto triggering

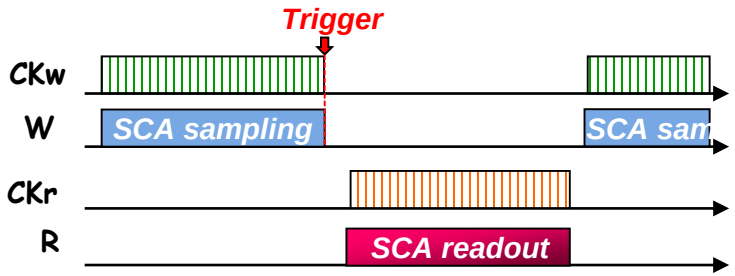
AFTER ASIC for T2K project : Architecture

- **72 analog channels:** *CSA, Filter, SCA (511 cells)*
- **Input current polarity:** *positive or negative*
- **4 Gains:** *120 fC; 240 fC; 360 fC; 600 fC*
- **16 peaking time values:** *100 ns to 2 µs*
- **SCA:** ***511 analog memory cells/channel***
- **Fsampling:** *1 MHz to 50 MHz*
- **Fread:** *20 MHz*
- **Slow control (SPI)**
- **Test inputs:** *calibration & test*

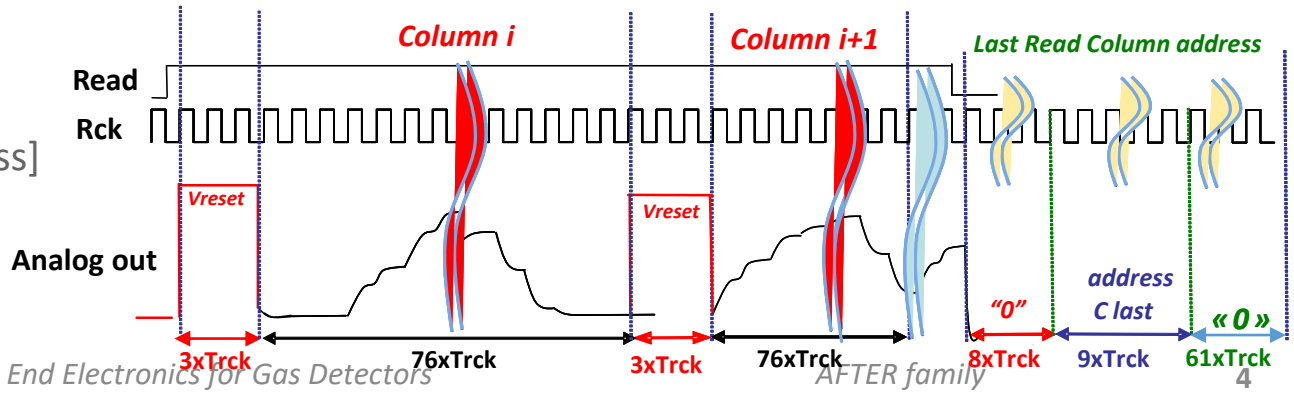


external 12-bit ADC [AD9229]

- **Sampling Phase**
  - Detector signal is converted, amplified, filtered & continuously sampled in SCA
- **Readout Phase (Trigger)**
  - Digitization of all 76 x 511 analog samples



- **Readout format**
  - Column by column, memory cell of the first to the last channel
  - 511 x [3 bits “reset” + 76 channel cells] + [last read column address]



Requirements

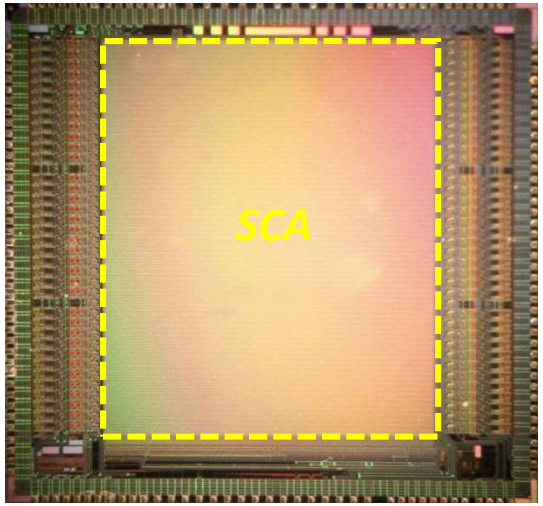
Parameter	Value
Polarity of detector signal	Negative or Positive-selectable by external resistors
Channels number	72
Charge measurement	
Input dynamic range	120 fC, 240 fC, 360 fC, 600 fC
Output dynamic range	2V p-p (differential)
I.N.L	< 2%
Resolution	< 850 e- (Gain: 120fC; Peaking Time: 200ns; Cinput < 30pF)
Sampling	
Peaking time	100 ns to 2 µs (16 values)
SCA time bin number	511
Sampling Frequency	1 MHz to 50 MHz
Readout	
Readout frequency	20 MHz-25 MHz
Readout mode	All channels; Number of time buckets readout out programmable from 1 up to 511
Minimum dead-time	Fixed 78 x 40 ns x Number of Time buckets
Test	
calibration	1 channel among 72; 1 external test capacitor
test	1 channel among 72; internal test capacitor (1 among 4)
functional	1 to 72(76) channels; 1 internal test capacitor per channel
Counting rate	< 0.3 Hz/channel
Power consumption	< 8 mW / channel @ 3.3V

"AFTER, an ASIC for the Readout of the Large T2K Time Projection Chambers"

IEEE Transactions on Nuclear Science (Volume: 55, Issue: 3, June 2008)

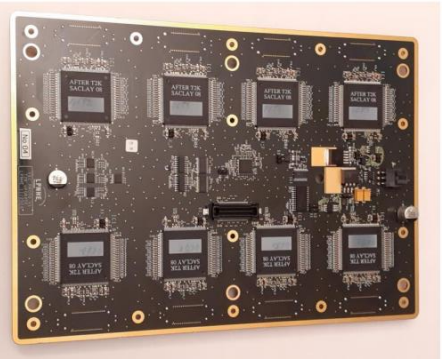
Layout & Package

- Technology: AMS CMOS 0.35 µm
- Area: 7.8 x 7.4 mm^2
- Components # 500 000
- Package: LQFP 160 (28 x 28 x 1.4 mm)



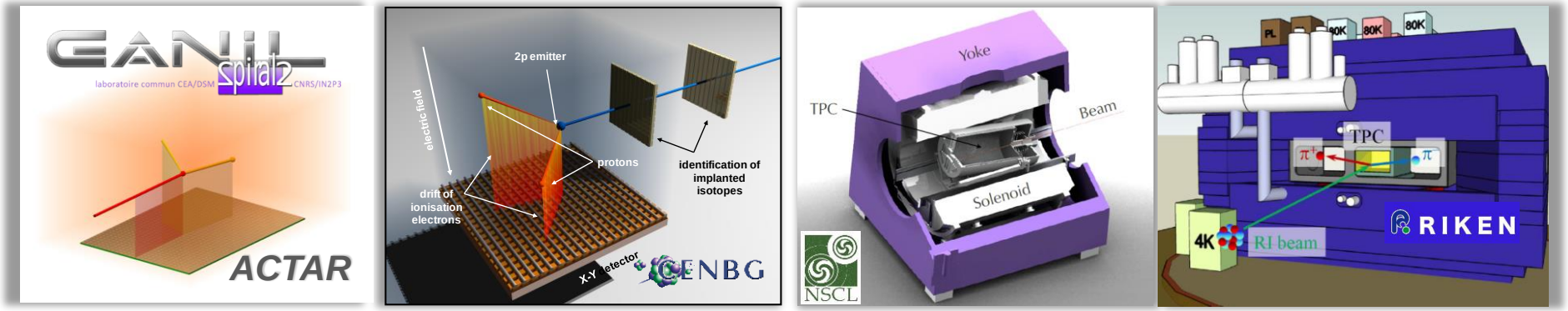
T2K FEC card:

T2K-II upgrade FEC card:



GET Project: Electronic for nuclear physic experiments

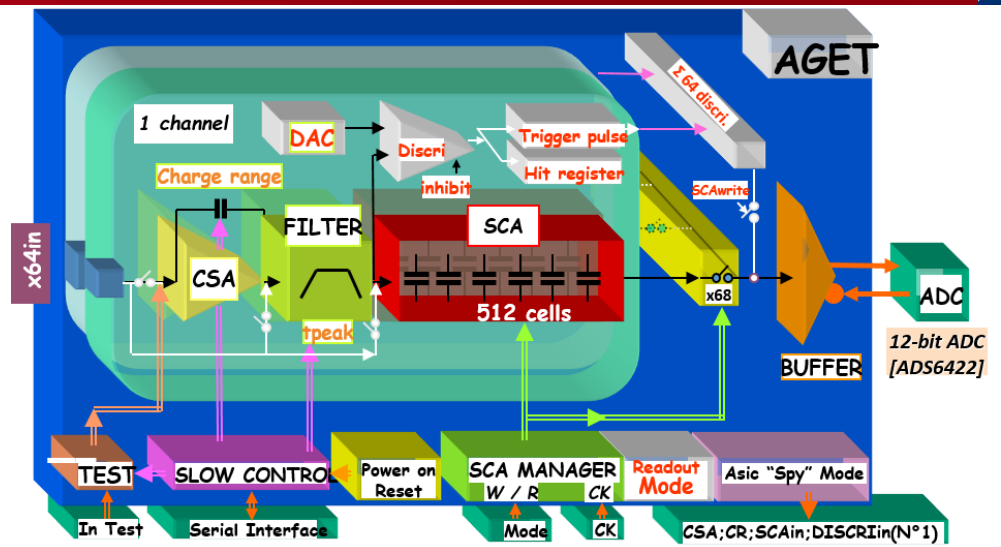
- **Goal**: Full data acquisition system for TPC readout used for the measurement of the nuclear reaction processes occurring between the beam particles and the nuclei of the gas in the detector chamber
- **TPC**: active target & detector
- **Nuclear Physics community: National** [CENBG; GANIL; IRFU]; **International** [NSCL-MSU (USA); RIKEN(Japan)]
- **Project financing**: **ANR** [1/10/2009-30/09/2014]; **NSF** (MSU)

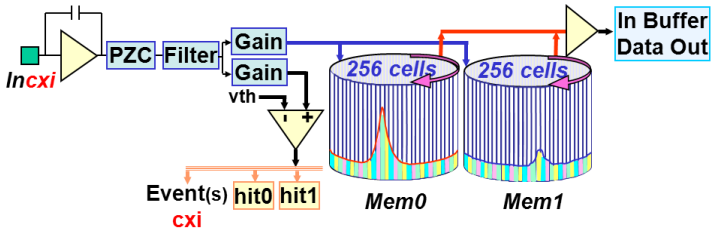


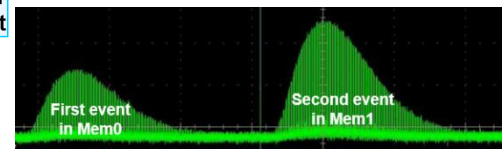
- **Specifications**
  - High dynamic range: 100keV/nucleon to some 10 MeV/nucleon
  - Versatile system for medium sized instrumentation [32 k channels maximum]
  - Counting rate: < 1kHz
  - TPC Trigger: selective readout

AGET ASIC: Architecture

- **64 analog channels :** *CSA, Filter, SCA (512 cells), Discriminator*
- **Auto triggering :** discriminator + threshold (DAC)
- **Multiplicity signal :** *analog **OR** of 64 discriminators*
- **Address of the hit channel(s)**
- **SCA readout mode:** *all, hit or specific channels*
- **4 Gains/channel:** *120 fC; 240 fC; 1 pC; 10 pC*
- **16 peaking time values:** *50 ns to 1 µs*
- **Fsampling:** *1 MHz to 100 MHz*
- **Fread:** *25 MHz*
- **Input current polarity:** *positive or negative*
- **Possibility to bypass the CSA:** *enter directly into the RC2 filter or SCA inputs*
- **SCA:** *the memory can be split in 2 x 256 cells to process 2 consecutive events (implantation & decay event)*

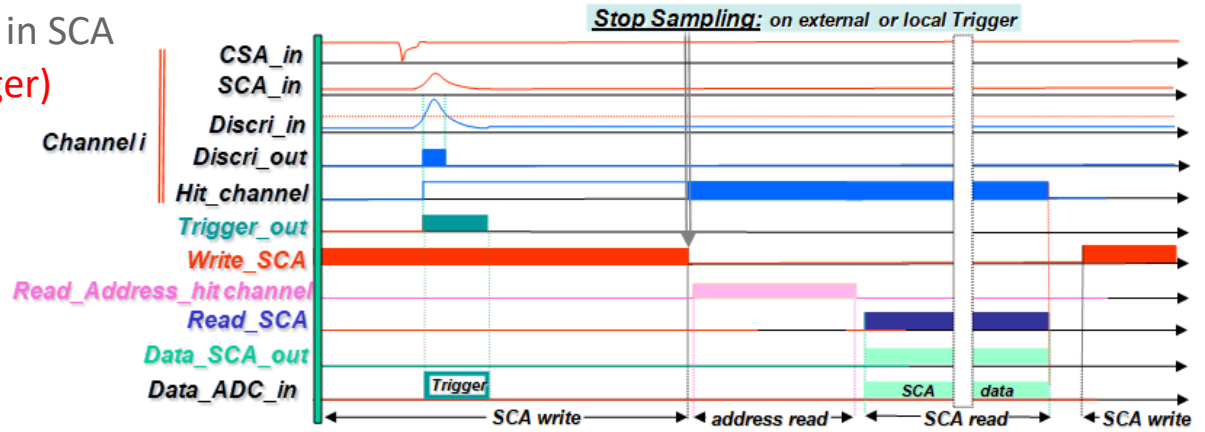






- **Sampling Phase**
  - Detector signal is converted, amplified, filtered & continuously sampled in SCA
  - Filtered signal is compared to threshold giving a Multiplicity signal (Trigger) digitized by external ADC and memorized in temporary Hit Register

- **Readout Phase (Trigger)**
  - HIT register (64-bit) readout
  - Possibility to modify this HIT register for selective readout
  - SCA readout of selected channels or all channels (AFTER mode)



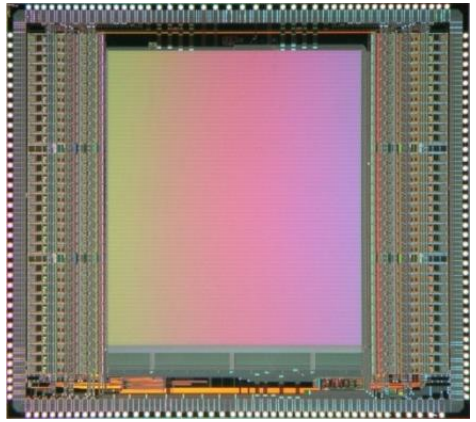
Requirements

Parameter	Value
Polarity of detector signal	Negative or Positive
Channels number	64
External Preamplifier	Yes; access to the filter or SCA input (external CSA)
Charge measurement	
Input dynamic range	120 fC, 240 fC, 1 pC, 10 pC
Gain	Adjustable per channel
Output dynamic range	2V p-p (differential)
I.N.L	< 2%
Resolution	< 850 e- (Gain: 120fC; Peaking Time: 200ns; Cinput < 30pF)
Sampling	
Peaking time	50 ns to 1 µs (16 values)
SCA time bin number	512 or 2 x 256 cells
Sampling Frequency	1 MHz to 100 MHz
Multiplicity	
Multiplicity signal	Analog "OR" of 64 discriminator outputs
Input dynamic range	5% or 17.5% of input channel input charge range
I.N.L	< 5%
Threshold value	7-bit DAC [(3-bit + polarity bit) common DAC + 4-bit DAC/channel]
Readout	
Readout frequency	25 MHz
Channel Readout mode	Hit, selected or all
SCA Readout mode	1 to 512 cells
Test	
calibration	1 channel among 64; 1 external test capacitor
test	1 channel among 64; internal test capacitor (1 among 4)
functional	1 to 64(68) channels; 1 internal test capacitor per channel
Counting rate	< 1 kHz
Power consumption	< 10 mW / channel @ 3.3V

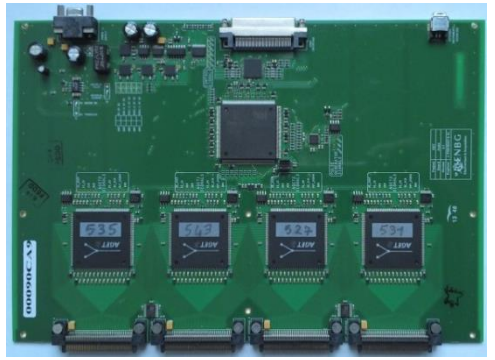
"GET: A generic electronics system for TPCs and nuclear physics instrumentation"
Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment
volume 887, 11 April 2018, Pages 81-93

Layout & Package

- Technology: AMS CMOS 0.35 µm
- Area: 8.5 x 7.6 mm^2
- Components # 700 000
- Package: LQFP 160 (28 x 28 x 1.4 mm)



GET AsAd board:



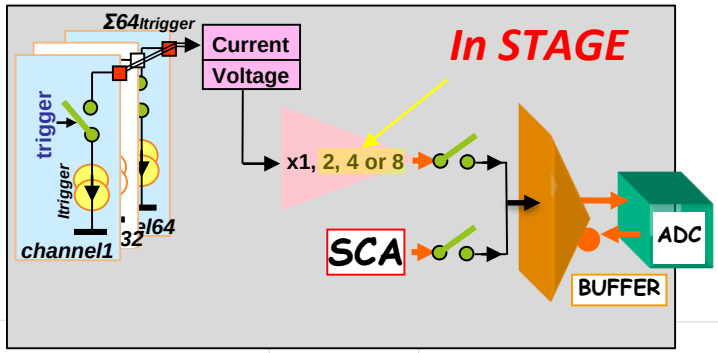
- **STAGE is the upgrade version of AGET with new features as:**
  - New peaking time range value which permits to read TPCs with a highest time window
  - A highest unity value of multiplicity signal which allow a better detection of the signal for triggering

- **STAGE ASIC *Peaking Time: 75 ns to 8 µs [75 ns to 1 µs]***

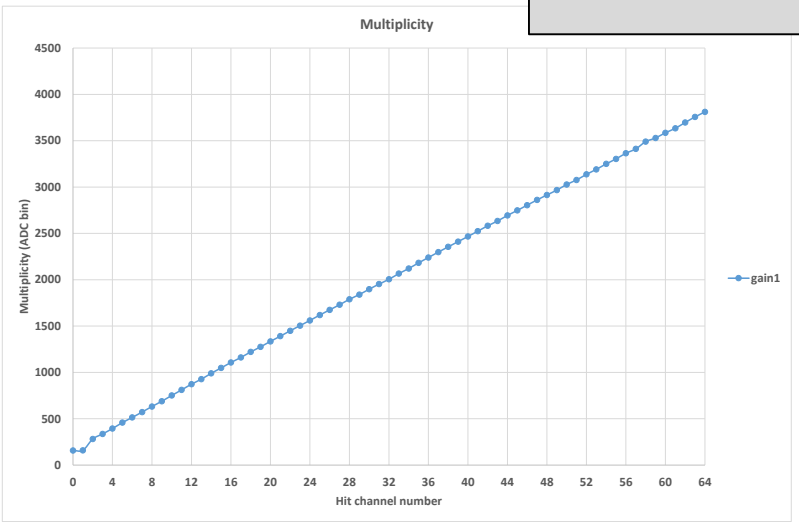
AGET		*STAGE*		
Peaking Time	**FWHM simulation**	**Peaking Time**	**FWHM simulation**	**FWHM measurement**
62 ns	120 ns	**68 ns**	118 ns	125 ns
109 ns	210 ns	**116 ns**	192 ns	240 ns
219 ns	440 ns	**180 ns**	304 ns	361 ns
266 ns	520 ns	**225 ns**	387 ns	462 ns
320 ns	610 ns	**343 ns**	604 ns	696 ns
364 ns	700 ns	**442 ns**	785 ns	904 ns
478 ns	930 ns	**541 ns**	963 ns	1,1 µs
522 ns	1,020 µs	**641 ns**	1,147 µs	1,314 µs
566 ns	1,030 µs	**739 ns**	1,315 µs	1,491 µs
604 ns	1,1 µs	**836 ns**	1,496 µs	1,7 µs
711 ns	1,31 µs	**943 ns**	1,681 µs	1,908 µs
751 ns	1,38 µs	**1039 ns**	1,86 µs	2,106 µs
817 ns	1,52 µs	**2034 ns**	3,597 µs	4,022 µs
855 ns	1,58 µs	**3985 ns**	6,898 µs	7,625 µs
963 ns	1,8 µs	**5770 ns**	9,761 µs	10,69 µs
1004 ns	1,86 µs	**7700 ns**	13,02 µs	14,21 µs

Peaking time:
interval time between 1 % to 99 % of Vmax
FWHM measurement:
mean of 18 x 64 channels

- **Multiplicity signal unity level:** x1, x2, x4 or x8 [*x1 for AGET*]

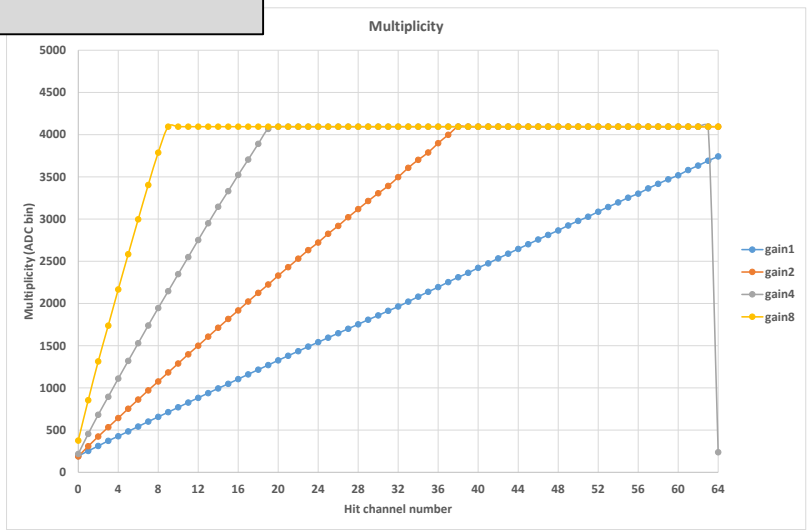


AGET



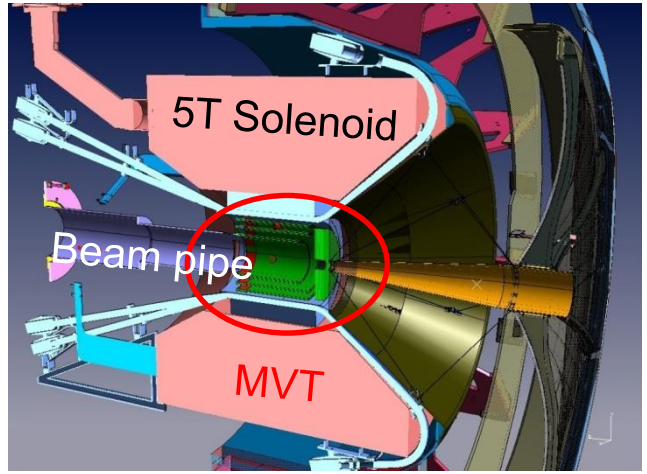
Unity level:
59 bin-ADC

STAGE



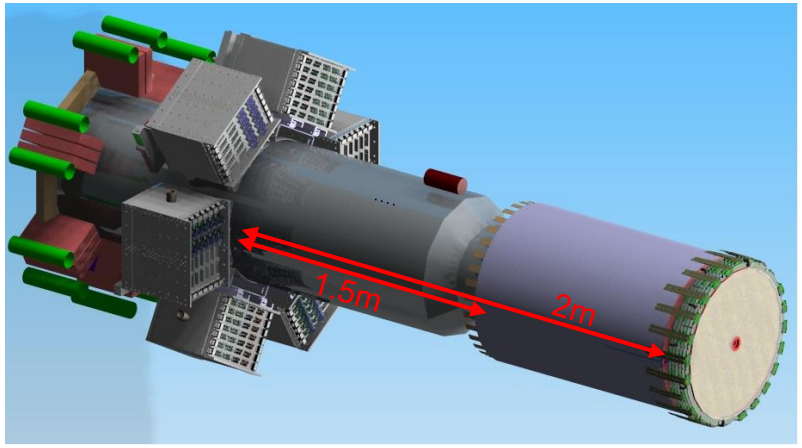
Unity level:
***STAGE n°21**: 57,6; 109; 210; 412; **STAGE n°19**: 60, 116, 212, 418*

CLAS12: Hadronic physic at Jefferson Lab (Virginia)



- **C**ebaf **L**arge **A**cceptance **S**pectrometer for **12** GeV (CEBAF upgrade)
- Electronic for the Micromegas Vertex Tracker (& detectors):
  - ***Barrel MVT*** (6 cylindrical layers): coverage: 145°-35°, 2.7 m2;~18 000 Z & C strips
  - ***Forward MVT*** (6 disks): coverage: 55°-5°, 1.3 m2;~6 000 X & Y strips

Electronic requirement

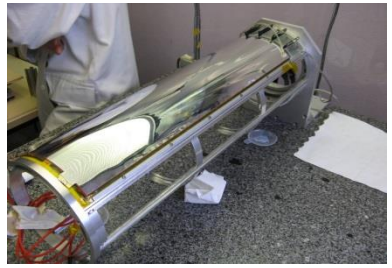


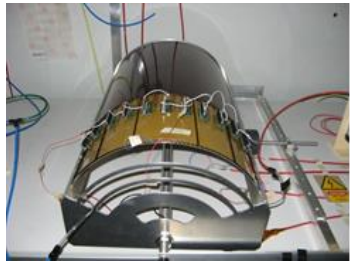
- Space constraint
- High input capacitance: 100 to 200 pF
- 20 kHz trigger rate
- 50 kHz of counting rate / channel
- Trigger latency of 16 µs
- Channel number: 18000 + 6000
- Residual Magnetic field of 1 T

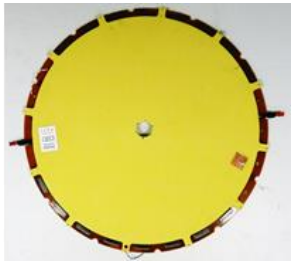
=> **NEW ASIC**: **DREAM** [**D**ead-timeless **R**ead-out **E**lectronics **A**SIC for **M**icromegas]

DREAM / AGET

- **New CSA**: to drive the input capacitance; to reduce its noise contribution
- **New SCA management**: to provide the write and read phases in parallel
- **New global architecture**: to cope with the 128-pin of the package
- **New dynamic range**: 50 fC, 100 fC, 200 fC & 600 fC
- **Discriminator threshold**: 1 common DAC (7-bit)
- **Hit channel register**: removed
- **Multiplicity**: logic signal (LVDS level; specific pads); programmable threshold (8 levels)

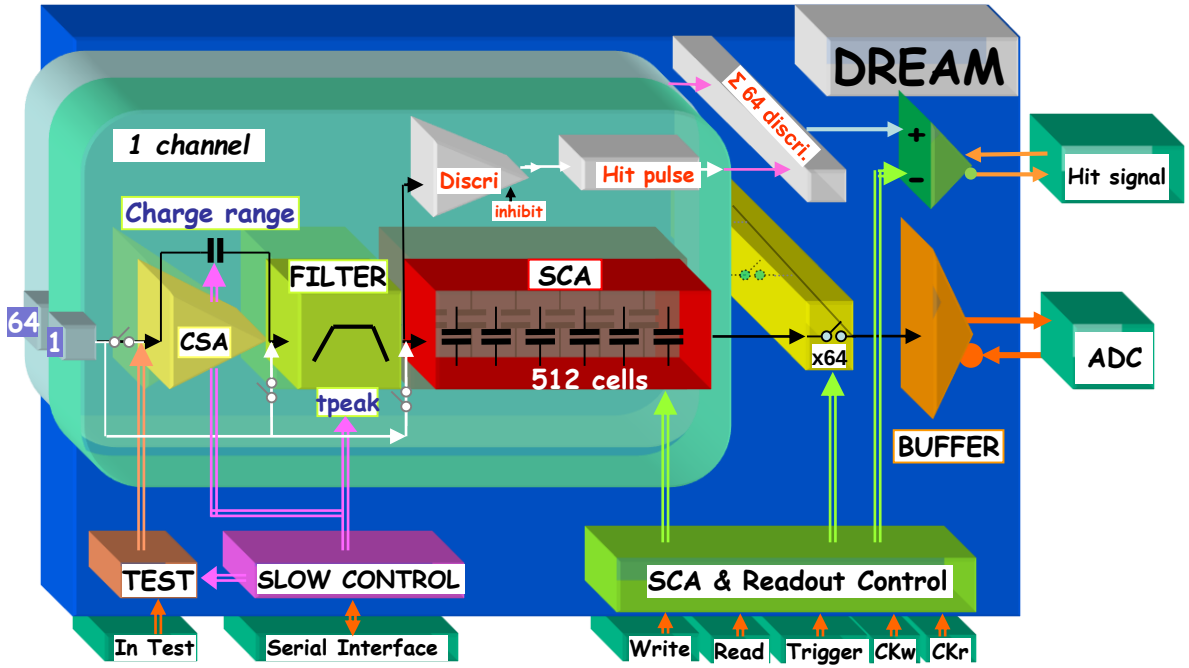






DREAM ASIC: Architecture

- **64 analog channels:** *CSA, Filter, SCA (512 cells), Discriminator*
- **Auto triggering:** discriminator + threshold (DAC)
- **Multiplicity signal:** ***LVDS level; 8 levels of multiplicity***
- **Address of the hit channel(s): no**
- **SCA readout mode:** ***triggered cells of the 64 channels***
- **4 Gains/channel:** *50 fC; 100 fC; 200 fC;600 fC*
- **16 peaking time values:** *50 ns to 0.9 µs*
- **Fsampling:** *1 MHz to 50 MHz*
- **Fread:** *20 MHz [# 33 MHz]*
- **Input current polarity:** *positive or negative*
- **Possibility to bypass the CSA**

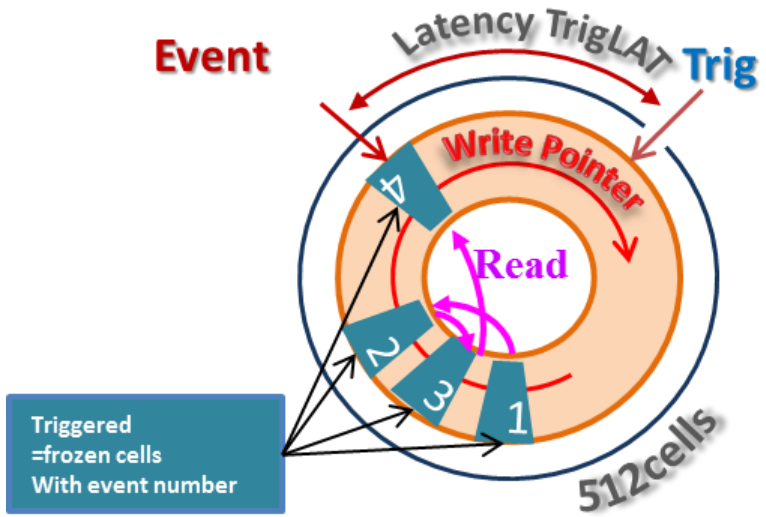


- **Sampling Phase**
  - For DREAM, the signals are continuously sampled in the SCA without interrupt

- **Trigger signal is send to the chip with a fix latency time**
  - **N** samples on all SCA channels are frozen for each triggered event

(**N** = **TRIGGER**width/**Tck**sampling; **Latency time** = Slow Control register 9-bit)

- **Readout Phase**
  - After readout, the frozen cells of the 64 channels are reused for sampling
  - Several triggered events can be stored in the SCA waiting for readout
  - Event number is joined with analog data



Requirements

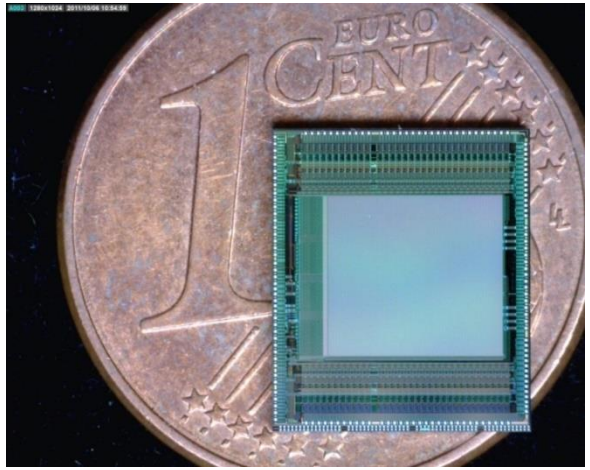
Parameter	Value
Polarity of detector signal	Negative or Positive
Channels number	64
External Preamplifier	Yes; access to the filter or SCA input (external CSA)
Charge measurement	
Input dynamic range	50 fC, 100 fC, 200 fC, 600 fC
Gain	Adjustable per channel
Output dynamic range	2V p-p (differential)
I.N.L	< 2%
Resolution	< 2500 e- (Gain: 200fC; Peaking Time: 180ns; Cinput < 200pF)
Sampling	
Peaking time	50 ns to 900 ns (16 values)
SCA time bin number	512
Sampling Frequency	1 MHz to 50 MHz
Multiplicity	
Multiplicity signal	LVDS signal; 8 multiplicity levels
Input dynamic range	5% or 17.5% of input channel input charge range
I.N.L	< 5%
Threshold value	7-bit DAC + polarity bit
Readout	
Readout frequency	20 MHz
Channel Readout mode	All channels
SCA Readout mode	Triggered columns only
Test	
calibration	1 channel among 64; 1 external test capacitor
test	1 channel among 64; internal test capacitor (1 among 4)
functional	1 to 64 channels; 1 internal test capacitor per channel
Counting rate	< 50 kHz / channel
Trigger rate	Up to 20 kHz (4 samples read/trigger)
Power consumption	< 10 mW / channel @ 3.3V

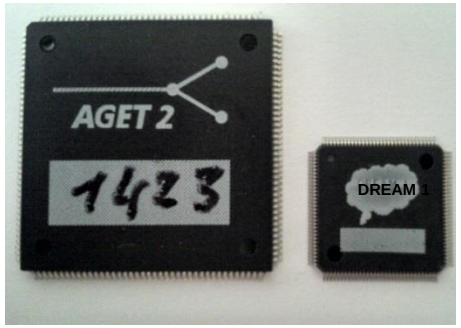
"The readout system for the Clas12 Micromegas vertex tracker"

2014 19th IEEE-NPSS Real Time Conference

Layout & Package

- Technology: AMS CMOS 0.35 µm
- Area: 8.6 x 7.5 mm^2
- Components:# 700 000
- Package: LQFP 128 (14 x 14 x 1.4 mm)





Clas12 FEU board:

AFTER family: 4 ASICs based on SCA with different gain, peaking time & Readout mode

Parameter	AFTER	AGET/STAGE	DREAM
Polarity input signal	Negative or Positive	Negative or Positive	Negative or Positive
Number of channels	72	64	64
External mode	No	access to the filter or SCA inputs	access to the filter or SCA inputs
Charge measurement			
Input dynamic range	120 fC; 240 fC; 360 fC; 600 fC	120 fC; 240 fC; 1 pC; 10 pC /channel	50 fC; 100 fC; 200 fC; 600 fC /channel
Noise (120 fC; 200ns)	370 e- + 14,6 e-/ pF	580 e- + 9 e-/ pF	500 e- + 7 e-/ pF (100 fC; 180 ns)
Gain Cdet (200pF/0)			
120 fC; tp = 230 ns	- 13%	- 13%	-0,9%
Sampling			
Peaking time value	100 ns to 2 µs (16 values)	50 ns to 1 µs/ 8µs (16 values)	50 ns to 900 ns (16 values)
SCA Time bins	511	512	512
Sampling Frequency	1 MHz to 100 MHz	1 MHz to 100 MHz	1 MHz to 50 MHz
Triggering			
Multiplicity	No	OR of 64 discri. outputs in analog level [full scale: 8, 16, 32 or 64/64]	No
Trigger LVDS	No	1/4 multiplicity level	8 multiplicity level
Threshold Range		5% or 17.5% of the dynamic range	5% or 17.5% of the dynamic range
Threshold value		(3-bit + polarity bit) common DAC + 4-bit DAC / channel	(7-bit + polarity bit) DAC common to all channels
Readout			
Readout frequency	20 MHz	25 MHz	25 MHz
Channel Readout mode	All channels	All, hit or selected	All channels
SCA cell Readout	1 to 511	1 to 512	Triggered columns only
Trigger rate			Up to 20kHz (4 samples read/trigger).
Counting rate	< 0.3 Hz / channel	< 1 kHz / channel	< 50 kHz / channel
Power consumption	< 8 mW / channel	< 10 mW / channel	< 10 mW / channel

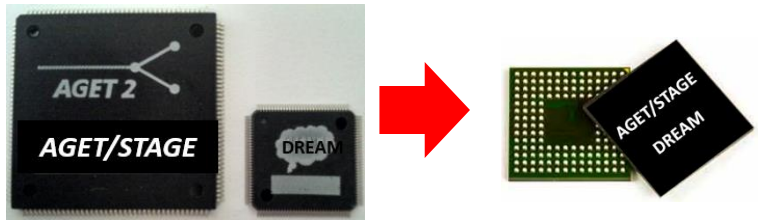
Packaging:

PLASTIC LQFP 128 (14x14x1.4 mm) & LQFP 160 (28x28x1.4 mm) are no longer available !!

Solution:

BGA 192-ball in 16x16 array with 1 mm pitch (256-ball BGA with central area without balls)

First prototype will be tested this summer



BGA Size: 17.00 X 17.00 mm;
Pitch: 1.00 mm; 192 balls