VFAT3:

an ASIC for the CMS GEM muon upgrades

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INFN – Section of Bari

RD51 Topical Workshop:

Front End Electronics for Gas Detectors

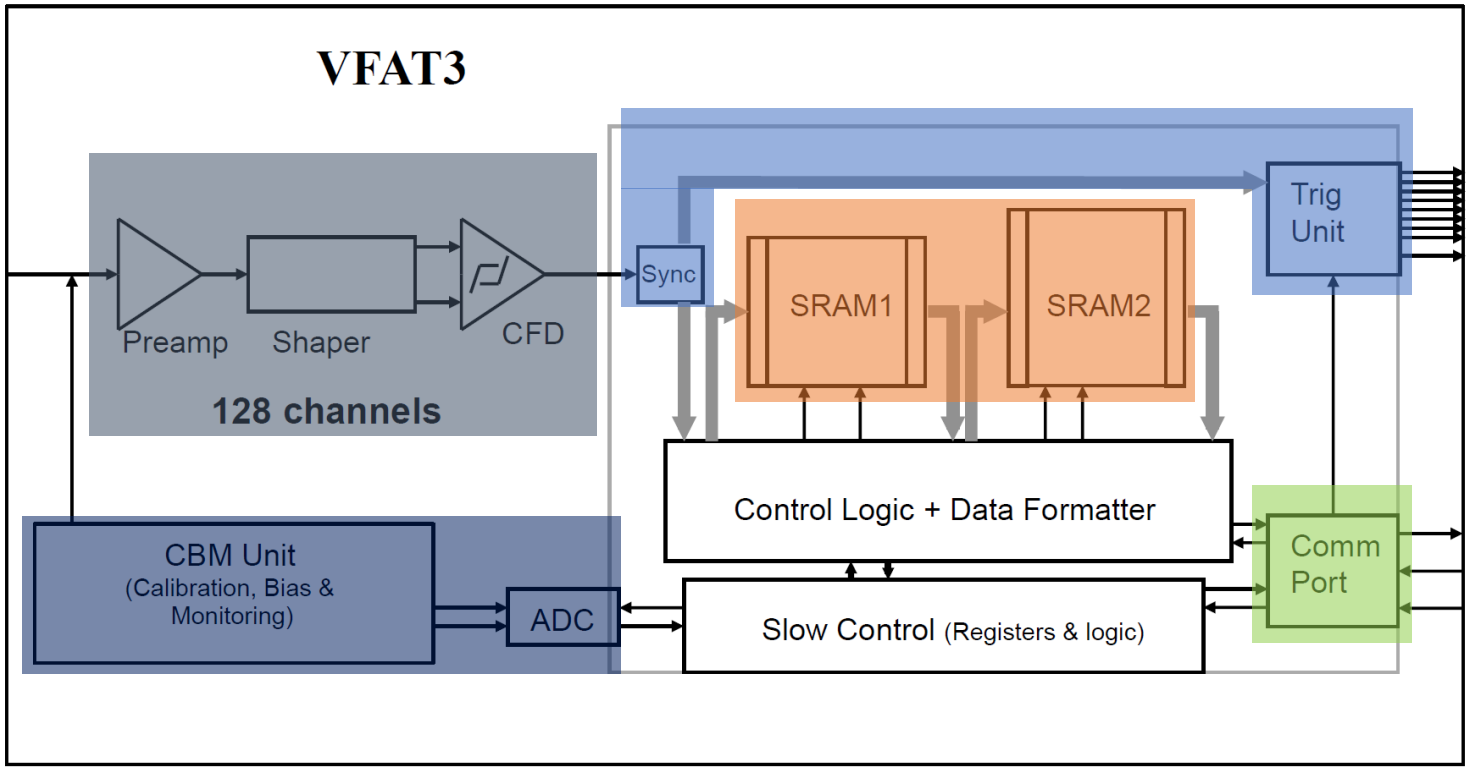
Thursday, 17 June

Outline

- VFAT3 architecture overview
- CBM: calibration, bias and monitoring
- The analog channel: front-end & costant fraction discriminator
- The back-end
- VFAT3 application: GE2/1 chamber

VFAT3 architecture overview

- **VFAT3 trigger and tracking chip designed according to the CMS Phase 2 requirements.**



128 analogue channels:
- Optimized for detector capacitance from 20 pF to 80 pF
- Programmable gain, peaking time and signal polarity
- Max channel hit rate = 2 MHz
- Additional input protections (2 different version of VFAT3)

Trigger path:
- Fixed latency, synchronuos with the LHC 40 MHz clock
- 8 SLVS pairs operating at 320 MHz

Data path:
- Full granularity after LV1a + time tag
- LV1a latency from 25 ns to 26.5 μs
- Max LV1a rate beyond 1 MHz

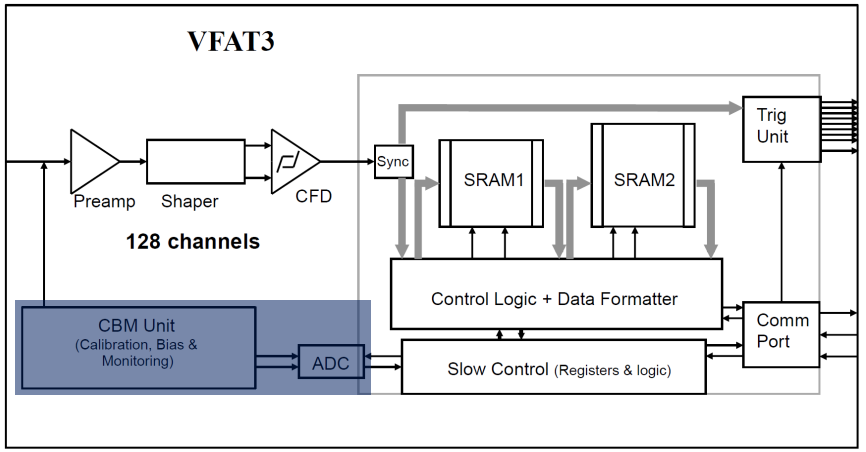
Calibration, bias and monitoring:
- Fine tuning of the bias point for the analogue section
- Channel calibration
- Monitoring of the internal bias currents and voltage references
- Internal and external temperature monitoring

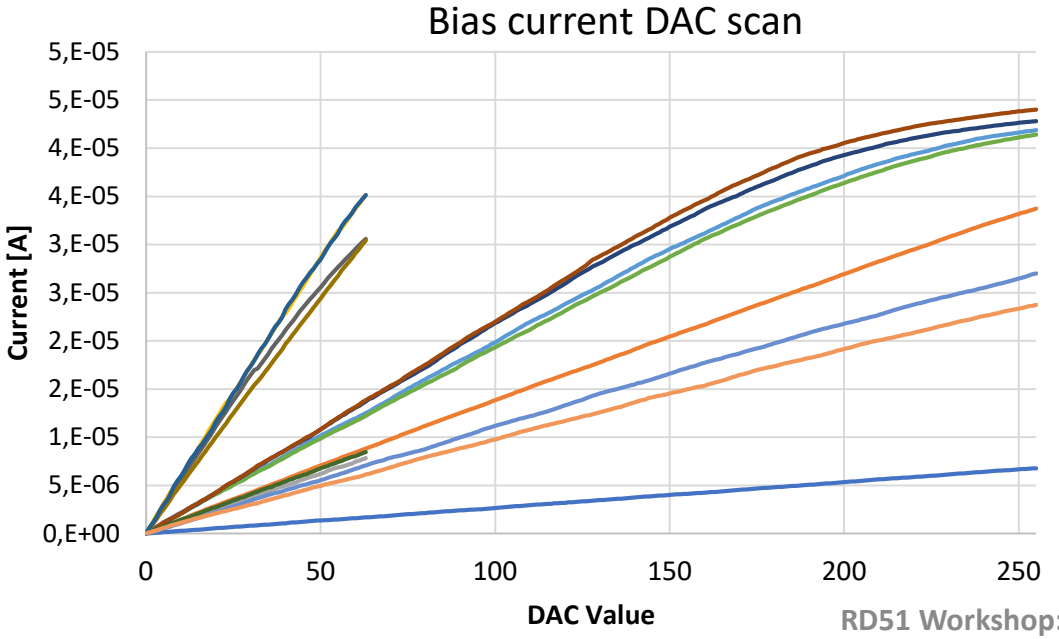
Comm Port:
- Direct compatibility with GBTx and LpGBT
- Bi-directional communication of control commands, slow control and data readout through a single port to the GBT.

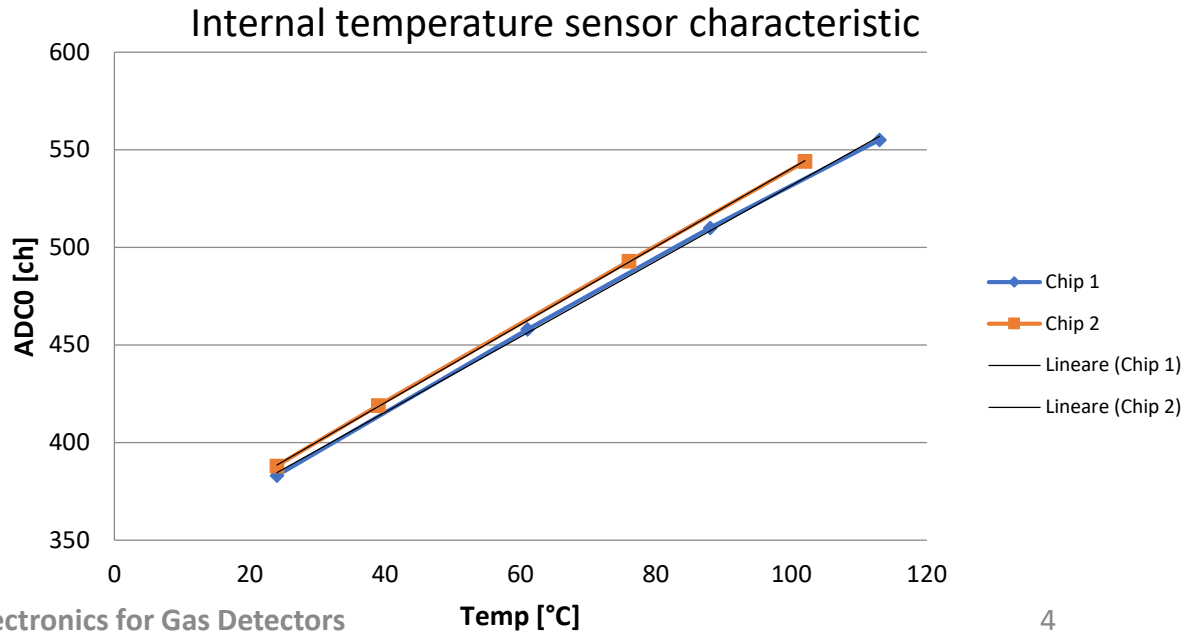
VFAT3 Calibration, Bias & Monitoring (CBM)

VFAT3 CMB:

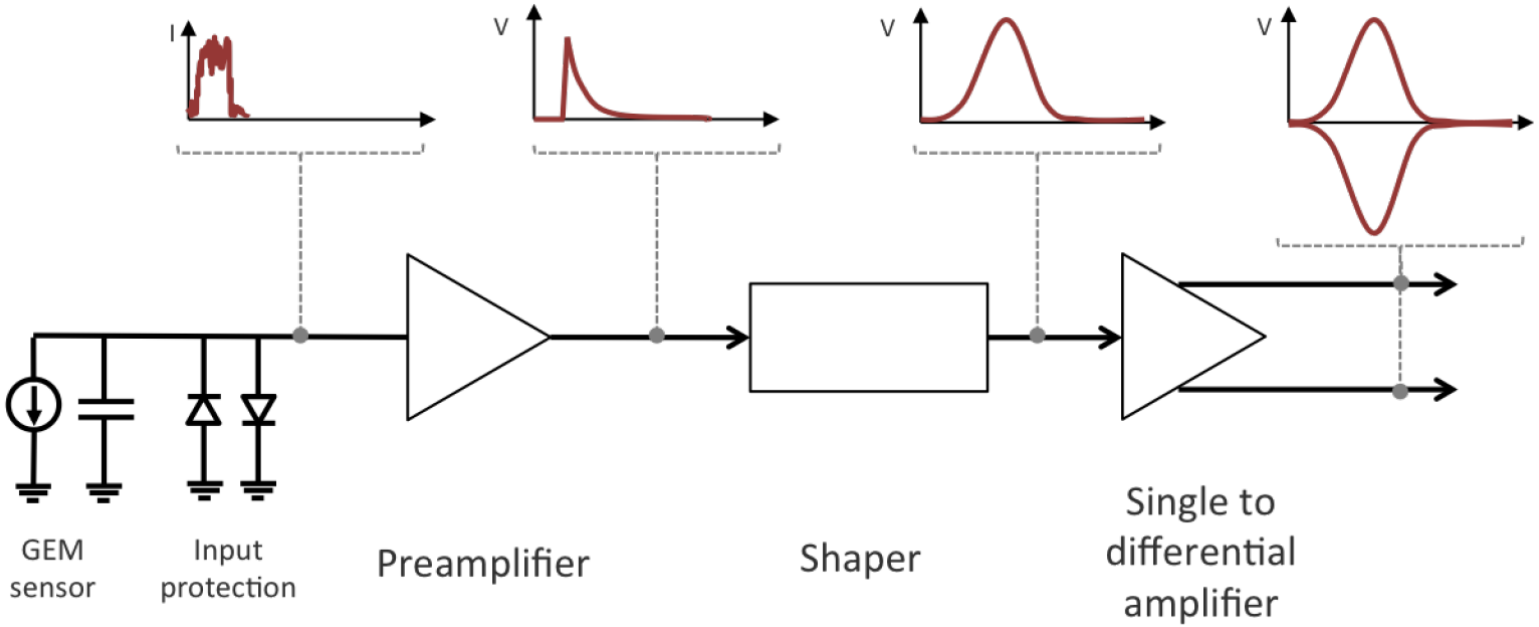
- Calibration block:
  - Gain, noise measurements and channel equalization
  - Voltage and current injection: programmable injection charge, polarity, phase and pulse duration (only for current)
- Bias block:
  - Provides precise and adjustable current and voltage bias references
  - References stable with temperature and power supply independent
  - 6 bit and 8 bit DACs to compensate process variations and degradation due to time and radiation
- Monitoring block:
  - Measurement of the internal voltage and current bias references
  - 2 internal 10 bit ADCs
  - Internal and external temperature monitoring

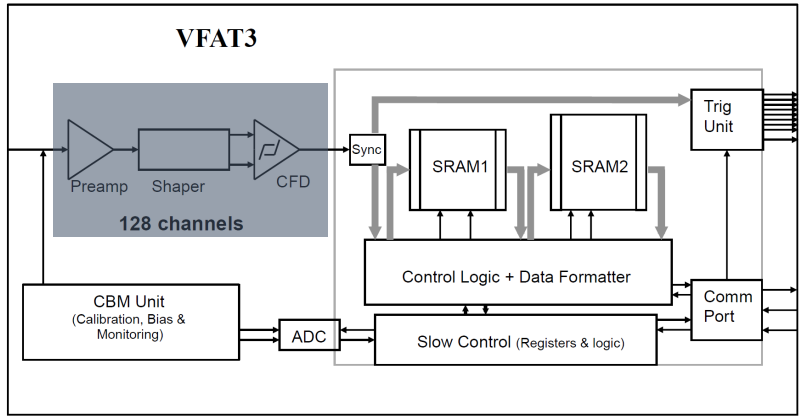






VFAT3 analogue channel: front-end



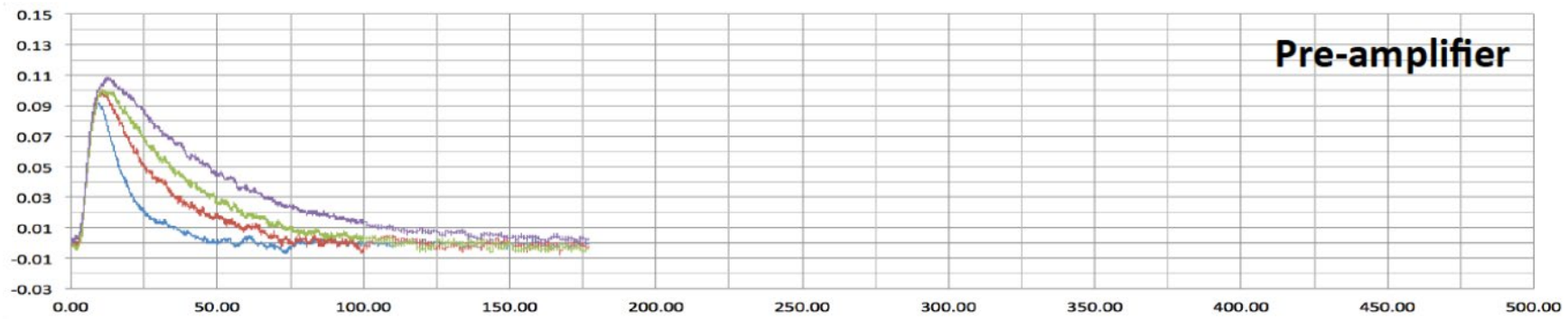


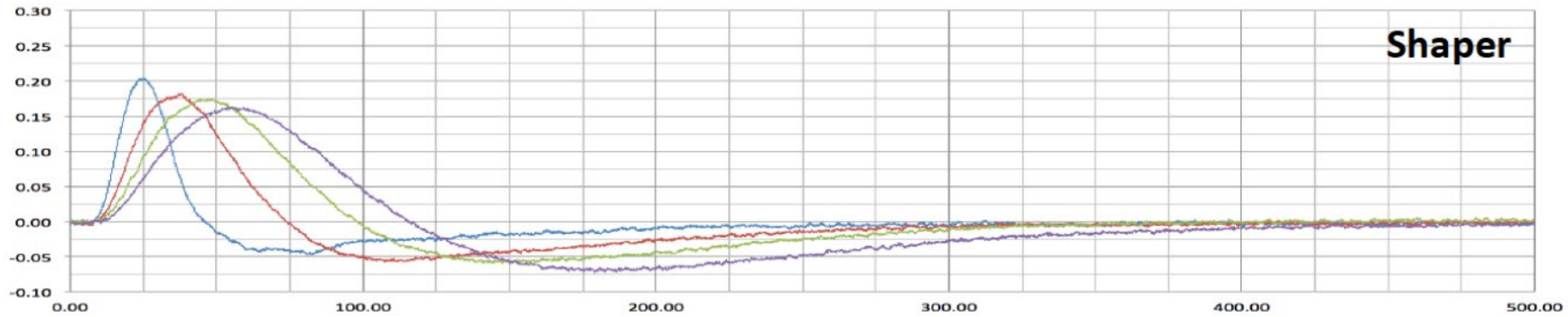
Gain Setting	Sensitivity [mV/fC]	Linear Range [fC]	ENC
HG	48	9.5	620 e- + 33 e-/pF
MG	16	28	1072 e- + 30 e-/pF
LG	8	55	1595 e- + 25 e-/pF

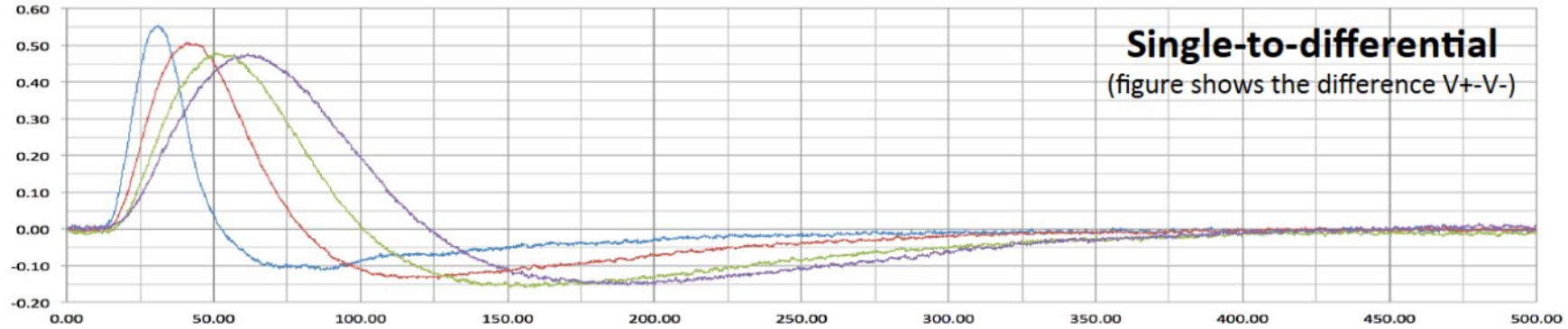
VFAT3 analogue front-end:

- Programmable gain
- Peaking time: 15 ns, 25 ns, 35 ns, 45 ns
- Input capacitance range: 20 – 80 pF
- Two different versions of input protection
  - VFAT3b_prot: resistor + diode
  - VFAT3b_noprot: diode

VFAT3 test-channel measurements



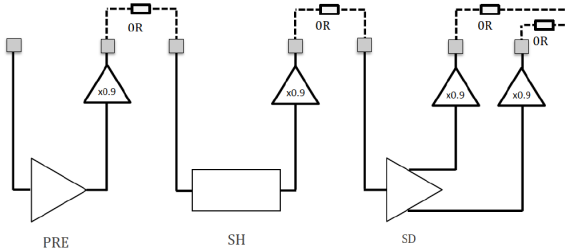




VFAT3 test channel:

- VFAT3 has 128 analog channels plus one for test purposes.
- The test channel has buffers to monitor the output voltage of each stage of the channel

Test Channel Architecture

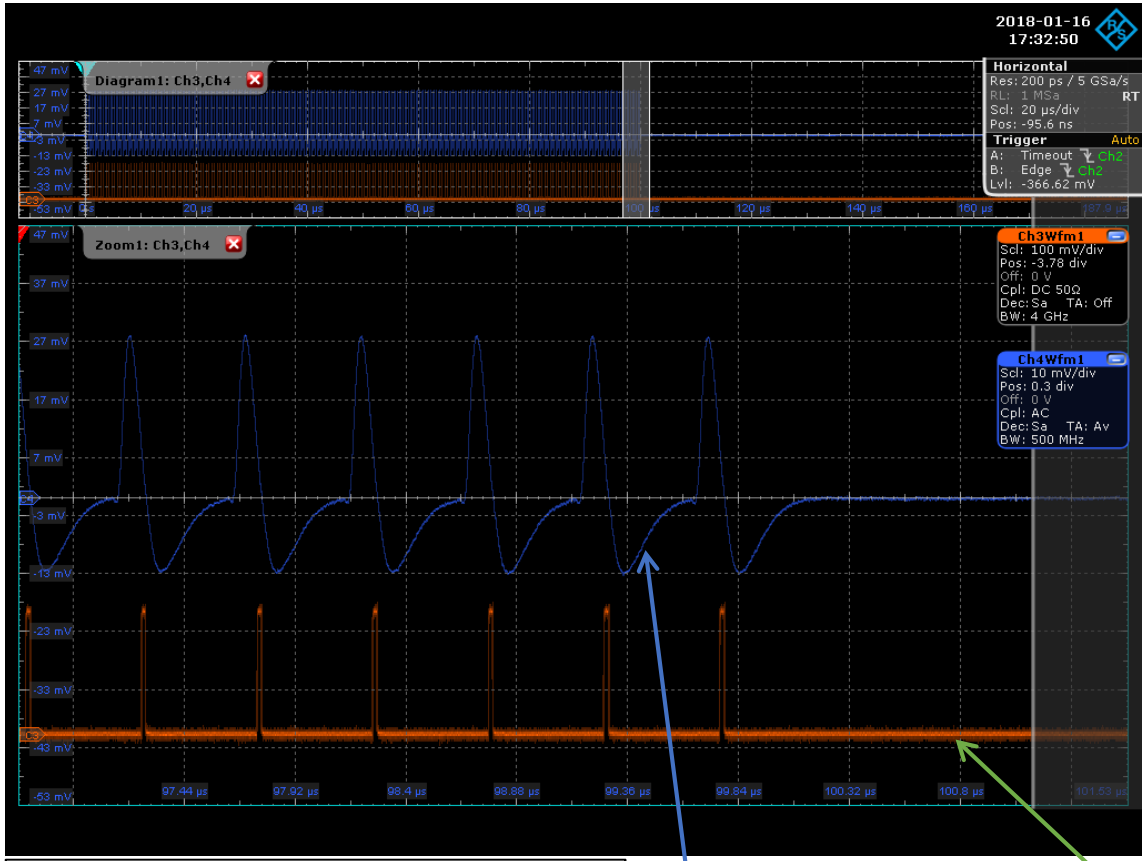


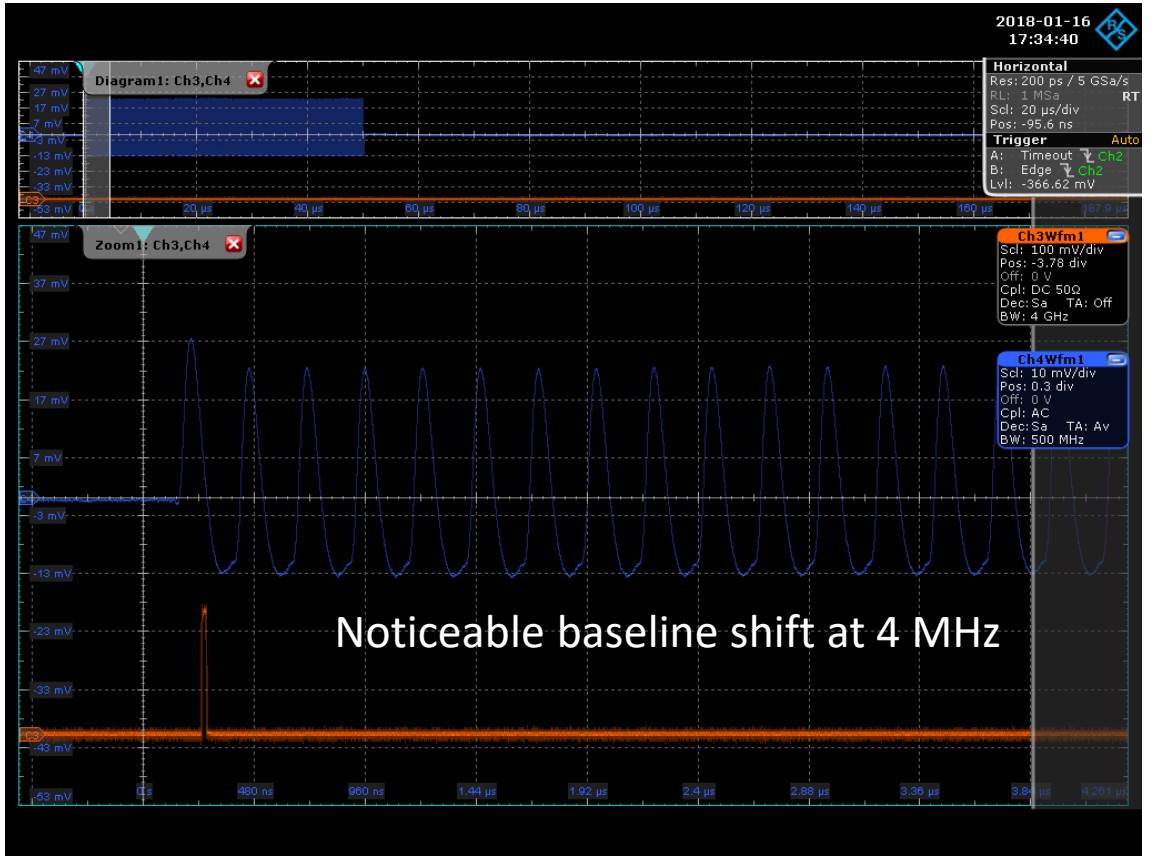
Measurements settings:

- HG mode
- 10 fC input charge

Baseline recovery within 500 ns, max channel hit rate up to 2 MHz

VFAT3 max rate measurement





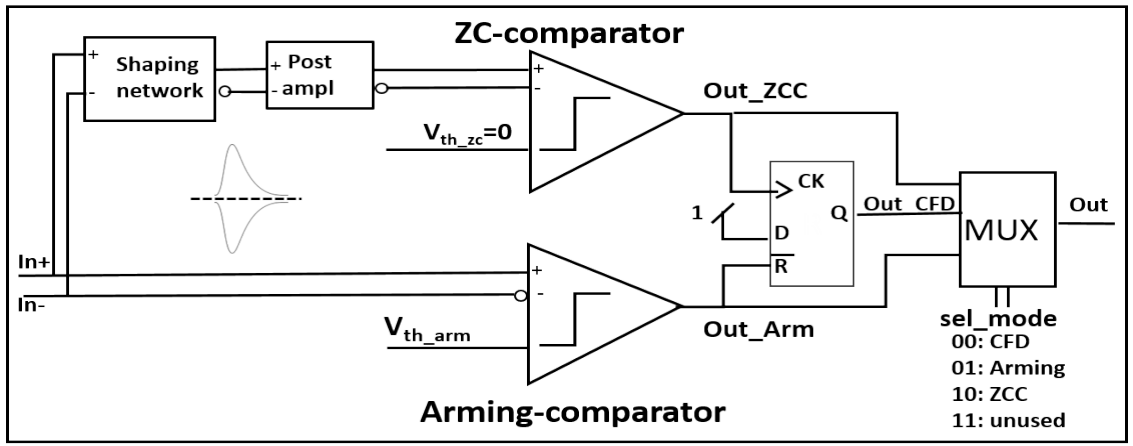
Medium Gain, max peak time
Ipulse: 12 fC @ 25 ns
Threshold: ~8 fC
Rate: 2 MHz → T=500 ns
Burst: 200 pulses

CFD input

CFD output

Medium Gain, max peak time
Ipulse: 12 fC @ 25 ns
Threshold: ~8 fC
Rate: 4 MHz → T=250 ns
Burst: 200 pulses

Analogue channel: Constant-Fraction Discriminator

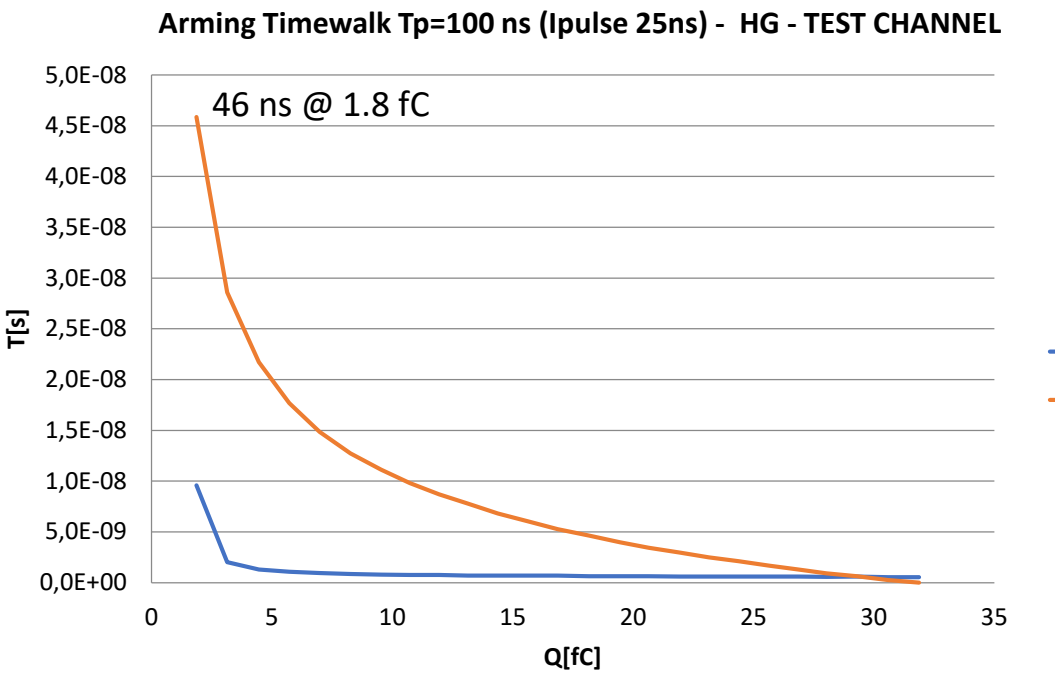


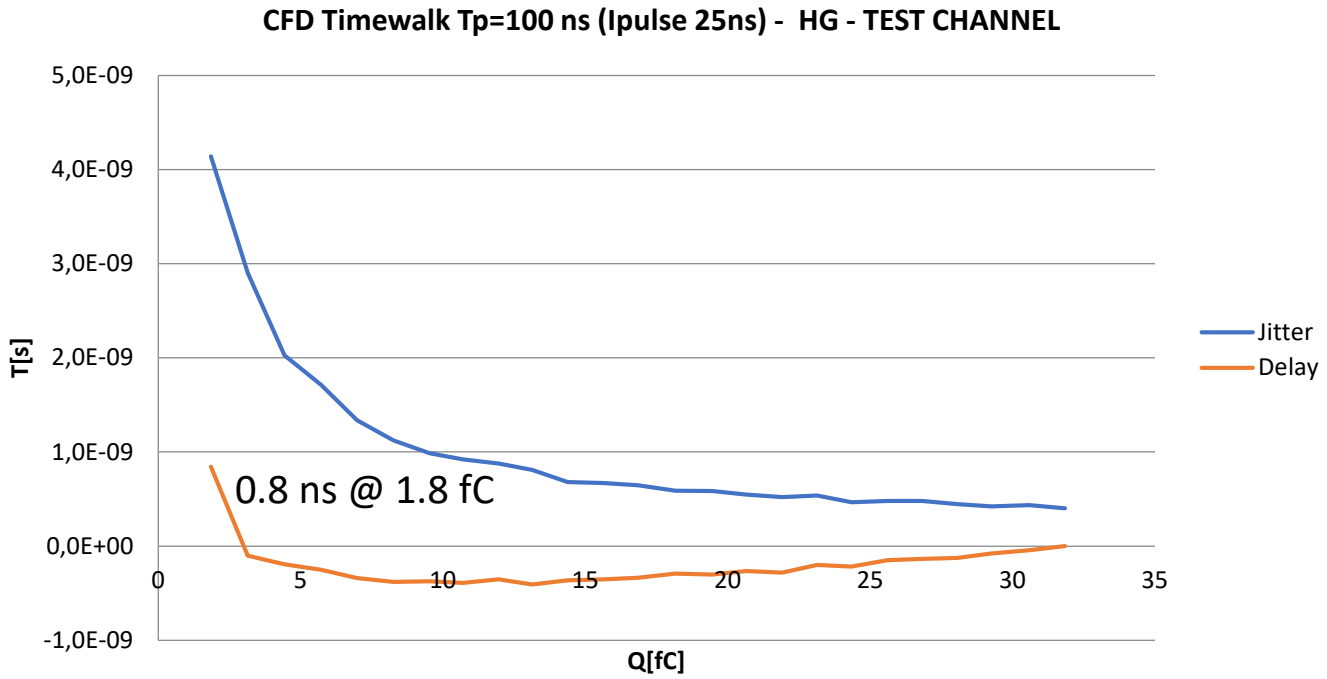
CFD:

- Arming comparator: input signal validation
- Zero-crossing comparator: provides amplitude-independent information about arrival time of an event

CFD thresholds:

- 2 global 8 bit DACs (ARM & ZCC)
- 2 local 6 bit DACs (ARM & ZCC) for channel equalization





Back-end: fixed and programmable latency paths

Fixed latency path

- provides fast hit information which is synchronous with the LHC 40 MHz clock
- 8 SLVS differential pairs running @ 320 MHz
- 1 SLVS differential pair for the Start of Transmission
- Choice of Single or Double Data Rate (SDR or DDR)

SDR: FAST-OR information, 8 x 8bits/bx = 64bits/bx for 128 channels, granularity 2 ch, 2.56 Gbps total bandwidth

DDR: Full channel information, 8 x 16bits/bx = 128bits/bx for 128 channels, granularity 1 ch, 5.12 Gbps bandwidth

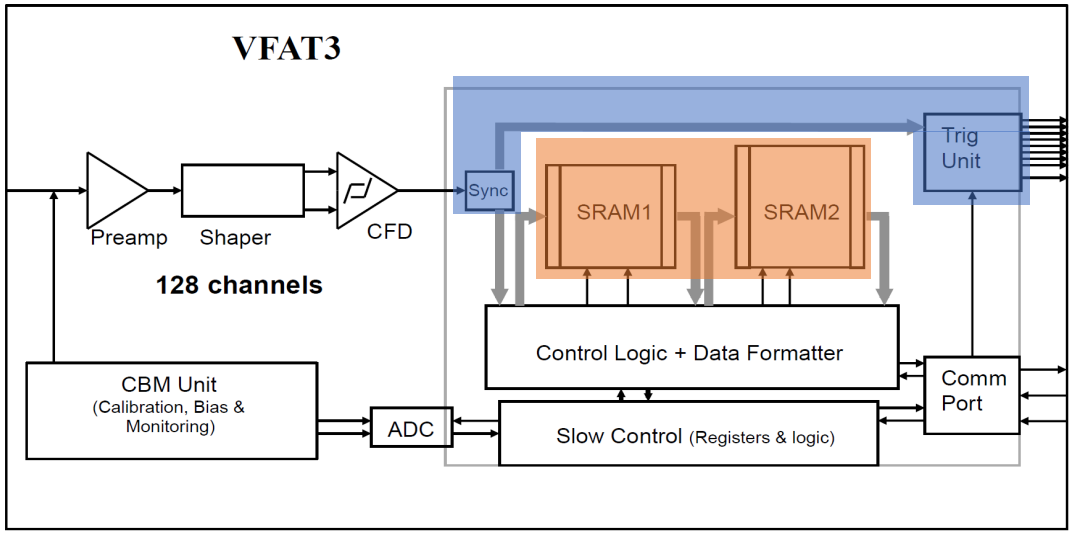
Data Path

SRAM1:

- Circular buffer sampling alla channel at 40 MHz
- Data size: 128 x 1024 bits -> memory depth 25.6 us
- LV1A trigger latency programmable from 1 bx to 1024 bx

SRAM2:

- FIFO storing triggered events plus their time tag
- Data size: 176 x 512 bits
- 512 triggered events can be simultaneously stored



VFAT3 Data Formatter & Communication Port

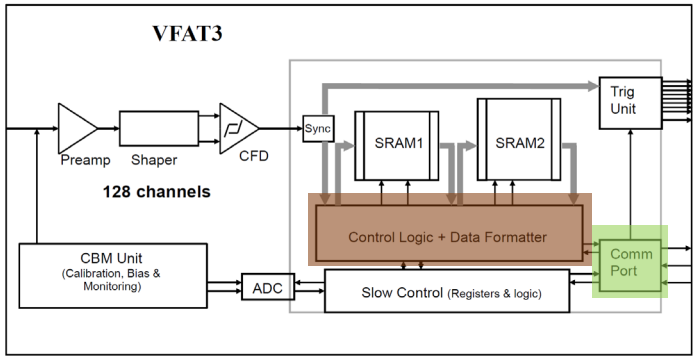
General Data Packet Structure

- Header
- Time Tags
- Data Field
- CRC

4 different versions of Header:
lossless data or zero suppression and SRAM2 half full

2 time tags:
bunch counter (BC) and event counter (EV), programmable number of bits

SPZS for data field, several options



SPZS (Sequential Partial Zero Suppression) Data Packets

Registers DT	SZP	SZD	Data Packet	No. Bits	Comment
1	0	0	Header I / Header IW	8	Basic SPZS data packet
			EC+BC / EC / BC	8 - 48	Size depends on Partitions/P16
			Data	16 - 144	
			CRC	16	
1	0	1	Header I / Header IW	8	Basic SPZS data packet
			EC+BC / EC / BC	8 - 48	Size depends on TT, Ecb, BCb
			Data	16 - 144	Size depends on Partitions/P16
			CRC	16	
			Header II / Header IIW	8	Zero Suppressed
			EC+BC / EC / BC	8 - 48	Size depends on Ecb
			CRC	16	
1	1	x	Header I / Header IW	8	Basic SPZS data packet
			EC+BC / EC / BC	8 - 48	Size depends on TT, Ecb, BCb
			Data	16 - 144	Size depends on Partitions/P16
			CRC	16	
			Header II / Header IIW	8	Zero Suppressed

Relevant registers

ECb	Size(EC)	
00	8	default
01	16	
10	24	
11	(8)	

BCb	Size(BC)	
0	16	default
1	24	

TT	EC+BC / EC / BC	
00	EC + BC	default
01	EC	
10	BC	
11	(EC + BC)	

Partitions	No. Partitions
0000	1
0001	2
0010	3
0011	4
0100	5
0101	6
0110	7
0111	8
1000	9
1001	10
1010	11
1011	12
1100	13
1101	14
1110	15
1111	16

P16	Comment	
0	Send numbers of partitions accodring to **Partitions** register	default
1	Send only high level information (16bit)	

Communication Port

- SLVS e-link at 320 MHz
- GBT compatible
- All communication: commands, data and slow control
- Generate the internal 40 MHz clock
- Separates the slow control and data
- Two operation modes:
  - SC only (DF data is not transmitted)
  - Run mode: DF data has the priority

VFAT3 irradiation perfomances

TID

- Facility at CERN
- X-ray, dose rate 1.84 Mrad/h

30 Mrad (@1.8 Mrad/h) is the limit for the chip to communicate and be alive.

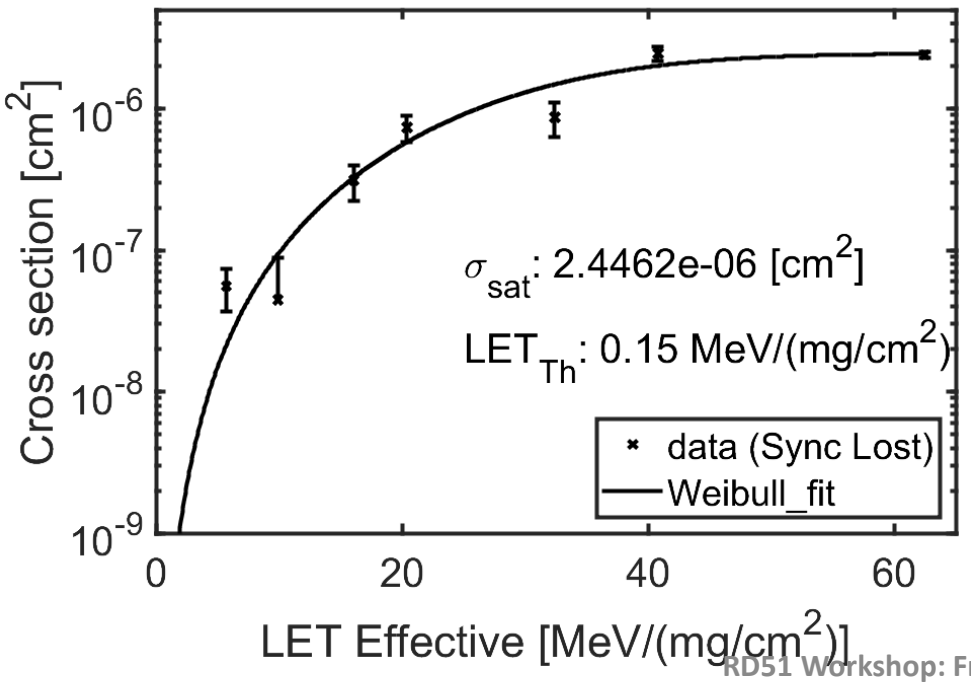
SEU

- UCLouvain cyclotron
- 9 ions

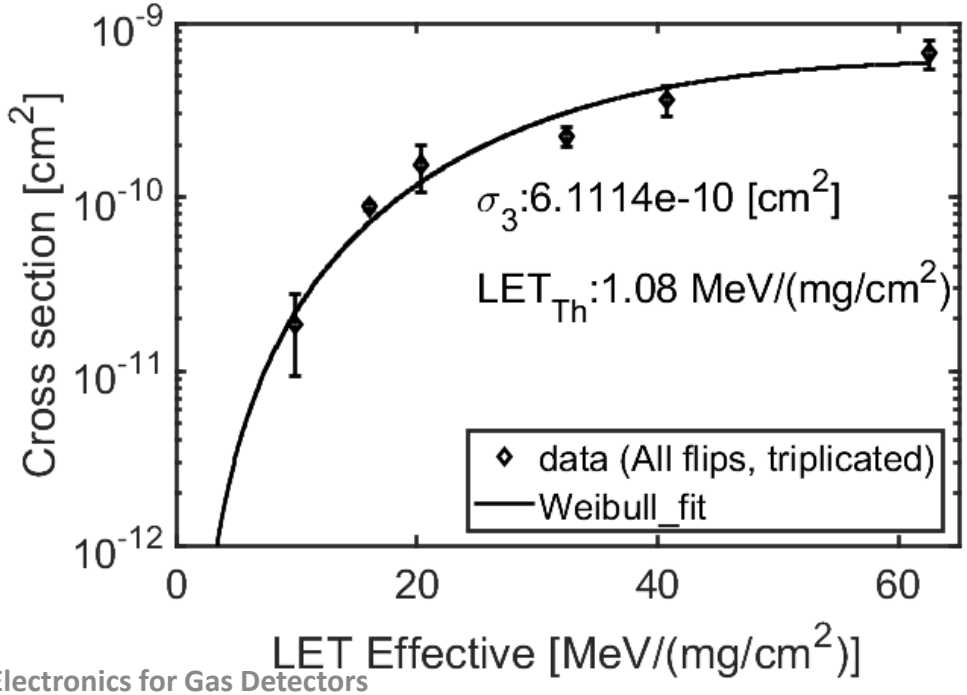
Two different effects observed due to SEUs:

- Synchronization Lost (Single Event Functional Interrupt, SEFI)
- Slow Control registers bit flips

SEU cross -sections for SEFI

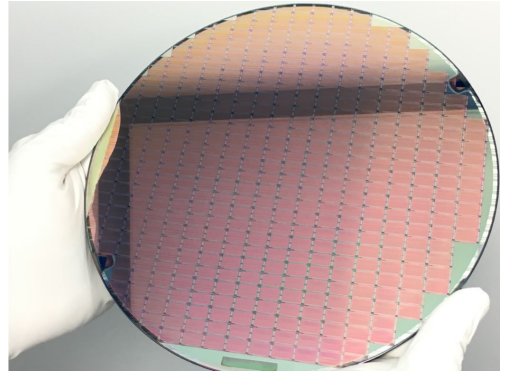


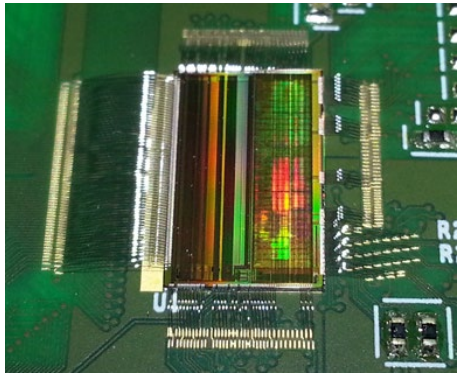
SEU cross-section (Slow Control registers)



VFAT3 key features

Feature	Parameter	Notes
N° of channels	128	129 incl. Test channel
Signal charge polaity	+ & -	
Programmable Gain & shaping time	Yes	3 gains, 4 peaking times
Comparator	Arming + CFD	CFD for time walk reduction
Rate per Channel	Up t o2 MHz	
Trigger Path granularity	FAST-OR 2 channels, Full granularity	8 SLVD outputs
Data Path LV1A programmable latency	25 ns to 25.6 us	
Consecutive triggers	Yes	Allow multiple time slot readout per LV1A
Max LV1A rate	Up to 2 MHz	
Zero suppression	Yes	Many options for ZS
Compatibility with GBTx and LpGBT	Yes	Includes HDLC addressing
Calibration, Bias and monitoring	Integrated	Internal ADCs
Channel threshold trimmable	Yes	Channel equalization
Temperature measurement	Yes	Internal and external
Radiation tolerance	Up to 30 Mrad	Triplication and SEL tolerance design
Power consumption	250 mW in run mode, 150 mW in Sleep Mode	
Technology node	CMOS 130 nm	





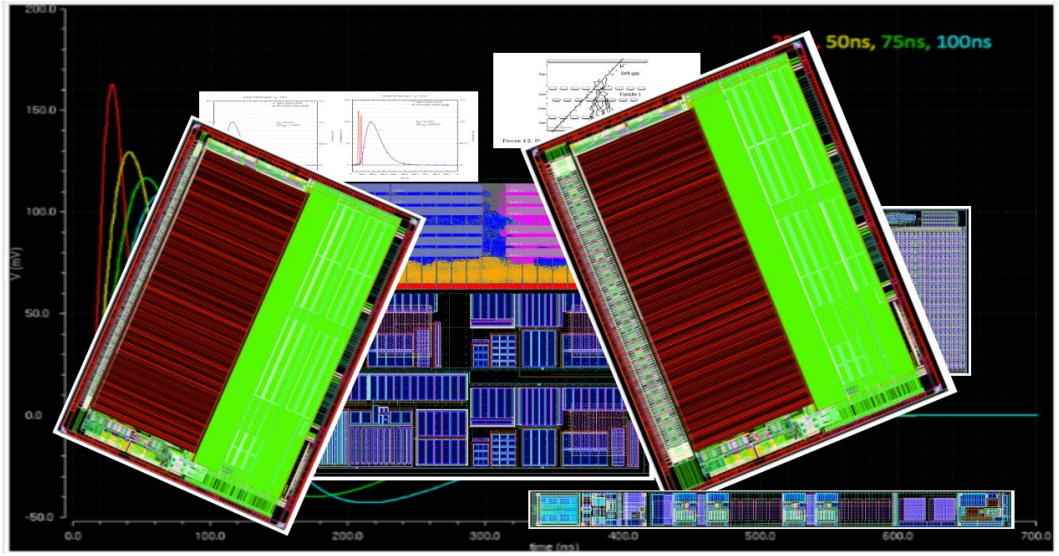
VFAT3 team

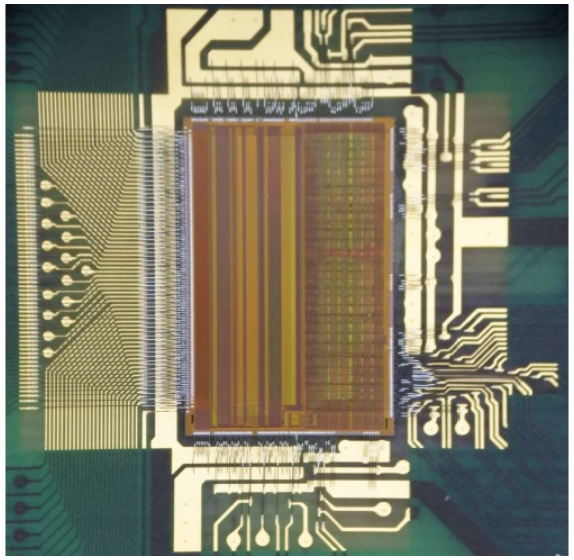
Design:

- CERN**:** P.Aspell, M.Dabrowski
- INFN: F. Loddo, G. De Robertis, F. Licciulli
- LUT: H.Petrow
- AGH: M. Idzik (AGH coordination)

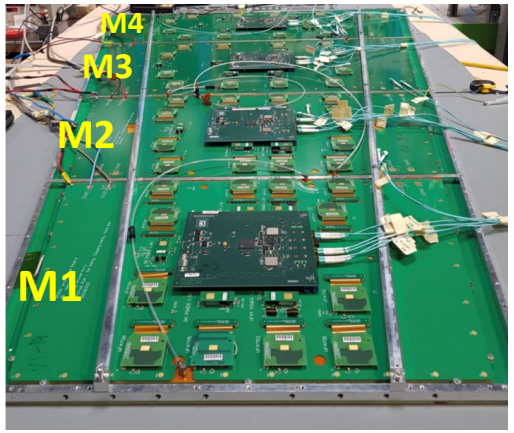
Measurement:

- CERN: A. Irshad
- INFN: F. Loddo, G. De Robertis, F. Licciulli
- NCP: M.Ali, M.Hayat
- UCLA: C. Bravo



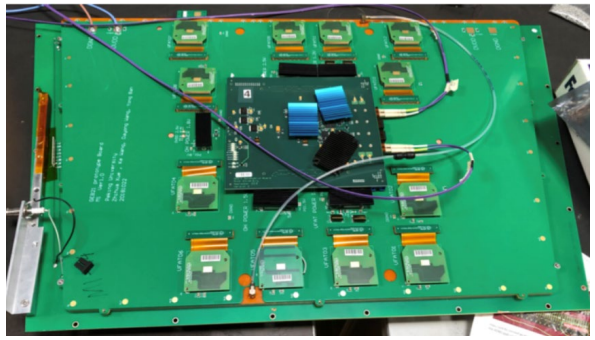


VFAT3 application: GE2/1 chamber



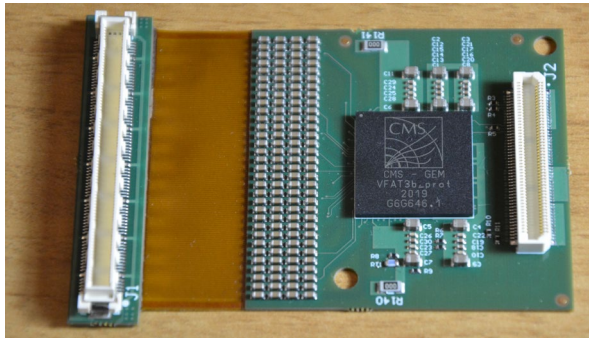
GE2/1 chamber:

- composed by 4 modules



GE2/1 module:

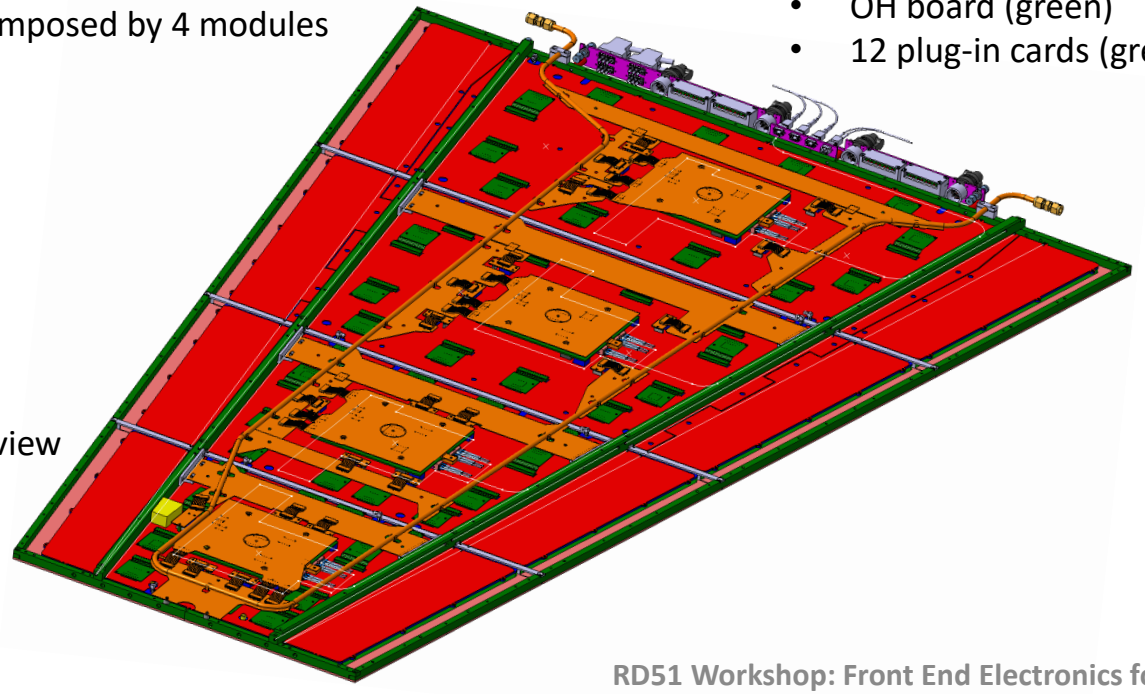
- GEM detector
- GEB board (red)
- OH board (green)
- 12 plug-in cards (green)

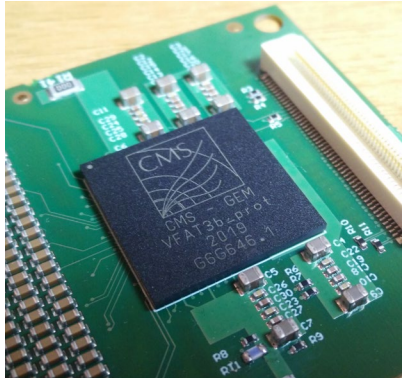


Plug-in card:

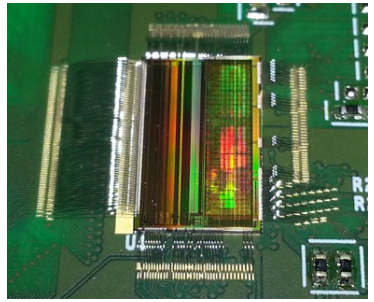
- Packaged VFAT3b
- Channel input protections

Full chamber view





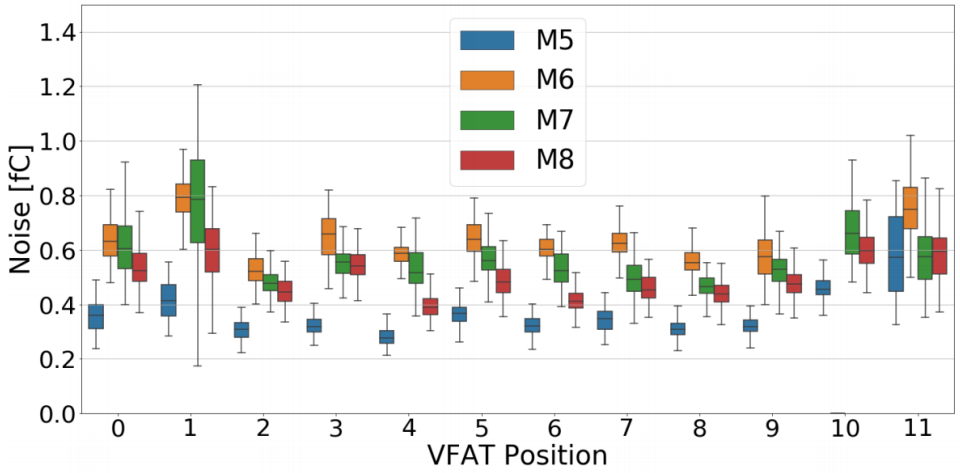
Packaged VFAT3b



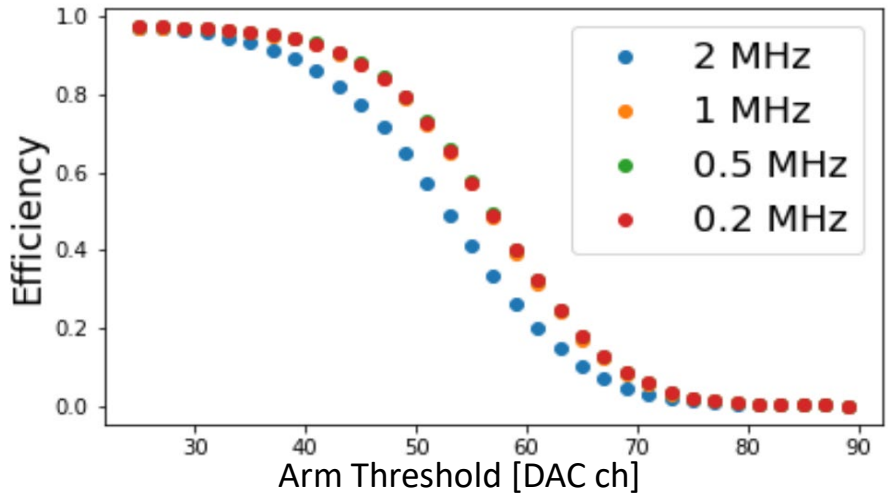
VFAT3b

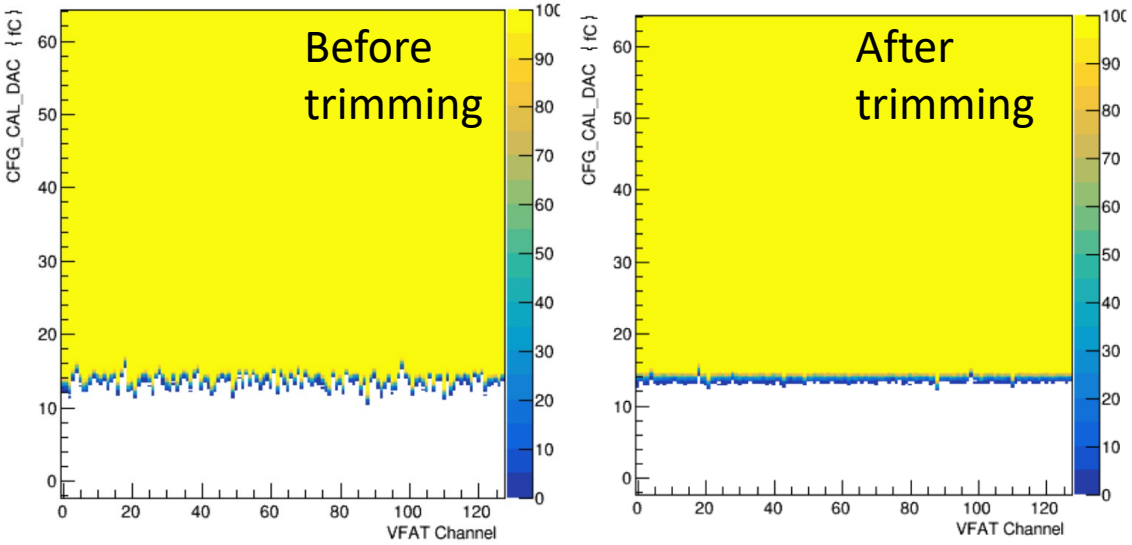
VFAT3 measurements with GE2/1 chamber

Noise measurements for different modules

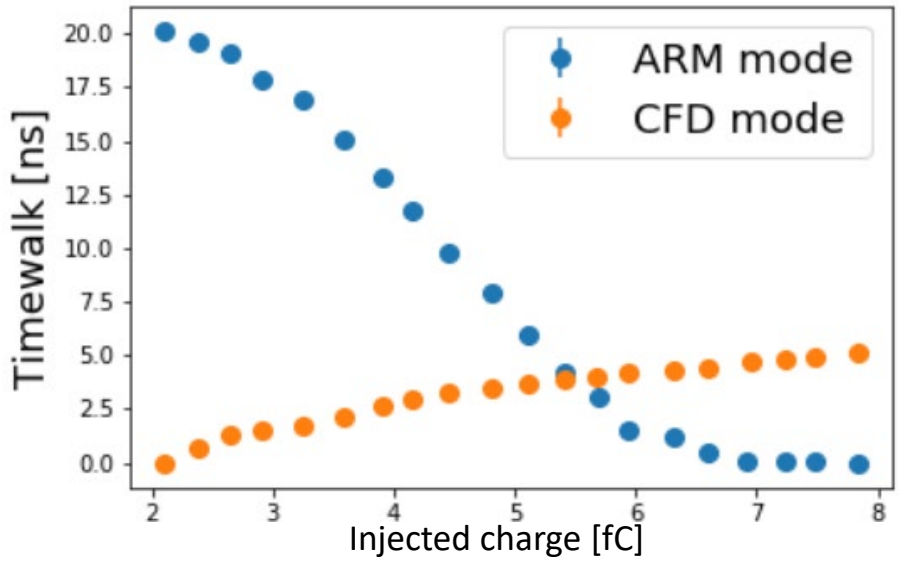


Max rate measurements





Time walk measurements



Single VFAT3 channel equalization

Plots from Piet Everaerts's presentation for GE2/1 ESR

A new ASIC development for gaseous detector

F. Licciulli

INFN – Section of Bari

RD51 Topical Workshop: Front End Electronics for Gas Detectors

Thursday, 17 June

Outline

- ASIC specifications
- ASIC and analogue channel architecture
- Analogue channel preliminary simulations

A new ASIC for gaseous detectors

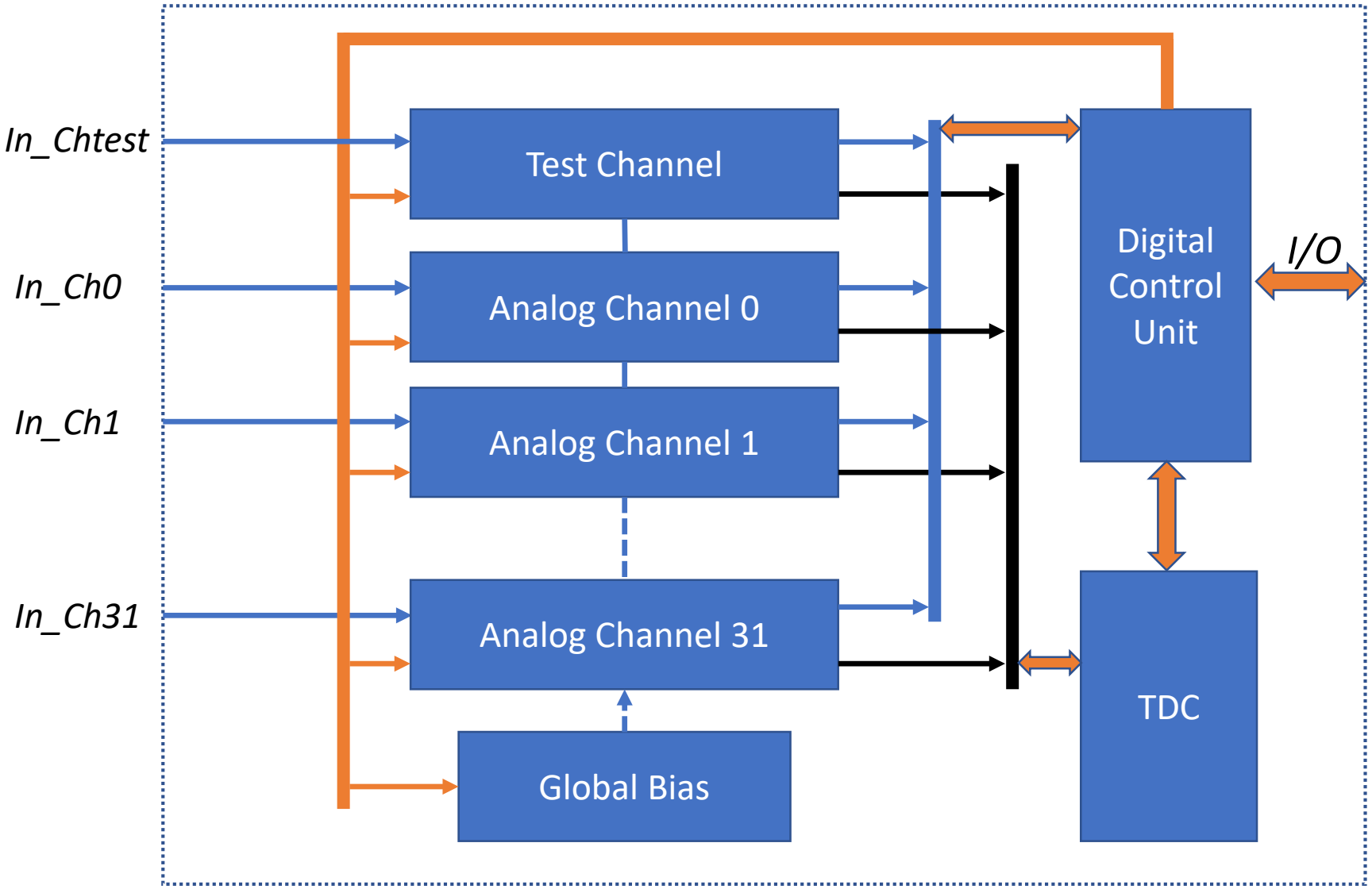
A new ASIC in the AIDA-INNOVA project

Initial specs:

- **Target detectors: FTM (Fast Timing MPGD), MPGD and RPC**
- **Technology: CMOS 130 nm**
- **32 channels**
  - Programmable polarity, gain and peaking time
  - Charge and time measurement
  - Time measurement using 100 ps TDC
- **Calibration, Bias and Monitoring**
  - ➢ Charge injection calibration
  - ➢ Programmable biases
  - ➢ Bias currents and voltage references monitoring

- **320 Mbps serial link, LpGBT compatible**
- **Power supply 1.2 V**
- **Radiation hardness: up to 100 Mrad**

ASIC Architecture



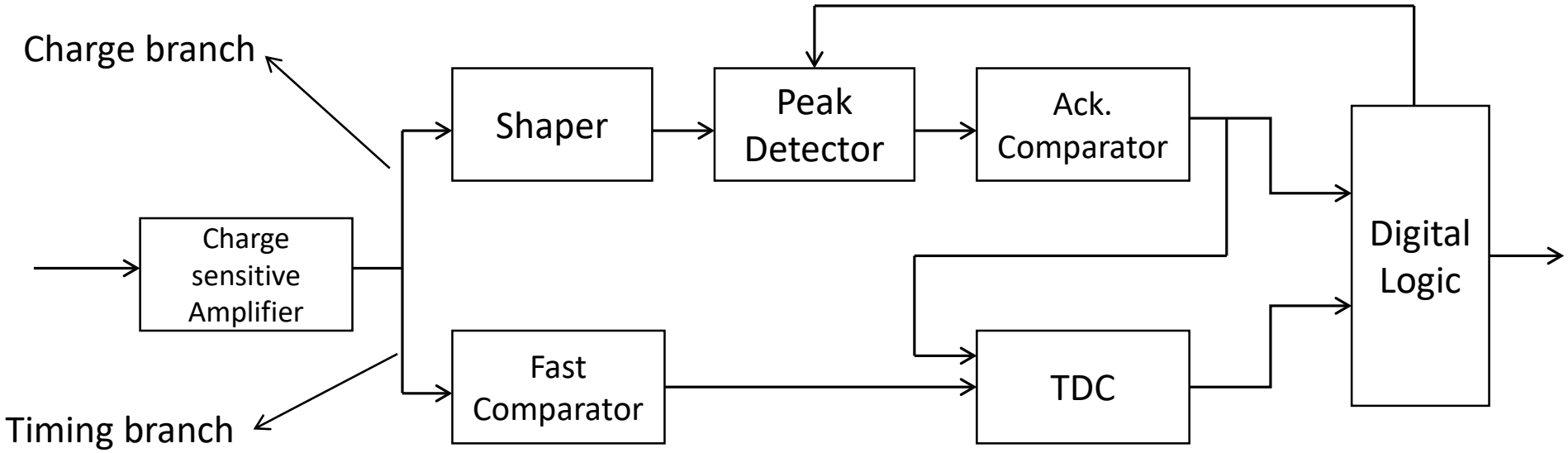
Analog Section:

- 32 Front-end channels:
  - Fast output: designed for timing measurements
  - Slow output: input signal acknowledgement and charge measurement
- Global Bias:
  - temperature and power supply independent
  - internal calibration
  - bias monitoring

Digital Section:

- Control Unit:
  - 320 MHz SLVS I/O link
  - Channel & Global bias adj. bits
  - TDC control

Channel architecture



Timing branch:

- Measures the arrival time of the input signal with low jitter

CSA settings:

- Input signal polarity: positive & negative
- Gain: High ≈ 50mV/fC, Low ≈ 10 mV/fC
- Recovery time: adjustable

CSA features (High gain & 15 pF input capacitance):

- Peaking time ≈ 8ns
- Time jitter s ≈ 350ps with 6180e- (1fC input charge)
- ENC ≈ 18.5e-/pF*Cin + 227.5e- (505e- Cin=15pF)

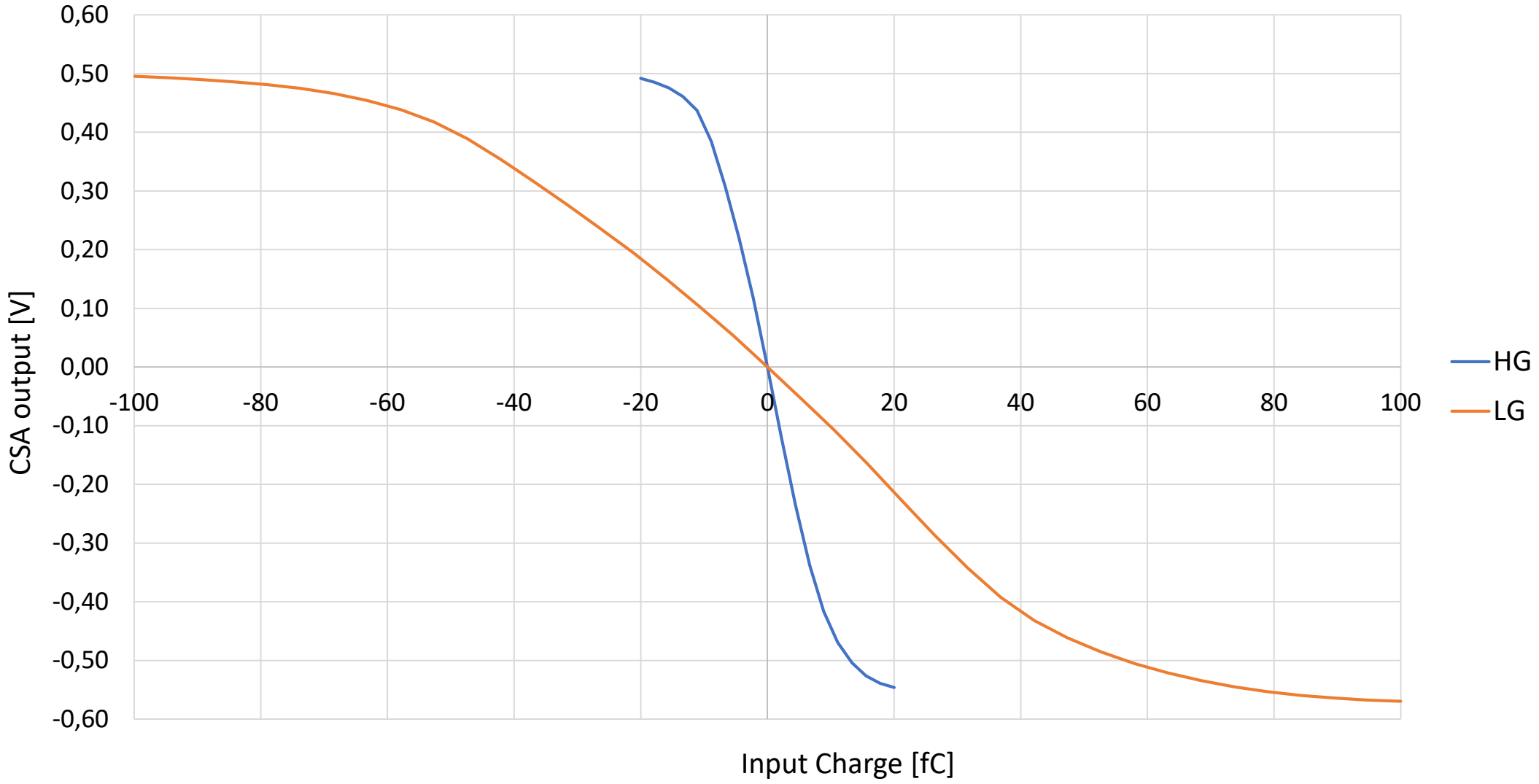
Charge branch:

- Acknowledgment of the input signal and charge measurement

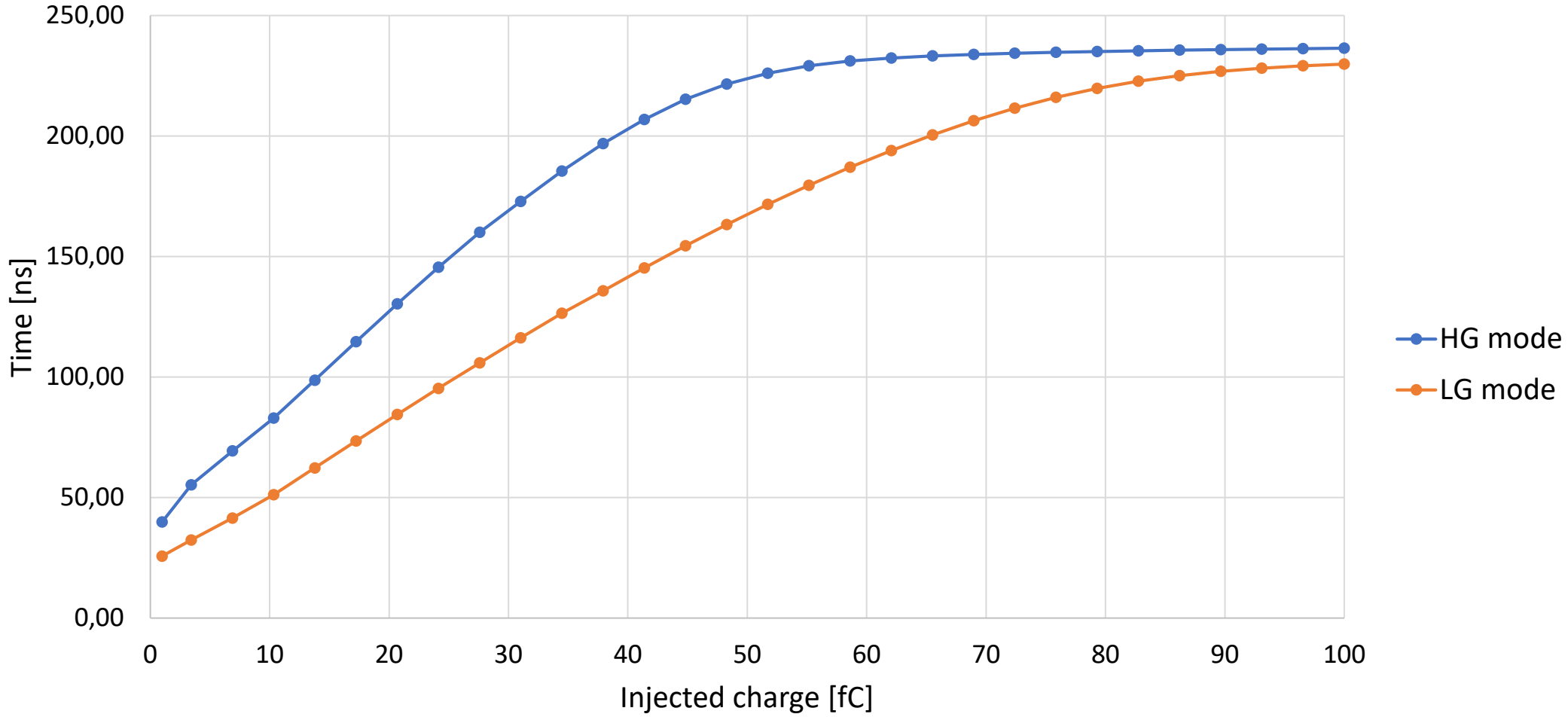
Shaper feature:

- Peaking time: 25ns, 50ns, 75ns, 100ns (polarity adj.)

CSA simulation: output dynamic



Charge branch simulation: time-charge characteristics



Simulation settings: peaking time 100 ns, discharge slope 2 mV/ns

Thanks