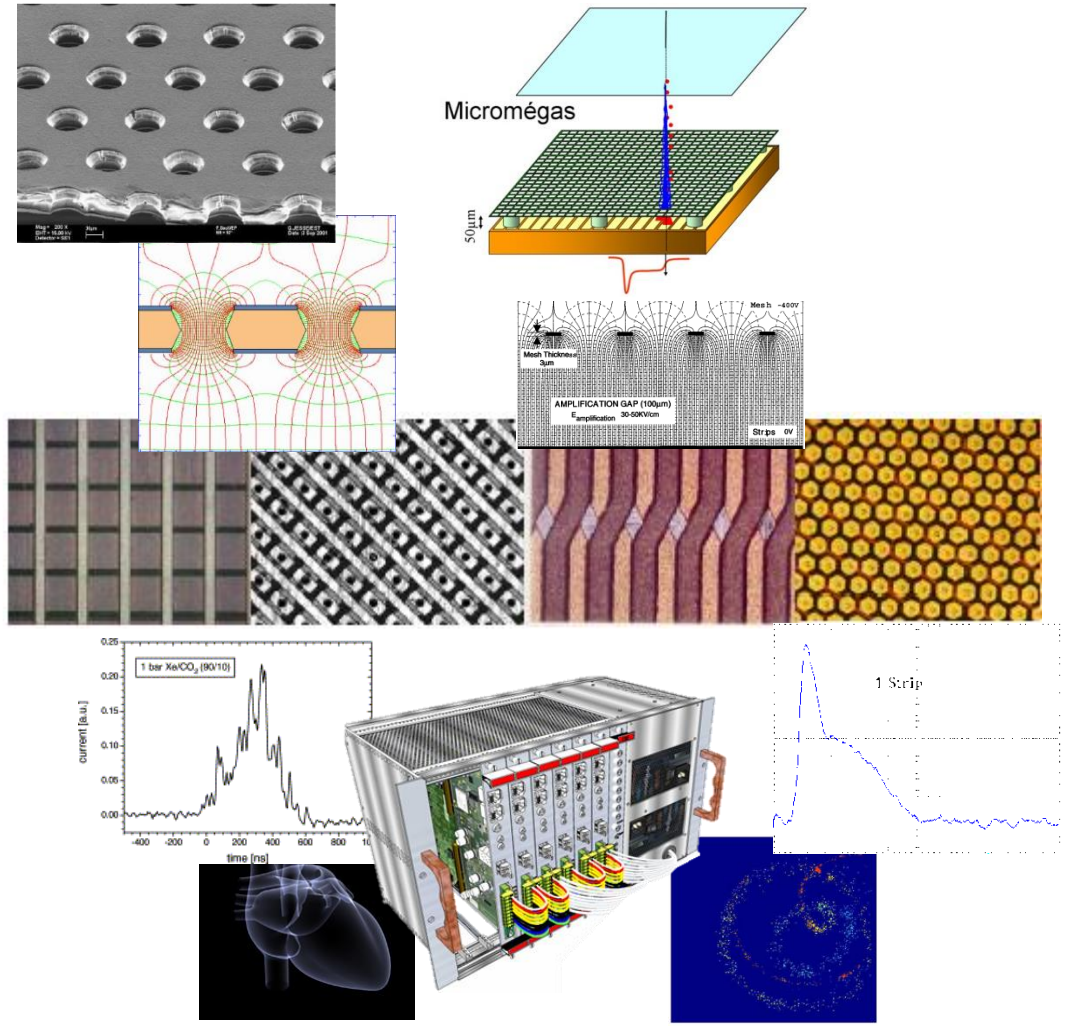
Topical Workshop on Front End Electronics for Gas Detectors: Linear Chips

INTRODUCTION

Sorin Martoiu (IFIN-HH, Bucharest)

Front-end Electronics for Gas Detectors



IONIZATION

DRIFT

MULTIPLICATION

READOUT

CHARGE COLLECTION

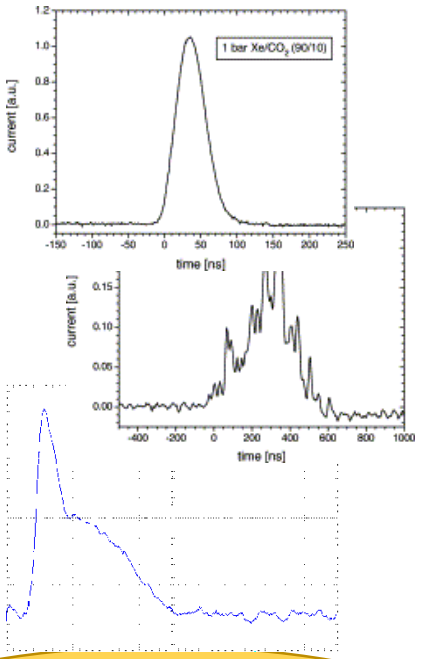
AMPLIFICATION/
CONVERSION

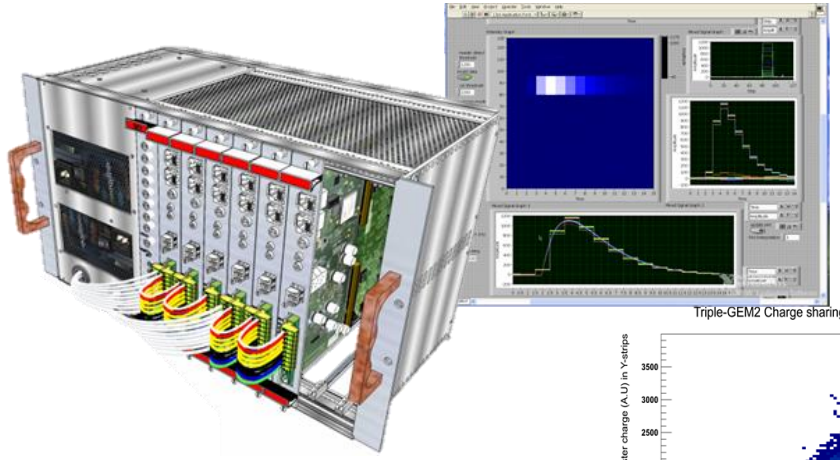
PROCESSING

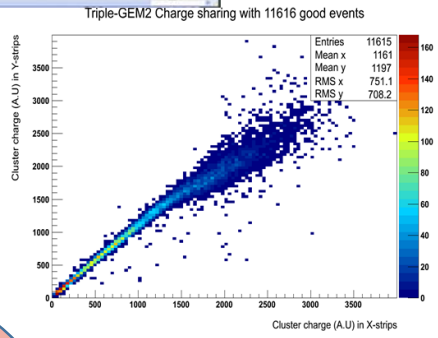
FEATURE EXTRACTION

EVENT CORRELATION

Front-End Electronics for (Gas) Detectors







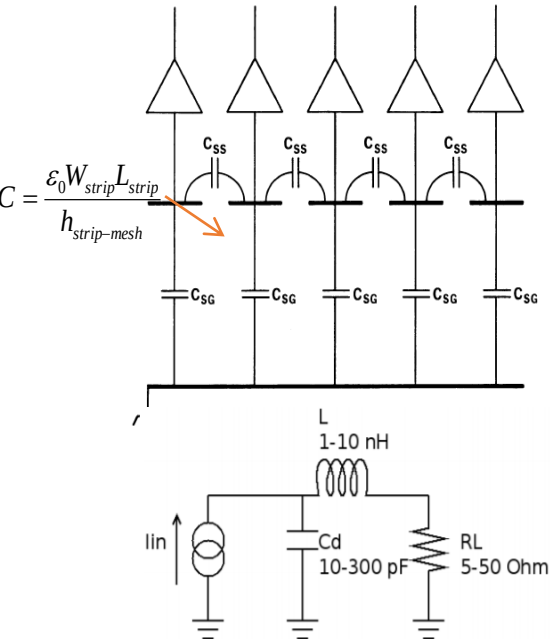
- signal range = 10 .. 1000 ke-
- signal width = 5 .. 200ns
- negative or positive polarity
- …

- Low noise *(0.1 ~ 1 ke)*
- High channel count *(up to millions of ch)*
- Discharge protection
- Radiation hardness

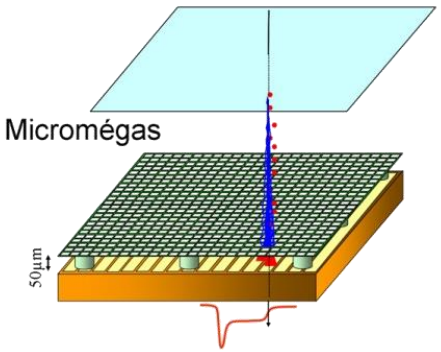
- Rate capability
- Efficiency
- Data Bandwidth
- Processing Power

- Spatial resolution
- Temporal resolution
- Energy resolution

Parasitics

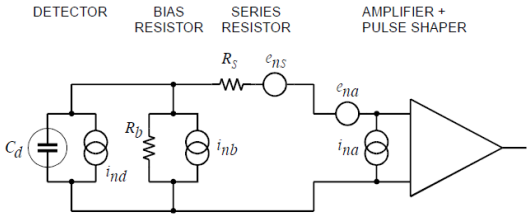


~ 0.1..1 pF/cm



C. de La Taille RD51 workshop 15 jun 2021

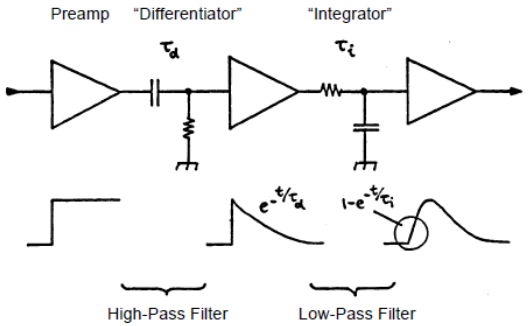
Noise



shunt resistance: $i_{nb}^2 = \frac{4kT}{R_b}$

series resistance: $e_{ns}^2 = 4kTR_s$

amplifier: e_{na}, i_{na}



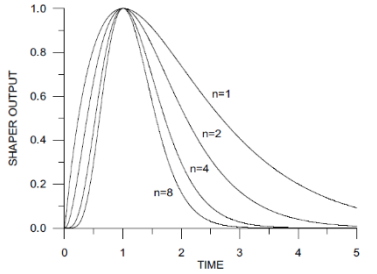
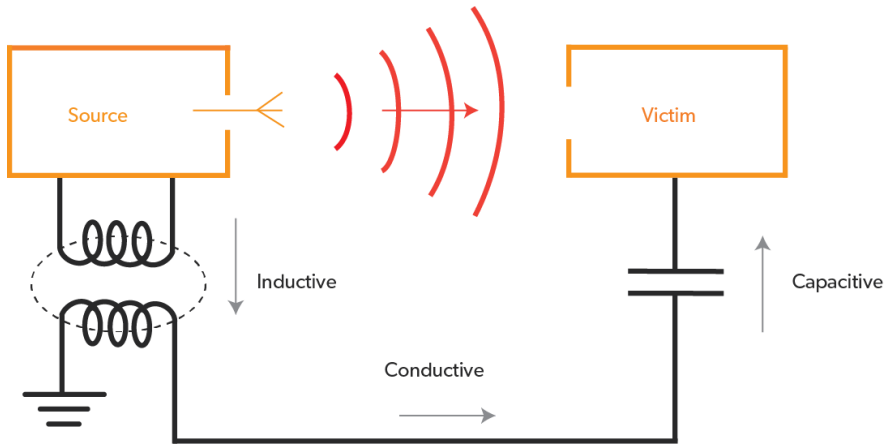
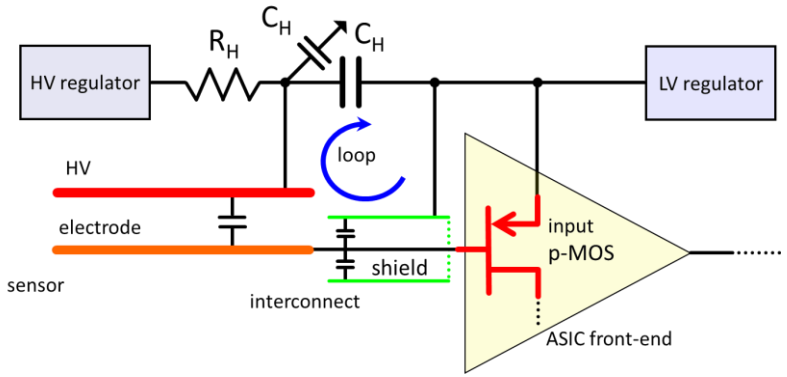


FIGURE 19. Pulse shape vs. number of integrators in a *CR-nRC* shaper

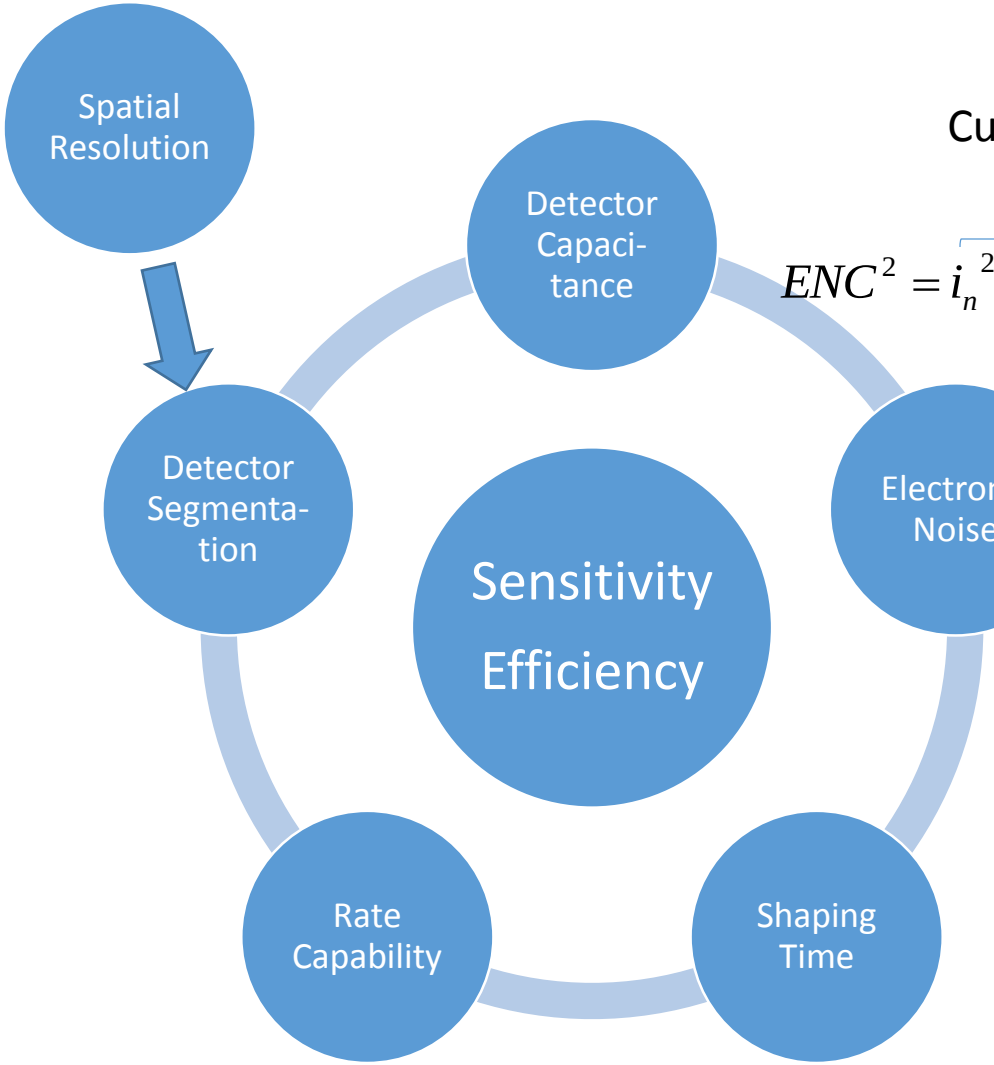
EMI



System effects



Sensitivity vs. Efficiency



Current Noise

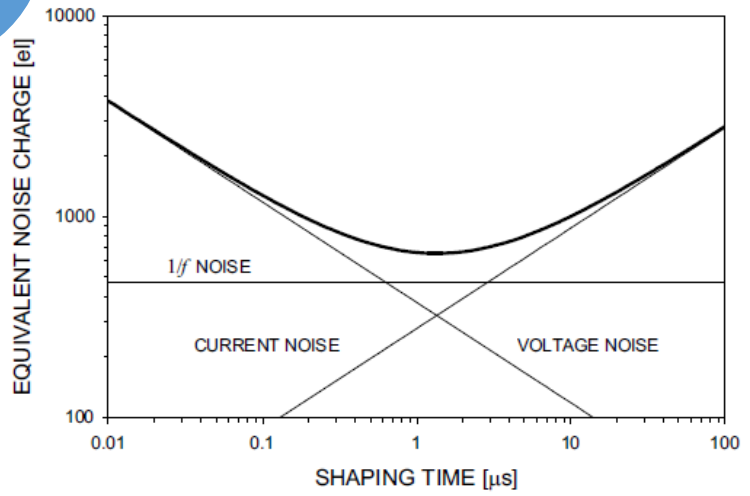
detector capacitance

$$ENC^2 = i_n^2 A_i \tau_S + \frac{S_w A_w (C_D + C_g)^2}{\tau_S} + S_f A_f (C_D + C_g)^2$$

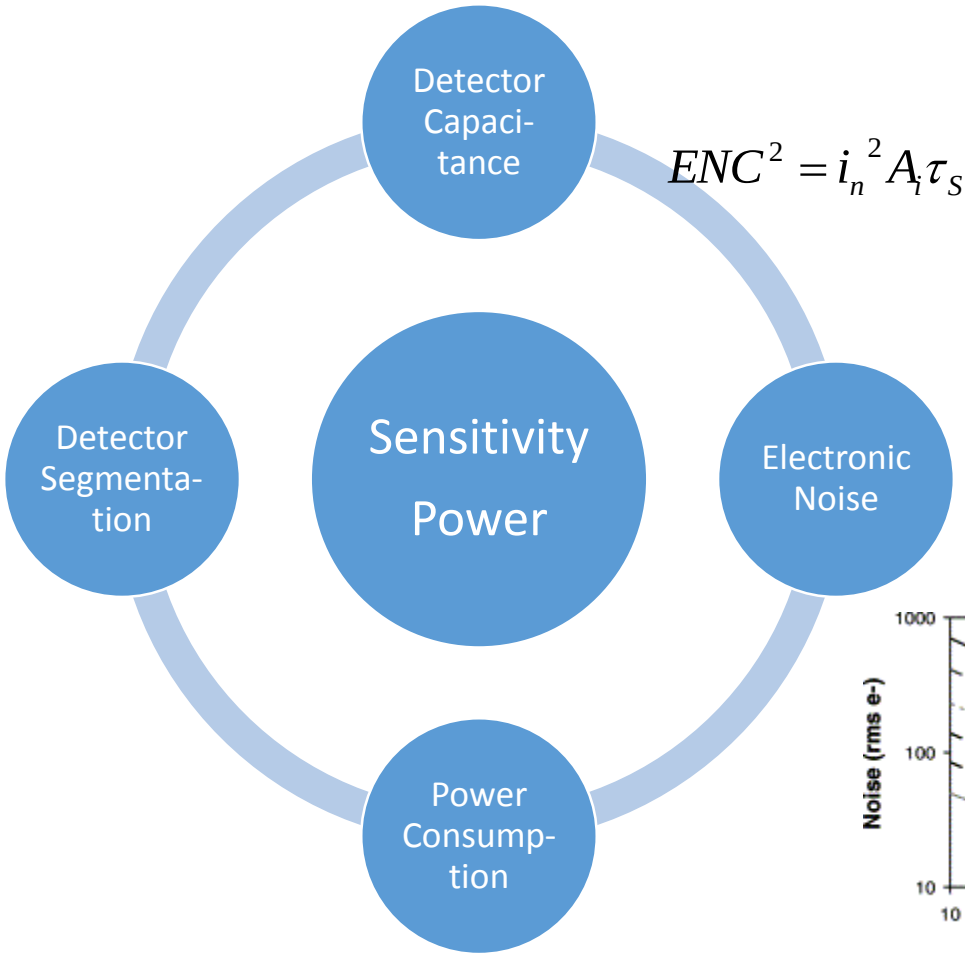
shaping time

White Noise

1/f Noise



Sensitivity vs. Power

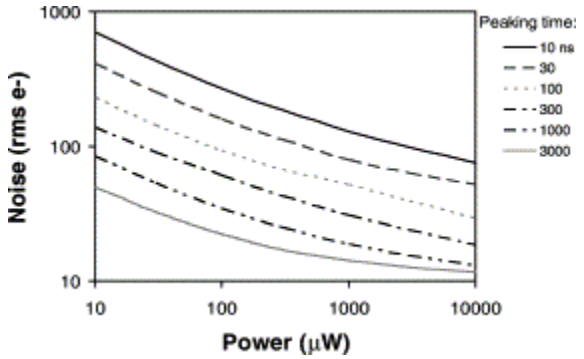


detector capacitance

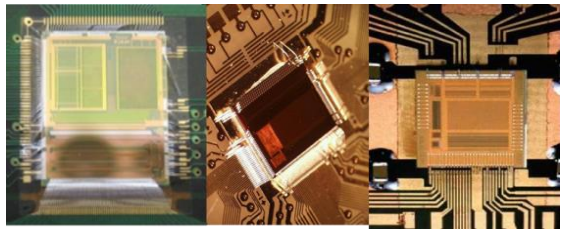
$$ENC^2 = i_n^2 A_i \tau_S + \frac{S_w A_w (C_D + C_g)^2}{\tau_S} + S_f A_f (C_D + C_g)^2$$

$$S_w = \frac{8}{3}\frac{KT}{g_m}$$

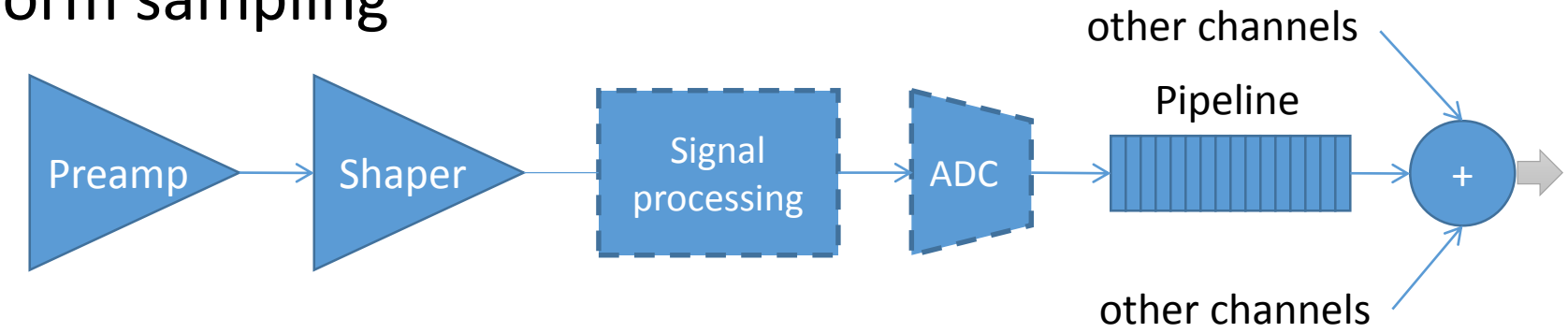
$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L} I_{DS}}$$



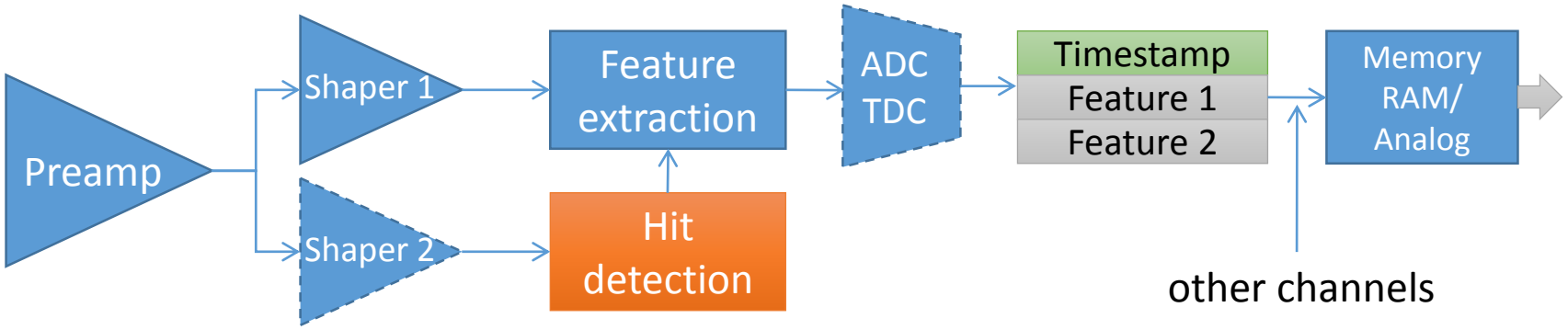
Front-End Architecture



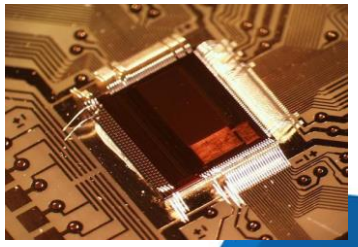
- Waveform sampling

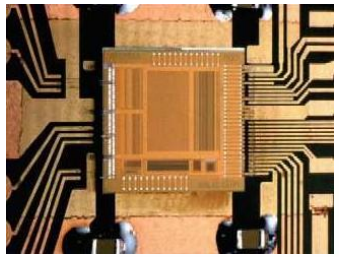


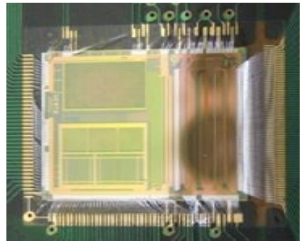
- Self-triggered channel



What front-end should I use?







- Progress in radiation detectors **tightly coupled** to progress in front-end ASICs
- Front-end ASICs
  - rapid increase in **demand, functionality, programmability, and complexity**
  - increase in **risk of failures** with consequent need to **accept trade-offs**
  - require continuous increase in **organizational and design resources**
  - main front-end ASIC enemies: "perfection" and "general purpose"

G. De Geronimo, RD51, June 2021, https://indico.cern.ch/event/1040996/contributions/4402471/

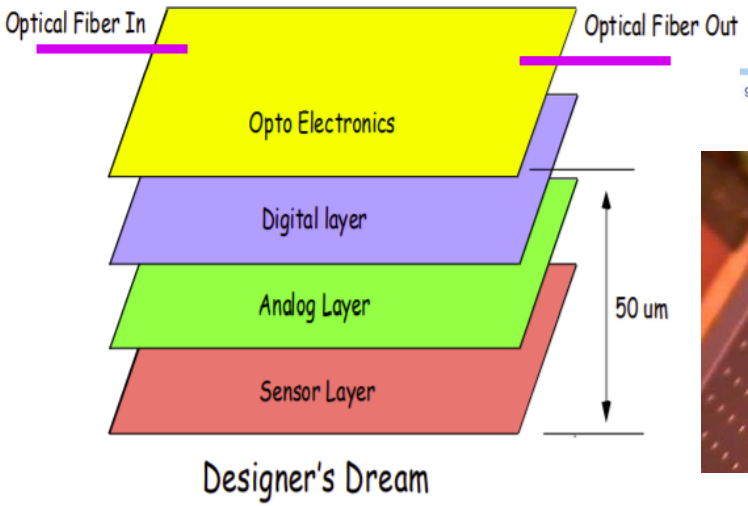
ChipMatrix (2009)

Name	Exp	Det	#ch	Shaper (ns)	Noise	Range (fC)	Pol.	ADC	f (MHz)	P/ch. (mW)	Feat.	Tech	Rad hard
APV25	CMS	Si strip	128	50	270+38e/pF	20	both	A	40	2.7	PD, PR	0.25 CMOS	10
AFTER	T2K	TPC	72	100-2000 s-gauss	(350-1800) + (22-1.8)e/pF	19	both	A	1-50 (100)	7.5	VG,VS	0.35 CMOS	no
MSGCROC	DETNI	Gas strip	32	T: 25 E: 85	2000e @ 40pF	800	both	A,1	2ns TDC		VG, ZS	0.35 CMOS	no
Beetle	LHCb		128	25	500+50e/pF	17.5	both	A/1	40	5.2	F-OR	0.25 CMOS	40
VFAT	TOTEM		128	22	650+50e/pF	18.5 (cal)	both	1	40	4.47	F-OR	0.25 CMOS	50
NINO	ALICE	TPC	8	1	1900+165/pF	2000 th<100	both	1	async	30	BR	0.25 CMOS	no
CARIOCA	LHCb	MWPC	8	<15 @ 220pF	2000+40e/pF	250	both	1	async	46	BR	0.25 CMOS	20
PASA+ ALTRO	ALICE TPC	TPC	16	190_{fwhm} s-gauss	570e @20 pF	160	both	10	20	< 40	BC, TC, ZS	0.35,0.25 CMOS	
SVX4	CDF, D0	Si strip	128	100-360	410+45e/pF	60fC	neg	8	106 (212)	2	ZS	0.25 CMOS	20
SPIROC	ILC, T2K	SiPM	36	A:25-175 T: 10	A: 1/11pe; T:1/24pe	2000 pe	neg	8-12	100ps TDC	0.025 *pulse*	dual-gain	0.35 SiGe	no

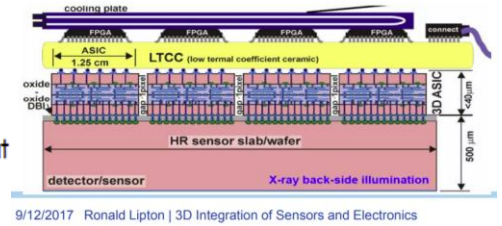
Legend:	PD = peak detection, PR = pile-up rejection, VG = variable gain, VS = variable shaping, F-OR = fast-OR, BR = baseline restorer, BC = baseline correction, TC = tail correction, DC = data compression, ZS = zero suppression

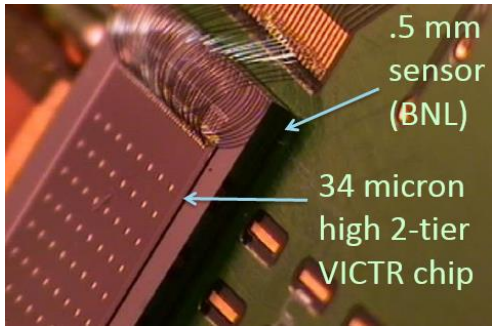
Future(?)

3D Integration



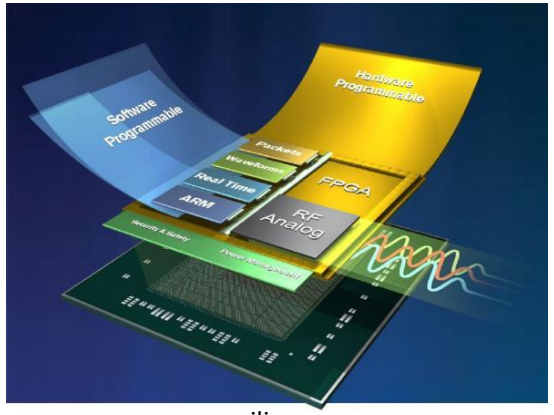
Designer's Dream





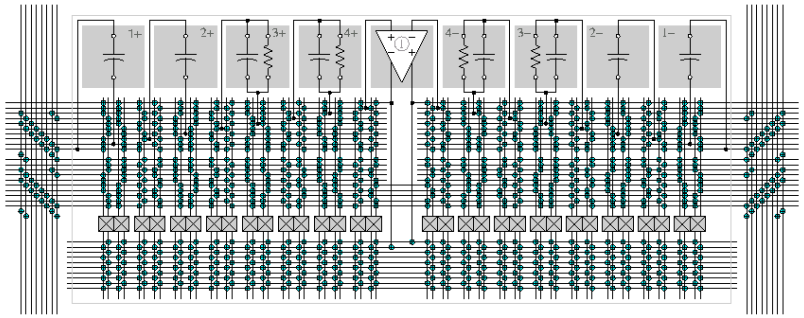
- Separate tiers for analog, mixed mode and digital functions
- May have interchangeable options for each tier depending on application
- Could add tiers for processing, *CPU cores, memory, neural networks*, etc.

RFSoC FPGAs



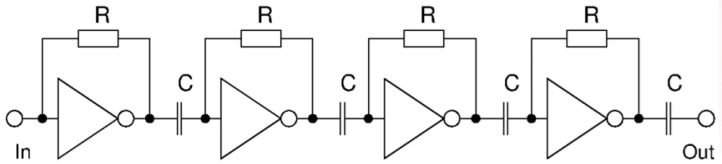
www.xilinx.com

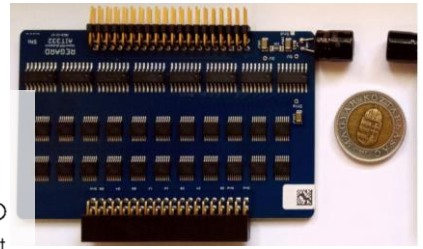
Field-Programmable Analog Array (FPAA)



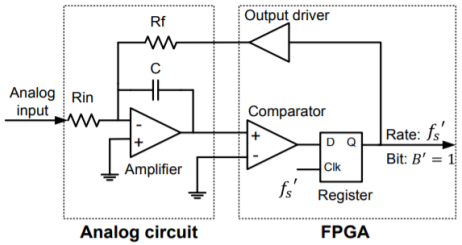
http://opencircuitdesign.com/~tim/research/fpaa/fpaa.html

"All-Digital" front-end

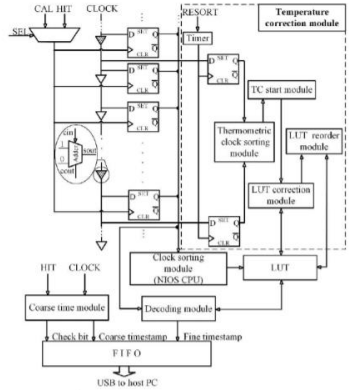


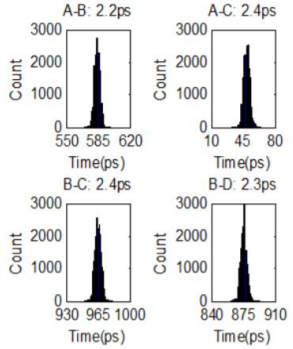


D. Varga, RD51 Coll. Meeting, https://indico.cern.ch/event/1040996/contributions/4406958/



Energy: high-performance 1-order, 1-bit over-sampled delta-sigma ADC





Nonuniform multiphase (NUMP)TDC implemented in a FPGA

ZHAO, Zhixiang, PicoPET -- An advanced data acquisition architecture for modern nuclear imaging, Virtual IEEE RTC, https://indico.cern.ch/event/737461/contributions/3725105

Present

Name	Exp	Detectors	#ch	Shaping	Noise	Range(ke)	Input signal	Pol	ADC # bits	fs (MHz)	P/ch (mW)	Features	Technology	Radhard
AFTER	T2K; T2K upgrade	TPC, micromegas end-plate	72	50-1000	(350-1800) + (22.2-1.8)e/pF	4 ranges: 750/1500/2250/3800	current	both	A	1-50 SCA	8	SCA	0.35 µm CMOS	NA
AGET	ACTAR, AT-TPC, SΠRIT	MGPD+DSSD	64	25-500	(435-34000) + (19-7.4)e/pF	4 ranges: 750/1500/6240/62400	current	both	A	1-100 SCA sampling	10	SCA; Triggerless; selective readout	0.35 µm CMOS	NA
STAGE	HARPO	MGPD+DSSD	64	25-4000	(435-34000) + (19-7.4)e/pF	4 ranges: 750/1500/6240/62400	current	both	A	1-100 SCA sampling	10	SCA; Triggerless; selective readout	0.35 µm CMOS	NA
DREAM	CLAS12	MGPD	64	25-450	(394-2140) + (10.2-0.34)e/pF	4 ranges: 312/624/1248/3744	current	both	A	1-50 SCA	10	SCA; Trigger	0.35 µm CMOS	NA
PETIROC2	CMS Muon	RPC (designed for SiPM)	32	25-100 (Q)		1mV (~1pe)	voltage	both	10		6		0,35 SiGe	
GEMROC	(Client under NDA)	GEMs	64	30-200		1fC -> 500fC	charge	negative		40	1		0,35 SiGe	
HARDROC3	ILC CALICE sDHCAL	RPC	64	50-150 (Q) / 20 (T)		10fC -> 50pC	current	negative		50	1	Zero Suppression	0,35 SiGe	
WASA	CEPC	TPC, GEM	16	160	533+9.1e/pF	748.8	charge	negative	10	<100	2.33	direct waveform output	65nm CMOS	
VMM3a	ATLAS	sTGC, Micromegas	64	25-200		2pC at 0.5mV/FC, in linear range	charge		10, 8, 6	200ns conv. time	~11	data driven, Baseline stabilization, neighbouring logic, fast digitisation, Peak Finding, timing information, and many more	130nm GF	>300kRad


THANK
YOU