



中国科学技术大学
University of Science and Technology of China

Fast timing electronics R&D based on waveform digitization

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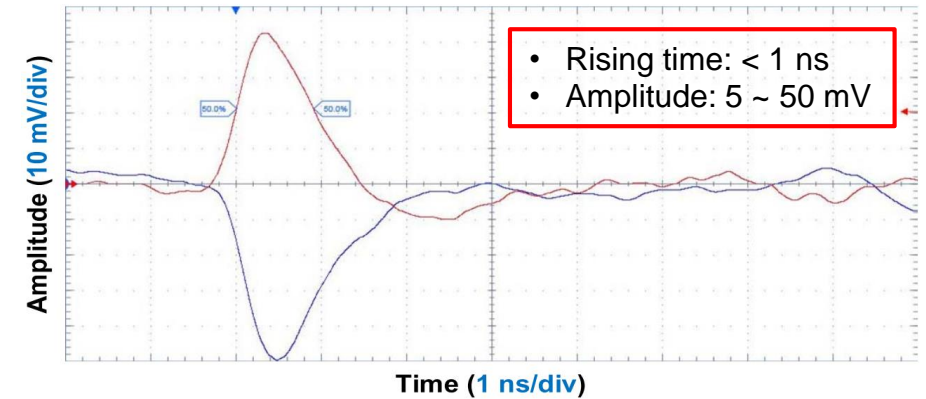
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Outline

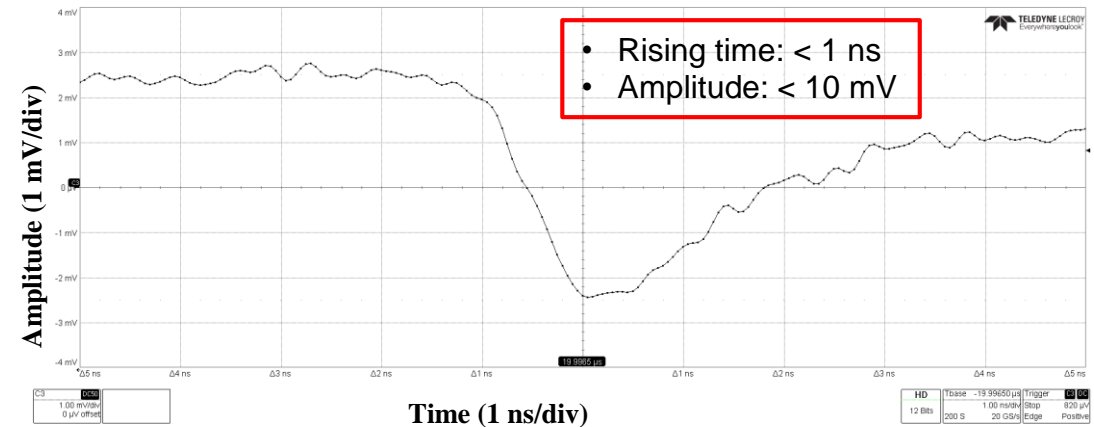
- Introduction
- DRS4 based fast timing electronics
 - Structure
 - Test results
- SCA ASIC developed in our lab
 - Architecture
 - Performance
- Summary

Introduction

- Timing requirement in future HEP experiments
 - 20~30 ps time resolution for detectors
 - Picosecond time resolution for electronics
- Fast gas detectors
 - MRPC (Multi-gap Resistive Plate Chamber)
 - PICOSEC-Micromegas
- Waveform feature
 - Rising time: < 1 ns
 - Amplitude
 - ✓ 5~50 mV for MRPC
 - ✓ < 10 mV for PICOSEC-Micromegas



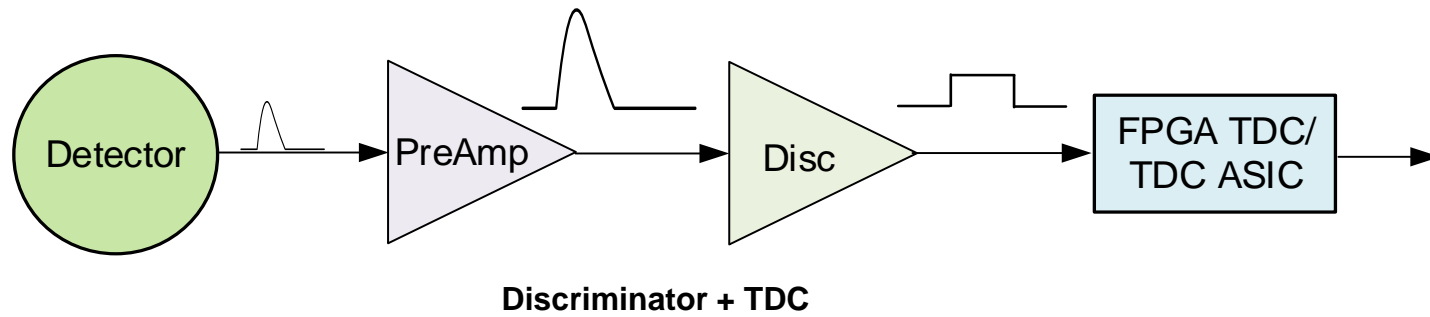
typical waveform from MRPC



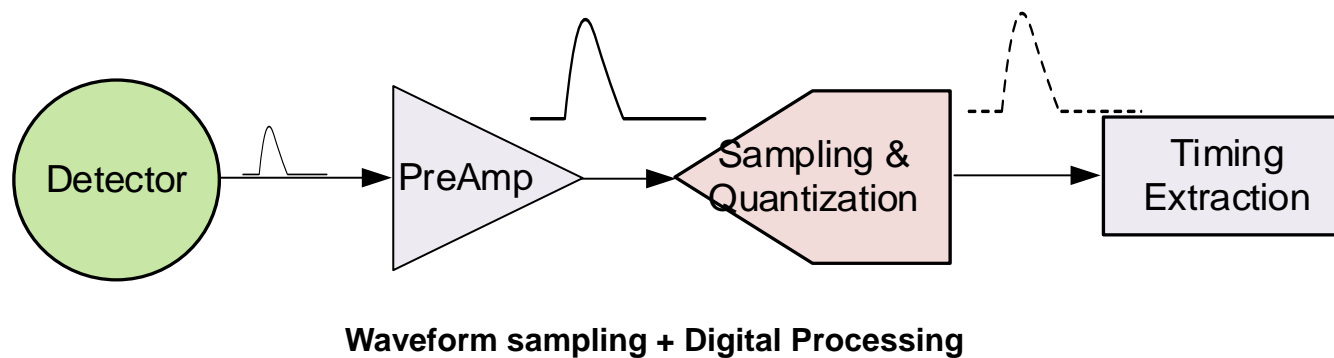
typical waveform from PICOSEC-Micromegas

Introduction

- Timing techniques



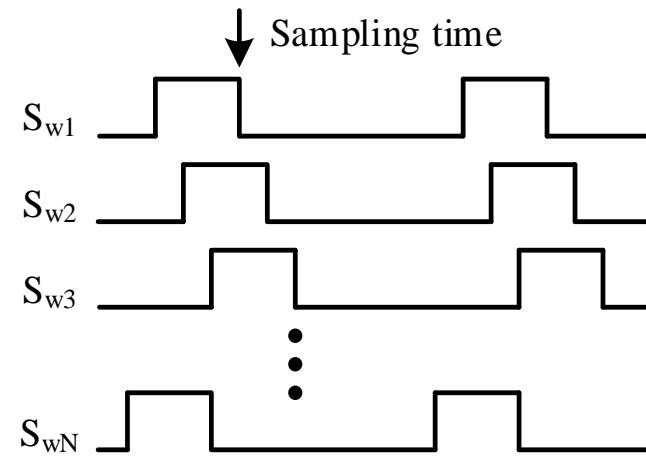
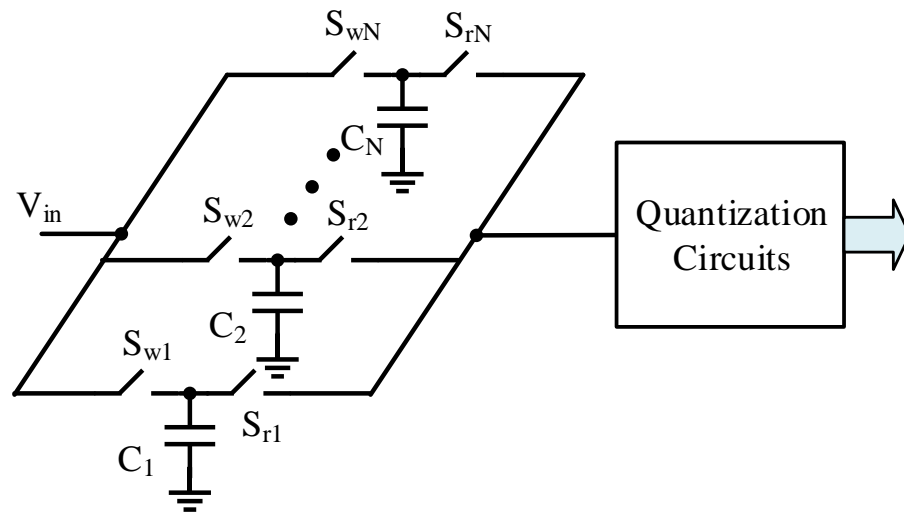
- TDC resolution < 10 ps
- Disc + TDC resolution is worse



- Timing resolution < 10 ps
- Flexible algorithm
- Switched Capacitor Array (SCA)
 - ✓ Low consumption
 - ✓ Compact
 - ✓ High channel density
 - ✓

Introduction

- SCA Operating Principle

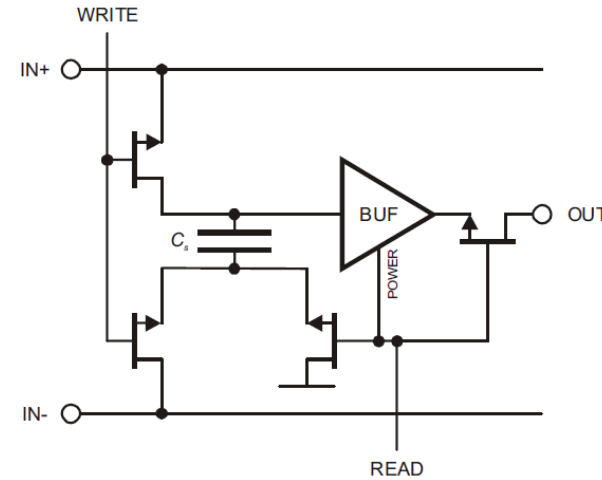
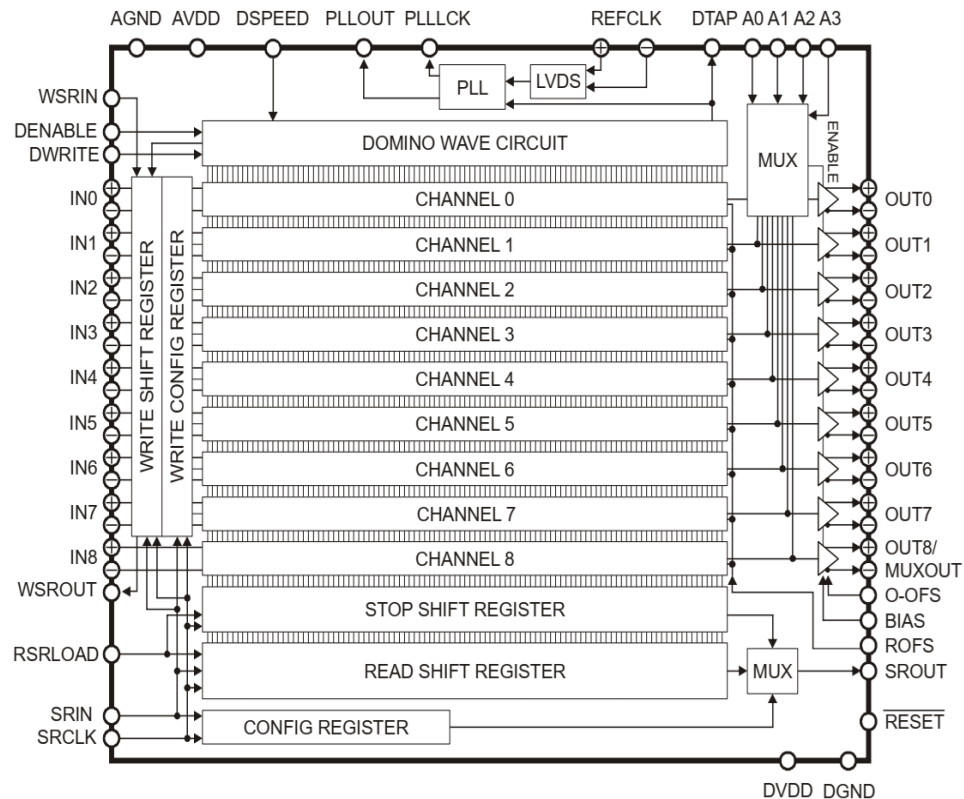


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DRS4 ASIC

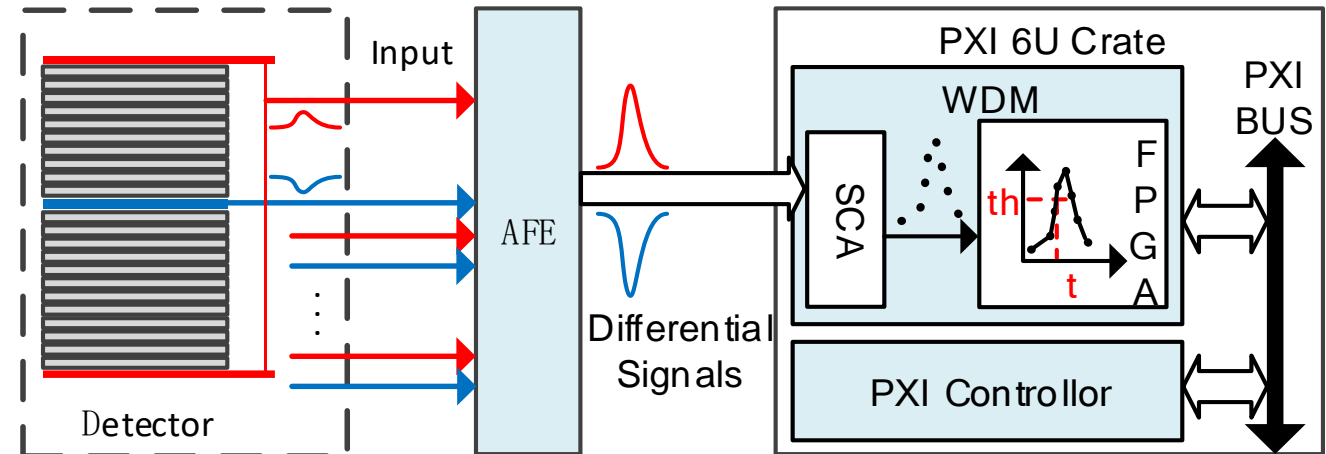
TNS: vol.61, no.6 (2014) 3607~3617



Parameters	Value
Sampling rate	0.7 ~ 6 Gsps
Number of channel	8+1
Sampling Depth	1024
Input Range	1 V
Noise	0.35 mV RMS
Analog BW	950 MHz

DRS4 based fast timing electronics - Structure

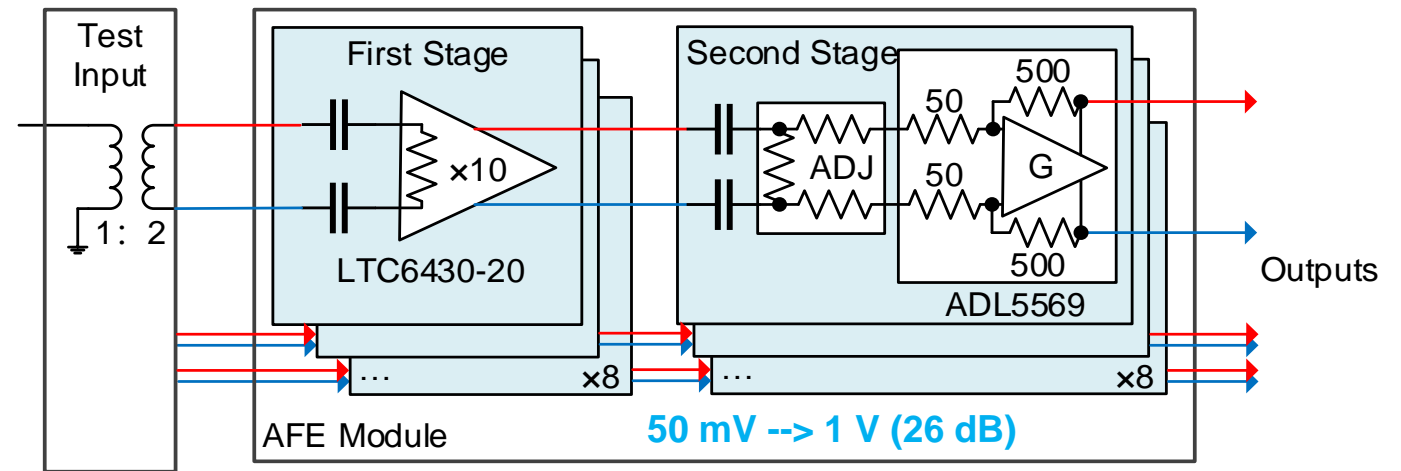
- Analog Front-end Electronics (AFE)
 - Low noise, high bandwidth preamp
 - Placed close to detectors
- Waveform Digitization Module (WDM)
 - DRS4 ASICs
 - ADCs
 - FPGA



Analog Frontend Electronics

- AFE for MRPC

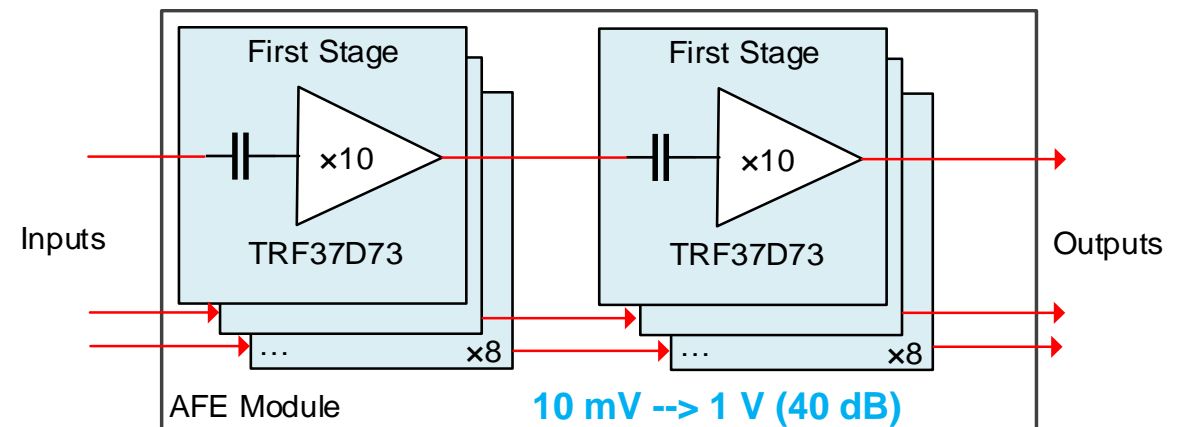
- Full differential
- First Stage
 - ✓ RF amplifier, 20 dB gain
 - ✓ Ultralow noise, high bandwidth
- Second Stage
 - ✓ OPA, adjustable gain



AFE for MRPC Detector

- AFE for PICOSEC-Micromegas

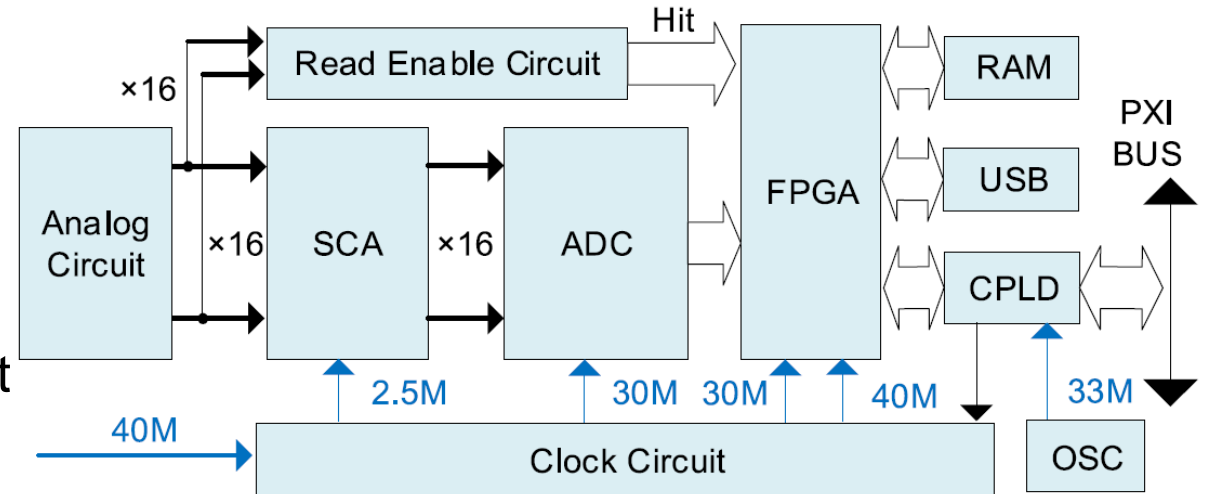
- Single-end
 - ✓ RF amplifier, Fixed gain
 - ✓ Ultralow noise, high bandwidth



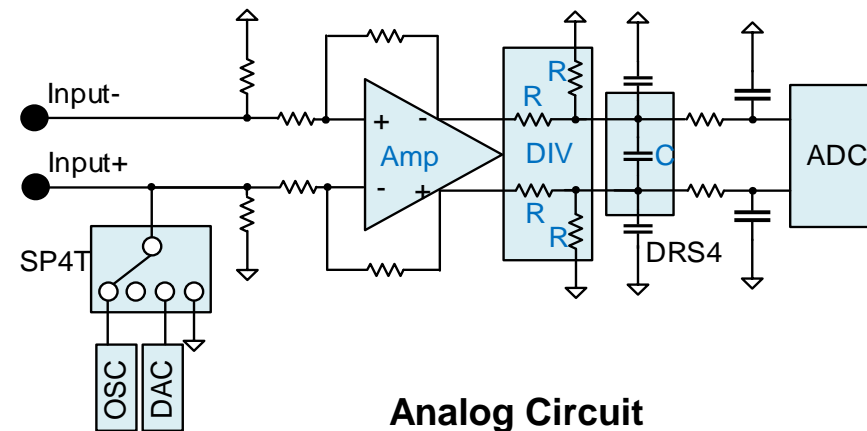
AFE for PICOSEC-Micromegas Detector

Waveform Digitization Module

- Analog Circuit
 - Increase drive capability
 - Two kind amplifiers are compared
 - THS4508 & LTC6409
- Hit Generation
 - High speed comparator + stretch circuit
 - Delayed by FPGA to control SCA
- Sampling Circuit
 - 2 DRS4s (16 channels)
 - 2 14-bit 8-channel ADC
- FPGA
 - Coarse counter: 24 bits
 - Fine timing extraction logic



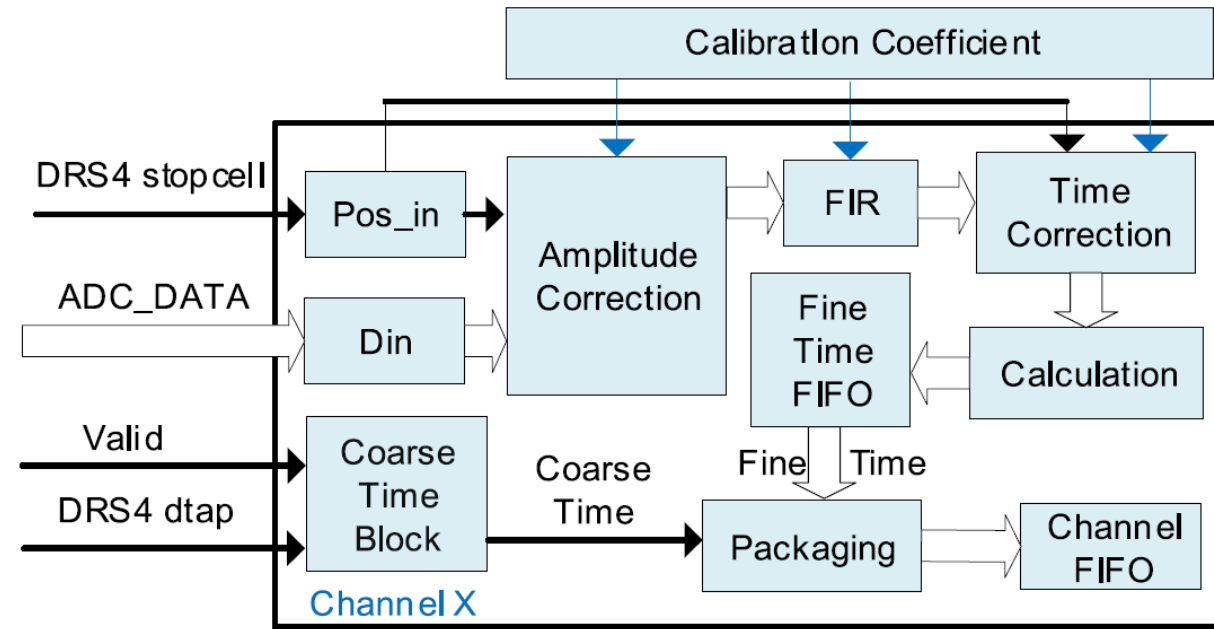
Waveform Digitization Module



Analog Circuit

Time Measurement Logic

- Amplitude Correction
 - Gain and offset
- FIR – Low Pass Filter
 - Reduce noise
- Time correction
 - Sampling interval variations
- Fine time measurement
 - Leading edge discrimination
 - Other methods to be compared

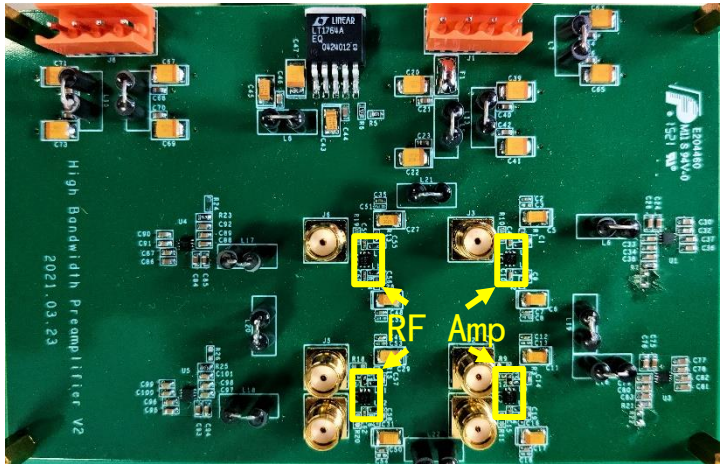


Block diagram of the time measurement logic

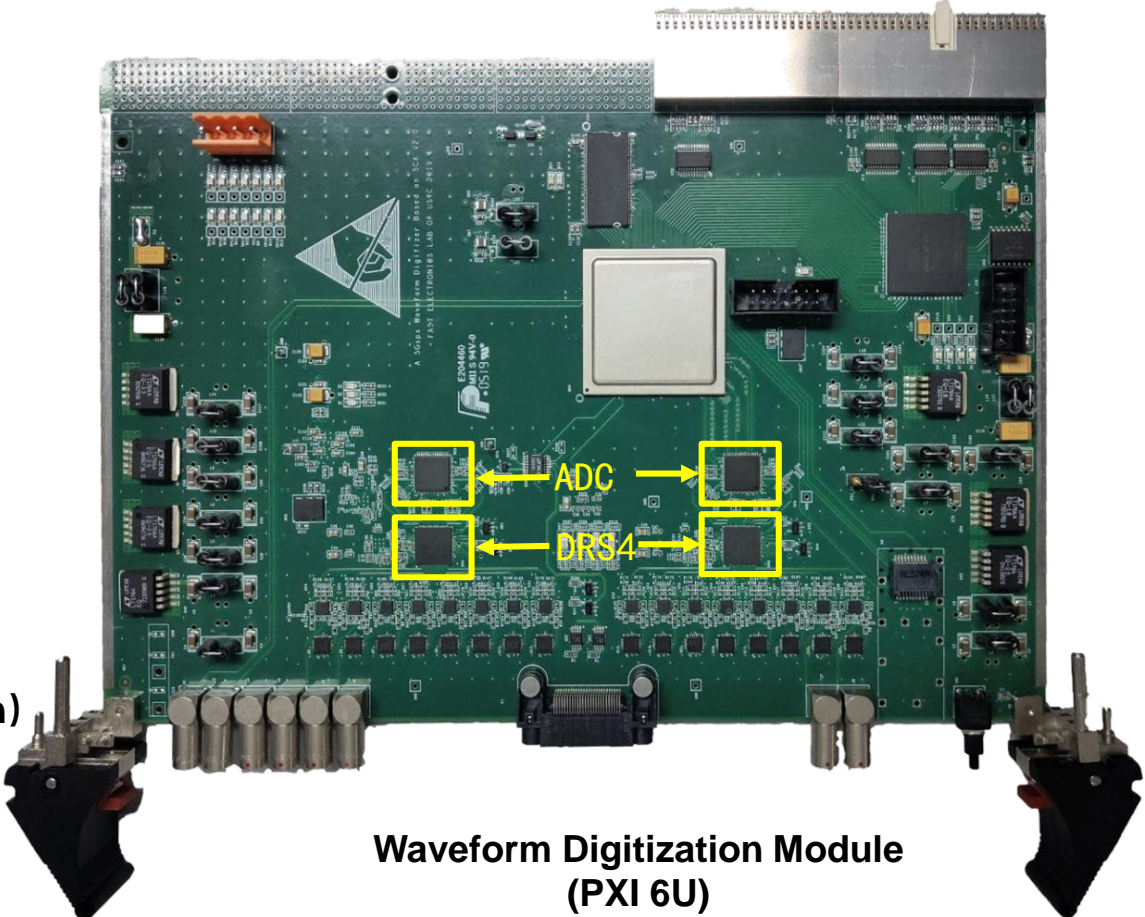
Electronics Cards



AFE for MPRC

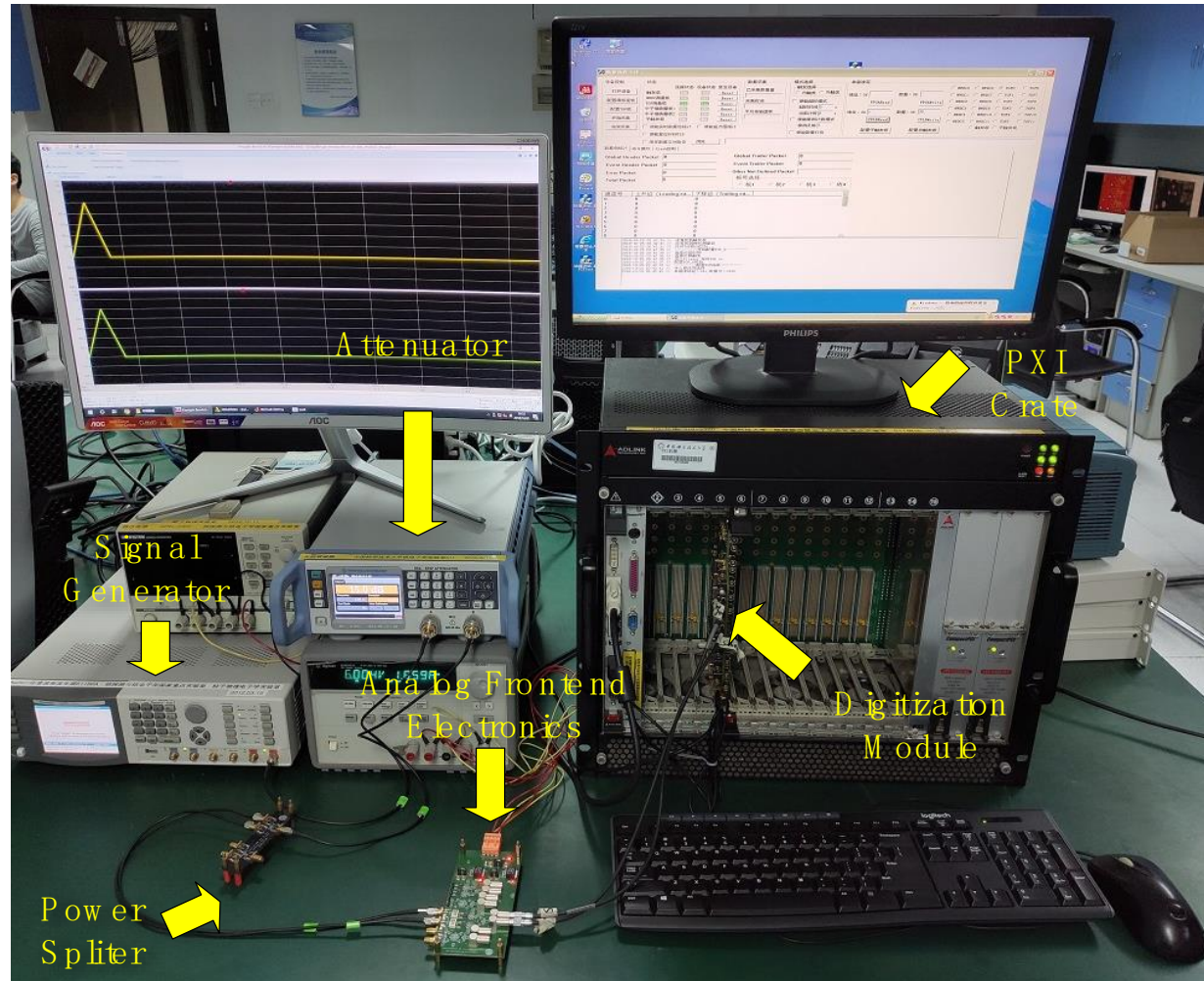


AFE for Micromegas
(2 channels for verification)



Waveform Digitization Module
(PXI 6U)

Test Setup

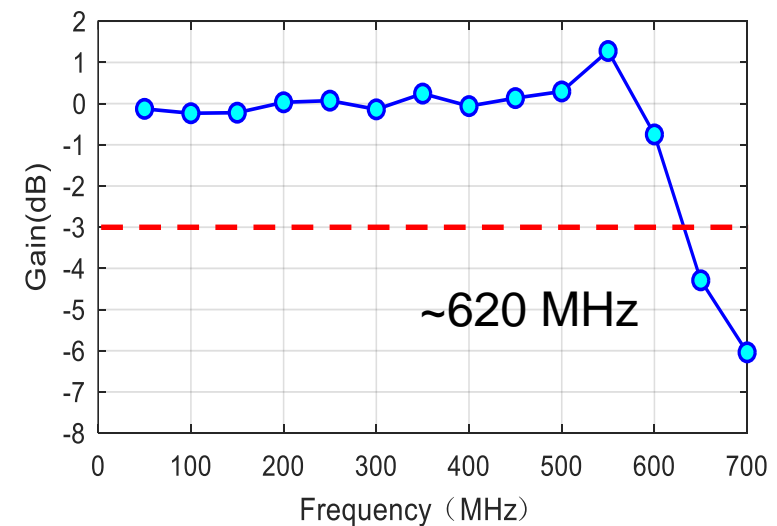
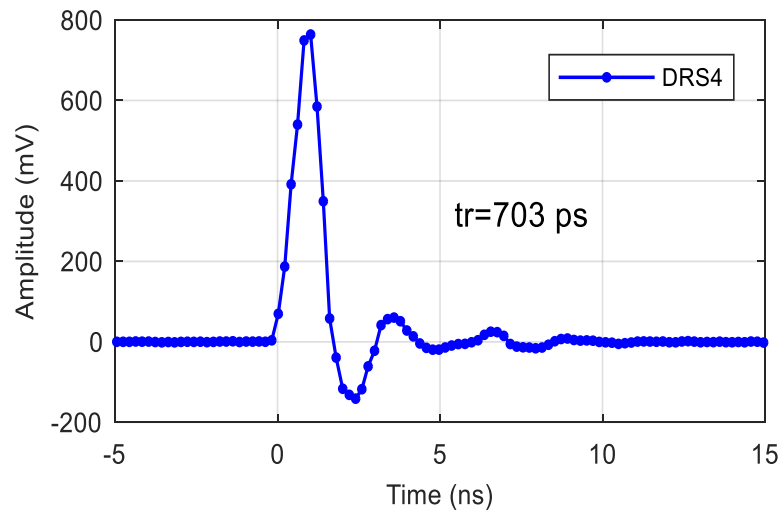
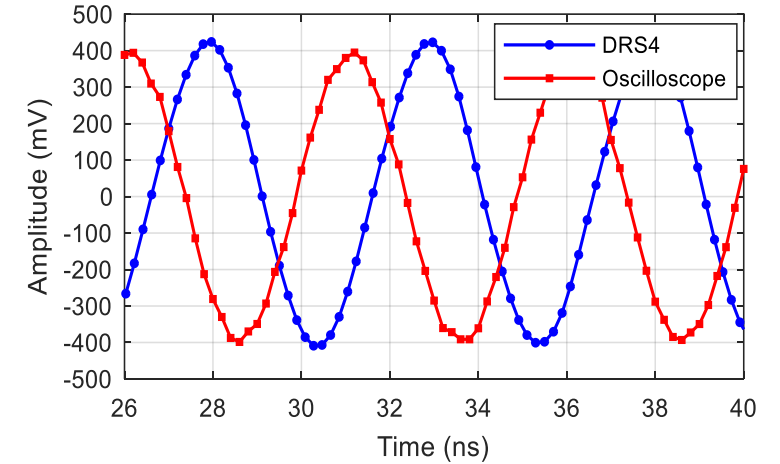
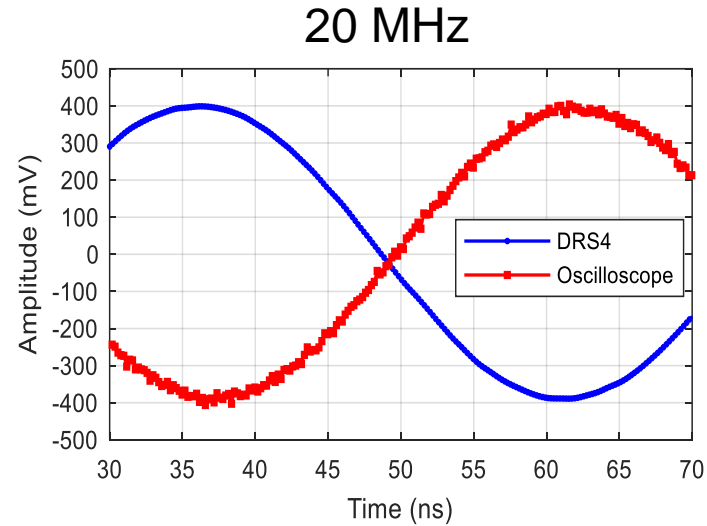


Test Result

- Waveform capture

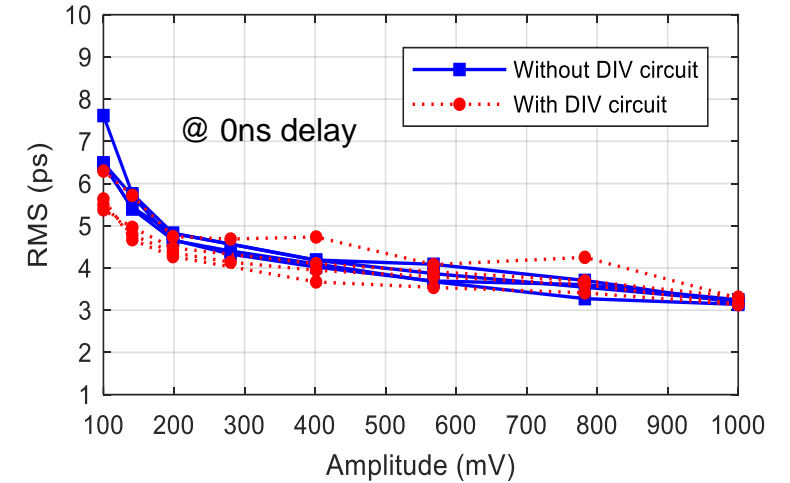
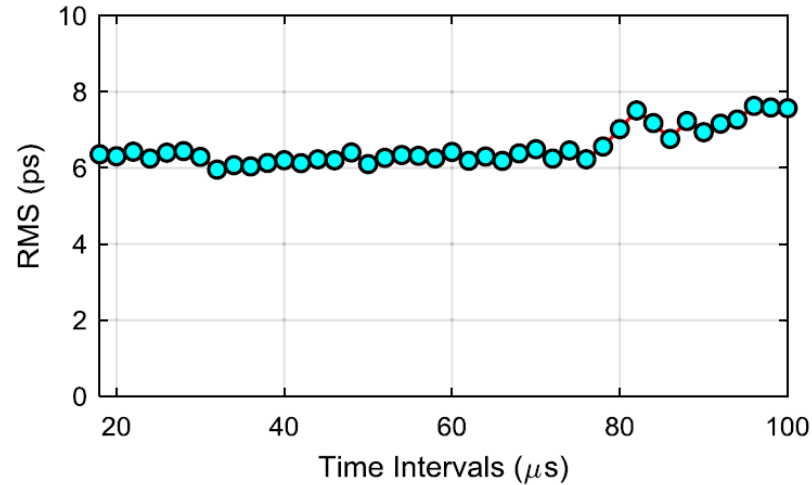
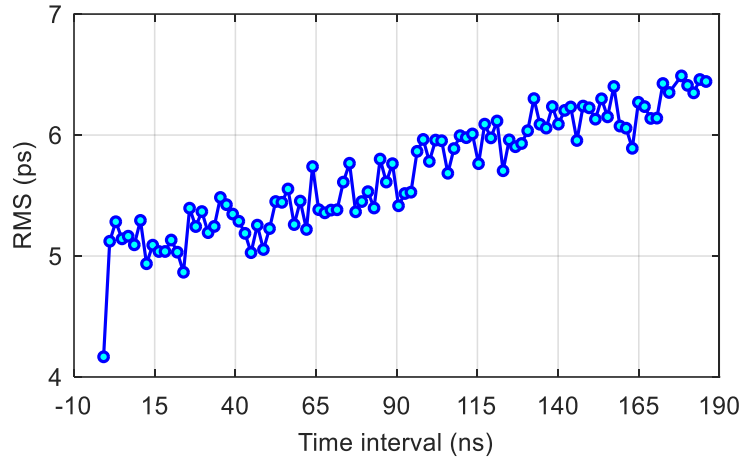
Oscilloscope: Lecroy 760 Zi-A

- 6 GHz ABW
- 5 Gsps (40 Gsps)



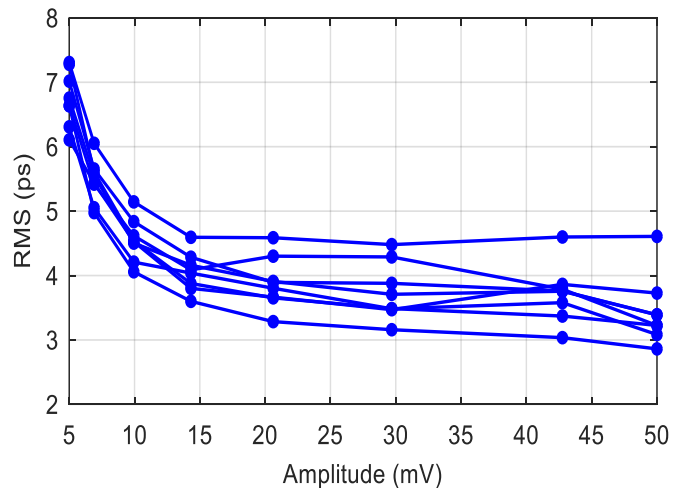
Test Result

- Time resolution of Digitization Module

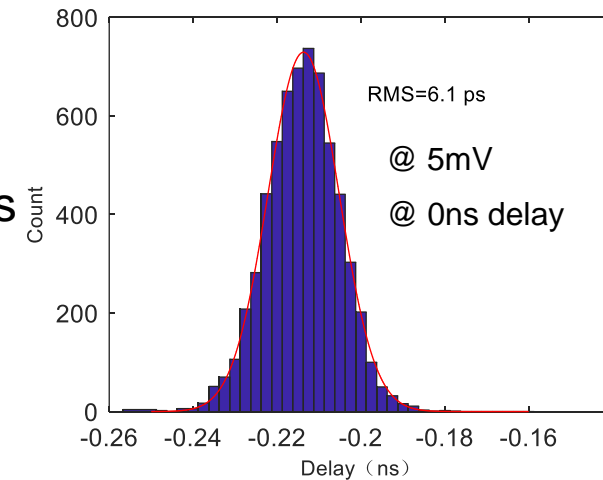


- Time resolution of readout electronics (AFE + WDM)

For MRPC



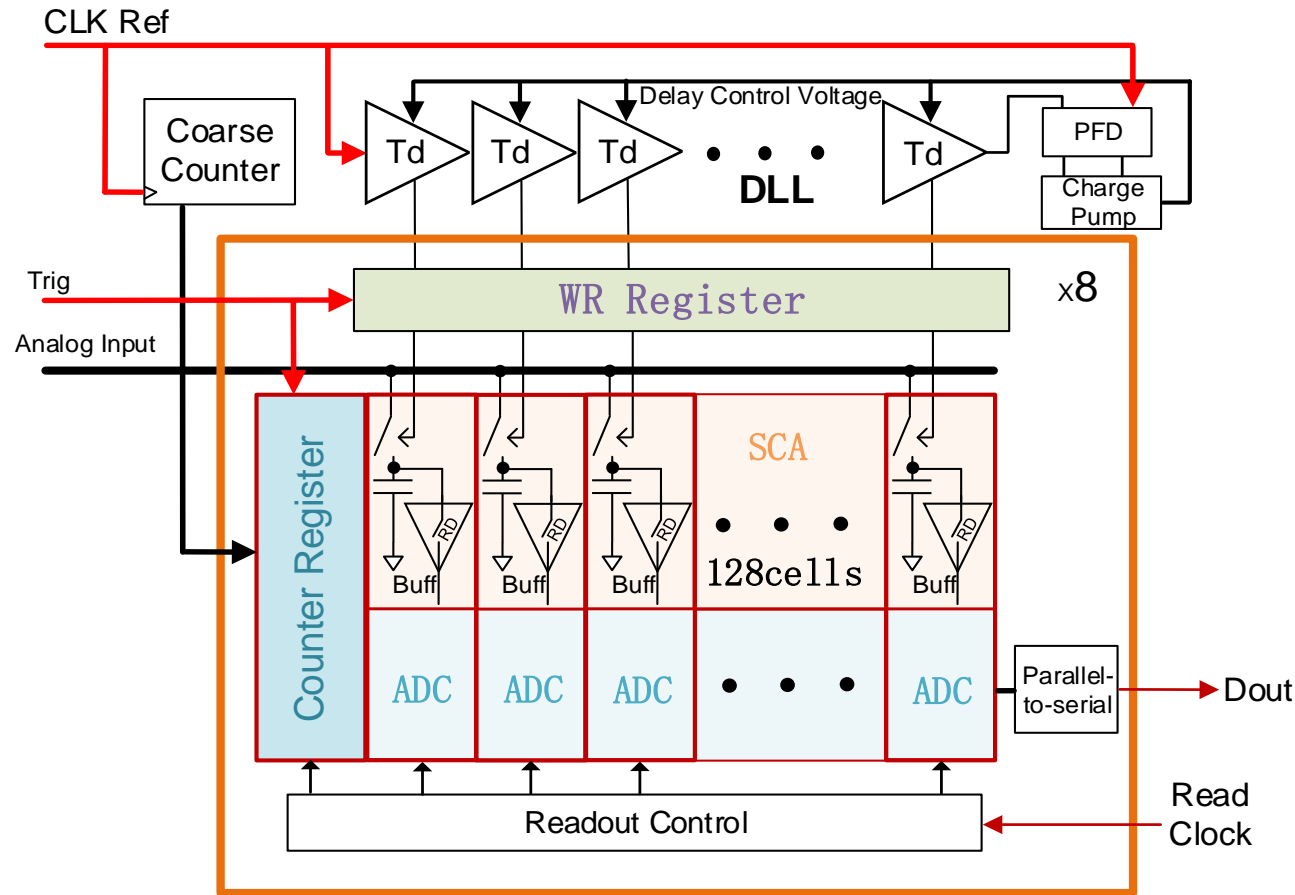
For Micromegas



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Architecture

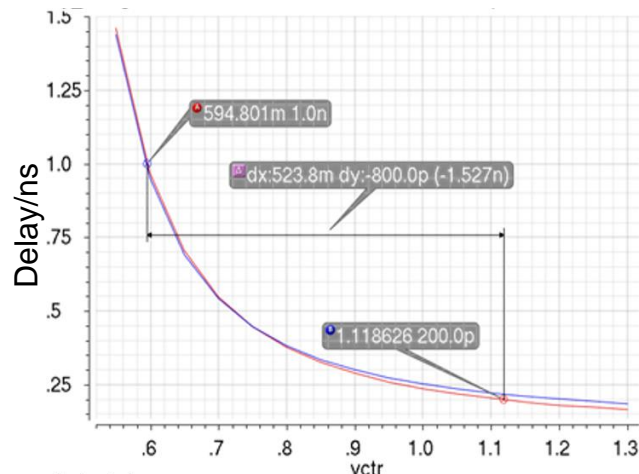
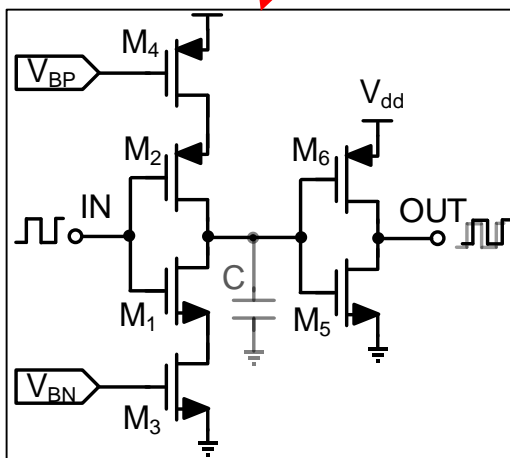
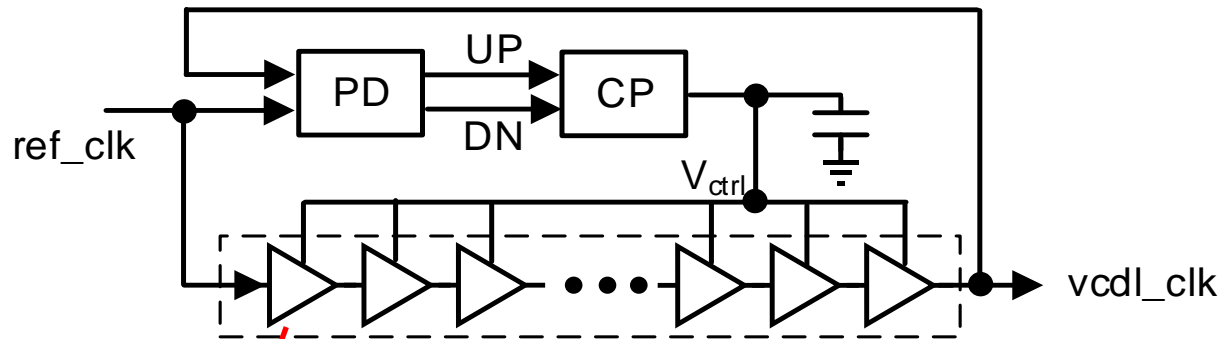


Parameters	Value
Sampling rate	1~5 Gsps
Number of channel	8
Sampling Depth	128
Input Range	1 V
Noise	< 1 mV RMS
ADC resolution	12 bits @ 1 GHz
Conversion time	4 μ s
Trigger	External

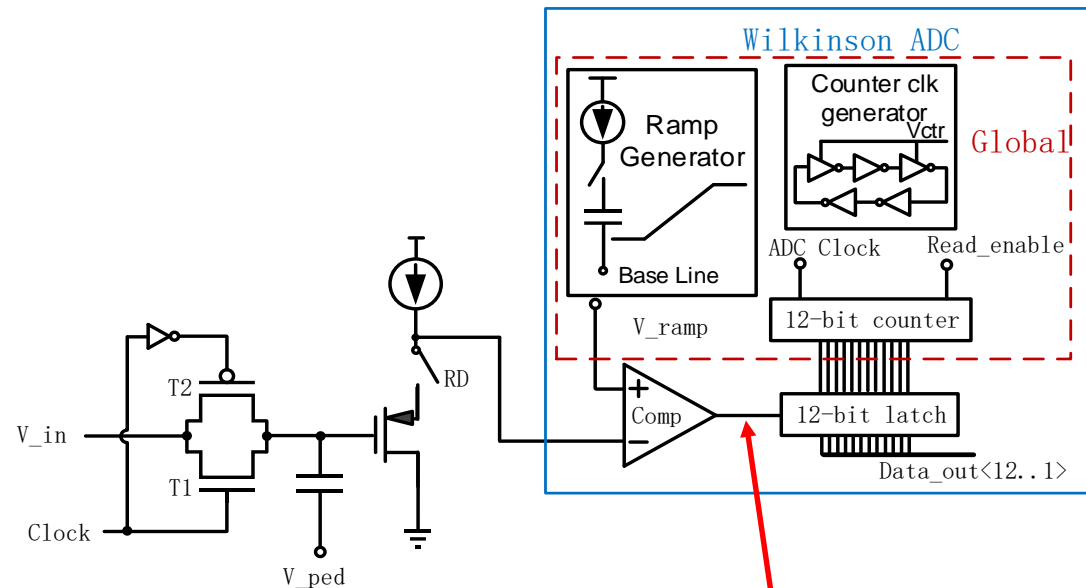
Both single-ended input and differential input have been designed

Architecture

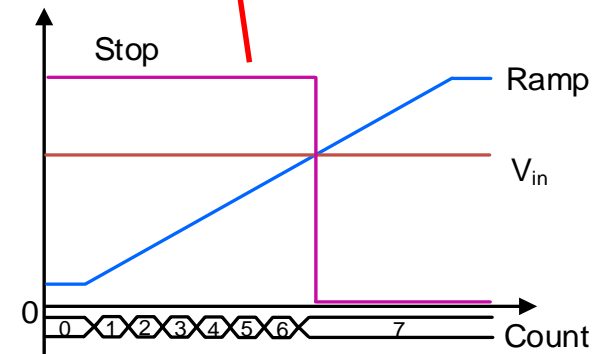
- Sampling clock



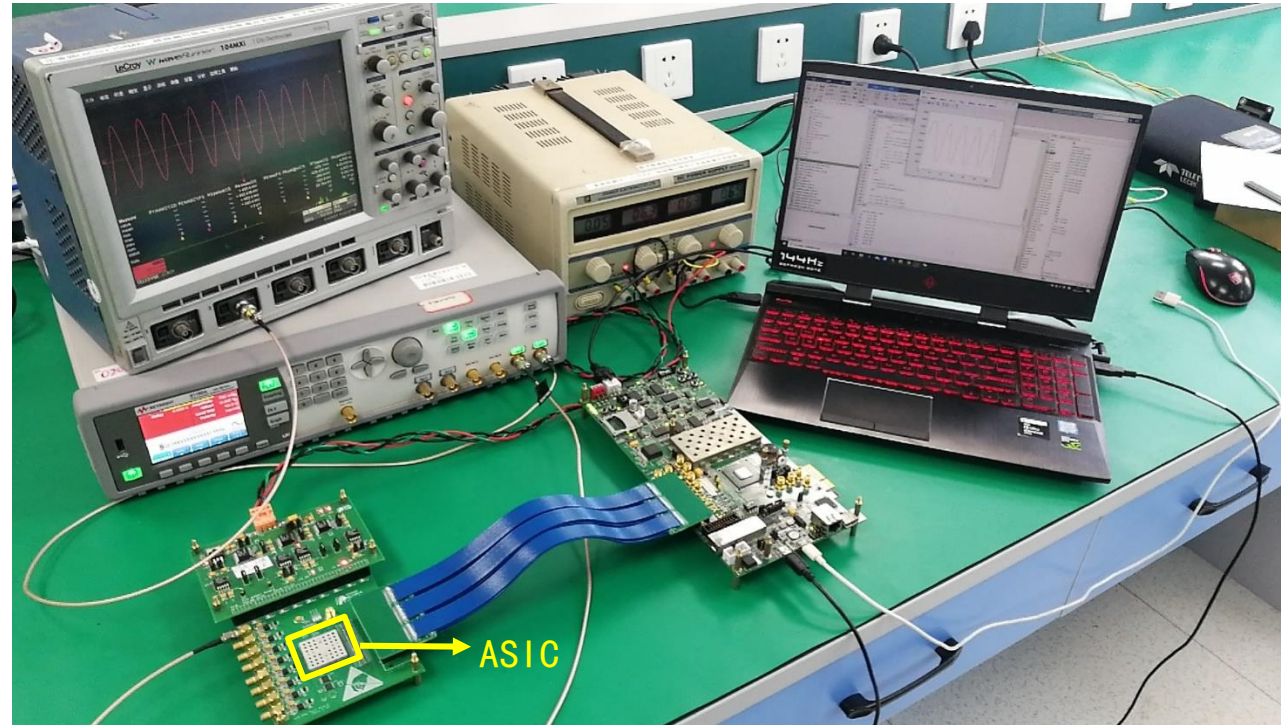
Simulation results of delay cell



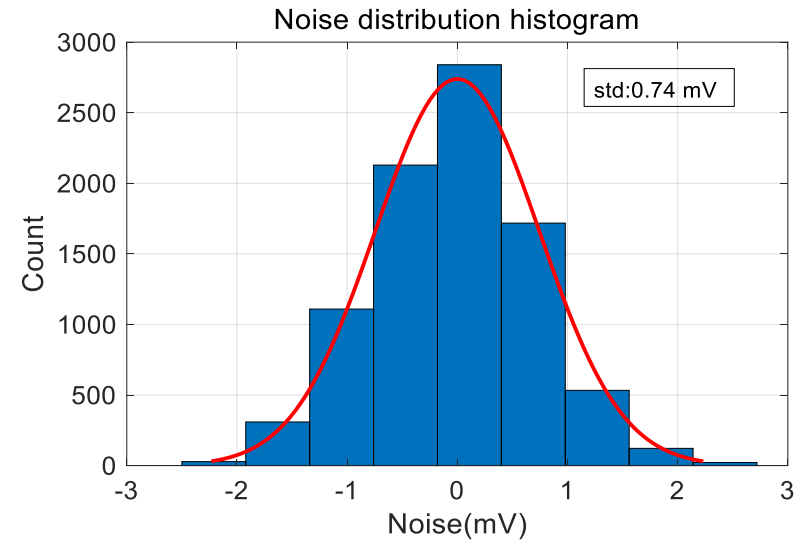
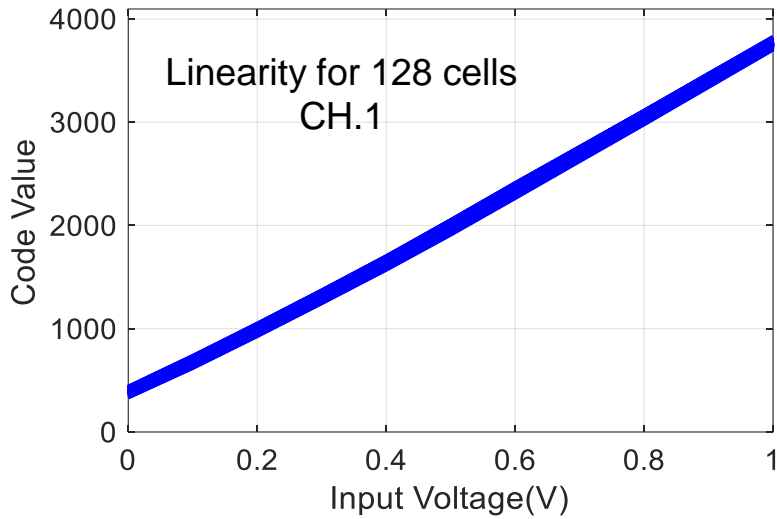
- Ramp and counter shared
- Gray counter
 - ✓ 12 bits, 1 GHz
 - ✓ 4 μ s Conversion time
- 1 latch per cell



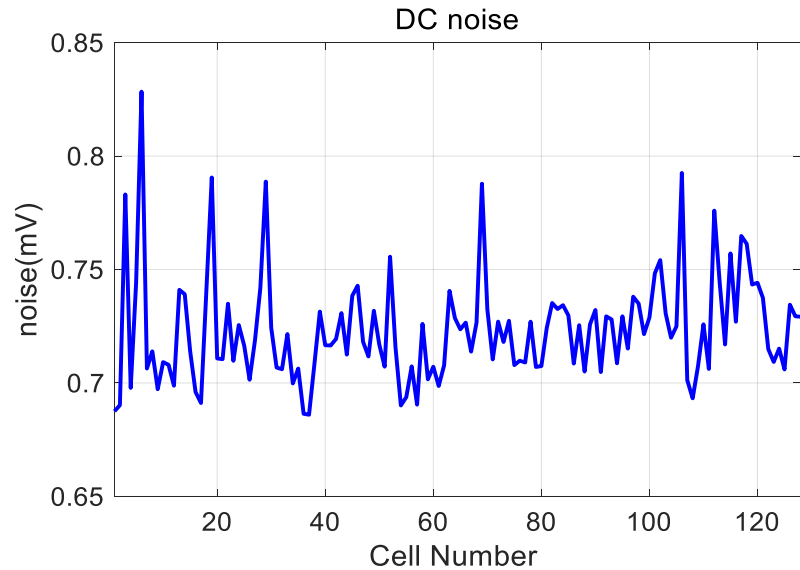
Test Setup



Preliminary test results



- DC linearity
 - ✓ Good gain uniformity
 - ✓ Offset slightly different
 - ✓ For amplitude correction
- Noise: ~ 0.75 mV



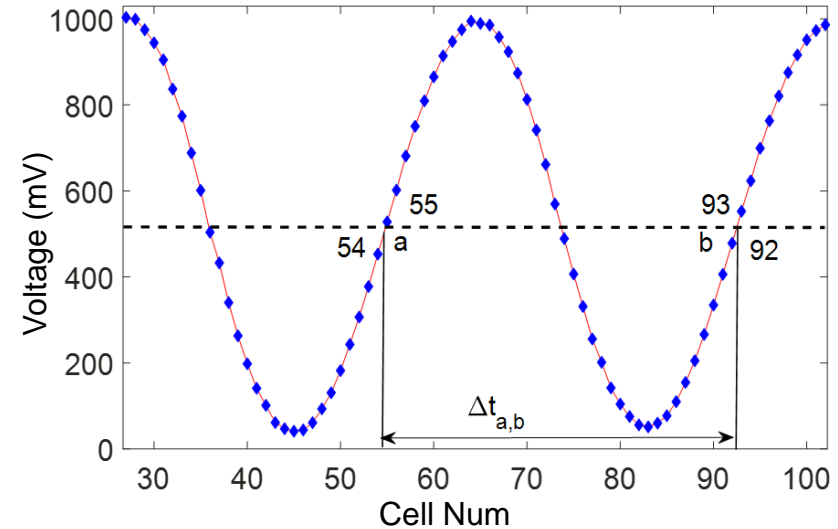
Sampling time correction

NIMA 916 (2019) 71-76

- Time between a and b is equal to one period of the input signal

$$\alpha \Delta t_{n_1} + \sum_{i=n_1+1}^{n_2-1} \Delta t_i + \beta \Delta t_{n_2} = T_S \quad (1)$$

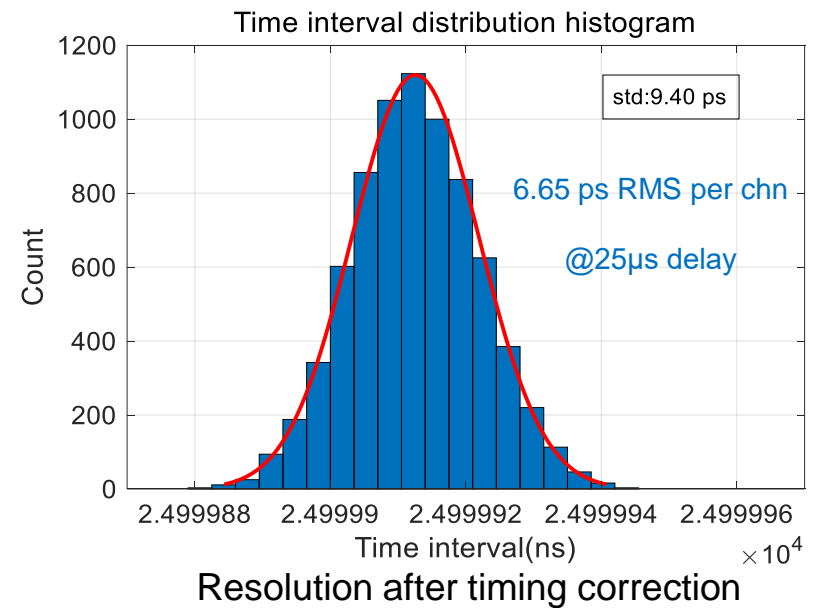
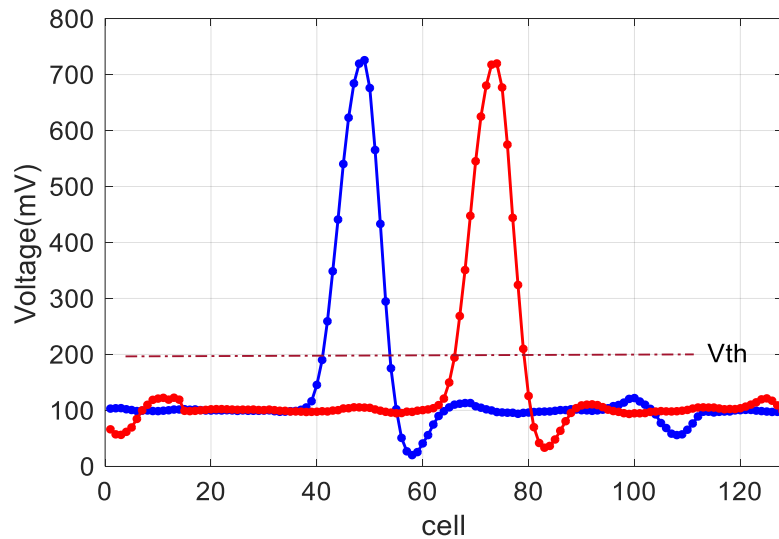
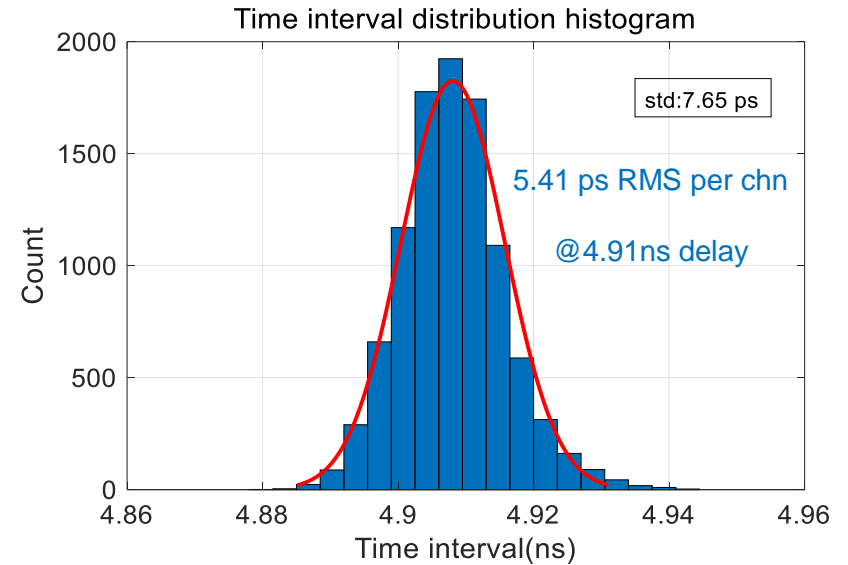
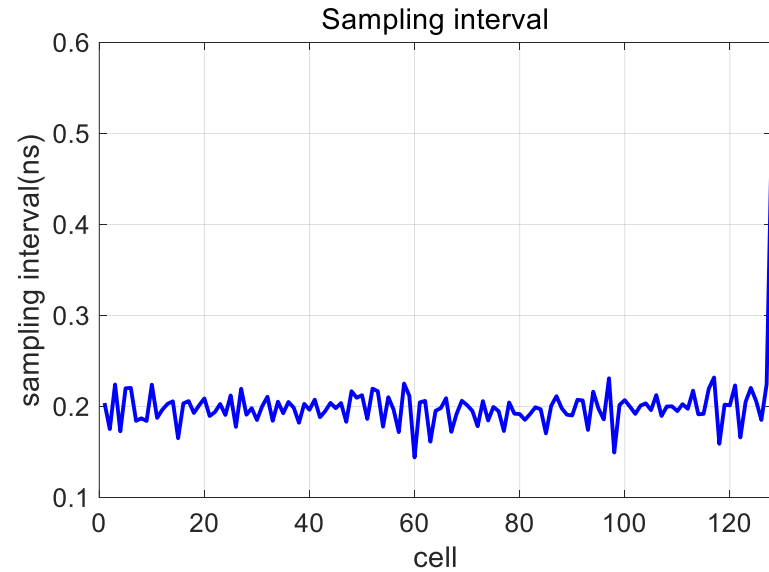
$$\alpha = \frac{V_{n_1+1} - V_{DC}}{\Delta V_{n_1}}, \beta = \frac{V_{DC} - V_{n_2}}{\Delta V_{n_2}} \quad (2)$$



- α and β are voltage ratio, slightly affected by amplitude attenuation

$$\begin{pmatrix} 0 & \dots & 0 & \underline{\alpha_1} & 1 & \dots & 1 & \underline{\beta_1} & 0 & \dots & 0 \\ 0 & \underline{\alpha_2} & 1 & \dots & 1 & \underline{\beta_2} & 0 & 0 & 0 & \dots & 0 \\ \dots & 1 & \underline{\beta_3} & 0 & 0 & \dots & 0 & 0 & \underline{\alpha_3} & 1 & \dots \\ \vdots & & & & & & & & & & \\ 1 & \dots & 1 & \underline{\beta_M} & 0 & 0 & \dots & 0 & \dots & 0 & \underline{\alpha_M} \end{pmatrix} \cdot \begin{pmatrix} \Delta t_1 \\ \Delta t_2 \\ \Delta t_3 \\ \vdots \\ \Delta t_N \end{pmatrix} = \begin{pmatrix} T_S \\ T_S \\ T_S \\ \vdots \\ T_S \end{pmatrix} \quad (3)$$

Preliminary test results



Summary

- DRS4 based fast timing electronics
 - Prototype consists of an AFE and a 16-channel WDM
 - Better than 10 ps RMS timing resolution is achieved for MRPC signal from 5 mV to 50 mV
 - Better than 10 ps RMS for PICOSEC-Micromegas, detailed measurements should be done
- SCA ASIC
 - Preliminary test has been done
 - ✓ 5 Gsps sampling rate
 - ✓ < 1 mV RMS noise
 - ✓ timing resolution < 10 ps RMS @ 5 ns & 25 μ s
 - Detailed measurements to be done
 - Differential Input SCA ASIC to be measured



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Thank you for your attention