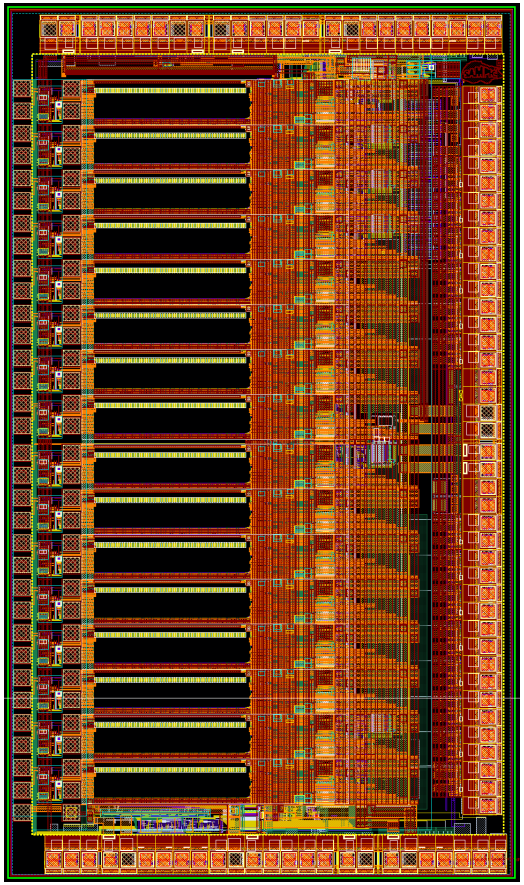

UPDATE ON SAMPIC DEVELOPMENTS

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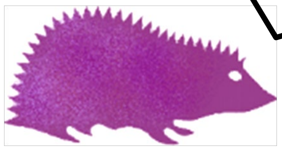
The *TICAL* ERC project (grant number 338953 from EU; PI: Paul Lecoq) has also contributed to the developments of the TOT features integrated in the chip

INTRODUCTION

- I would like to measure the time precisely …
- I have quite a lot of channels …
- I have a reasonable counting rate …
- I have limited money …
- …and I really would like to see the shape of my signals!

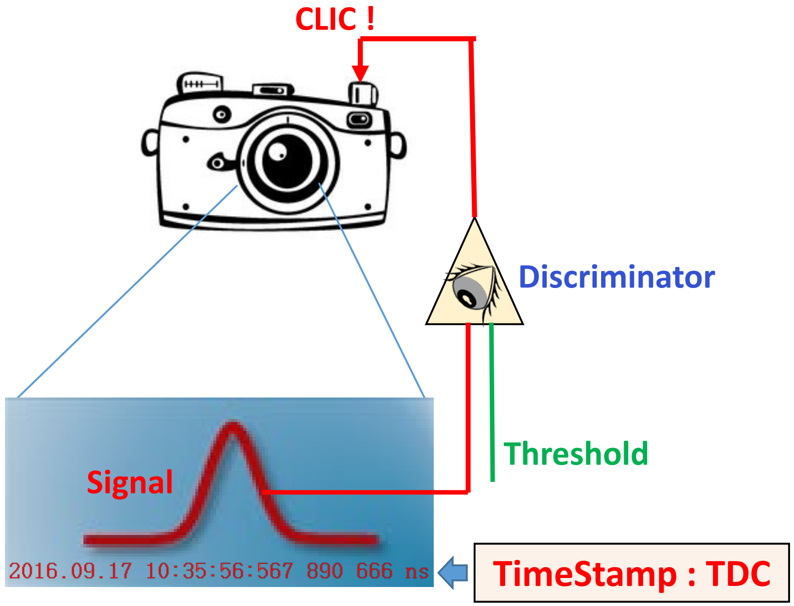
A trade-off would be **a TDC providing just the adequate slice of Waveform** …

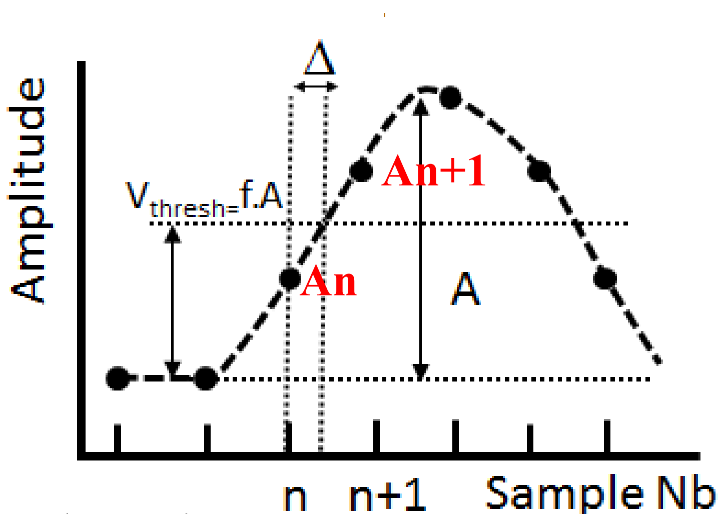


The « Waveform TDC » Concept (WTDC)

WTDC: a TDC which also permits **taking a picture of the real signal**. This is done via sampling and digitizing only the interesting part of the signal.

Based on the digitized samples, making use of **interpolation** by a digital algorithm, fine time information will be extracted.





$$t_0 = (n + \Delta) * T_s$$

$$\text{with } \Delta = \frac{f*A - A_n}{A_{n+1} - A_n}$$

- Advantages:

- Time resolution ~ **few ps rms**
- **No "time walk" effect**
- Possibility to extract other **signal features**: charge, amplitude…
- **Reduced dead-time**…

- But:

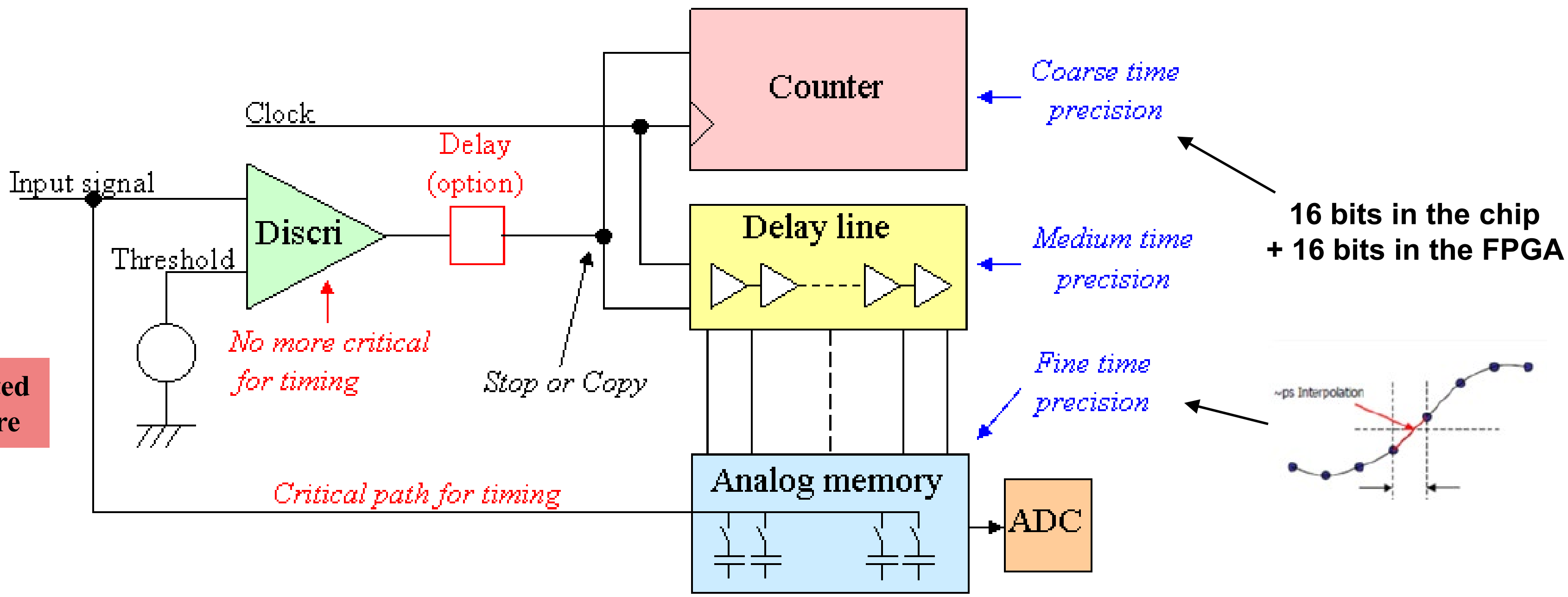
- waveform conversion (200 ns to 1.6 μs) and readout times don't permit counting rates as high as with a classical TDC

- **Mix of DLL-based TDC and of analog-memory based Waveform Digitizer**

- The TDC gives the time of the samples and the samples give the final time precision after **interpolation** => **resolution of a few ps rms**

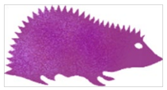
- Digitized waveform gives **access to signal shape**…

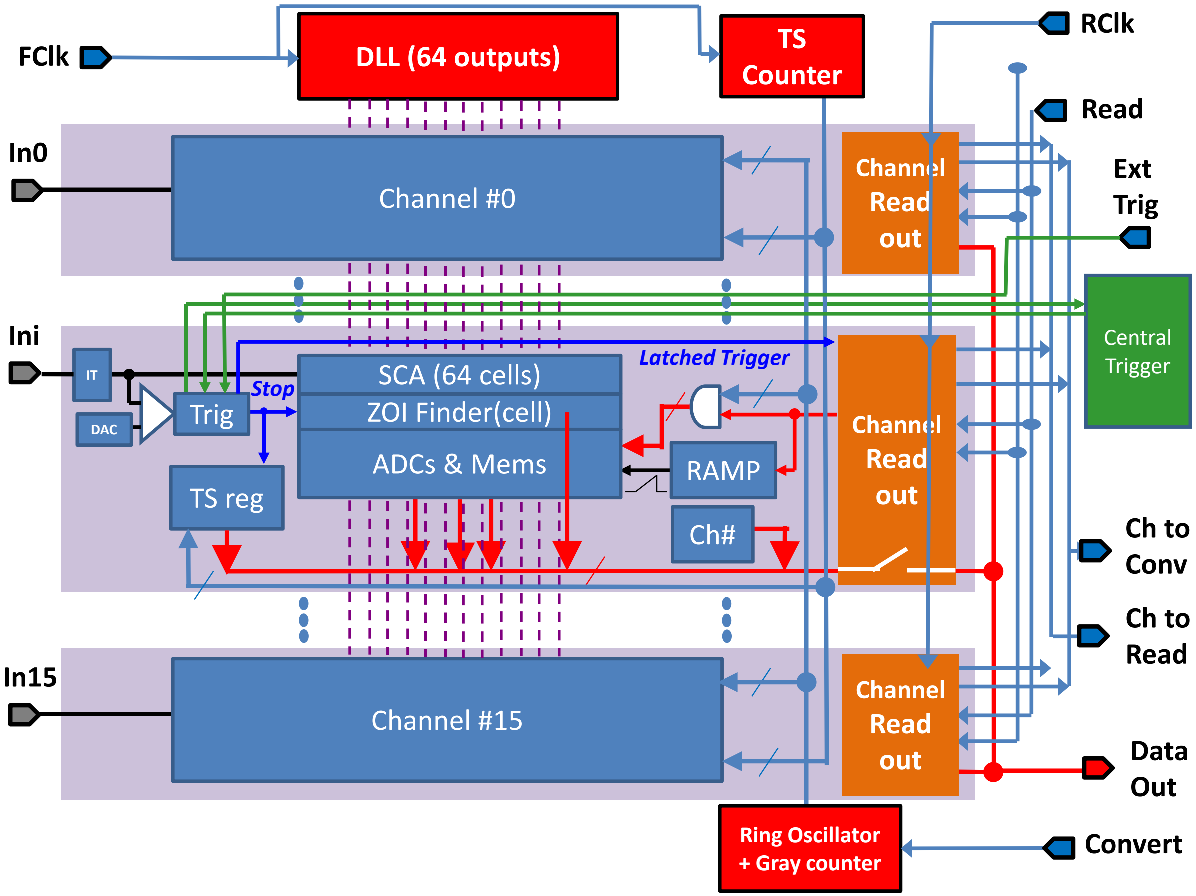
- Conversely to TDC, discriminator is used only for triggering, **not for timing**



© Patented Structure

Global architecture of the SAMPIC WTDC





- **One Common 16-bit Gray Counter** (FClk up to 160MHz) for **Coarse Time Stamping (TS)**.

- **One Common servo-controlled DLL**: (from 0.8 to 8.5 GS/s) used **for medium precision timing & analog sampling**

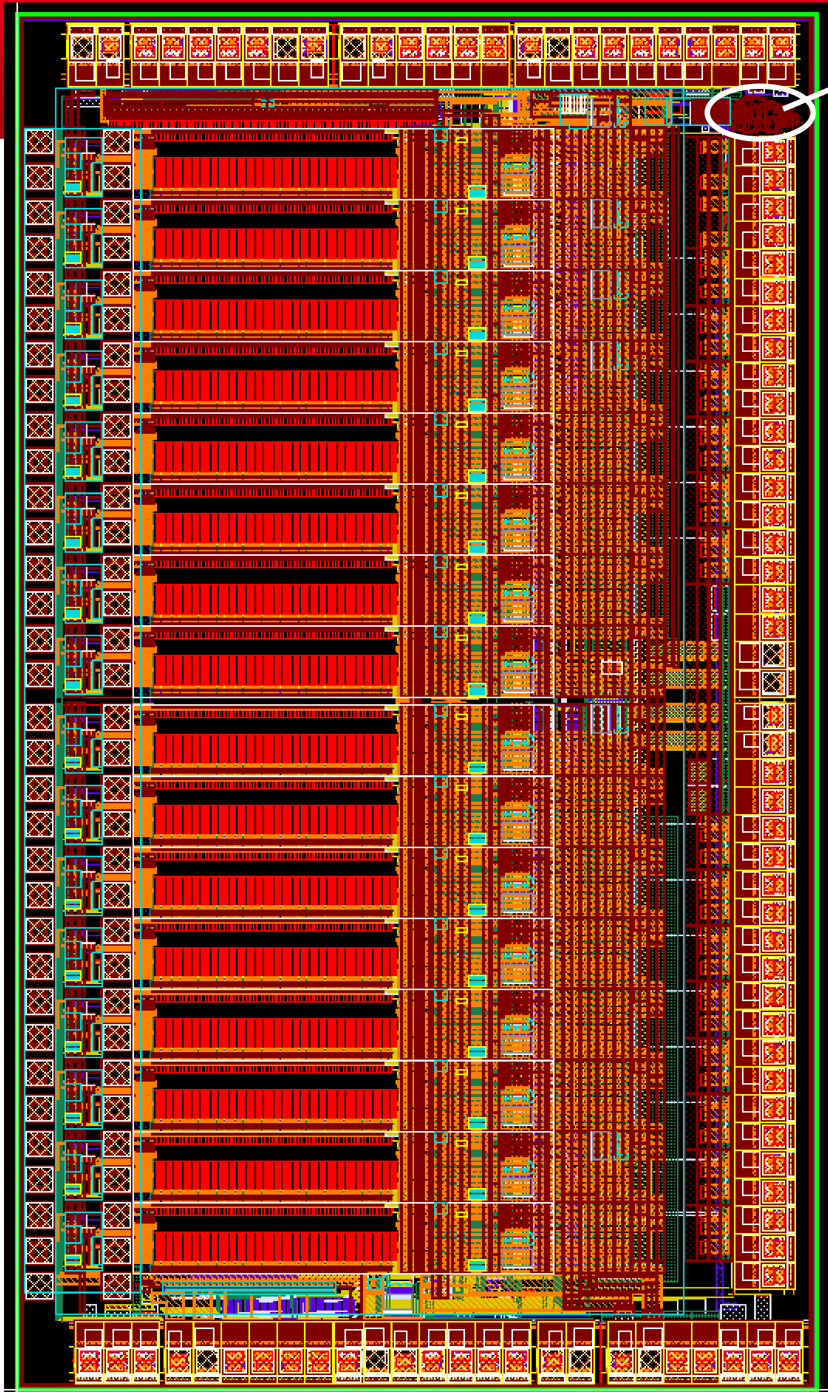
- **16 independent WTDC channels each with :**
  - ✓**1 discriminator for self triggering**
  - ✓**Registers to store the timestamps**
  - ✓**64-cell deep SCA analog memory**
  - ✓**One 11-bit ADC/ cell**

  (Total : 1024 on-chip ADCs)

- **One** Central Trigger block

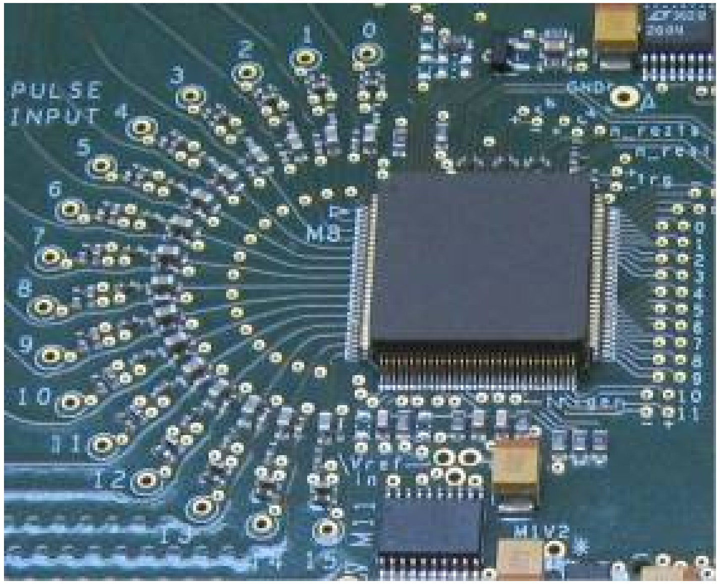
- **One** common 1.3 GHz oscillator + counter used as timebase for all the **Wilkinson A to D converters**.

- **Read-Out interface: 12-bit LVDS bus running at > 160 MHz (> 2 Gbits/s)**
- **SPI Link** for Slow Control



SAMPIC (V3)

- Most produced version is V3D (should have been called V4) submitted in December 2017 but received only in January 2019
- 1300 chips have been packaged in 128-pin plastic TQFP package



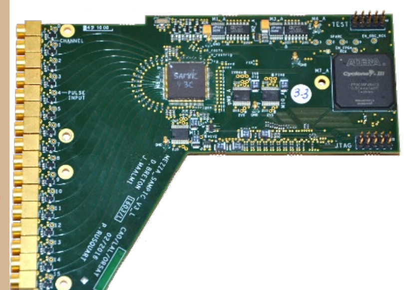
- Technology: **AMS CMOS 180nm**
- Surface: 8 mm^2
- Package: QFP 128 pins, pitch of 0.4mm

MODULE DEVELOPMENTS

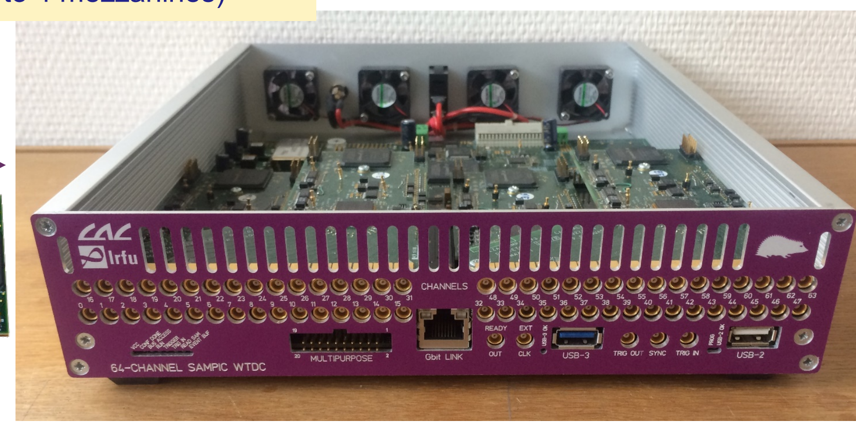
- Based on users request, we developed **many different types of modules** in order to offer a wide range of channel number and connectivity options
- They all make use of the motherboards also developed for the **WaveCatchers**.
- **16-, 32-, 48- and 64-channel** modules are available.
- Acquisition through **Gbit Ethernet UDP** (RJ45 or Optical), **USB2** and soon **USB3**

16 or 32-channel module
(1 or 2 mezzanines)

16-channel mezzanine



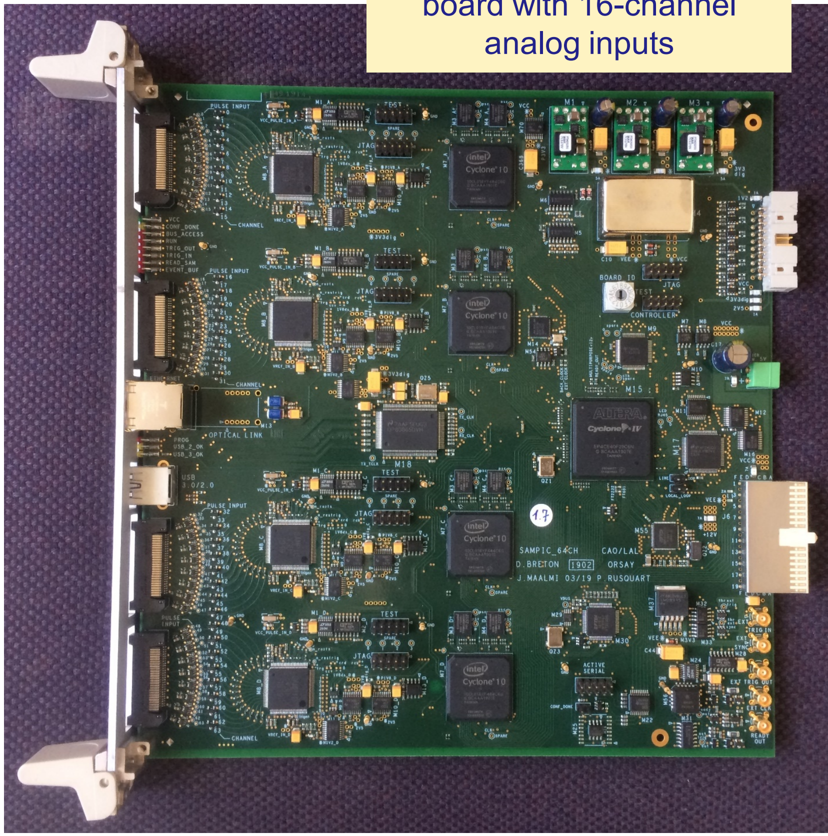
64-channel module with individual MCX inputs (up to 4 mezzanines)



64-channel module with 16-channel input connectors (can be analog or differential digital)

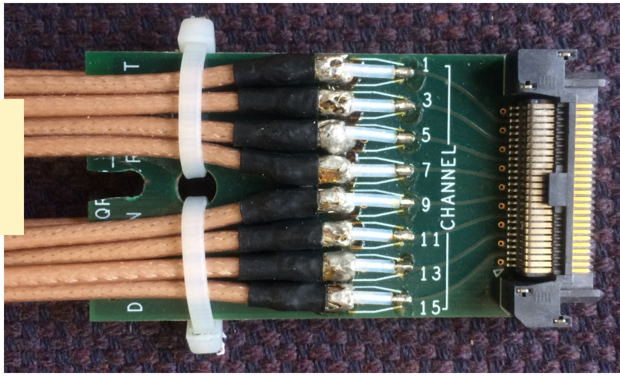
LAST DEVELOPMENTS

- In order to build systems with more channels, a **64-channel board** has been developed.
- It makes use of SAMTEC QRF8 16-channel input connectors (very low crosstalk)
- **256-channel mini-crates** (standard and compact versions) have also been developed based on this new board.
  - A new control and DAQ software has been developed together with a C library
- Central control board permits smart **2nd level triggering** and acquisition through **Gbit Ethernet UDP** (RJ45 or Optical), **USB2** and soon **USB3** (firmware work remaining)
- Time resolution at crate level remains **at ~5ps rms**.



64-channel integrated board with 16-channel analog inputs

256-channel crate



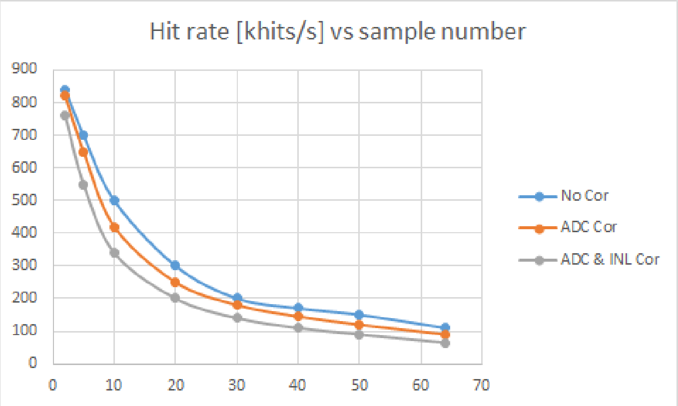
16-channel coaxial to SAMTEC QRM8 interface board

ACQUISITION SOFTWARE

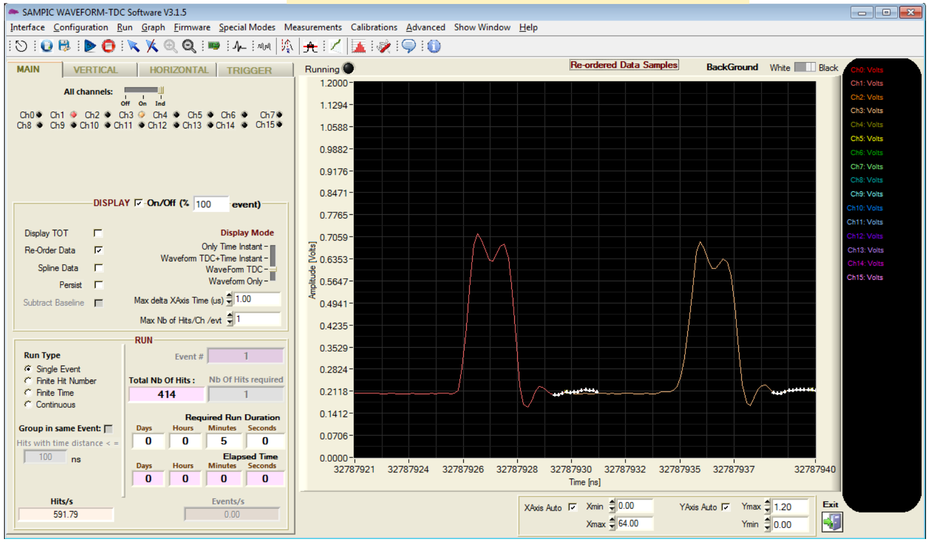
- **Acquisition software** has been developed up to 64 or 256 channels (also C libraries)

=> full characterization of the chip & modules

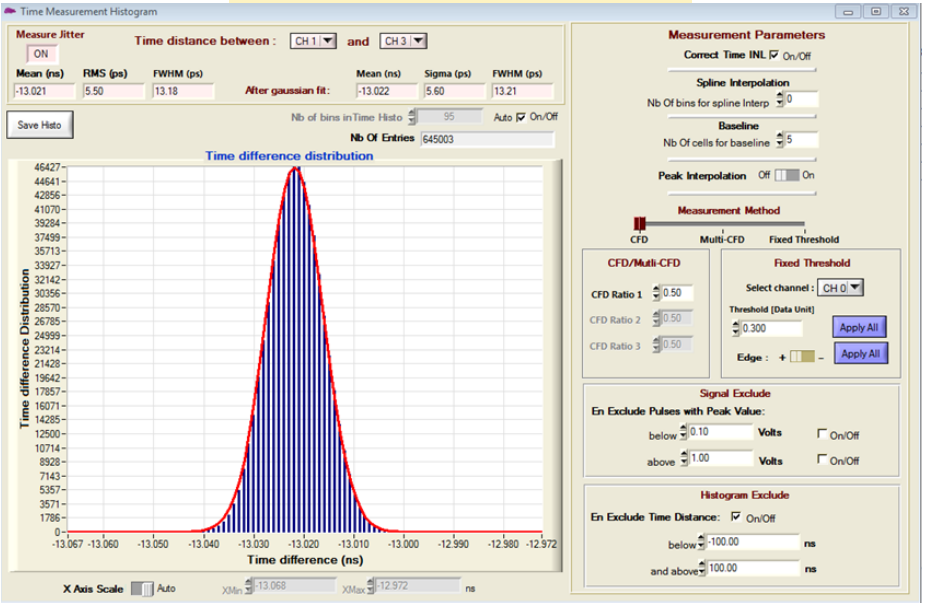
- **Special display** for **WTDC mode**
- Data saving on disk.
- Used by all SAMPIC users.
- A smart panel dedicated to time measurement is available. It permits selecting the parameters used for **extraction of time**
  - Optional spline interpolation on the peak area and on the threshold area
  - Fixed threshold option
  - CFD: ratio, nb of applied thresholds (1 to 3)
- **Recorded hit rate** depends on: the number of waveform samples, the corrections applied (ADC, Time INL), the mode for saving on disk (ASCII, binary)...



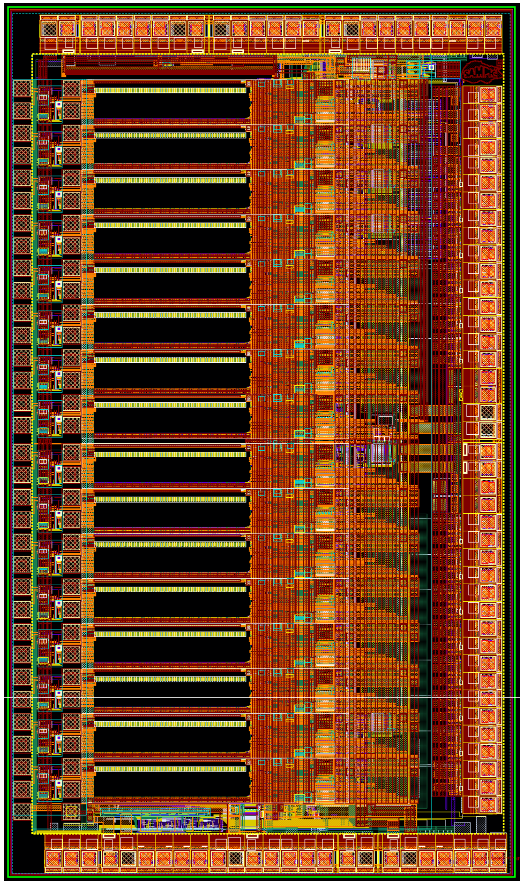
Main panel



Time Measurement panel



RECENT ASIC DEVELOPMENTS

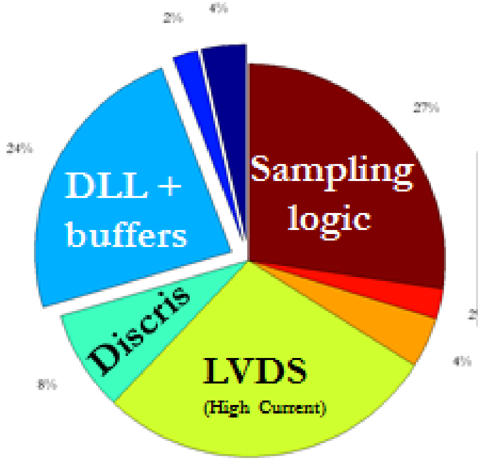


SAMPIC_V5
(TSI 0,18µm technology)

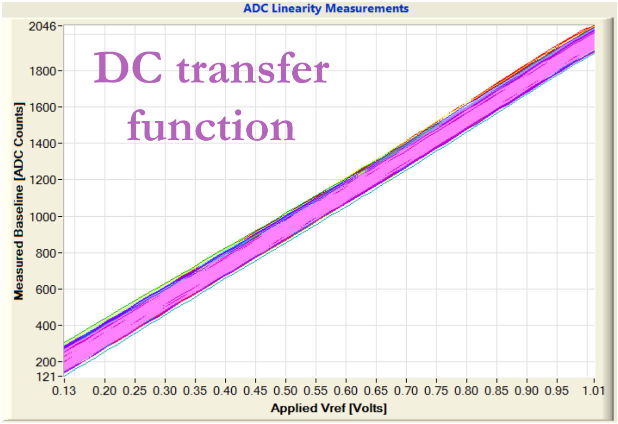
- Due to the (temporary ?) stop of the CMOS 0.18µm technology at AMS, we looked for equivalent ones.
- **TSI Microelectronics** is also proposing his own version of the former IBM CMOS 0.18µm technology, with some rule differences with AMS on the top metal layers.
- **We migrated** the design to TSI technology => **SAMPIC_V5**.
- We took benefit of this new submission for improving some historical weaknesses (sampling at 10.2 GS/s, first sample, linearity of posttrig delays, internal calibration of ADC, version register, …)
- We also designed **a second version dedicated to slower sampling,** covering the range **between 350MS/s and 2GS/s**.
  - Fully pin to pin compatible. Only difference is the main clock frequency.
- Both versions submitted in January 2021. Back in May (very effective work of TSI), packaged end of May => **hot from oven!**
- **Both work as expected!**

SAMPIC GLOBAL PERFORMANCES (V3-V5)

- Power consumption: **~10mW/channel** → Power distribution

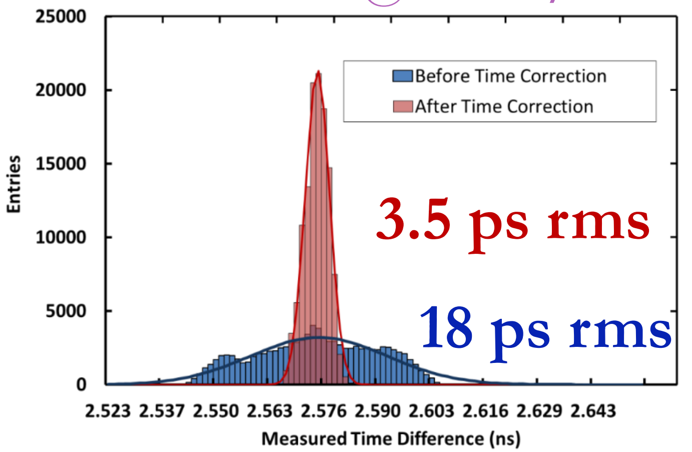


- 3dB bandwidth > **1 GHz**
- Sampling rate up to **8,5 (10.2) GS/s**
- Discriminator noise **~ 2 mV rms**
- Counting rate **> 2 Mevts/s** (full chip, full waveform), up to 10 Mevts/s with Region Of Interest (ROI)
- Wilkinson ADC conversion @ **~1 (1,45) GHz**
  - Dynamic range of **1V**
  - Gain dispersion between cells ~ **1%** rms
  - Non linearity **< 1.4 %** peak to peak
  - After correction of each cell (linear fit): noise = **0.7** (10GS/s) **to 1.3 mV rms** (1.6 GS/s)



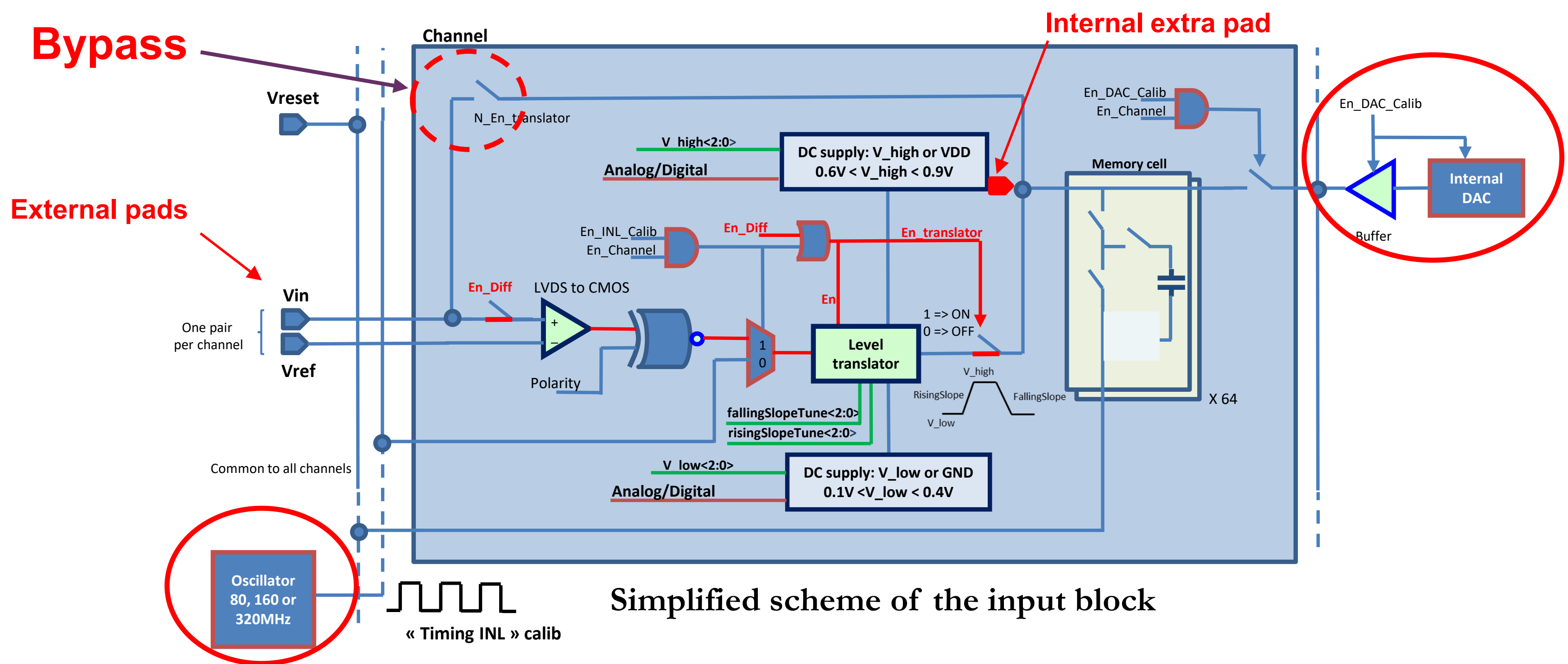
- Time Difference Resolution (TDR):
  - Raw non-gaussian sampling time distribution due to DLL non-uniformities (TINL)
  - Easily **calibrated & corrected** (with our sinewave crossing segments method [D. Breton&al, TWEPP 2009, p149])
  - TDR goes from ~ **< 5** (10GS/s) **to ~18 ps rms** (1.6 GS/s)

Ex: TDR @ 6.4 GS/s



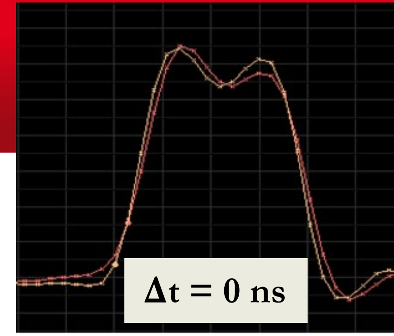
SAMPIC INPUT BLOCK (FROM V3)

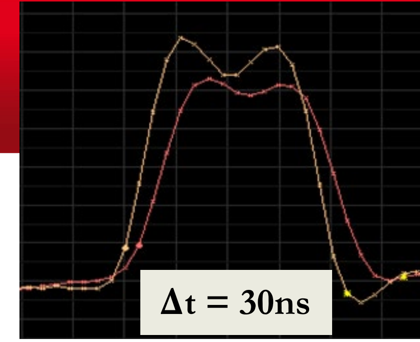
- **Translator input block** :
  - **Input signal can feed the memory directly** (**Bypass Mode**) or pass through a **translator block**
  - It permits among others:
    - **Self calibration of the chip (amplitude & time)**
    - Compatibility with **digital unipolar & differential signaling**
- **When fixed amplitude** at translator output → we only need to read a **few samples** (ROI) and fast conversion can be used (≤ 8 bits) => behaves like a TDC



Simplified scheme of the input block

TIME RESOLUTION:
External vs Self Calibration

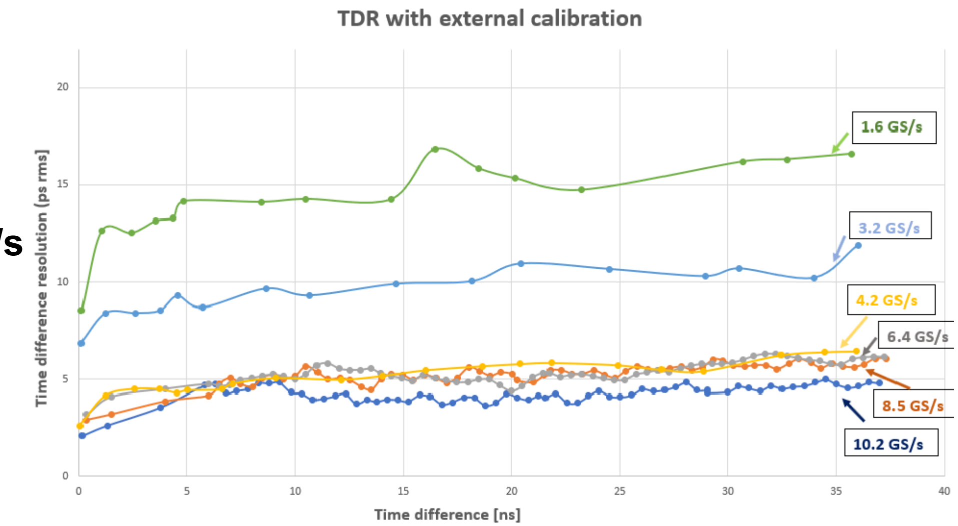




- The DLL has been re-worked for improving the resolution for the **lower sampling frequencies**

(3 different sizes of starving transistors can be selected in the main DLL in order to optimize its INL and jitter)

- Delays made by a cable box => rise time degrades with delay …
- With external time-calibration :
  - A TDR of **~5 ps rms** for **4.2< Fs<8.5 (10,2) GS/s**
  - **TDR < 10 ps rms** for **3.2 GS/s**
  - **TDR < 18 ps rms** for **1.6 GS/s**
- With **self-calibration**
  - Limited jitter degradation (~20%)
  - Permits **full integration** in **compact detection systems …**

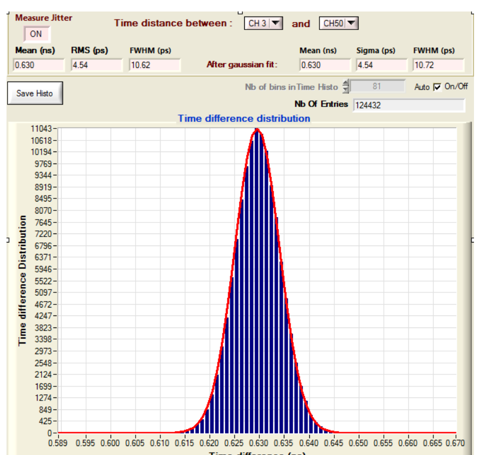


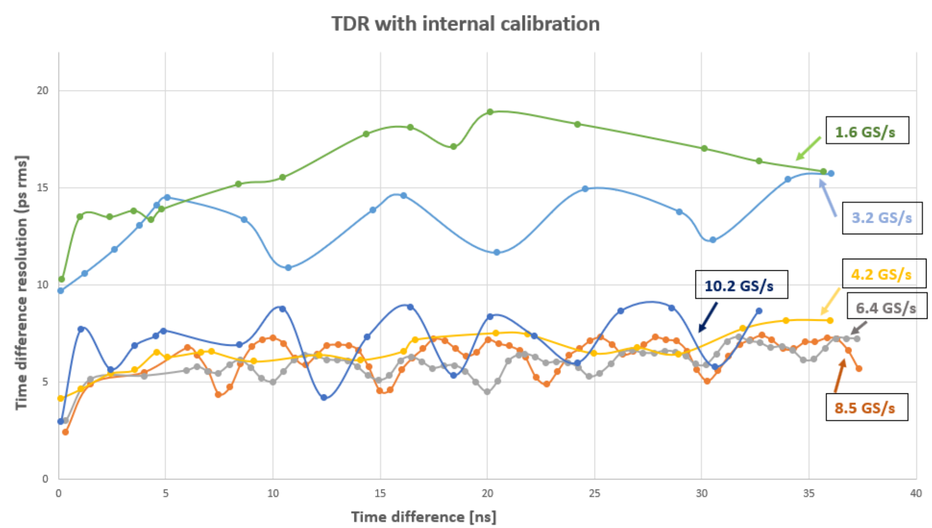
- **Between 2 chips**:

@ Fs = 6.4 GS/s

Δt = 0.63 ns

=> **TDR = 4.5 ps rms**





TIME RESOLUTION (DIGITAL CFD) VS SIGNAL AMPLITUDE

- ADC conversion time can be reduced (by decreasing the resolution): factor 2 for 10 bits (800 ns), 4 for 9 bits (400 ns), 8 for 8 bits (200 ns), 16 for 7 bits (100 ns).

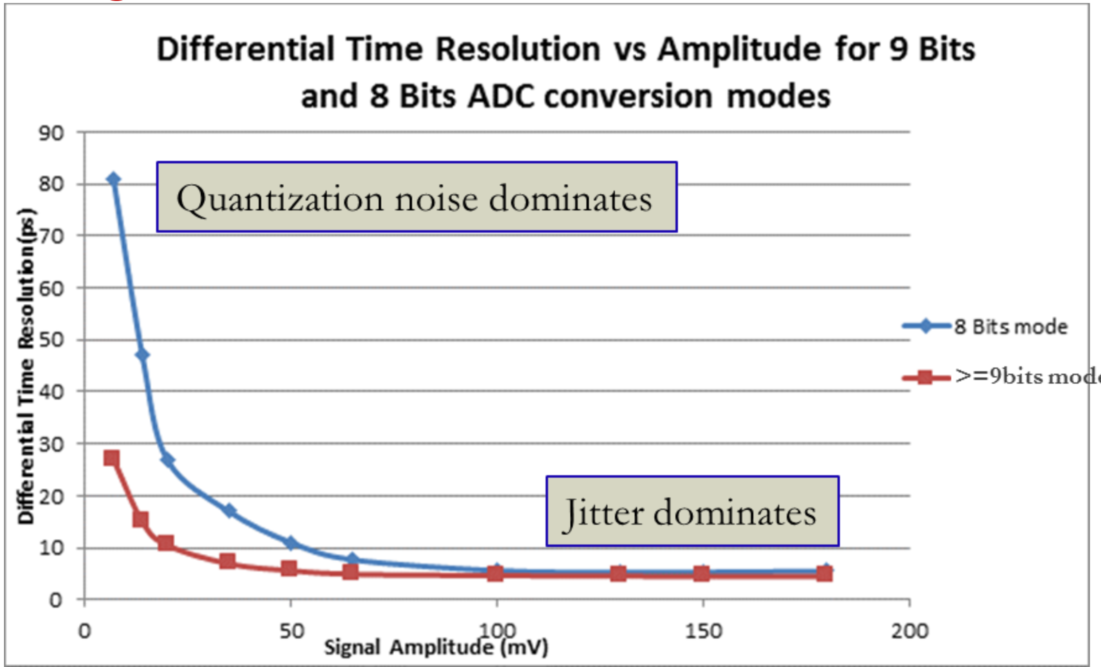
➔ decrease of channel instantaneous dead time

- The quantization noise could affect the timing precision especially for small signals

But QN= 400µVrms for 9bit mode negligible compared to SAMPIC noise = 950µVrms

- **As expected no significative change measured for 11, 10 and 9-bit modes**

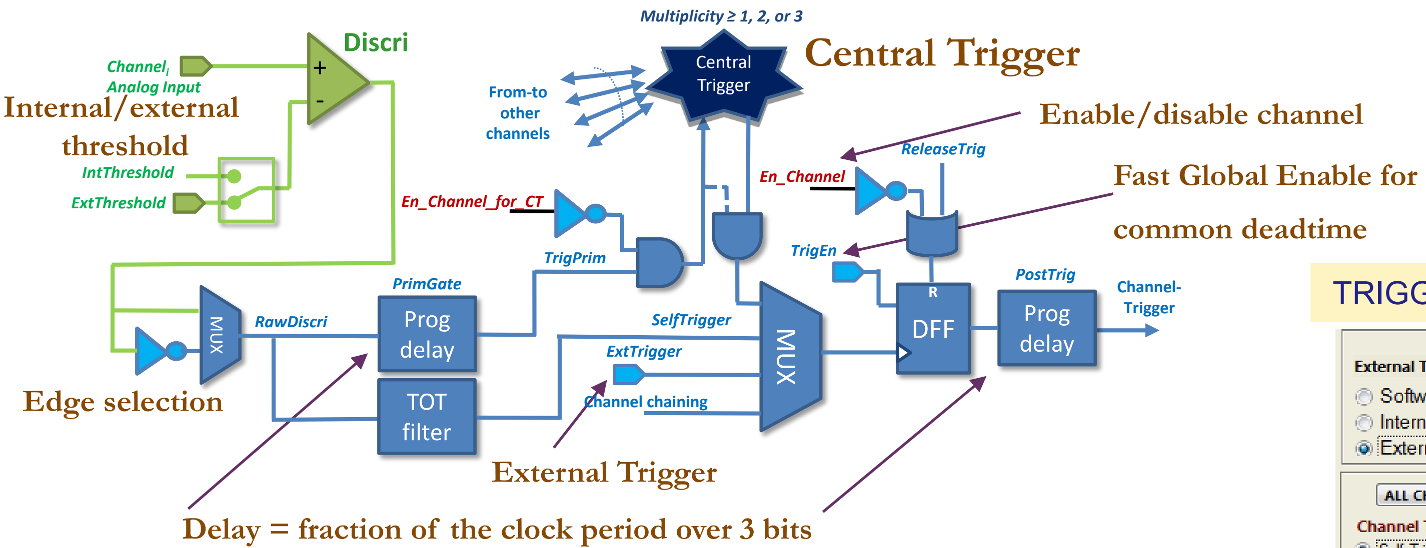
No degradation on timing for pulses above 100mV for 8 bits



NEED FOR EVENT FILTERING…

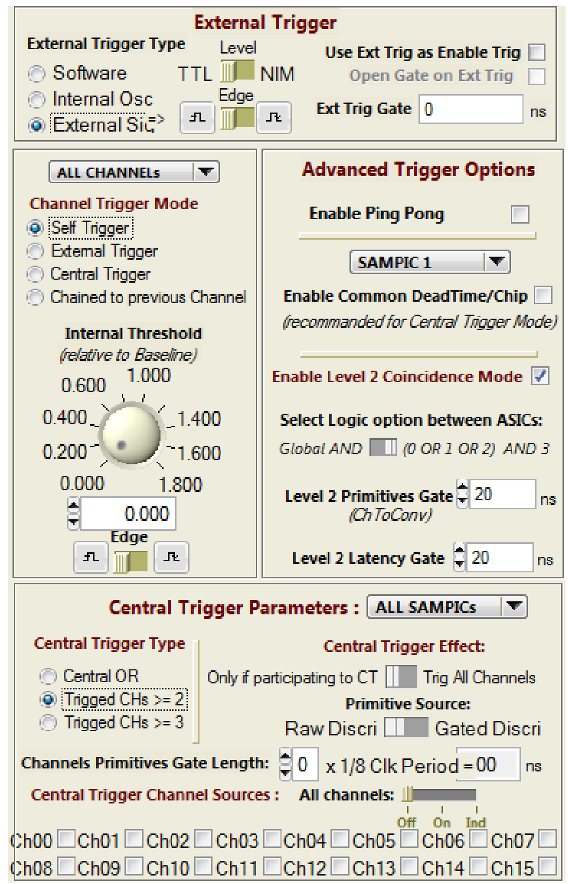
- Whatever the application, it is mandatory to find ways to **reject the wrong events** as early as possible in the readout chain in order to keep the dataflow at a reasonable level.
- Like a standard TDC, the Waveform TDC is natively **self-triggered** on each of its channels. This may produce very large hit rates, which may cause a saturation of the output buffers, especially since the waveforms have to be extracted (partially or in totality) together with the time information.
- In order to reduce the dataflow, it is necessary to filter the good events before conversion. A **central trigger located in the ASIC** can then help defining trigger conditions and drastically reducing the hit rate.
- Moreover, providing the adequate signals out of the chip permits performing in the surrounding FPGAs **a second level trigger** based on smarter detector conditions and increasing the counting noise rejection by a huge factor.
- Noise filters can also be based on the characteristics of the signals as produced by the different detectors. For instance, a **real time filter based on the TOT** has been implemented in SAMPIC. When used with signals issued from crystals and SiPMs, it permits rejecting above 99% of the dark count noise from the SiPMs.

INTERNAL TRIGGER SCHEME



- One **very low power** signal **discriminator/channel**
- One 10-bit DAC/channel to set the **threshold** (which can also be external)
- Programmable primitive gates
- Several trigger modes programmable **for each channel**
- **Central trigger with multiplicity up to 3**
- Possibility of **chaining** and **ping-pong** modes
- Available I/Os permit building **smart second level triggers**

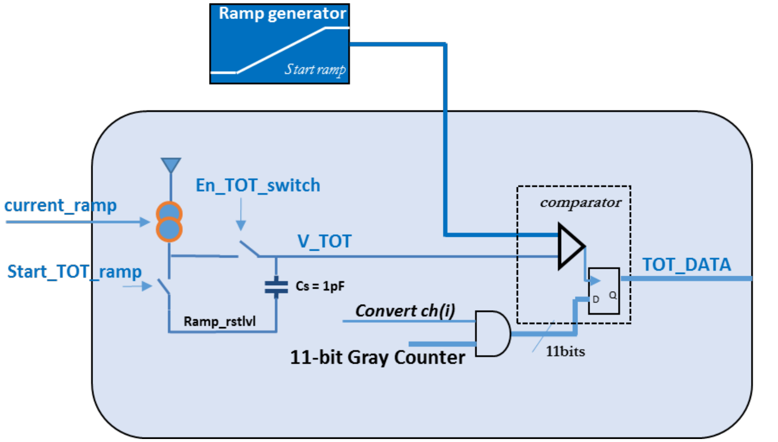
TRIGGER PANEL in the DAQ software

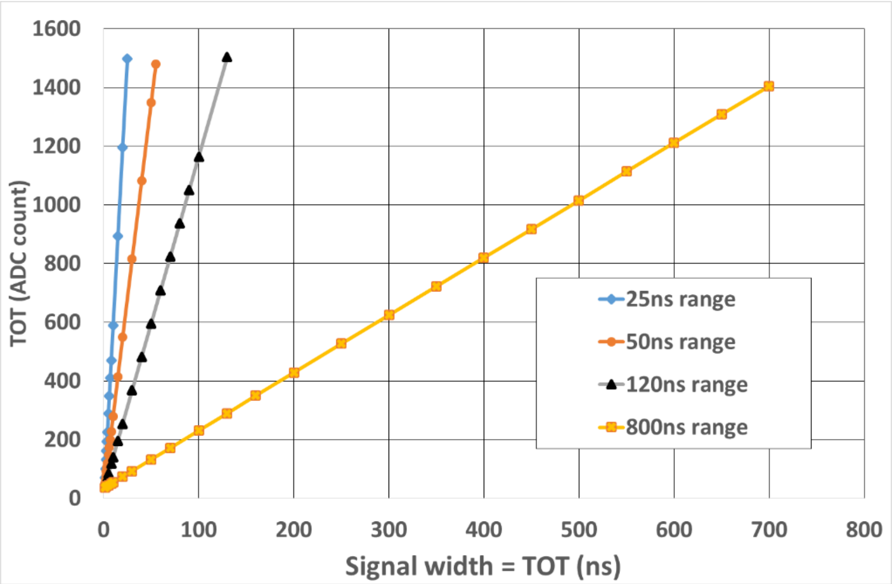


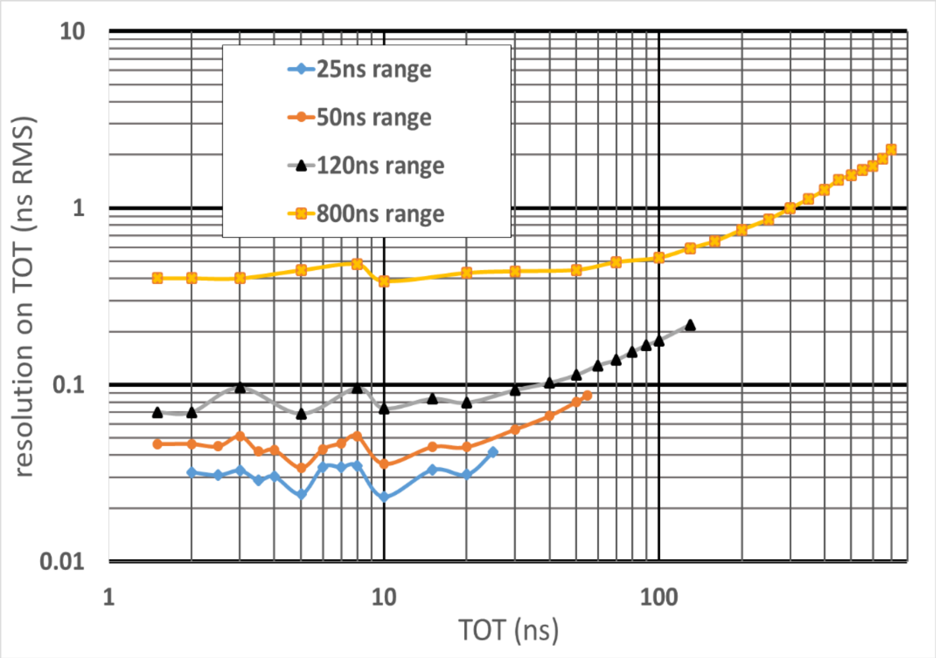
⚠ **Only the triggered channels are in dead time**

TOT MEASUREMENT

- SAMPIC is meant for digitizing a short signal, or only a small part of a longer one (eg rising edge) to extract the timing ➔ then **the other edge** is missed
- Addition of a **ramp-based** **Time to Amplitude Converter** for each channel seen as a 65th memory cell during digitization ~10bit TOT TDC →
- A **TOT-based filter** is also integrated in the chip



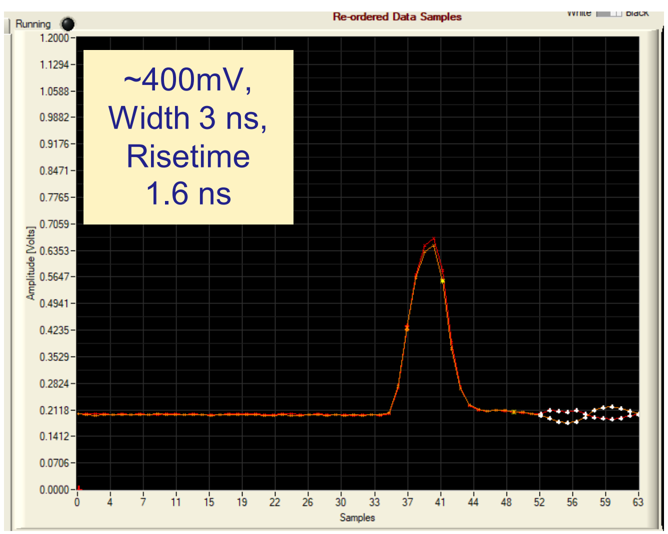


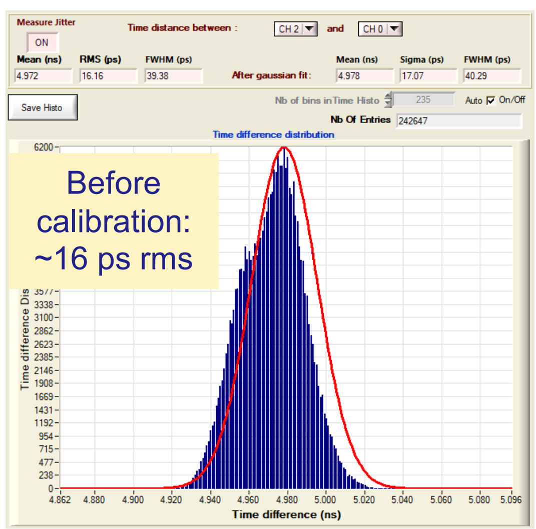


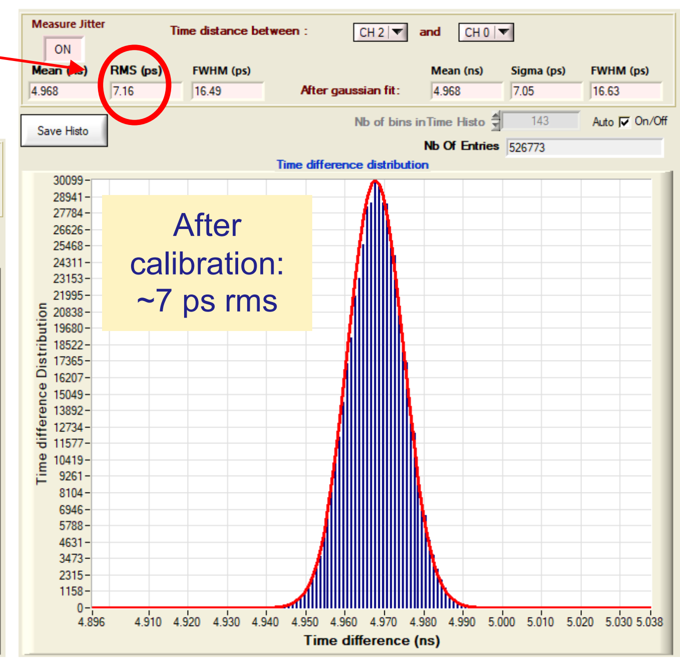
Measurement ranges between 2 and 700 ns.

SAMPIC_SLOW

- A second version dedicated to slower sampling has been developed.
  - **Wider window and high resolution** would permit effective multi-sample offline reconstruction
  - Pin to pin compatible with standard version. Only difference is the main clock frequency.
  - DLL optimized for running between 350MS/s and 2GS/s
  - All delays servo-controlled to main clock have been adapted
  - Analog memory cell has been enlarged
- First **very preliminary tests** are very encouraging.
  - TDR @ 1.6 GS/s < 10ps rms !
  - Noise @ 1.6 GS/s ~ 1.05 mV rms







SUMMARY OF MAIN FEATURES OF SAMPIC (from V3)

- Smart "central trigger" (OR, **multiplicity of 2 & 3**) with possibility of **common deadtime or selecting only channels participating in decision**
- **8-step full window PostTrig** (very useful for low frequencies)
- **Channel chaining option**: user-defined sets of channels can be chained in time.
- **"Ping-Pong" (toggling) mode:** channels work in pairs.
- **Integrated TOT measurement and trigger filter based on TOT**
- **All DACs necessary for controlling the chip are integrated**
  - ADC resolution **internally selectable between 7 and 11 bits**
- **Auto-conversion mode for ADC: the conversion can be automatically started when an event is detected, independently for each channel.**
  - Reduce the required external digital electronics
  - **But the handshake mode** with the FPGA **permits building 2nd and 3rd Level triggers based on many chips or boards for a common event selection**
- **Auto-calibration** (Time INL): dedicated signal sources are implemented in the chip in order to perform time INL calibrations in standalone.

TAKING DATA WITH DETECTORS

- SAMPIC modules are already used with different detectors on **test benches or test beams.** A lot of examples were already presented at the **WaveCatcher and SAMPIC Workshop** in February 2018 in Orsay **(second workshop soon ?).**
- Tested with **PMTs, MCP-PMTs, APDs, SiPMs, fast Silicon Detectors, Diamonds**: performances are equivalent to those with high-end oscilloscopes
- Different R&Ds ongoing with the **TOF-PET** community (CERN, IRFU, IN2P3…)
- SAMPIC is used for many test beams **at CERN**
- **TOTEM** has developed a CMS-compatible motherboard housing SAMPIC mezzanines. 192 measurement channels are in use on the LHC.
- SAMPIC is the baseline readout option for **many detectors** of the **SHIP and SND@LHC** collaborations**.**
- Used for the readout of the **new LiquidO detector R&D concept**
- Used for **T2K** near detector Upgrade: 256-channel **Timing Detector**.
- Used by **Photek** for characterization of new ultra-fast MCP-PMTs (IEEE paper)
- Used by **University of Kansas** for satellites test benches at **NASA.**
- …

SUMMARY

- SAMPIC is a full **System On Chip**:
  - Analog or digital input, fully digital output, sampling from 1.6 to 10.2 GS/s
  - All the DACs and calibration generators are integrated
  - It just requires power, clock, and a simple interface with an FPGA
  - Small power consumption ~10 mW/channel
  - All the channels can be fully independent
  - Raw counting rate can go >> 100 kHz/ch.
  - Large choice of smart triggers
- It can be used for a highly integrated tiny module (cm³) as well as for large scale detectors (nuclear or high energy physics, TOF-PETs, …).
- Successful migration to TSI 0.18µm (also sourced from IBM 0.18µm)
- **A second version has been designed for slower sampling**

  => ~350 MS/s to ~2 GS/s
- Many types of **autonomous systems** have been developed: **16 to 256-channels**
- **Developments will be pursued** both on the chips and the systems…

SUMMARY

- Backup slides …

SAMPIC: PERFORMANCE SUMMARY

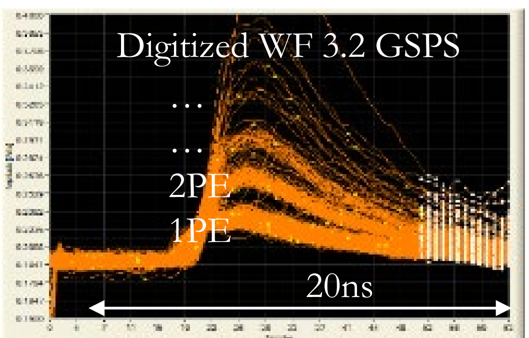
		Unit
Technology	AMS CMOS 0.18µm	
Number of channels	16	
Power consumption (max)	180 (1.8V supply)	mW
Discriminator noise	2	mV rms
SCA depth	64	Cells
Sampling speed	0.8 to 10.2	GSPS
Bandwidth	> 1	GHz
Range (unipolar)	~ 1	V
ADC resolution	7 to 11 (trade-off time/resolution)	bits
SCA noise	~ 1	mV rms
Dynamic range	> 10	bits rms
Conversion time	0.1 (7 bits) to 1.6 (11 bits)	µs
Readout time / ch @ 2 Gbit/s (full waveform)	< 450	ns
Single Pulse Time precision before correction (4.2 to 10.2 GS/s)	< 15	ps rms
Single Pulse Time precision after time INL correction (4.2 to 10.2 GS/s)	< 3.5	ps rms

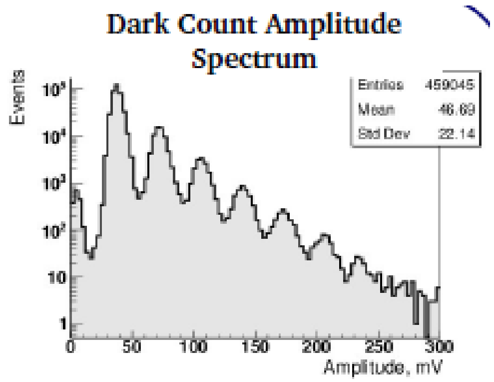
ON-CHIP TOT FILTER

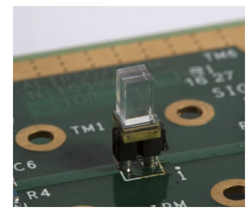
Initial request for SAMPET & funding by C. Williams (CERN+INFN) & K. Doroud (CERN)

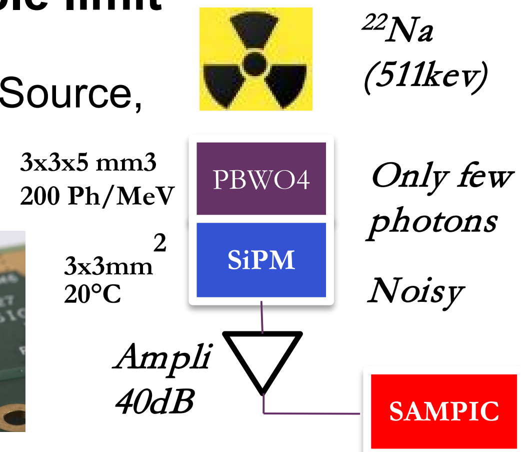
- **Goal: demonstrate the noise rejection capability using the TOT filter which rejects events with TOT < programmable limit**
- SiPM coupled to crystals (here KETEK SiPM + PbWO4 + ^{22}Na Source, **@ 20°C => 1PE ~ 40mV**
- Th = 20 mV (0.5 PE), **TOT_Filter OFF:**

=> 700 kHz rate of events / **4.5 MHz raw rate** (dark count)



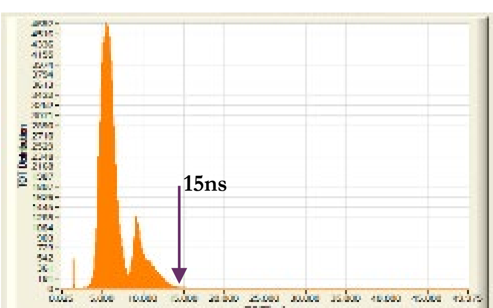




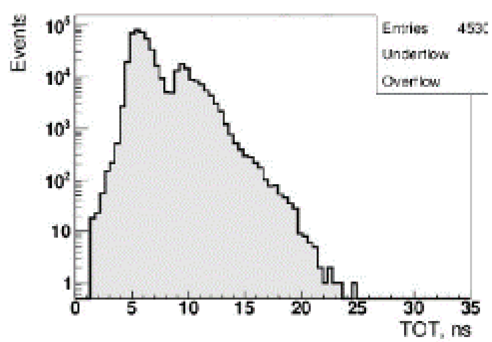


SiPM: KETEK PM3350TP-SB0
3x3 mm², 50µm pitch, trench design,
Operation @ 29V (2.5V overvoltage)

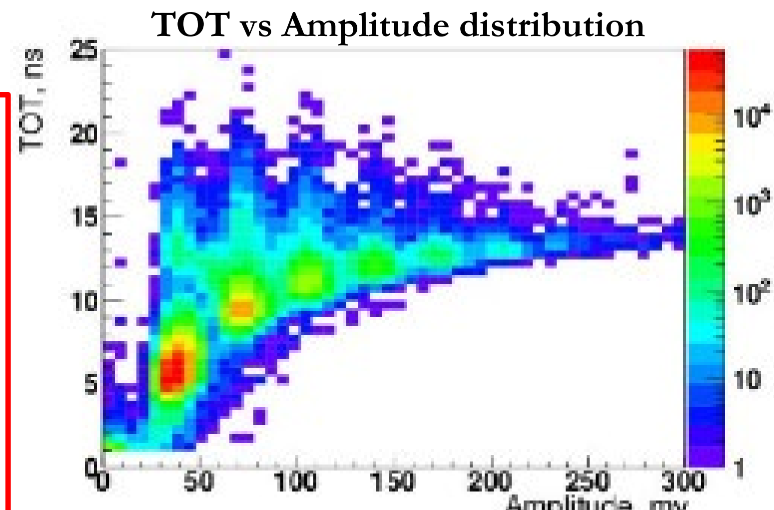
TOT spectrum (digitized by the chip)



Lin scale

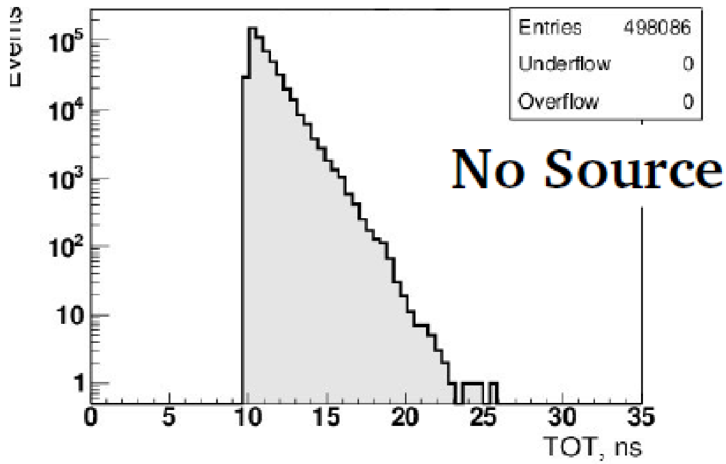


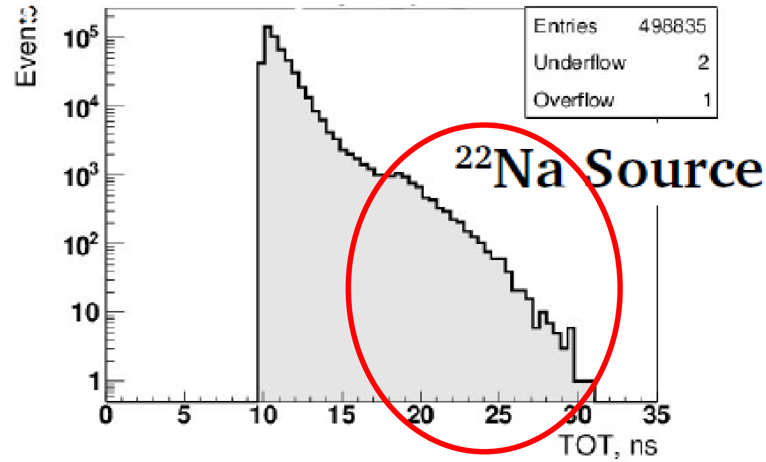
Log Scale



NEW IN SAMPIC V3 : ON-CHIP TOT FILTER
=> NOISE FILTERING

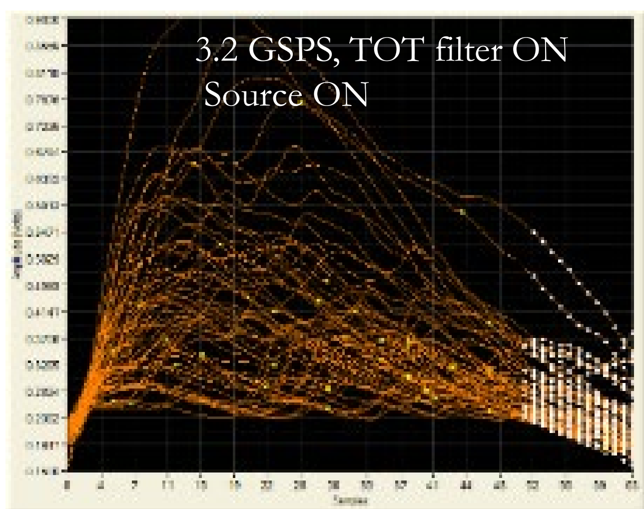
Threshold : 50 mV (1.25 PE), TOT filter = 10ns





TOT spectrum without source
(60kHz if TOT filter OFF)
60 Hz if TOT filter ON

TOT spectrum with source
(60kHz if TOT filter OFF)
200Hz TOT filter ON

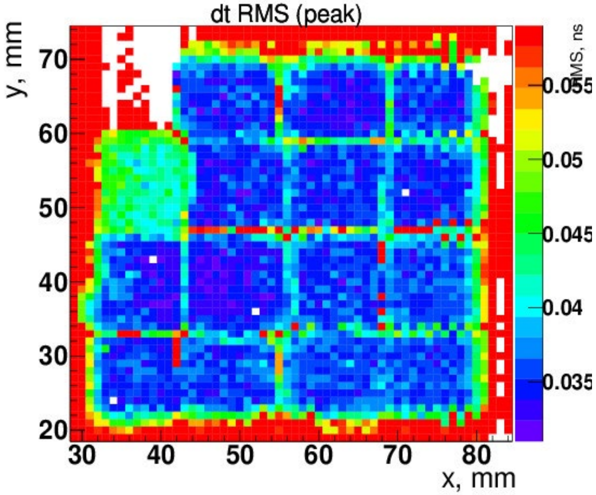


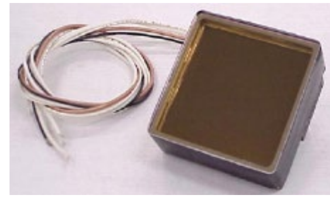
=> 140 Hz from source!

99.9% of the noise is rejected

SCAN TEST OF MCP-PMT © S. Sharyy

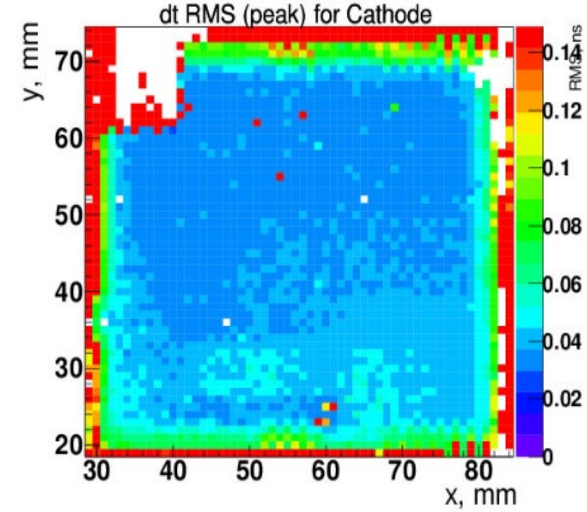
PMT resolution for anodes (ns rms)

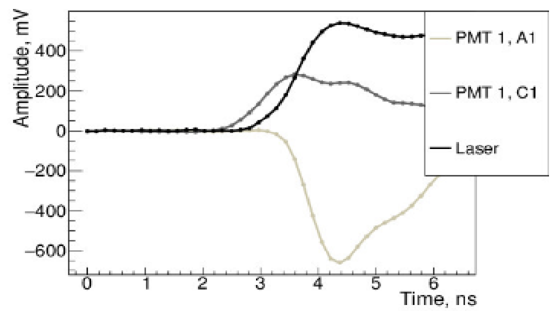




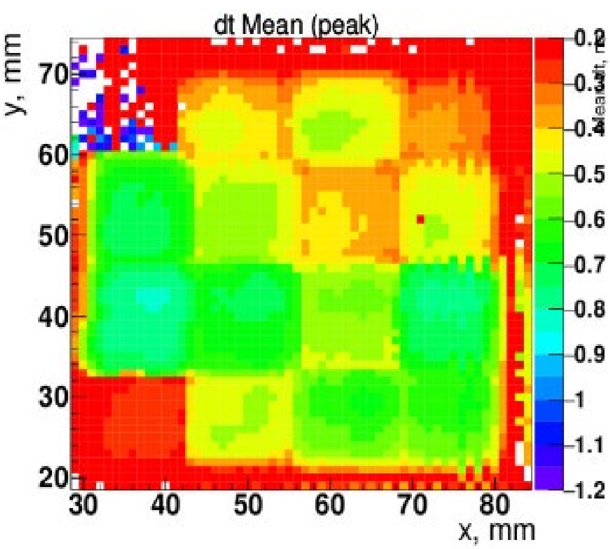
PLANACON XP85012 used for CALIPSO/PECHE: 64 channels grouped by 4.

PMT resolution for cathode (ns rms)





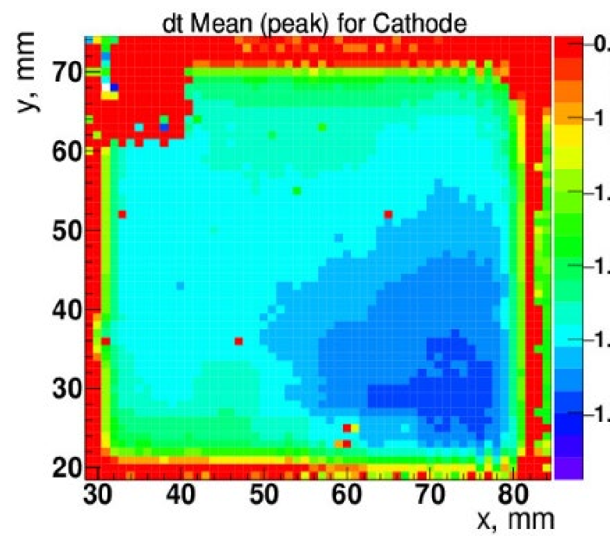
PMT delay for anodes (ns)



- We measure time difference between Laser and Signals.
- Step of 1mm, 2 sec / per stage, 0.5 sec / move
- SAMPIC in two-level trigger coincidence mode (anode & laser)
- Data taking rate: 50 kHz

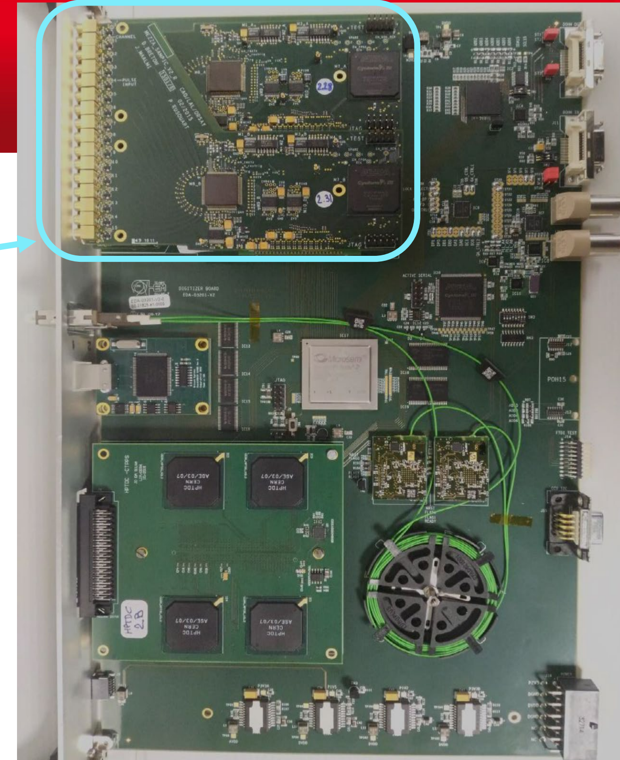
Total Scanning Time : only 2 hours!

PMT delay for cathode (ns)

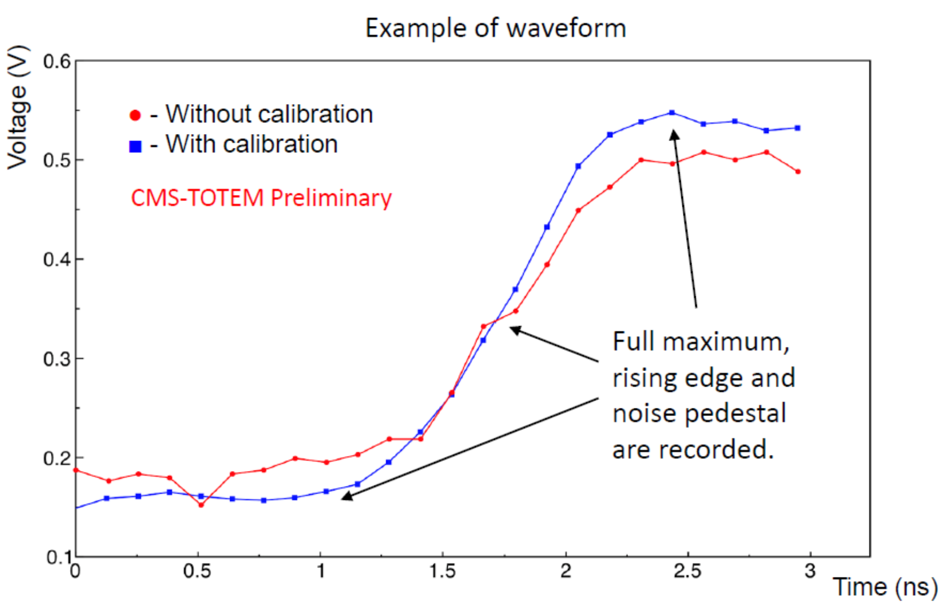


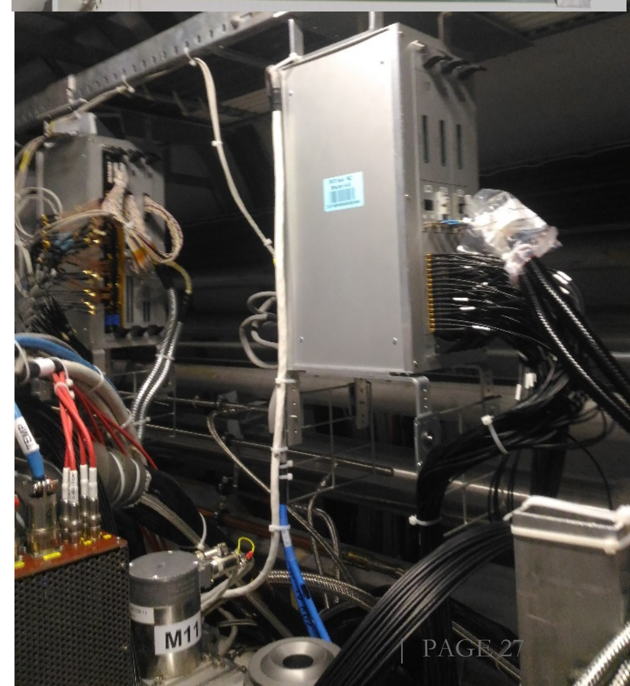
Same type of measurements have been performed by Photek => IEEE NSS 2019.

PROTON TIMING SYSTEM OF TOTEM (CMS) (© E.BOSSINI)



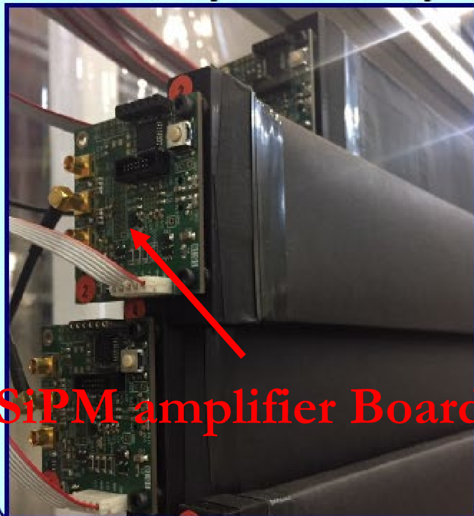
- **192 channels** of **SAMPIC mezzanines** were mounted **in the LHC tunnel** on motherboards especially designed by the **TOTEM** team, also housing HPTDCs
- The goal is to measure the **TOF of protons** from CMS vertex **with a precision of a few tens of ps**
- This permitted interfacing an almost standard SAMPIC firmware with the environment of the **CMS Trigger and DAQ**
- **Sampling frequency** was set to **7.8 GS/s** and ADC conversion to **8 bits**
- Waveform length was set to **24 samples**
- Hit rate per channel was close to **1 MHz**
- Calibration corrections were applied **offline**



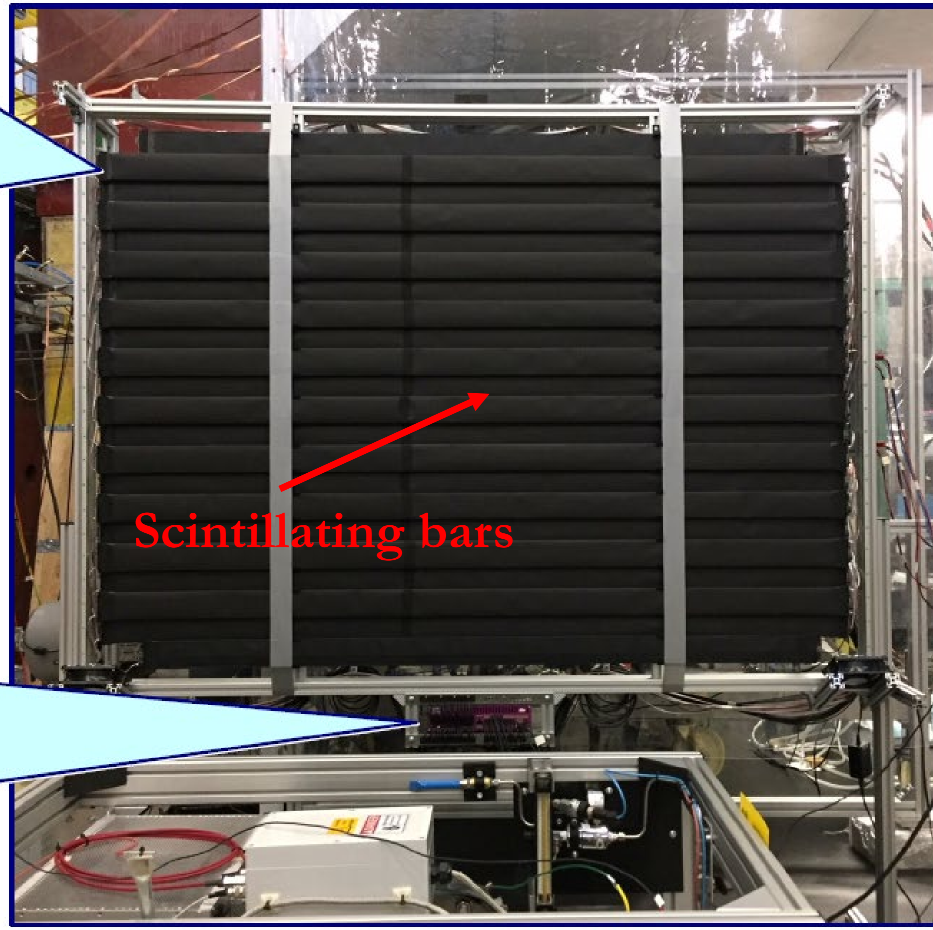


TIMING DETECTOR PROTOTYPE FOR SHIP (© A.KORZENEV)

Readout by SiPM-arrays



Testbeam Aug 15 – Sep 19, East hall T10 of CERN PS



Bar length 1.7m, 2 side readout, 80 ps time resolution
arXiv:1709.08972

64ch SAMPIC module

Same type of detector is being developed by Geneva Univ for T2K upgrade with 256 channels.