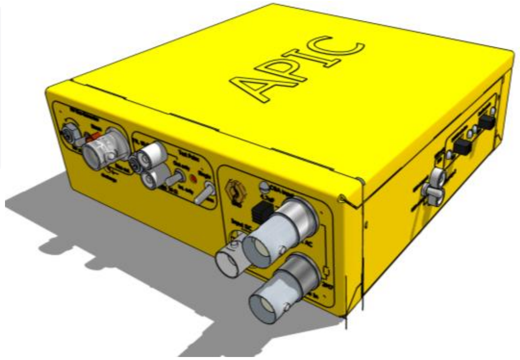
RD51 Collaboration



APIC
a study case for discrete detector electronics

RD51 Topical workshop on Front End electronics for gas detectors Tue 15th June – Thu 17th June 2021

Detector phase space <=> electronics

Detector capacity ($C_{det,}$ ENC noise)

➔ routing and signal transmission, low noise amplifiers, order-N noise filters

Source impedance (Q, V)

➔ preamp types and termination, over-Volt chip protection, AC –Dc coupling

feature extraction primary signal (x_0, t_0, Q, V)

➔ shaping, pole-Z matching, threshold vs. peak, linearity & dyn range,

EM-properties (electrons vs. ions, induced signals, fast and slow, polarities)

➔preamp type and polarity, adaptive baselines, sampling

Rates and recovery, pileup

➔ electronics-pileup & deadtime minimization, Fast OR & trigger generation

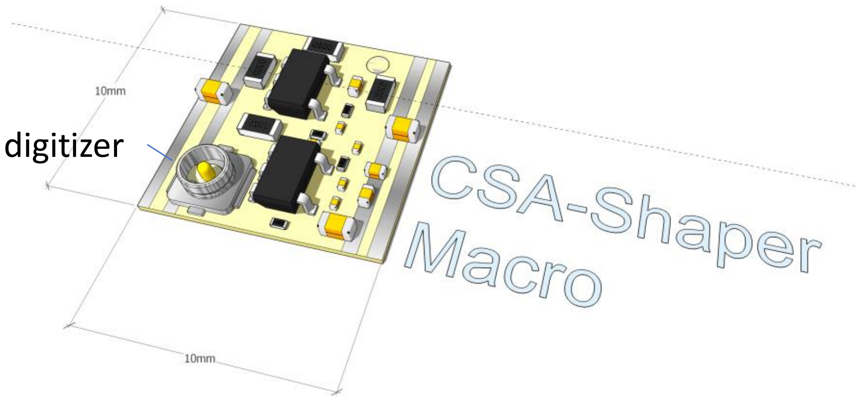
Signal confinement (x,y)

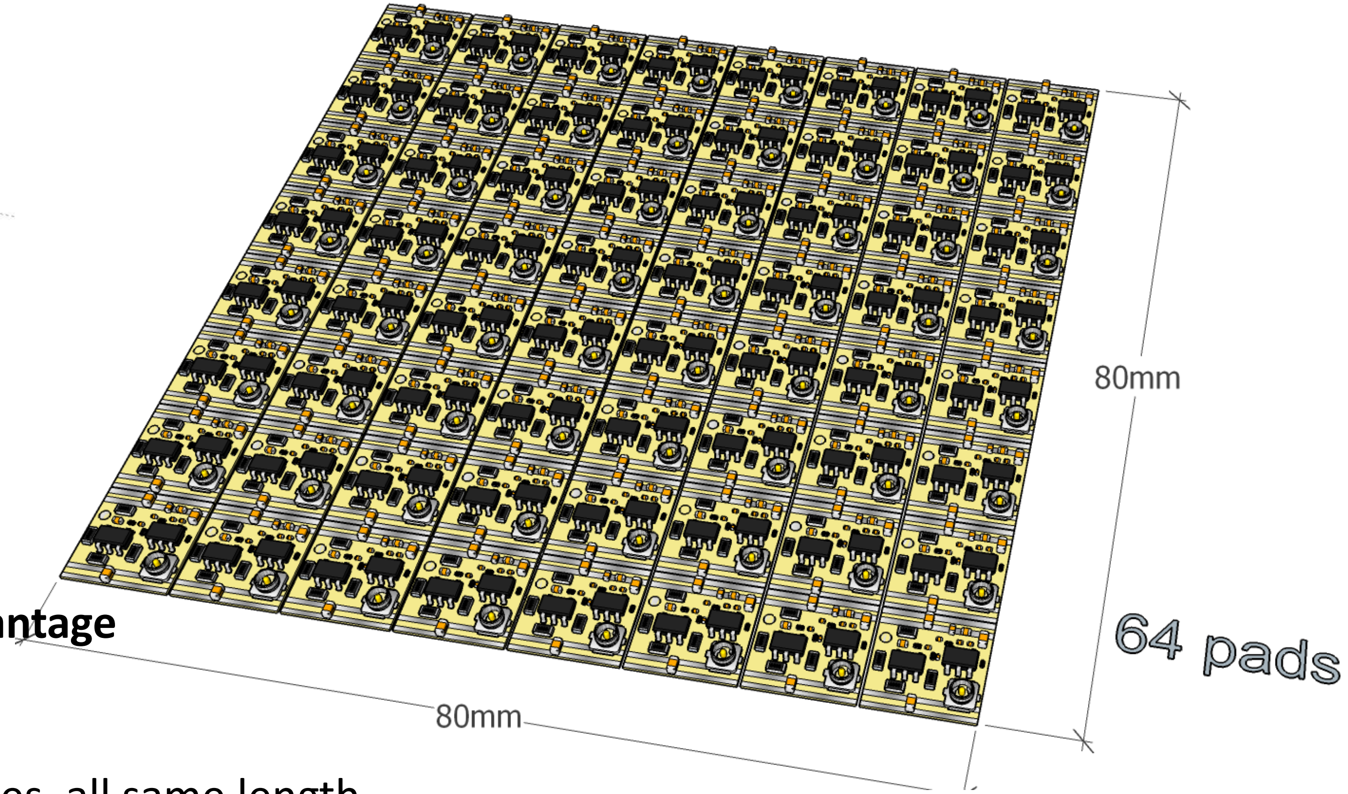
➔ uniformity calibration , S/N thresholds, cluster detection

Very good reasons for discrete logic

- **electronic design and test with state-of-art industry components**
  -> high GBP, low noise OP-Amps, lumped LRC's, fast digitizers
- **degrees of freedom beyond integrated solutions**
  -> large precision capacitors, current and HV resistors, inductances
- **dynamic ranges**
  -> higher supply Voltages, factor 10 times larger dyn. range
- **quasi-safe spark protection schemes**
  -> ESD diodes, metal film series resistors
- **integrated electronics: at least 1 mismatch**
  -> quick and cheap adaptation or upgrade
- **lacking features of integrated electronics**
  -> low budget, low timescale feature additions
- **no probing / optimization possible on integrated electronics**
  -> Oscilloscope probing on all levels

Discrete is sometimes an asset

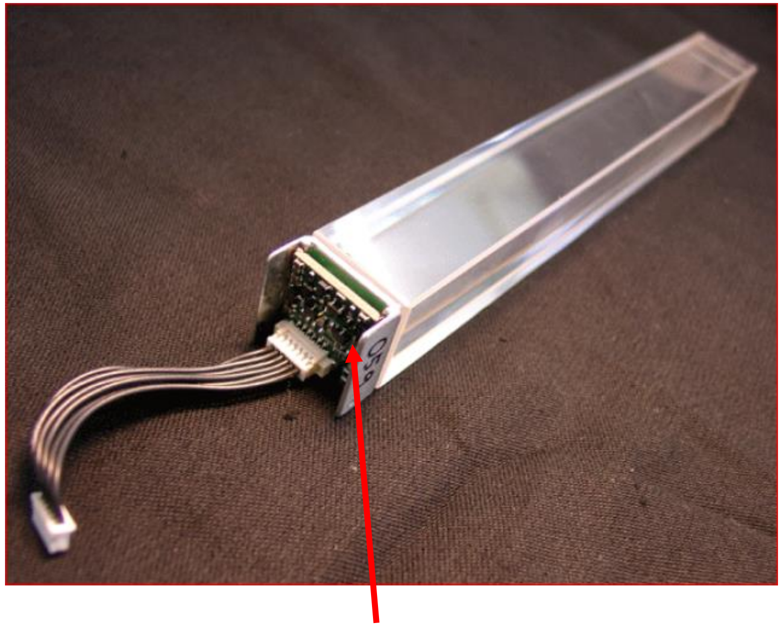




Specific detector geometries can take advantage of discrete electronics

-low noise due to very low C_{det} – v. short lines, all same length
-lower temperature for preamps, low noise
-higher dynamic range up 16 bit

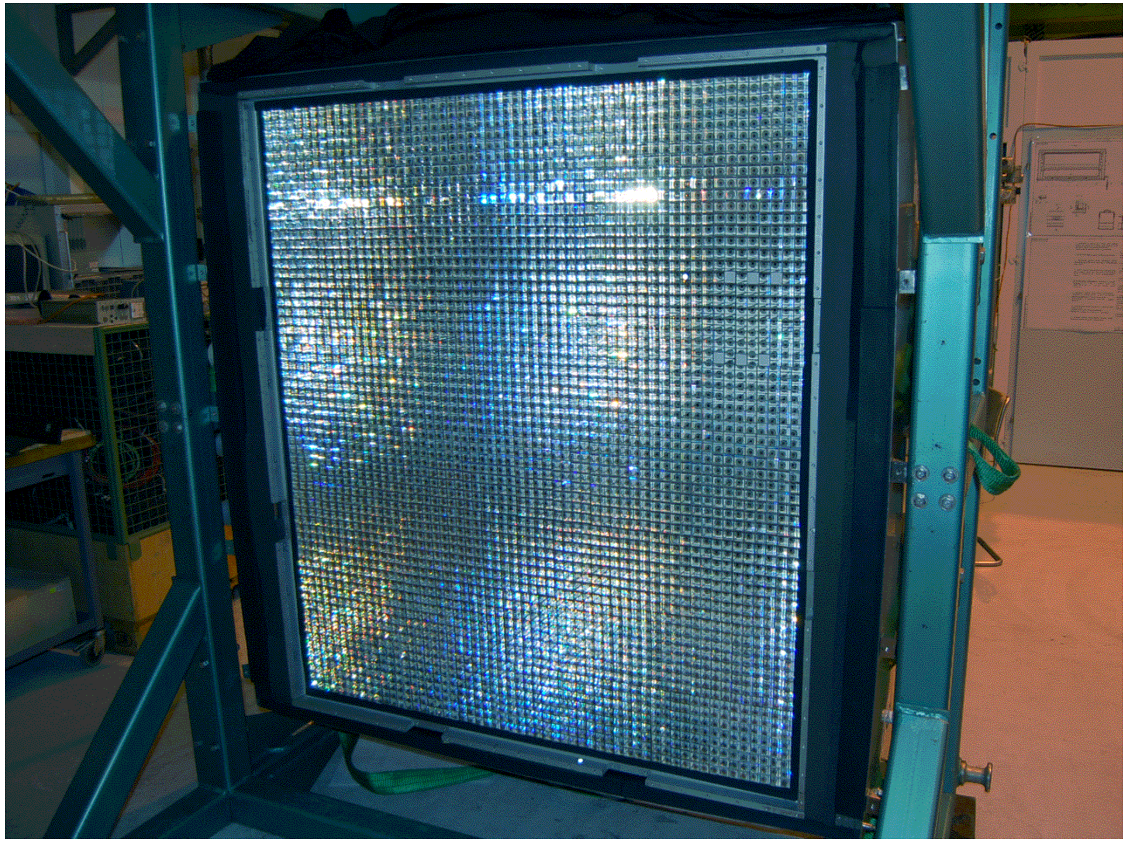
Example: LHC detector with discrete electronics FE



ALICE Calorimeters, PHOS, EMCal

PWO crystals with APD and discrete CSA preamp
14 bit dyn. Range, ENC 400e- @100pF ! @ -18 C

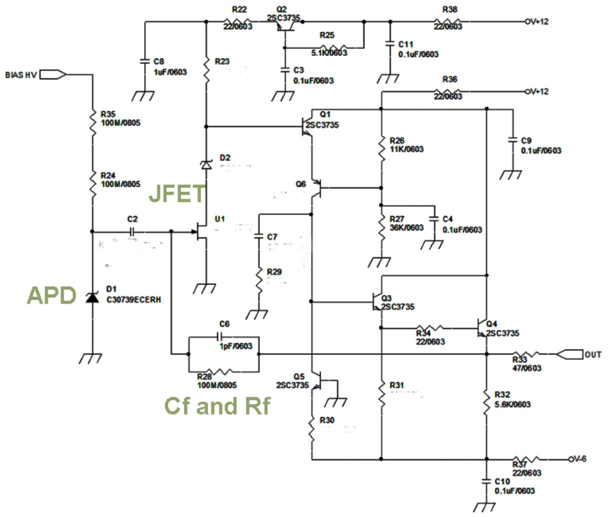
Details: Phos User manual

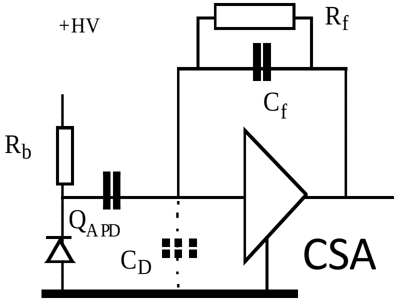


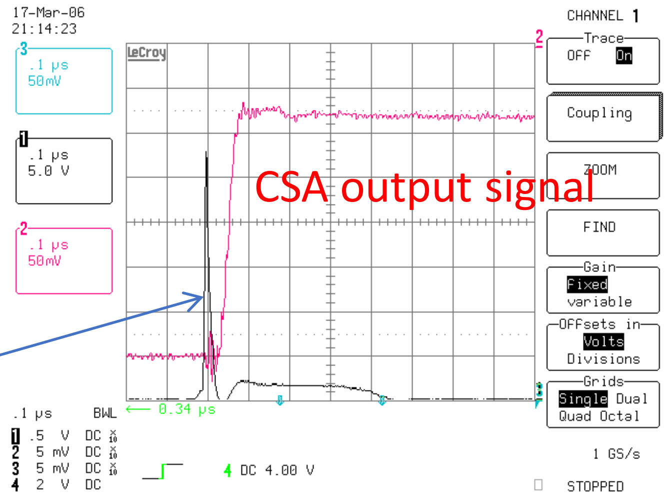
1 of 5 PHOS modules: 3584 crystals with discrete preamps

Discrete CSA's in Alice Calorimeters

- **charge /voltage gain: 1mV/fC**
- **dynamic range : 14 bit = 1/16000 (> 20 V full range)**
- **JFETs low noise, low leakage**





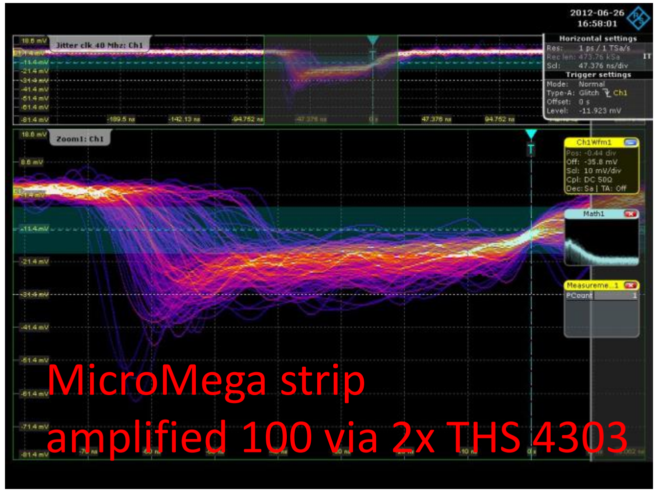


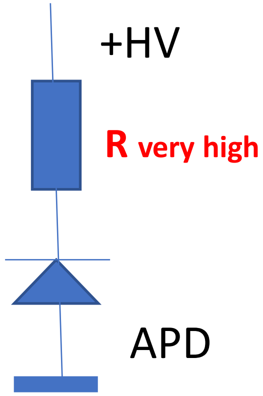
Input signal

Personal note: designing the APIC for MPGD's was inspired from experience building electronics for ALICE Calorimeter

Detector signals

Primary ionization < O(1pC) => charge over C

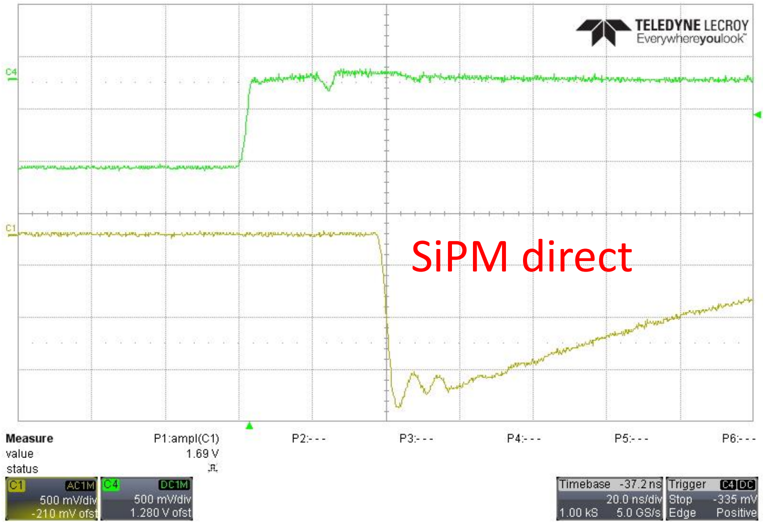


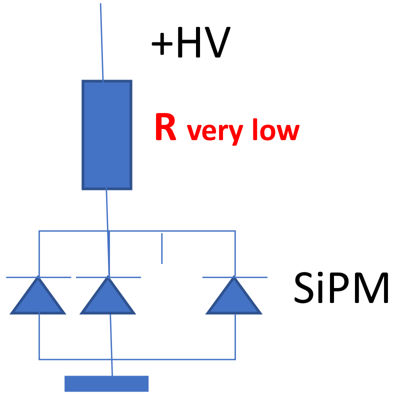


current source, high impedance
PMs, GEMs, MicroMegas, Photodiodes, APDs

Charge to Volt conversion

Primary ionization > O(1pC) => current (Volt over R)





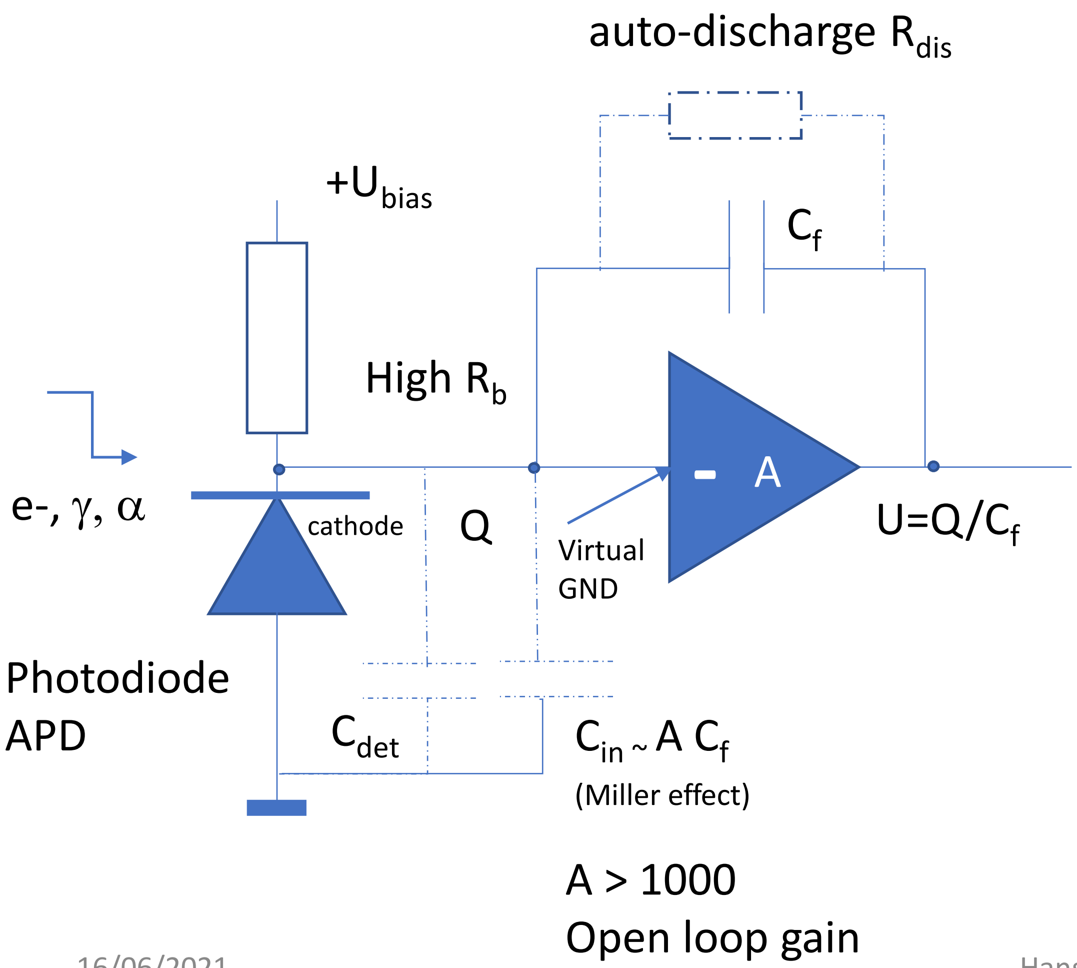
voltage source , low impedance
SiPMs, MWPC, RPC's

Current or Volt amplification

CSA amplifiers

unipolar charge integrator, high gain up 32 mV/fC

Low input impedance down to 25Ω, high input capacitance O(nF) -> high input immunity against spark charge



R_b very high (MΩ); only provides field for Diode depletion layer

⇒ Very high source impedance

e-, γ, α entering diode depletion layer generate e+/e- pairs

⇒ e- unipolar charge Q collection on cathode = C_{det}

⇒ C_{det} effectively in parallel with C_{in} of preamp

⇒ C_{in} effectively C_f multiplied by very high gain A -> O(nF)

⇒ Q shared in proportion of C_{in} and C_{det}

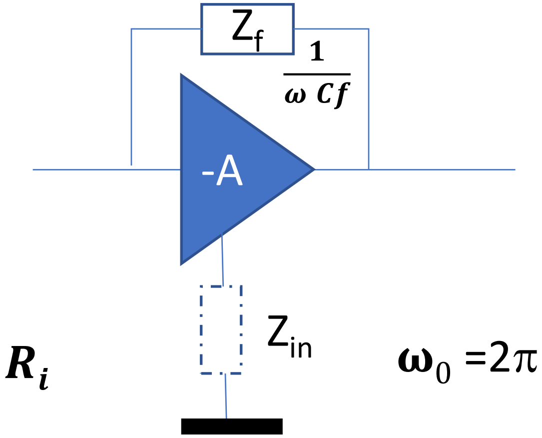
⇒ Normally $C_{in} >> C_{det}$ hence in good approx. > 98% on C_f

⇒ Output Voltage $U=Q/C_f = (1/C_f)^* Q$

⇒ Charge gain = $1/C_f$ [C_f=1 pF = 1mV/fC]

Input impedance CSA

Theoretical $Z_i = Z_f / A$



$$Z_i \text{ (CSA)* } = \frac{1}{\omega_0 \, Cf} = R_i$$

$\omega_0 = 2\pi$ GBP

Special note on spark protection:

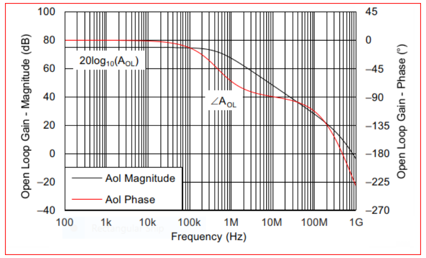
Spark voltages low over low input impedance and high input capacitance.

However only when the amplifier is also powered .

Always switch off frontend electronics after HV

Zi becomes a real number R_i at ω_0 which is the frequency where the amplifier gain A drops to 1

for OPA657 chip this is 1.6 GHz = GBP => ω_o(OPA657) = 2π *1.6 = 10 GHz



OPA657 chip
GBP=1.7GHz

C_f = 1pF => R_i = 99.5 Ω [CSA gain 1mV/fC]

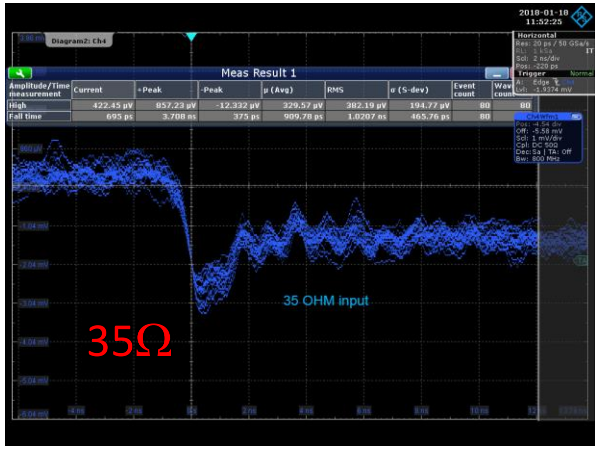
Cf = 1.6pF => R_i = 62.5 Ω [CSA gain 0.625 mV/fC]

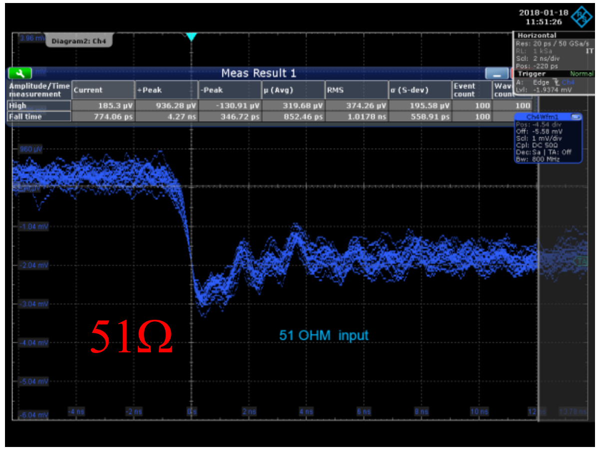
- Input impedance proportional to charge gain
- can/should match signal~ input impedances via gain

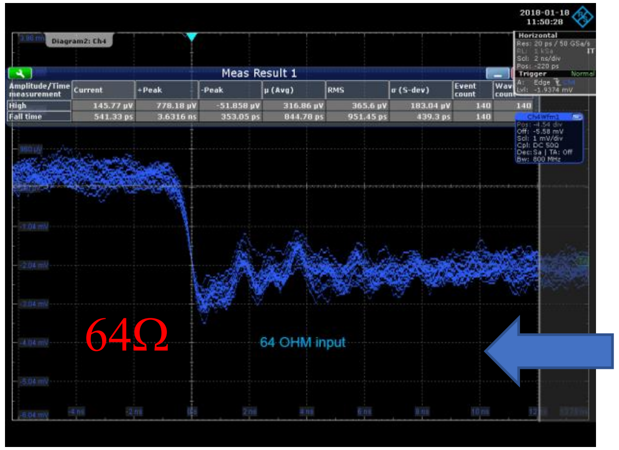
* tutorials H. Spieler on Electronics 1

Measurement input Impedance CSA on APIC

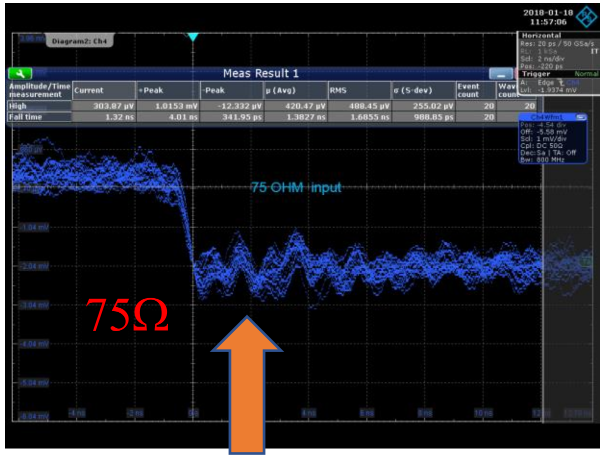
vary source impedance of pulse generator and monitor the reflections on the CSA output. Result for OPA657 with C_f =1.6pF and 10Ω input series protection: ~ 75Ω (corresponding calculation !)

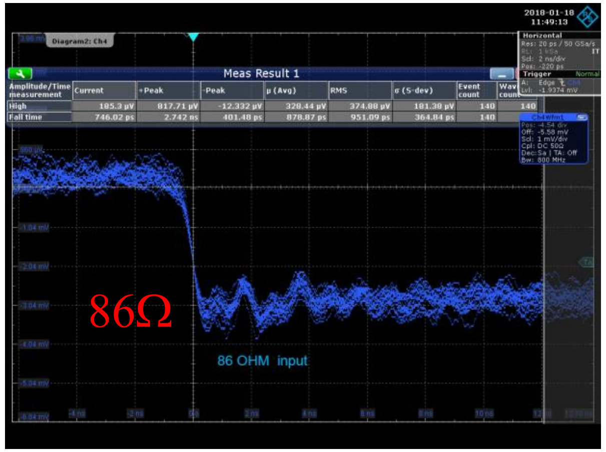


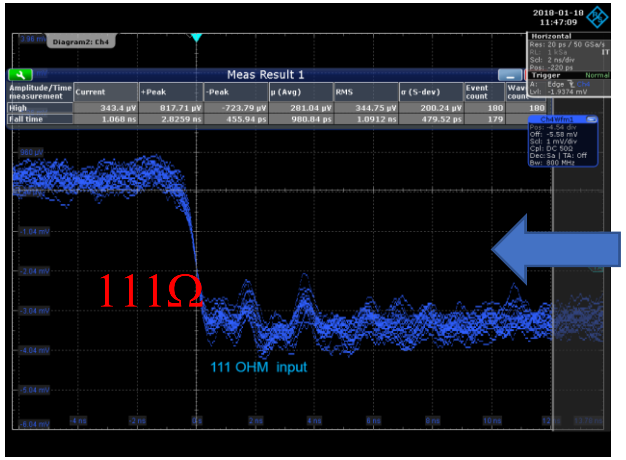




negative reflections superimposed: signal tail smaller than peak (R < Zin)







positive Reflections Superimposed: signal tail bigger than peak (R > Zin)

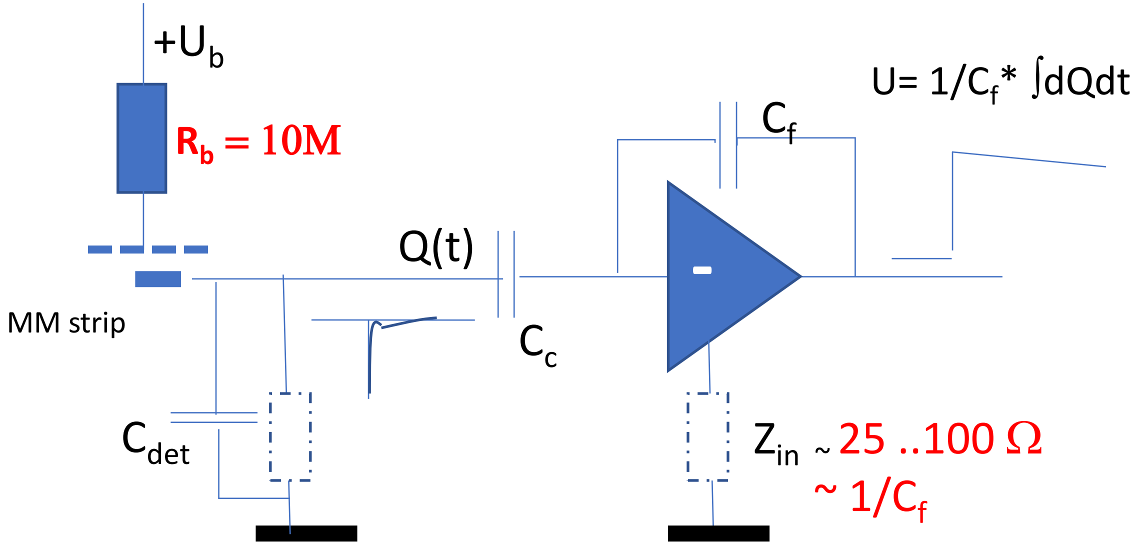
75 OHM: peak equal to tail , minimum reflections

Input impedance matters

low R_i : fast charge transfer from C_{det} to preamp input
: fast risetime
: low transfer of charge to neighboring channels
: low risk of input overvoltage / spark damage

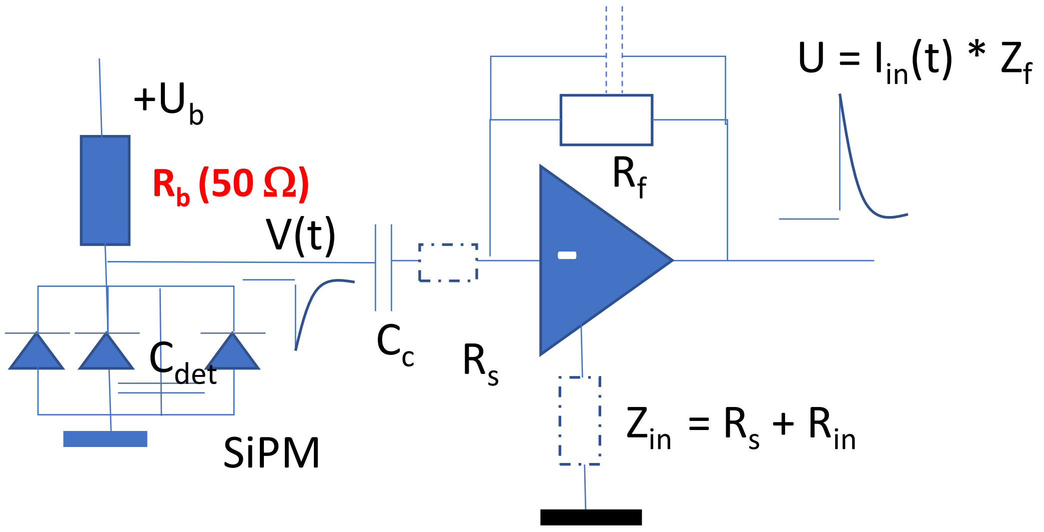
High impedance source detectors (low Q)

charge integration via CSA preamplifier
high C_{in}, high spark immunity
choose low R_i via C_f (gain)

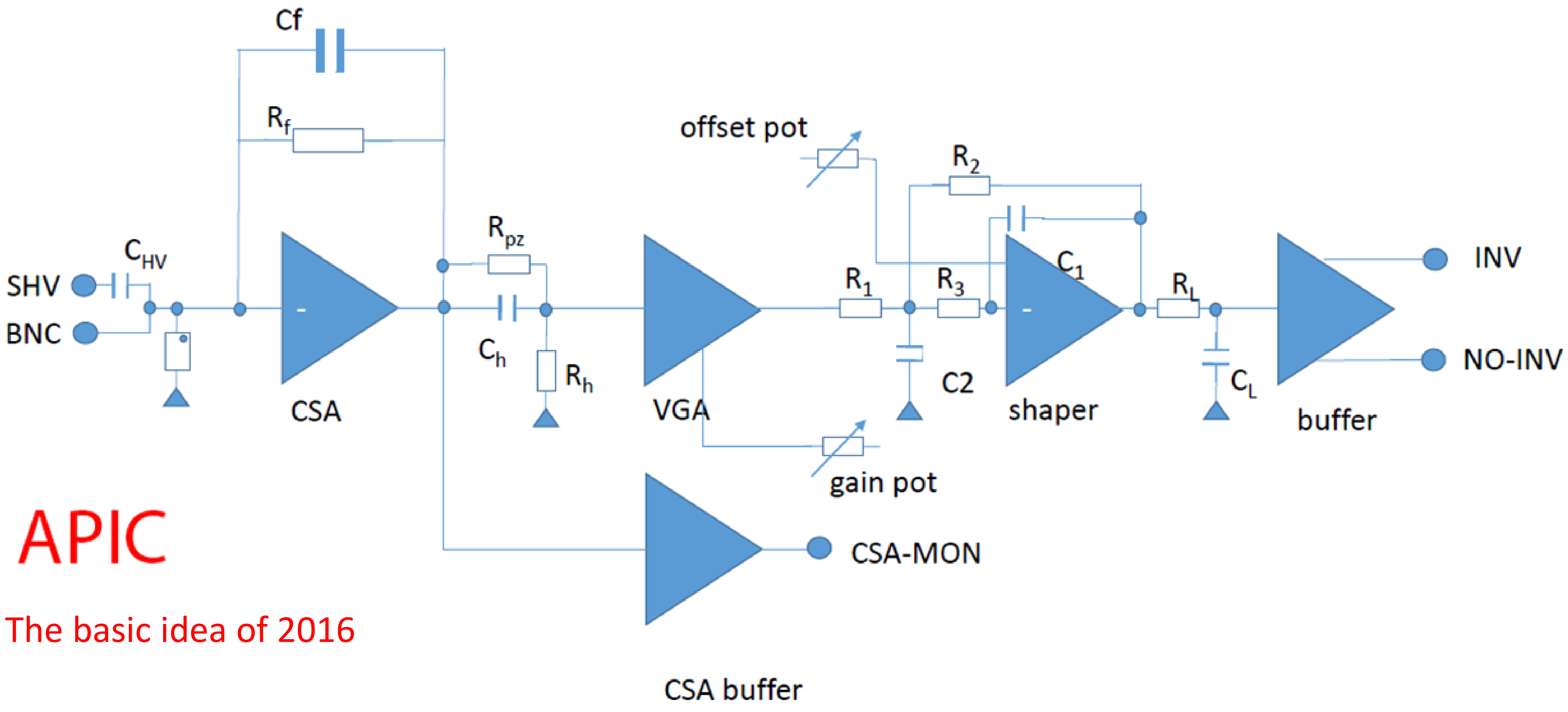


Low impedance source detectors (high Q)

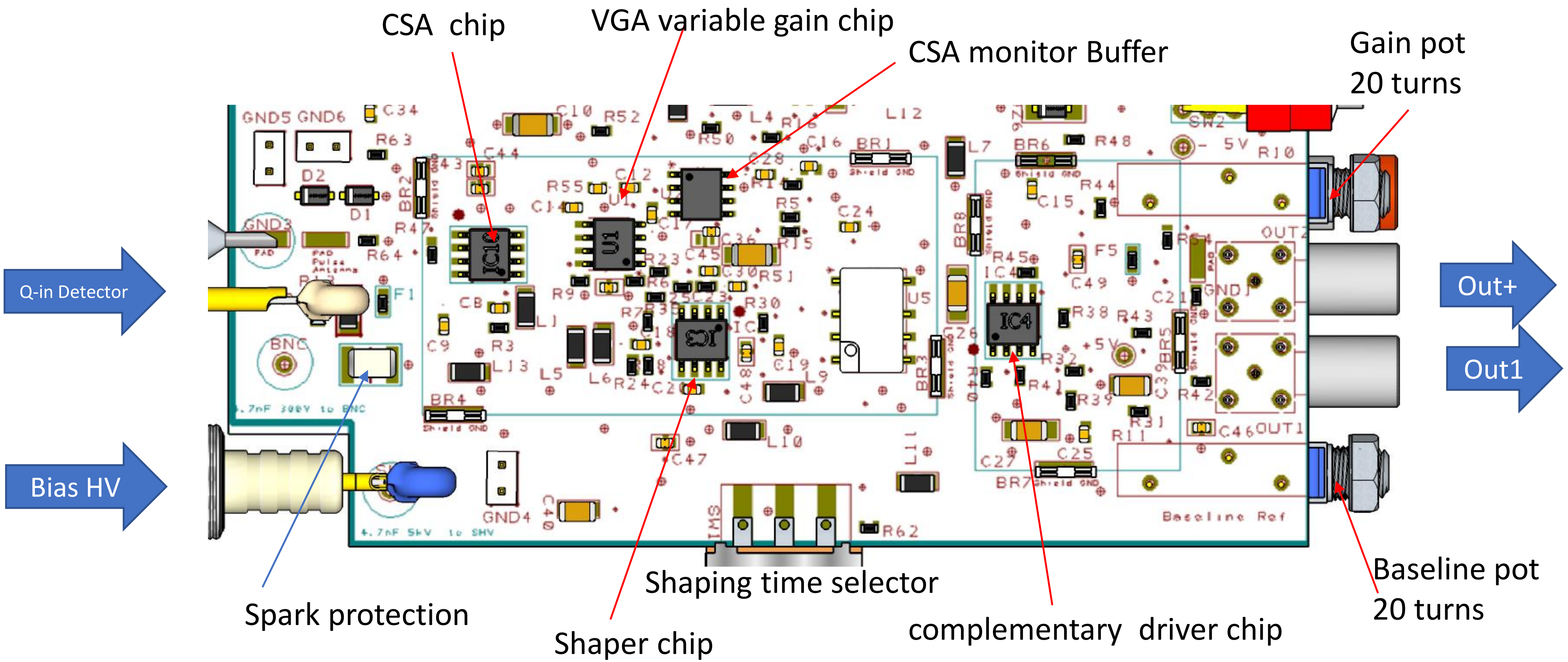
U,I source signal reproduction on TIA or current amplifier
low C_{in} , low spark immunity
Choose R_i low and match $R_i = R_B$ for minimal signal reflections



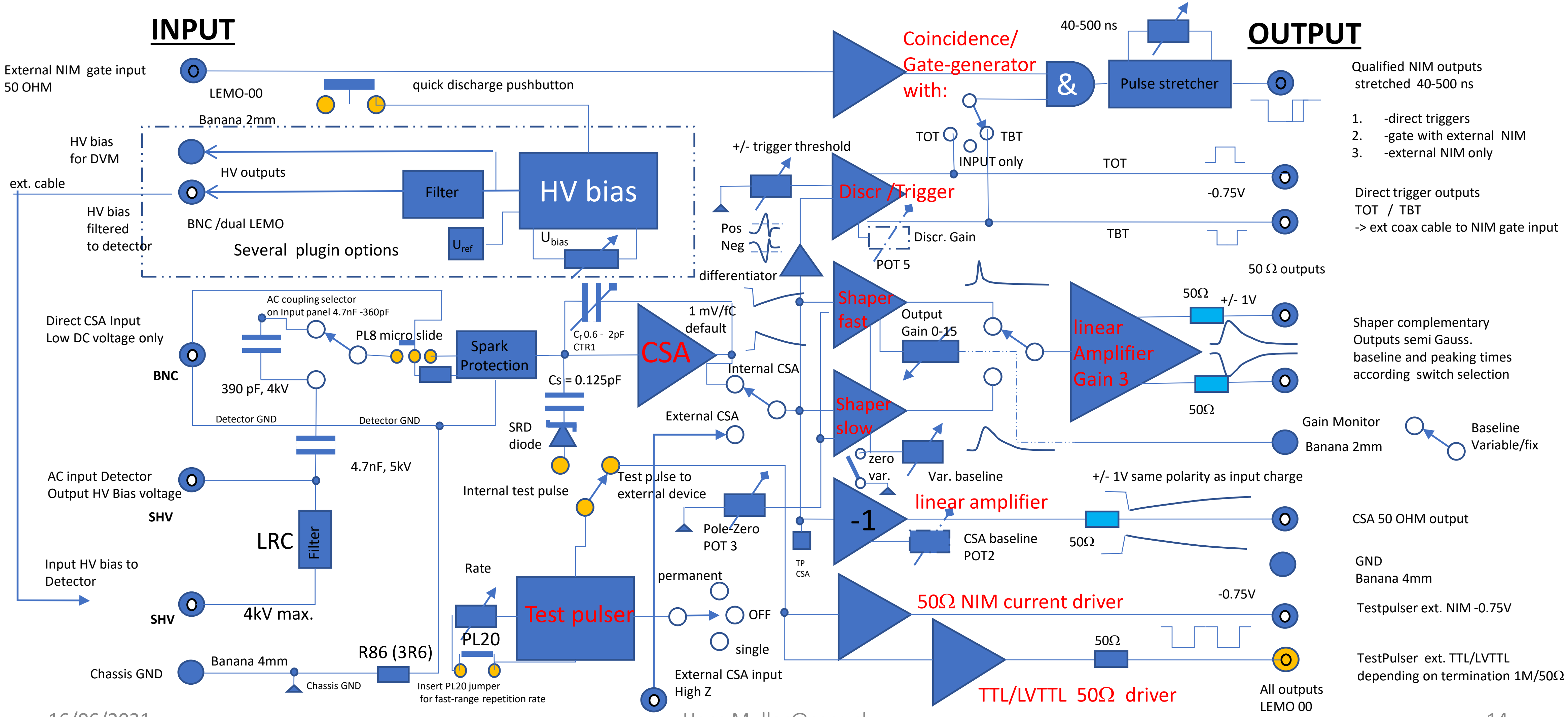
APIC preamplifier- shaper (2016)



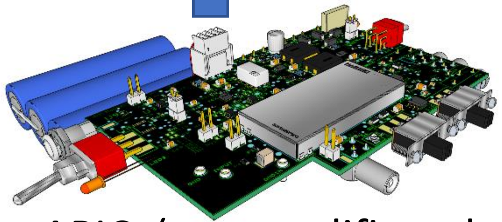
APIC$_{2016}$ discrete implementation CSA->VGA->shaper



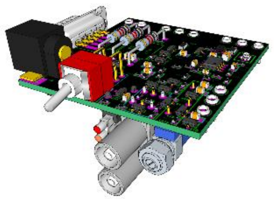
APIC V4 2020… many added features on user request



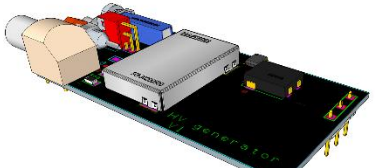
APIC V3



- APIC (preamplifier- shaper)



- Trigger and AUX power Unit



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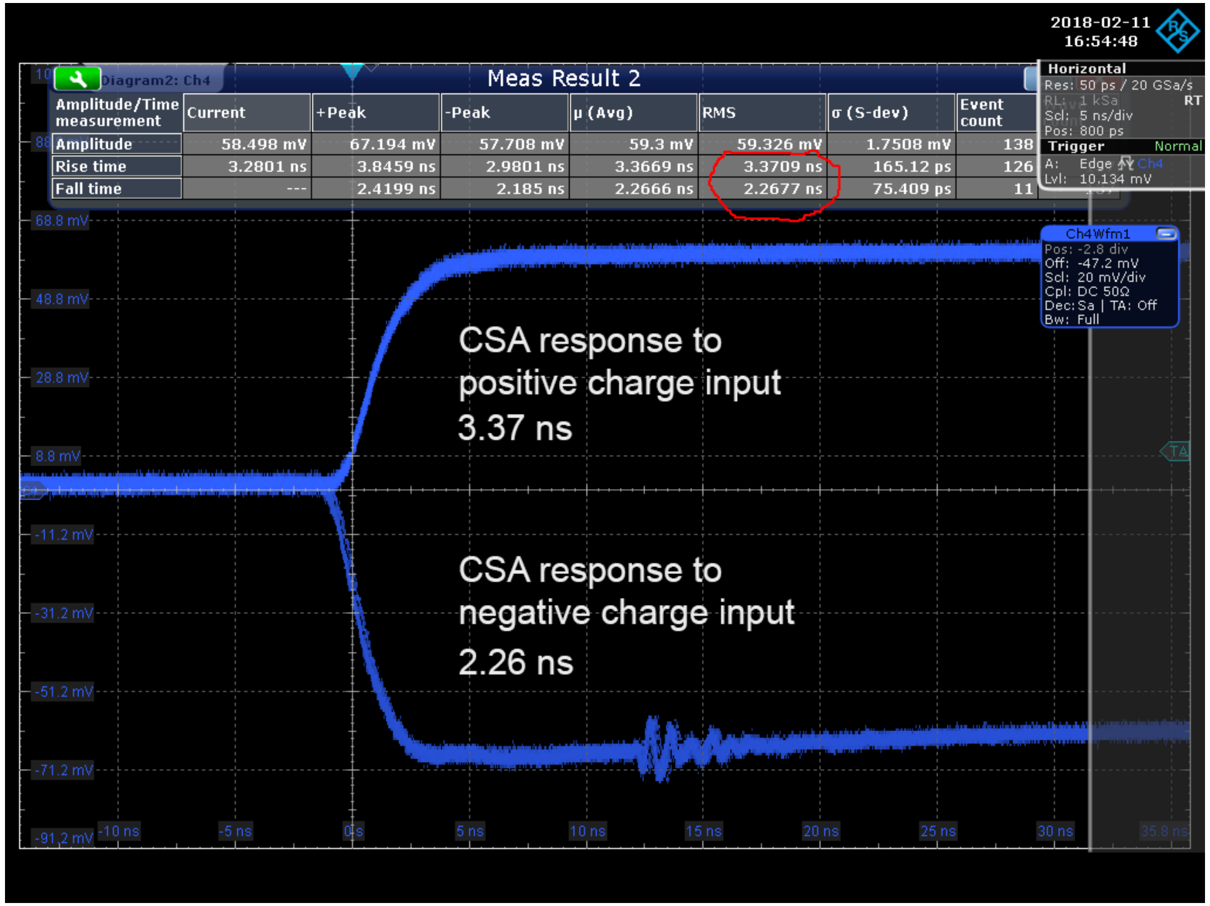
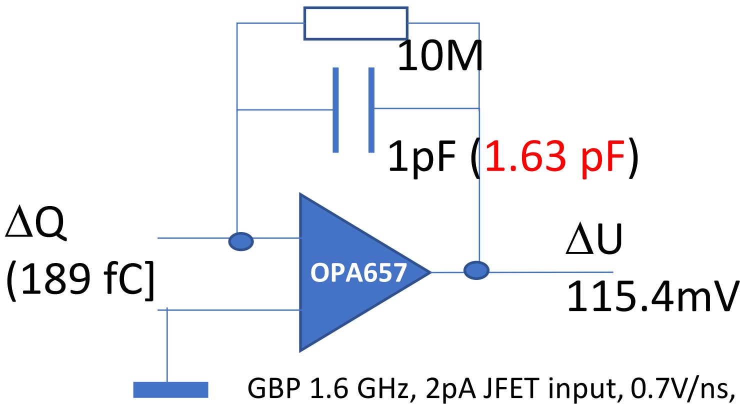
- HV Bias Unit (Option)

CSA gain calibration



stray capacitance matters for discrete



GBP 1.6 GHz, 2pA JFET input, 0.7V/ns,
A ~ 4000 (70dB open loop gain) -> C_{in} ~ 4nF

neg. test input charge t_r 200 ps , ΔQ = 189 fC

ΔU: 115.4 mV*, O(2.2ns) CSA rise/falltime

charge gain : 115.4 /189 = 0.61 mV/fC

=> C_f effective = 1/0.61 = 1.63 pF

* 57.7mV x 2 due to 50Ω + 50Ω output divider(½)

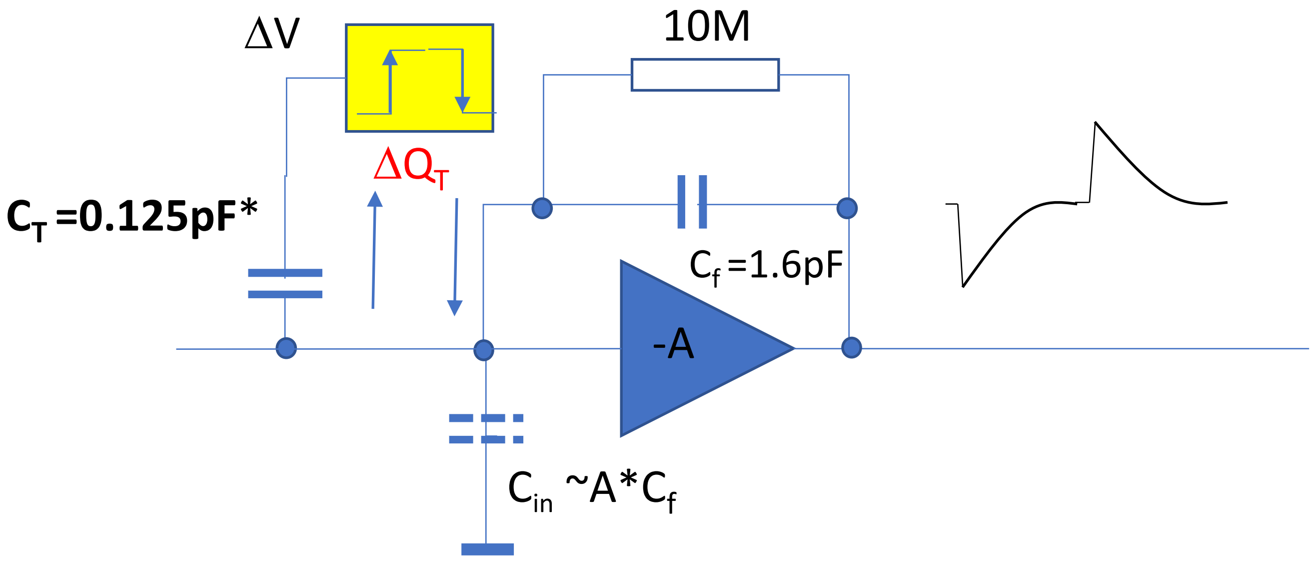
calibration charge Q_T

See appendix for preferred test pulse shape

use fast Voltage pulse transition to couple a unipolar charge to the preamp

fast risetime test pulse
(SRD diode 200ps)
ΔV amplitude = 1.51V

$\Delta Q_T \sim C_T * \Delta V = 189$ fC



*3x 0.5pF in series $\frac{1}{C} = \frac{1}{C1} + \frac{1}{C2} + \frac{1}{C3}$

Input test charge Q_T:

$$\Delta Q_T = \frac{C_T}{1+\frac{C_T}{C_{in}}} \Delta V \sim C_T[\,1-\frac{C_T}{C_{in}}\,]\,\Delta V$$

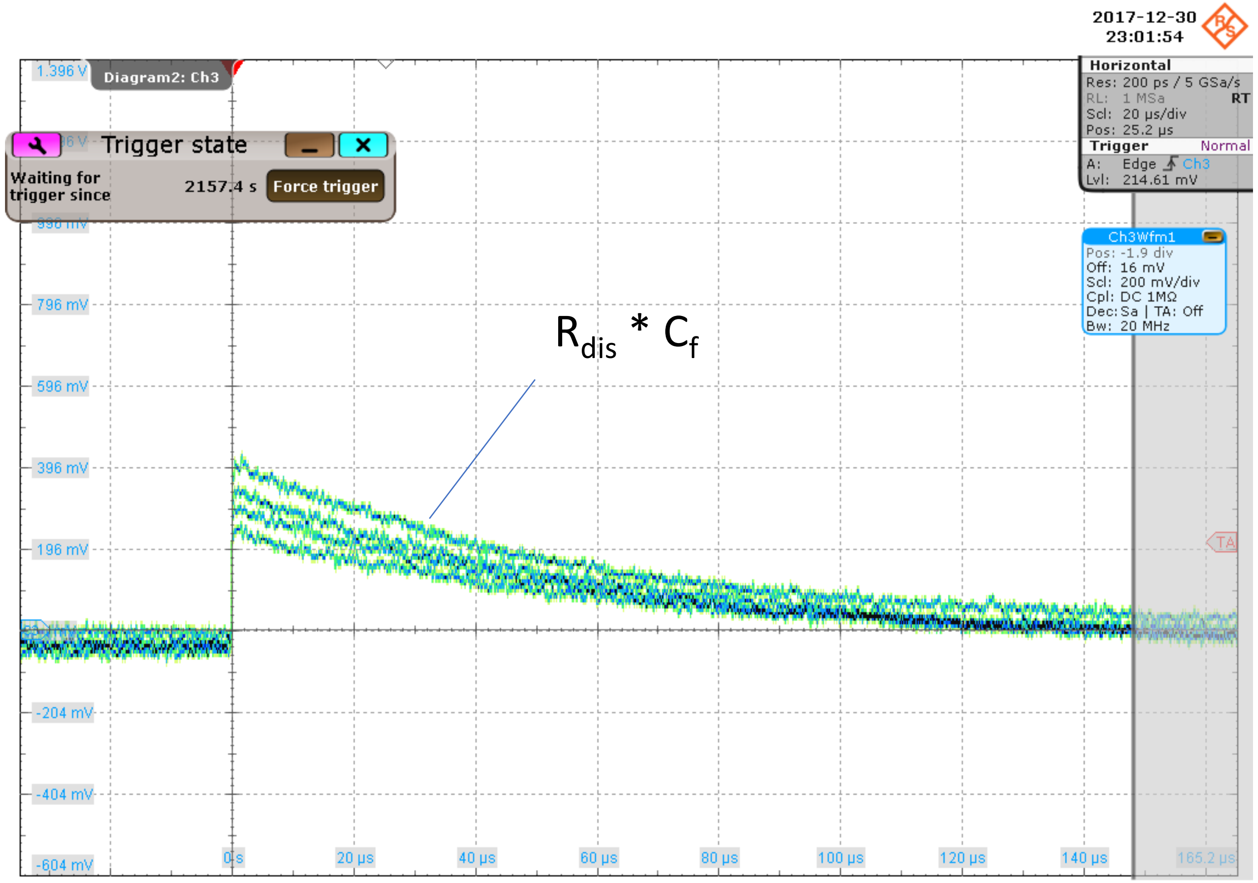
$\frac{C_T}{C_{in}} << 1$

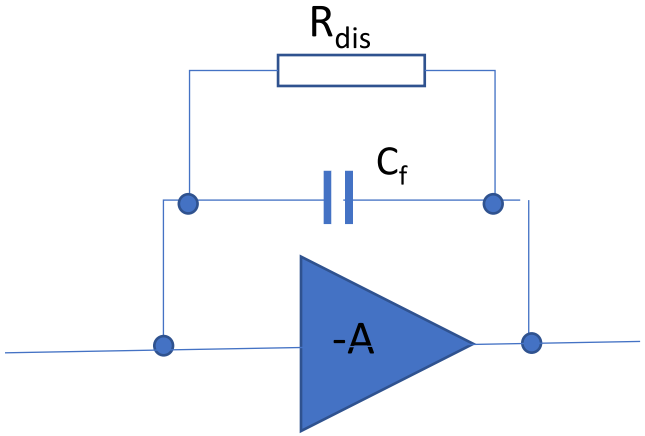
$C_T = 0.125$ pF
$C_{in} = O(4nF)$

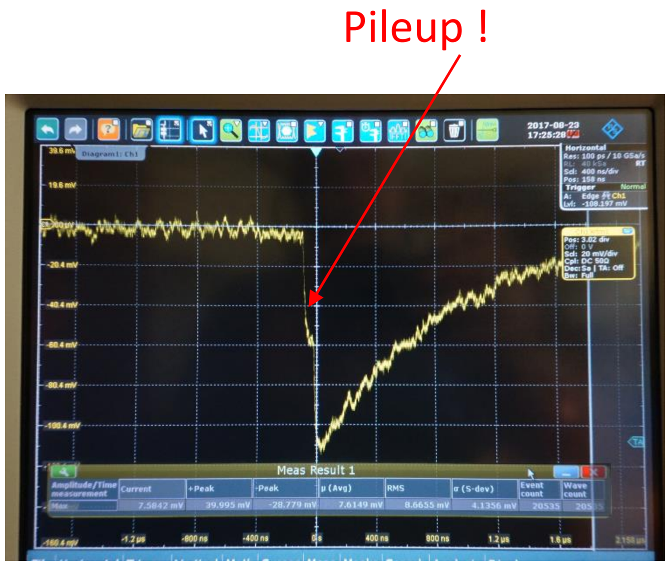
$\mathbf{\Delta Q_T \sim C_T * \Delta V}$

CSA auto-discharge and pileup

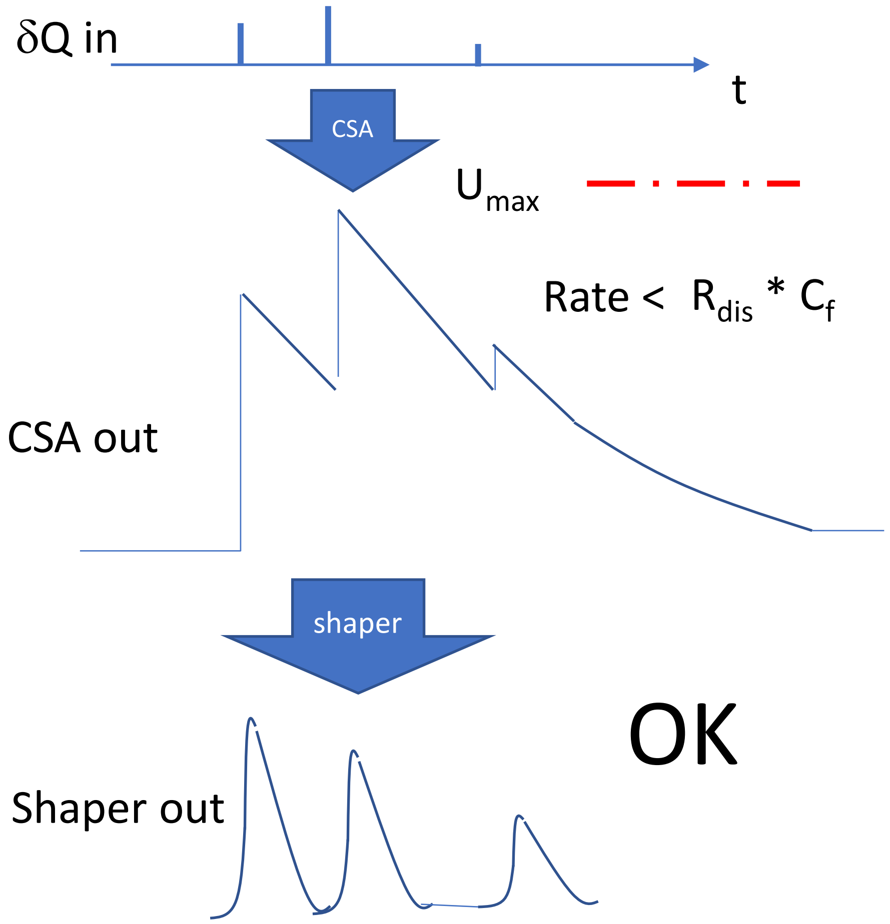
APIC uses classic discharge resistor R_{dis}

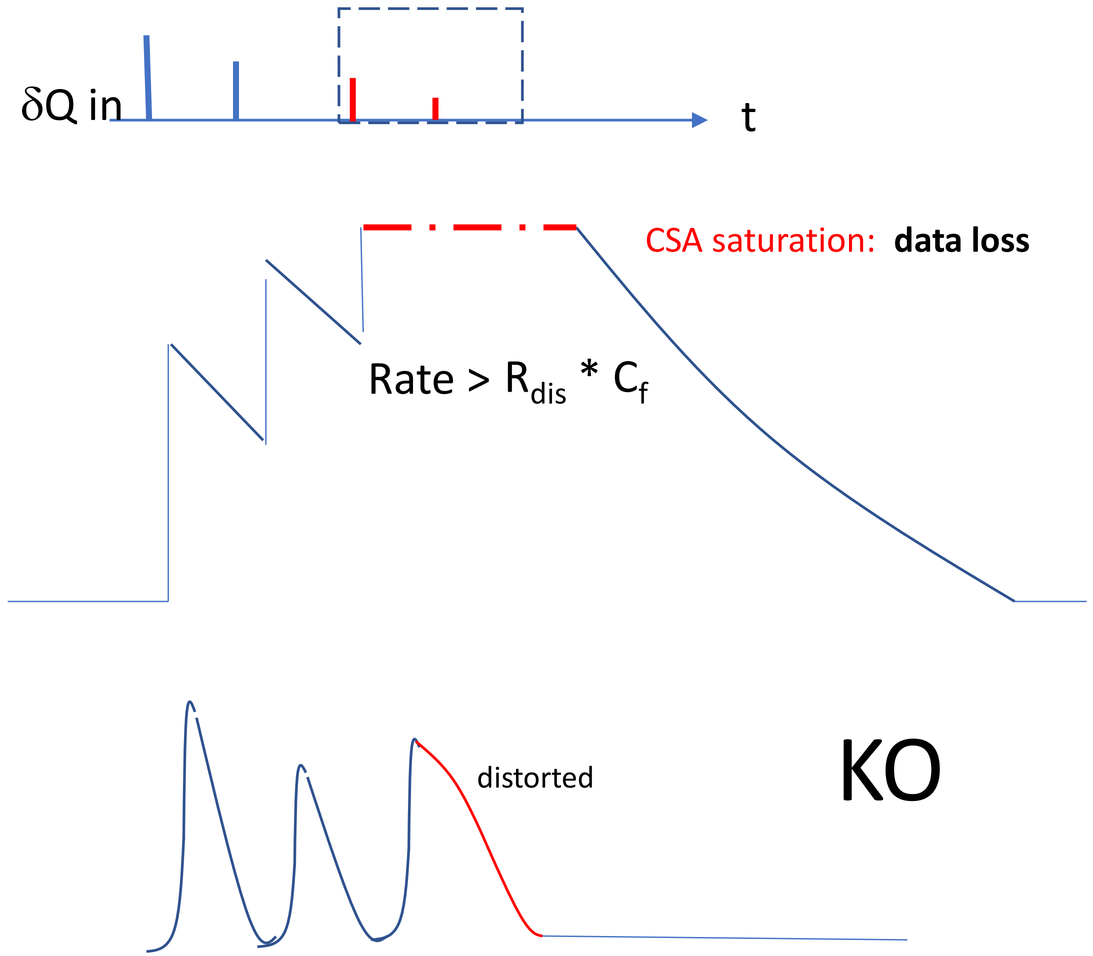




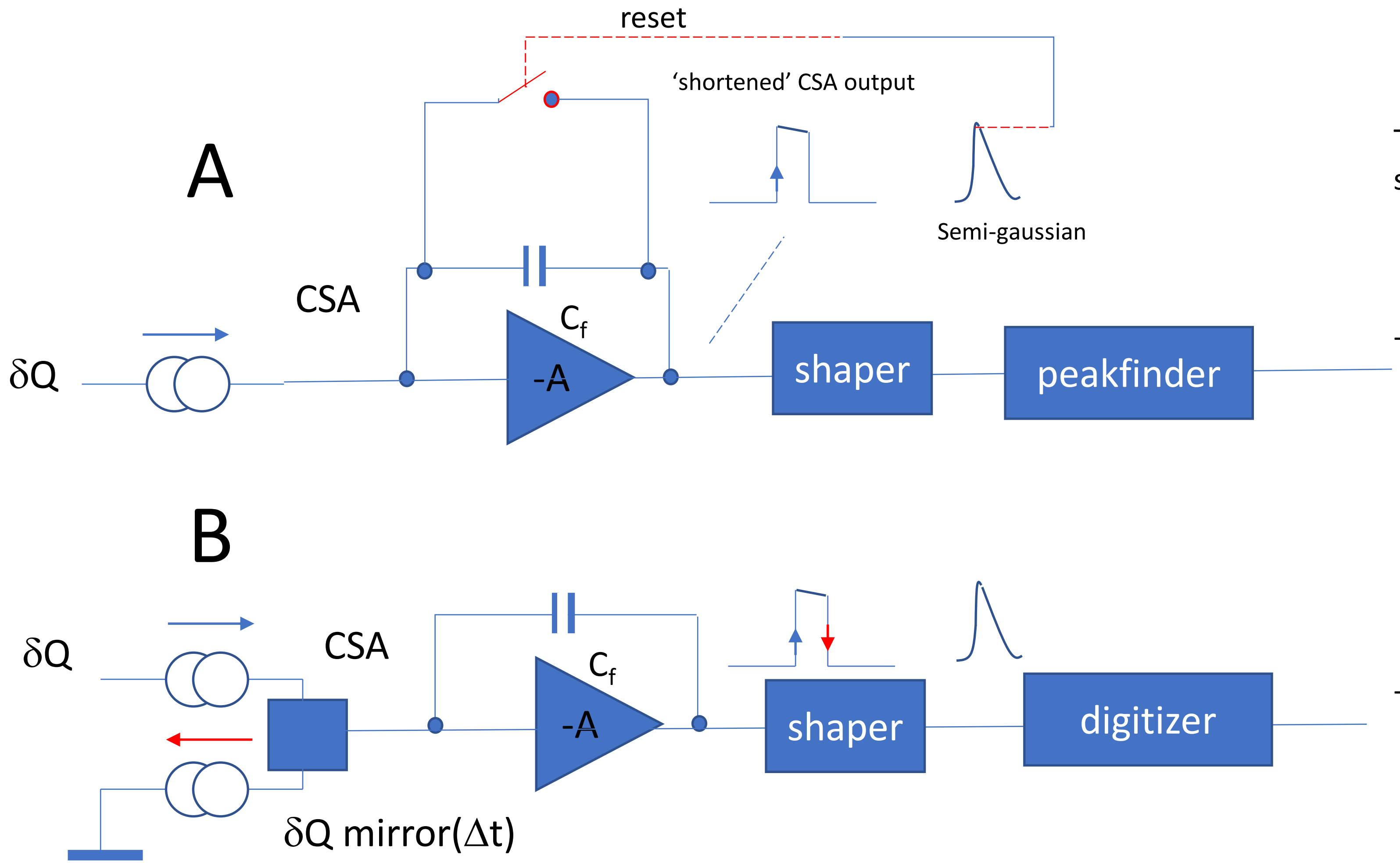


High-rate problem with autodischarge





High-rate preamps



The falling CSA slope is not required for signal feature extraction (charge, time)

-method A: using a peakfinder: reset the CSA when shaper signal peak detected (see VMM3a)

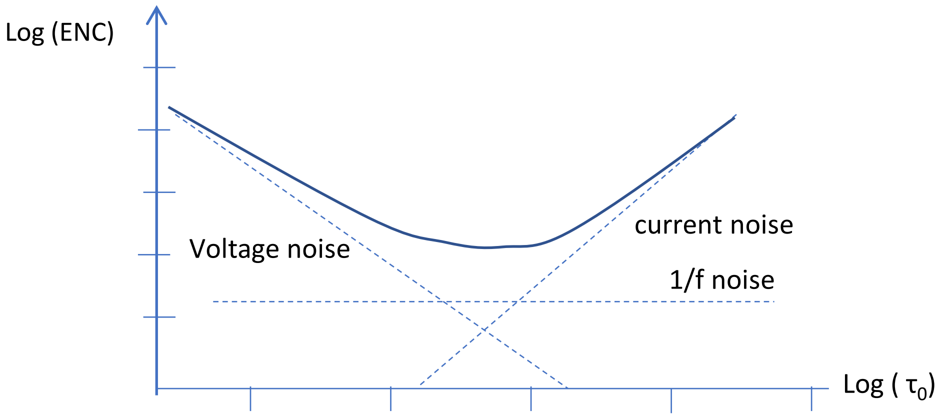
-method B: time-reverse input charge flow use digitizer for sampling the full shaper waveform (some R&D on APIC preamp with SiPMs)

Shaping matters

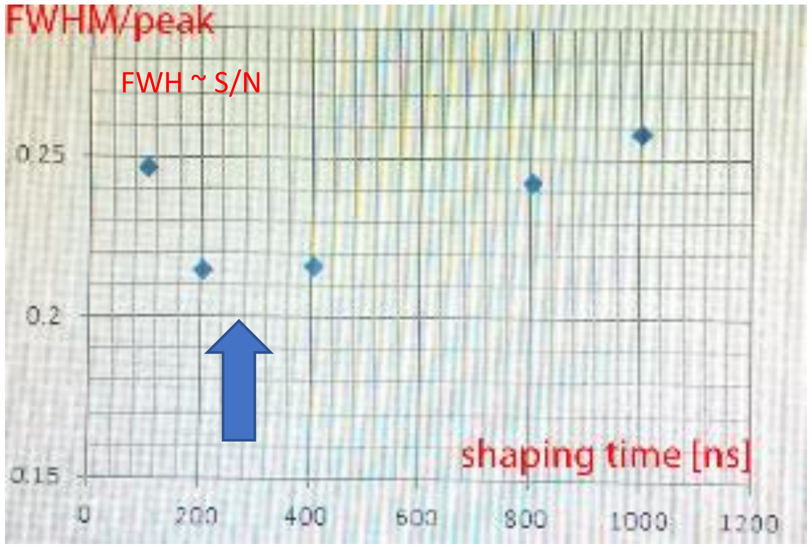
ENC noise dependence on shaping time τ_0

$$ENC^2 = \frac{4kT}{q^2 \cdot R_b} \cdot F_p \cdot \tau + \frac{4kT}{q^2} \cdot 2/3 \cdot \frac{1}{g_m} \cdot F_s \cdot \frac{C_d^2}{\tau} + C_d^{\,2} \cdot const$$

Current noise ~ τ_0 **Voltage noise ~ $1/\tau_0$** **1/f noise**



Summers student 2016 result with GEM



APIC shaping time vs
Energy Resolution on 10x10 GEM

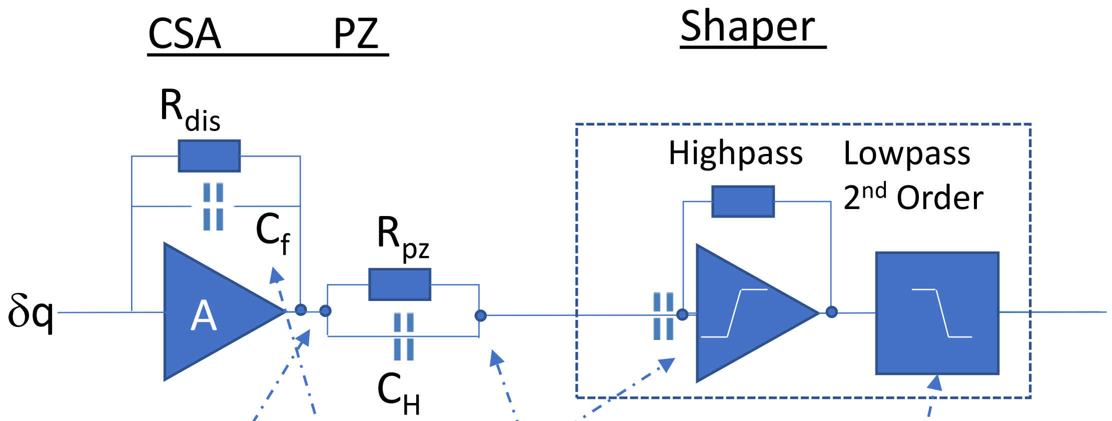
<u>Strategies to minimize ENC:</u>

....after removing
GND loops, RF noise,
HV bias crosstalk etc .....

Optimize shaping time τ_0
+ minimize C_D detector capacitance
+ reduce preamp temperature T
+ choose best technology

- Measure ENC noise dependence of shaping time (^{55}FE spectra)
- Avoid long traces, Coax cables add 1 pF/cm
- Cool CSA's if possible
- Low noise OPAMPs , thin-film resistors

‘semigaussian’ shaper implementation on APIC



Laplace operator method for the full chain

$$H_{shaper}(s) = \frac{1}{\cancel{s}}\left[\frac{\cancel{s}\tau_0}{1+s\tau_0}\right] \times \left[\frac{q/C_f}{\cancel{1+1/(R_{dis}\cdot C_f)}}\right]\left[\cancel{1+1/(R_{dis}\cdot C_f)}\right]\left[\frac{A}{1+s\tau_0}\right]^n$$

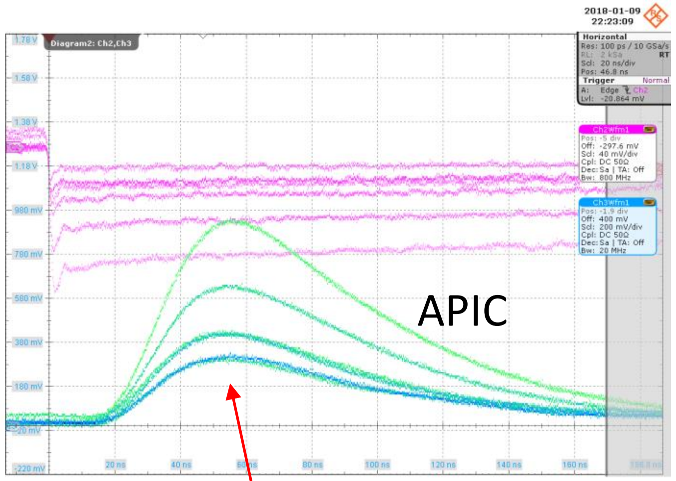
step function — differentiator — CSPdischarge — pole-zero — RC integrator n-th order

pole-zero cancellation

τ_0 = shaping time

$$H_{shaper}(s) = \frac{Q}{C_f}\left[\frac{\tau_0}{1+s\tau_0}\right]\left[\frac{A}{1+s\tau_0}\right]^n$$

Re-conversion Laplace to time domain



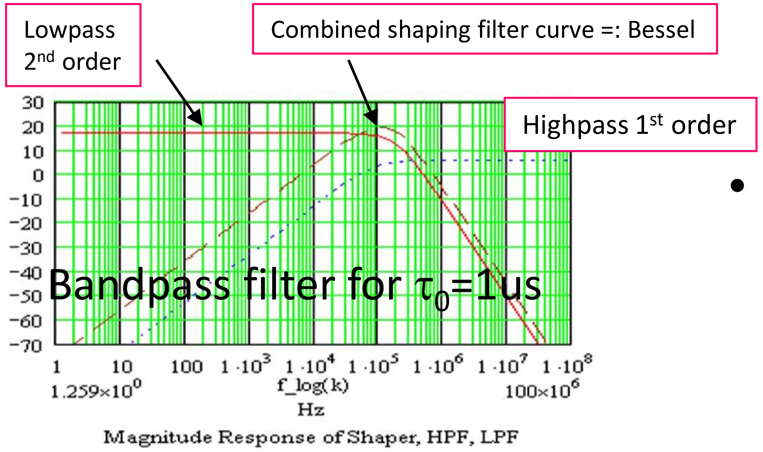
$$V(t) = \frac{2Q\cdot A^2}{C_f}\cdot\left[\frac{1}{\tau_0}\right]^2\cdot e^{-2\frac{t}{\tau_0}}$$

n=2

$$V(t) = \frac{n^n Q\cdot A^n}{n!\,Cf}\cdot\left[\frac{1}{\tau_0}\right]^n\cdot e^{-n\frac{t}{\tau_0}}$$

A: CSA Amplifier open loop gain
C_f: CSA feedback capacitor
Q: total input charge
τ_0: shaping time
n: order of H_{Lp} filter

Bandpass filter and shaping time



- CRnRC band-pass filters of order n: the low-pass slope is n * 20 dB / octave whilst for the single RC high pass it is -20 dB/octave. The -3dB **cutoff frequency f**c is given by

$$f_c = 1/(2\pi\ \tau_0)^*$$

$* \tau_0 = \tau_p/2$ is shaping time

- The time response function (shaped output) produced by CR-nRC bandpass filters closely resembles a semi-gaussian shape, properly implemented the analytic form is a $\Gamma_n(t)$ function of order n

$$Vout(t)) = \left[\frac{n^n Q \cdot A^n}{Cf}\right] \cdot \left[\frac{t}{\tau_p}\right]^n \cdot e^{-n\frac{t}{\tau_p}}$$

With: $\tau_p = n * \tau_0$

APIC: 2x shaping times

τ_p = 12.5 ns , **τ_p** = 25 ns, fc = 12.7 MHz

τ_p = 200 ns , **τ_p** = 100 ns, fc = 800 kHz

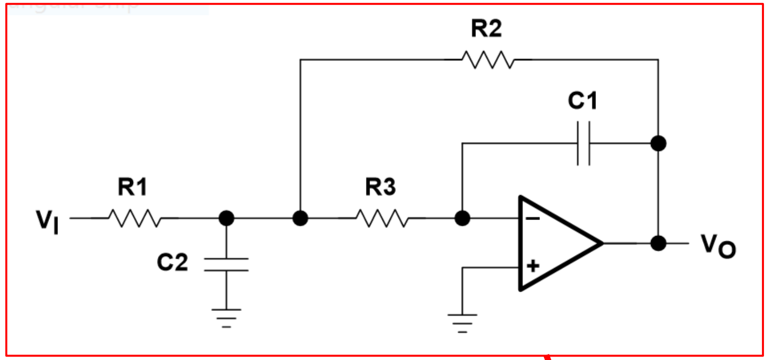
$$V_{max} = \frac{Q \cdot A^n \cdot n^n}{C_f \cdot n! \cdot e^n}$$

peak amplitude measures charge Q

APIC: discrete Lowpass implementation 2nd Order Bessel Filter

$$H(s) = \frac{K}{1 + as + bs^2}$$

APIC: Implement 2 shapers with 1 single OPAMP



Choose constants a,b,K for Bessel filter characteristics

2nd Order Bessel Filter circuit (APIC)
linear, high BW OP-AMP

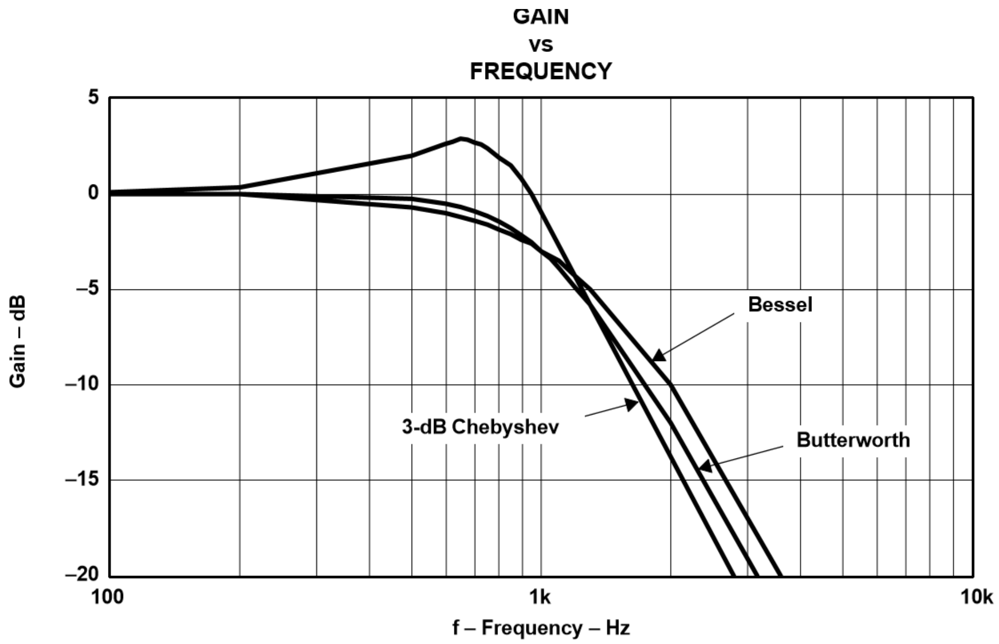


Figure 10. Second-Order Butterworth, Bessel, and 3-dB Chebyshev Filter Frequency Response

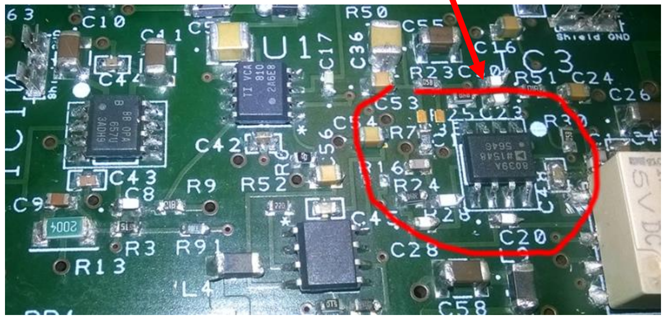
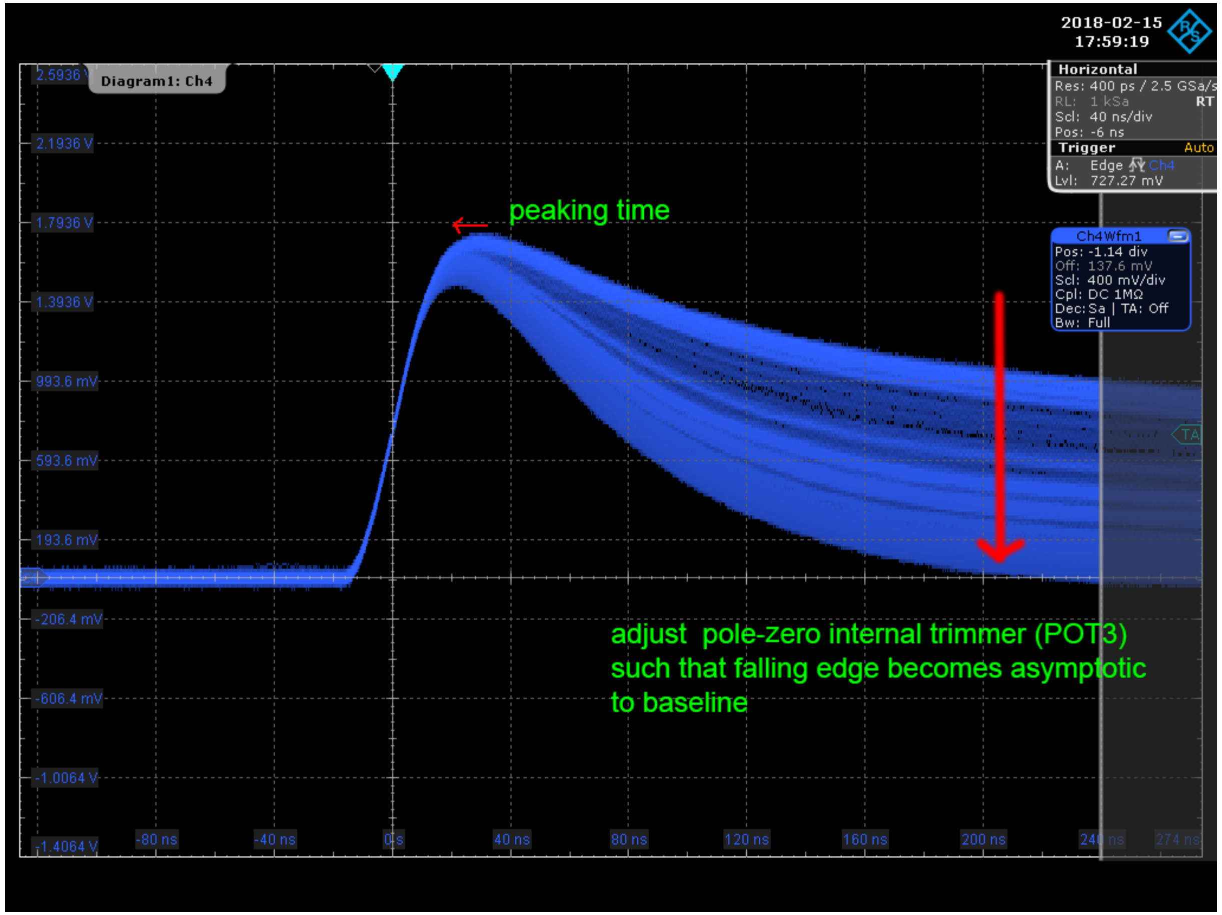


Photo: real estate of
2nd Order Bessel Filter
τ_s=12.5ns & 200ns **on APIC**

Pole-zero fine adjustment

asymptotic return to zero basline



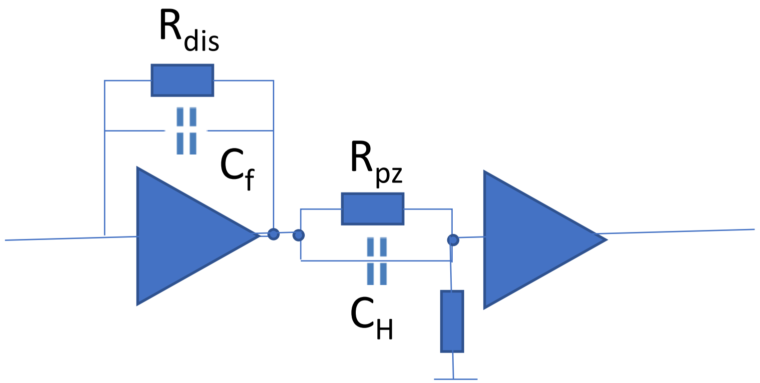
Make these 2 terms cancel

$$H_{shaper}(s) = \frac{1}{s}\left[\frac{s\tau_0}{1+s\tau_0}\right] \times \left[\frac{q/C_f}{1+1/(R_{dis}\cdot C_f)}\right]\left[1+1/(R_{dis}\cdot C_f)\right]\left[\frac{A}{1+s\tau_0}\right]^n$$

step function | differentiator | CSPdischarge | pole-zero | RC integrator n-th order

make equal:

$R_{dis} * C_f = R_{pz} * C_H$



Component tolerances:

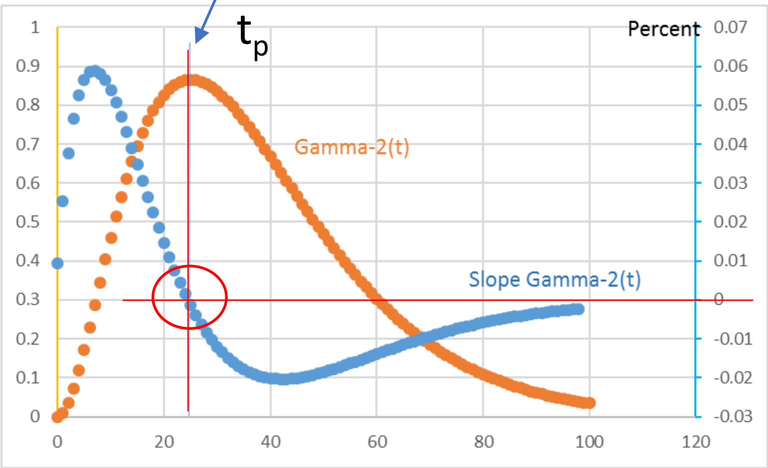
In discrete logic, the exact R_{pz} value can be determined by using a trimmer

peaking time invariance τ_p

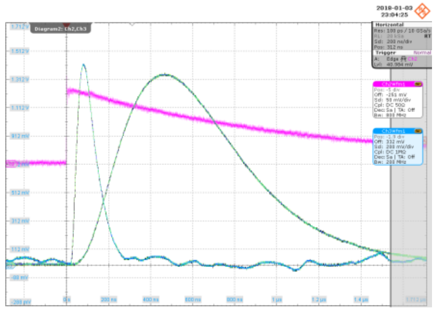
peak amplitude-independent

$$V_n(t) = \frac{n^n Q\cdot A^n}{n!\,Cf}\cdot\left[\frac{1}{\tau_0}\right]^n\cdot e^{-n\frac{t}{\tau_0}}$$

Set 1st derivative V(t) = 0
choose filter order
i.e. n=2 for APIC
$\tau_p = n^* \tau_0 = \mathbf{2}\ \tau_0$
➔ peaking time * 2x shaping time
➔ peak invariance of amplitude (!)

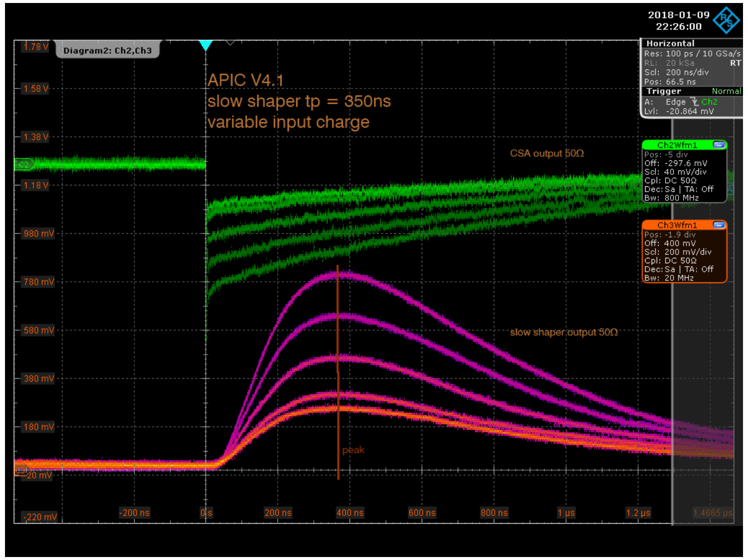


APIC:
2^{nd} order Filter, n=2
τ_{p1} = 25 ns
τ_{p2} = 400 ns



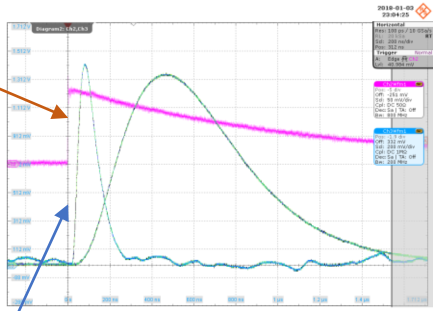
$$V(t) = \frac{2Q\cdot A^2}{C_f}\cdot\left[\frac{1}{\tau_0}\right]^2\cdot e^{-2\frac{t}{\tau_0}}$$

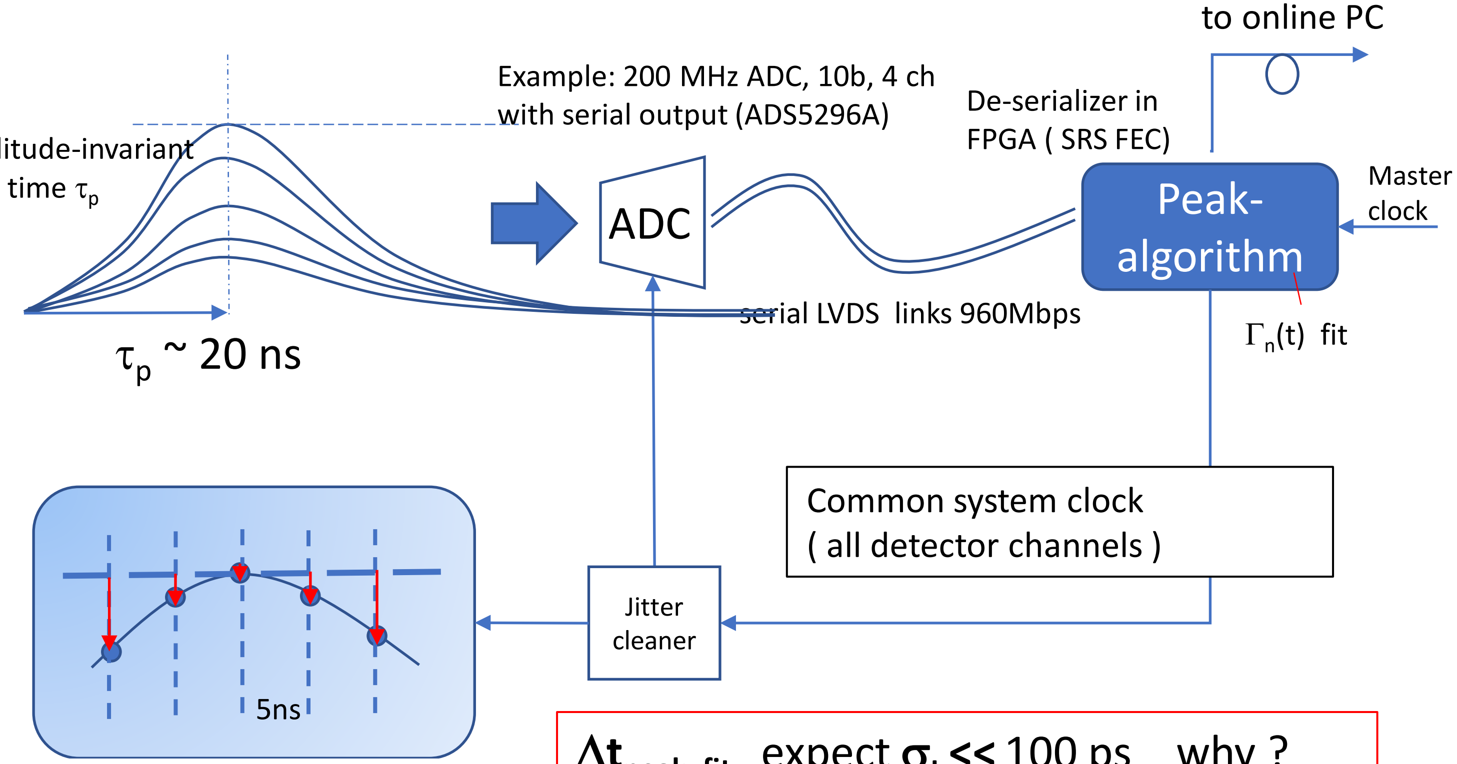
APIC output signal
(for VCA gain :=1)



$\Gamma_n(t)$ shaper sampling for ps time resolution
(project proposal)

CSA:
t_r O(1ns)





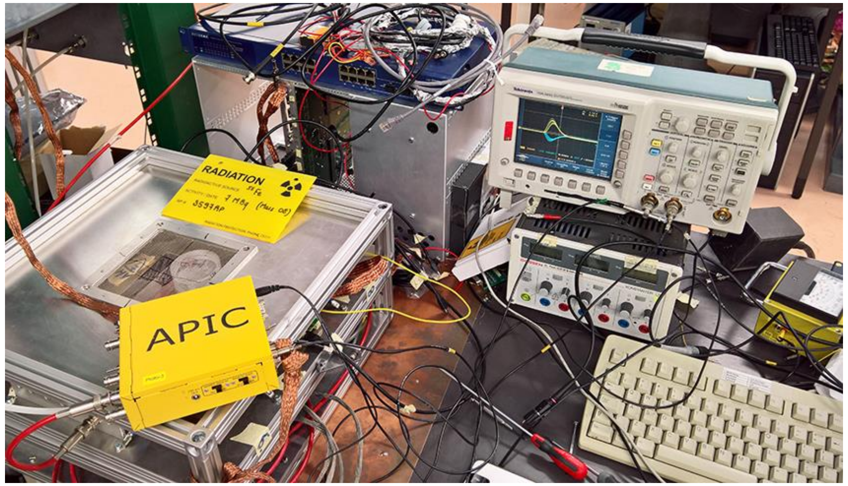
Sampling clock fs ~ 200 Mhz

Time resolution via peak-sampling

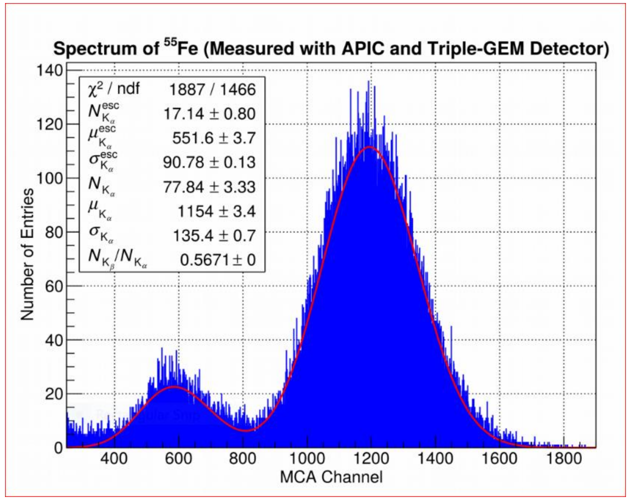
$\Gamma 2(t)$ shaper peaking time ~ 25 ns
signal envelope ~ 75 ns
~ 25 samples @ 200 MHz

$\Delta t_{peak, fit}$ expect **σ_t <<** 100 ps why ?
σ_t resolution via fit with known shape
-multipoint sampling (25) $\Gamma_n(t)$
-amplitude independence of peak : **$\sigma_{timewalk}$ ~0**
-referenced to common system clock , **$\sigma_{clockjitter}$ ~0**

APIC in GDD lab, GEM tests



2017 APIC V3

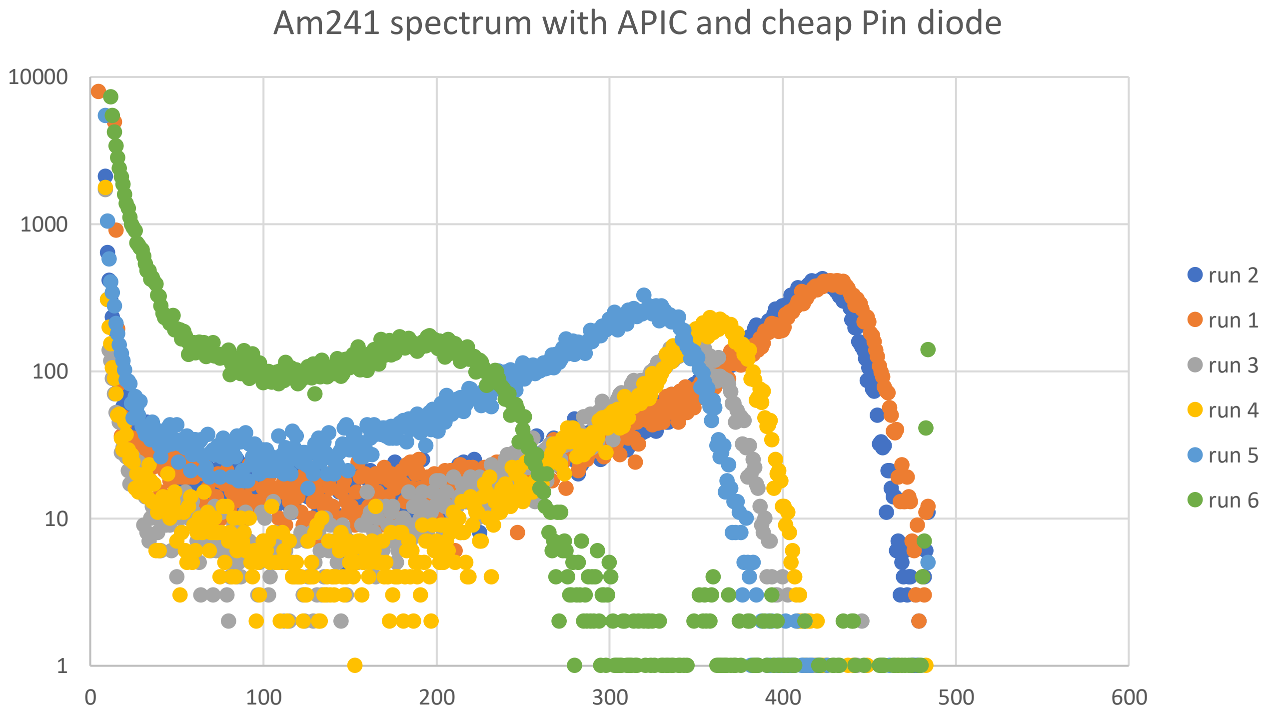


2021 APIC V4
preparation for high-rate
testbeam telescope

Alpha spectra with APIC and Pin photodiode

Photodiode

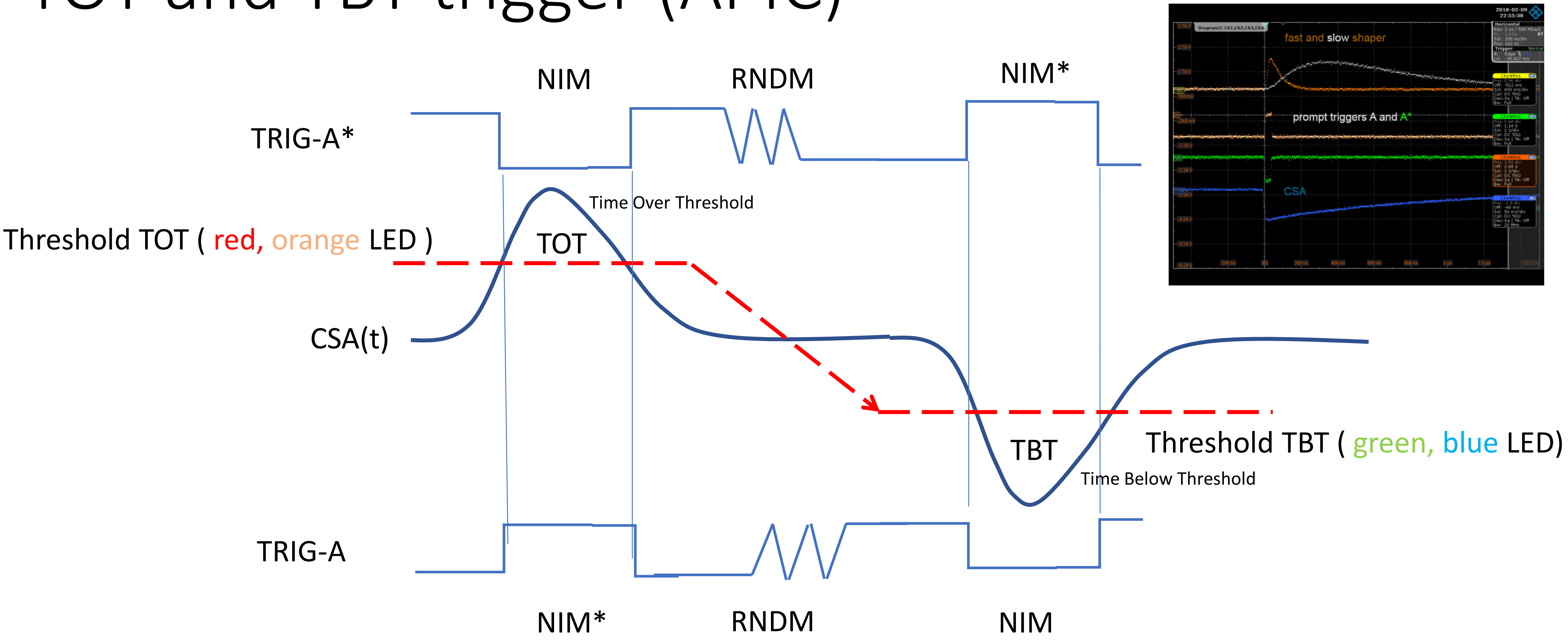
Test cover with ^{241}Am



A cheap commercial photodiode was biased at variable APIC generated bias voltages and the APIC shaper output connected to an MCA

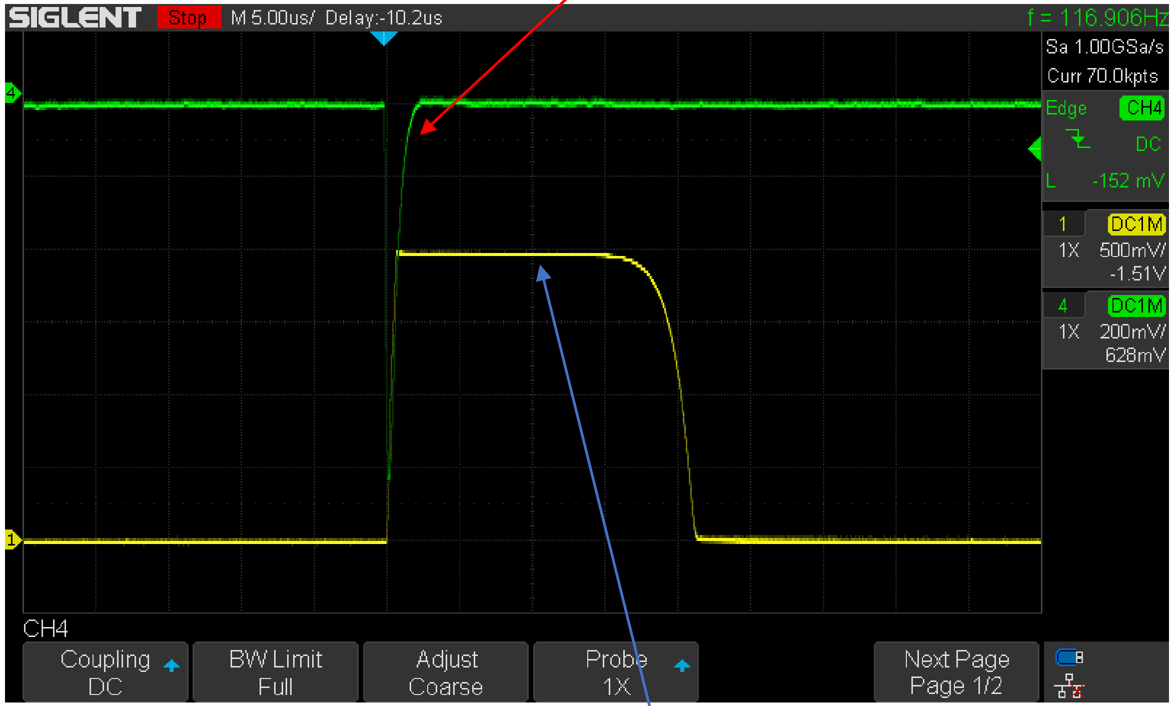
Run 1 with APIC internal Bias Voltage 20V , light shield around test box
Run 2 with 9V Battery Bias (~ noiseless crosscheck), light shield around test box
Run 3 and 4 like Run 1 with 4 and 5 mm wider separation, light shield around test box
Run 6 like Run 1 but lightshield replaced by 1 thin Alu foil 5uAlu+100u Mylar
Run 6 like Run 4 but 2 x Alu foil

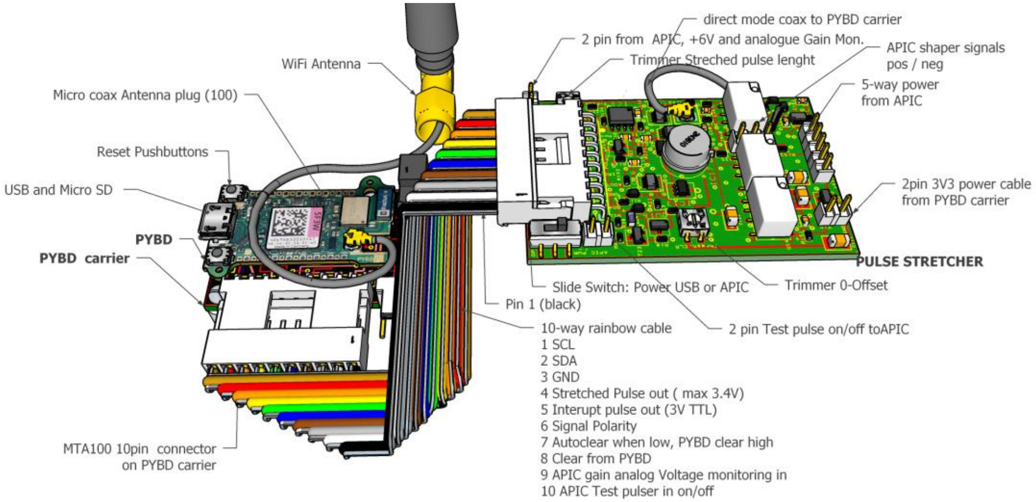
TOT and TBT trigger (APIC)



APIC$_{2019}$ peak finder-stretcher:
for use with 2.4 MS/s ADCs in SoC card for data conversion

APIC shaper





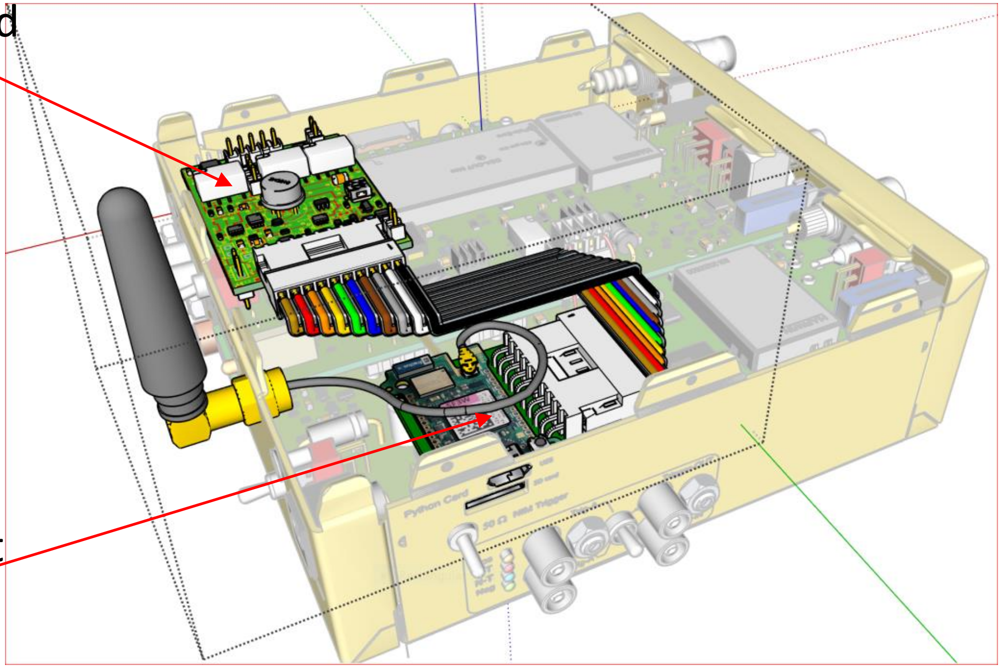
Peakfinder Controls via flat-cable from uPython SoC card

APIC pulse stretcher (15 us) => ADC

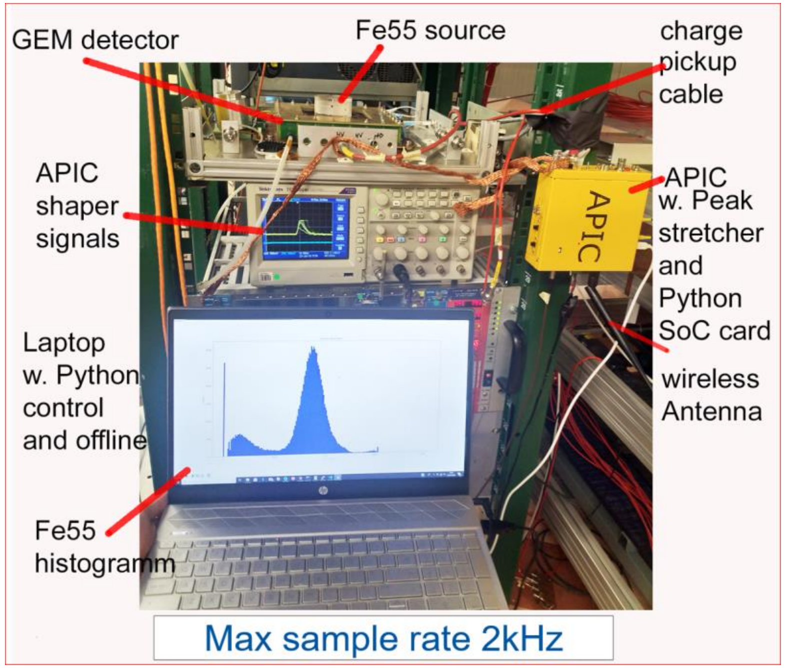
MAPIC 2019
APIC with embedded, networked MCA

2019 summer student project

added peakfinder card



added SoC with 12 bit 1MHz ADCs
includes:
uPython controls (I2C)
USB & wireless



Networked DAQ GUI-based

Summary

- discrete electronics matters
  - -R&D of concepts (before implementation in ASICs)
  - -verification / updates on real detectors
  - -training of students
  - -feature addition on user request
- Detectors with discrete frontends exist for good reasons
  - -lowest C_d , very high dyn. ranges, low noise ..
- Preamp technology keeps evolving
  - -high rate preamps
  - -matched impedance, fast risetime
- 0-timewalk shapers possible (at least in discrete)
  - - ps time resolution via peak fit
- APIC and MAPIC exist !
  - - updates planned: new preamp, 3day-autonomy, embedded MCA, networked DAQ and Ctrl

Thank you !

Les grandes choses sont souvent plus faciles qu'on ne pense

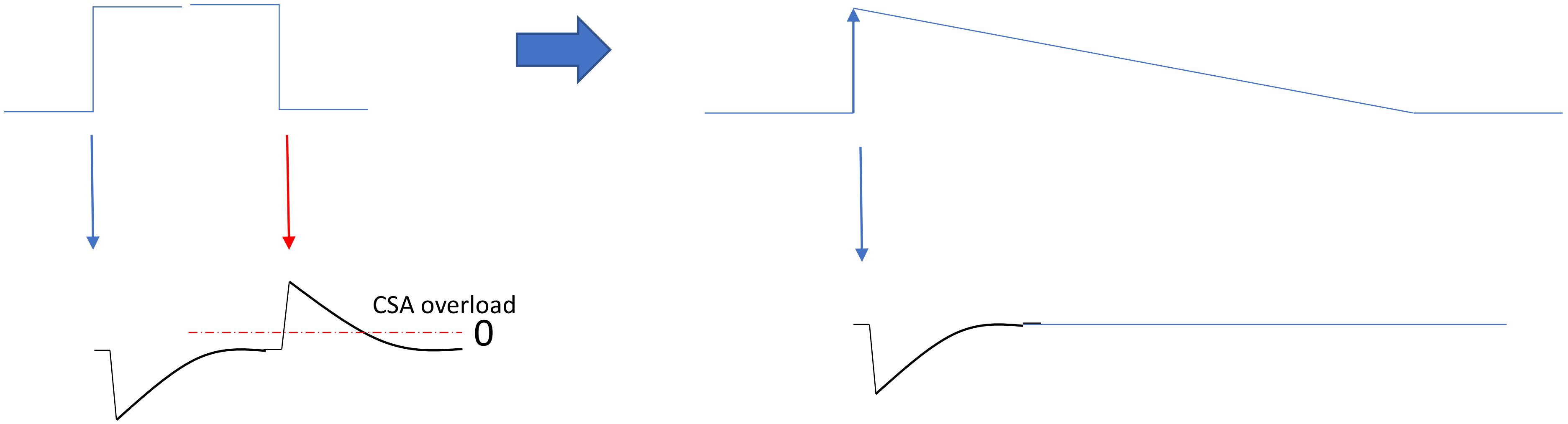
*François Marie Arouet, dit Voltaire

Backups

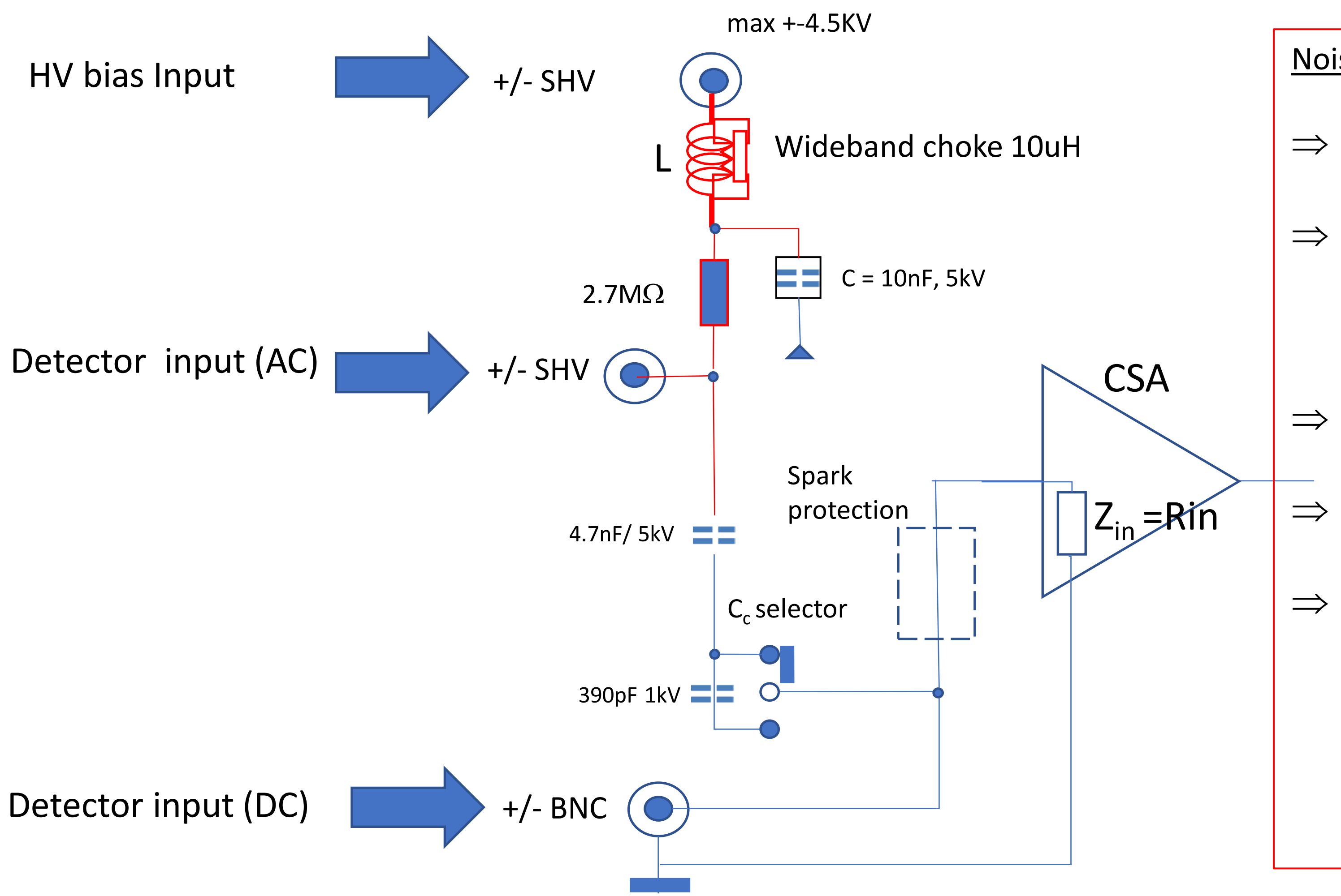
Test pulse shape

A rectangular pulse entails production of the opposite charge which can overload the CSA, at least temporarily

Saw-tooth test pulse shape avoids opposite polarity



HV bias and AC coupling (MPGD, APDs)



<u>Noise from HV bias directly coupled to CSA input</u>

⇒ wideband filtering LRC

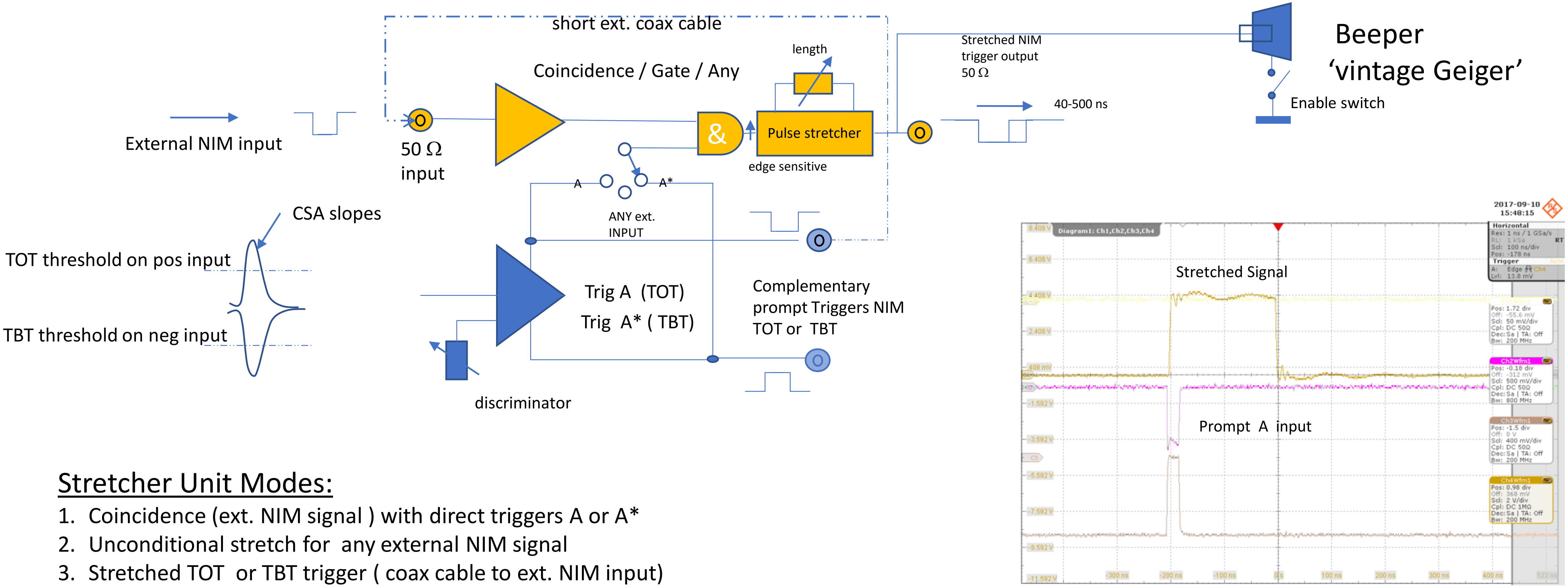
⇒ Lowpass filter L*C to reject noise
$f_0 = 2\pi$ /SQRT(LC)
10uH , 10nF ~ 500 kHz

⇒ High-ohm bias resistor (metal film , 5kV)

⇒ Capacitive coupling to separate HV-DC from AC

⇒ highpass filter $C_c * Z_{in}$ [Z_{in} ~ 75 Ω]
passes signals above $f_0 = 1/(2\pi R_{in}C_c)$
(390 pf ~ 5 MHz, 4.7nF ~ 0.4 MHz)

Stretcher & coincidence unit



Stretcher Unit Modes:

1. Coincidence (ext. NIM signal) with direct triggers A or A*
2. Unconditional stretch for any external NIM signal
3. Stretched TOT or TBT trigger (coax cable to ext. NIM input)

spark protection APIC

triple spark protection scheme:

ΔU_{in} >> 50V : 1 ns -> $\Delta U_{out\ max}$ = 3V