RD51 Collaboration Meeting and Topical Workshop on FE electronics for gas detectors
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BIS78 RPC Front-End electronics

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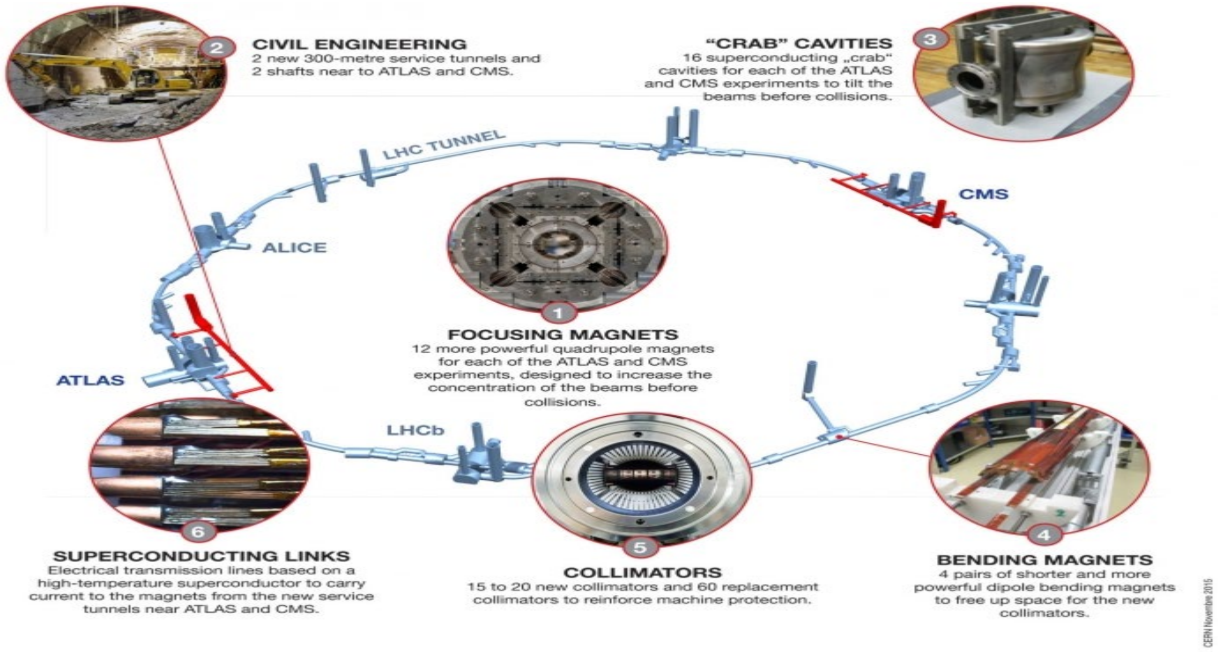
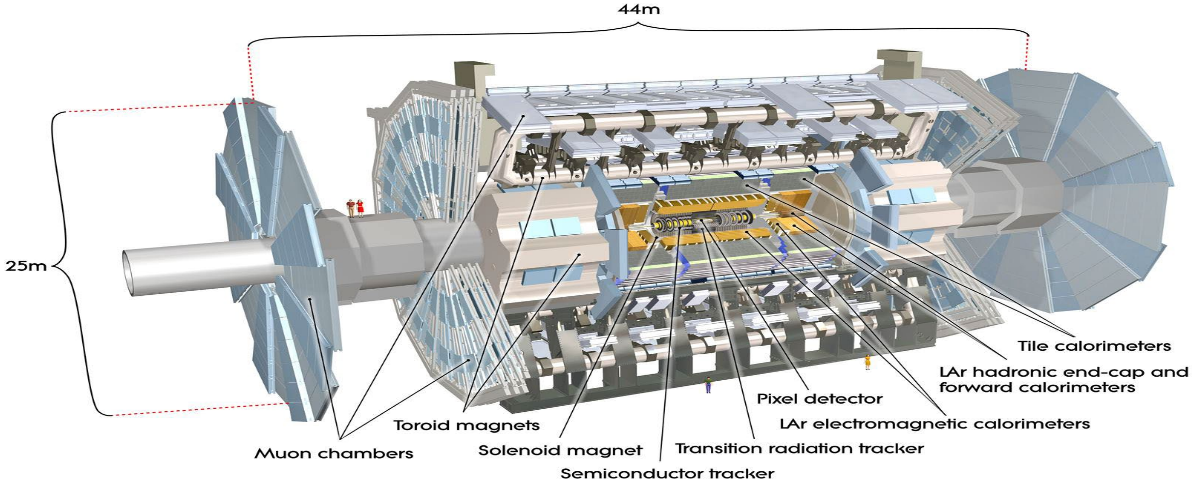
LHC and HL-LHC



	LHC	LHC Phase-1	HL-LHC (Phase-2)
E_{cm} TeV	7	13-14	14
L (10^{34} $cm^{-2}s^{-1}$)	1	3	7
L (fb^{-1})	30	300	3000
Interactions/Bunch Crossing	≈ 30	$\approx 55-80$	≈ 200



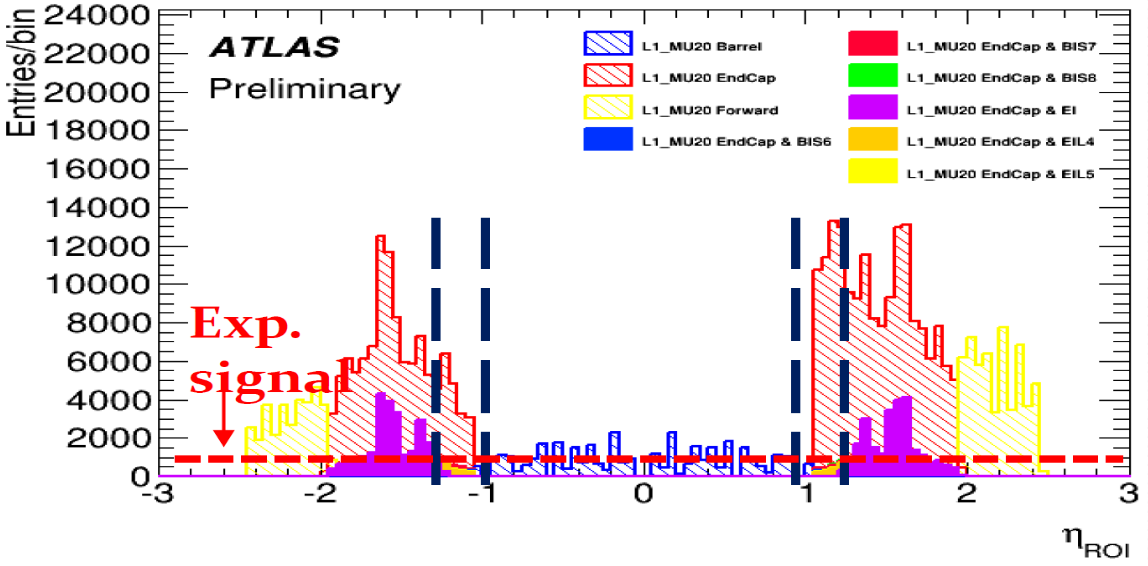
The challenge of Atlas Muon Spectrometer is to preserve its present muon identification and tracking performance, and its standalone and combined (with inner tracker detector) momentum resolution in much harsher conditions in terms of:

- particles rate
- integrated radiation
- pile-up

One of the upgrade scheduled for the HL-LHC, in order to improve the ATLAS muon spectrometer is the Resistive Plate Chamber (RPC) BI project

BIS78 project – BI pilot project

η distribution of muon trigger (p_T>20 GeV)

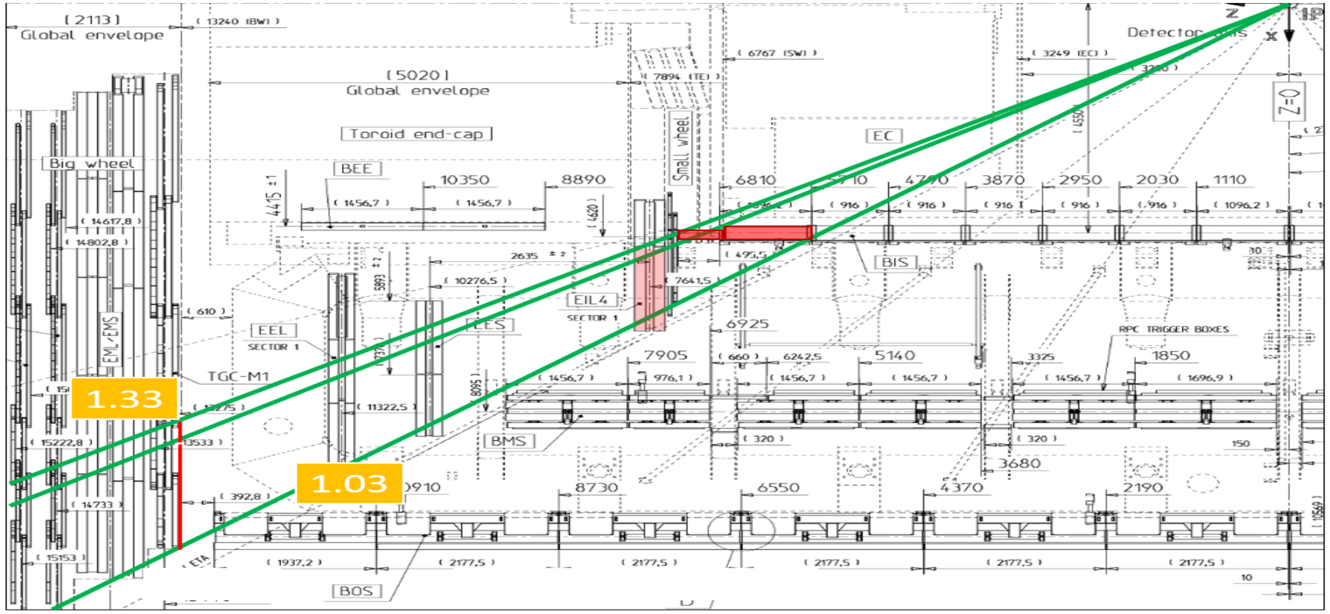


During the ATLAS Phase-1, the transition region 1<|η|<1.3 of the muon system will suffer of 2 severe problems with the increasing luminosity of LHC, concentrated in the far edges of small (even) sectors:

- High LVL1 fake rate expected and no trigger chambers present between the IP and the Big Wheel
- High photon induced counting rate, making in particular the BIS7 MDT performance insufficient for Phase II.

Two upgrades scheduled for the ATLAS spectrometer in Phase 1

1) Tracking and trigger upgrade in the η > 1.3 region with the New Small Wheel (NSW)
2) Upgrade of the ATLAS muon trigger in the barrel-endcap transition region with RPC



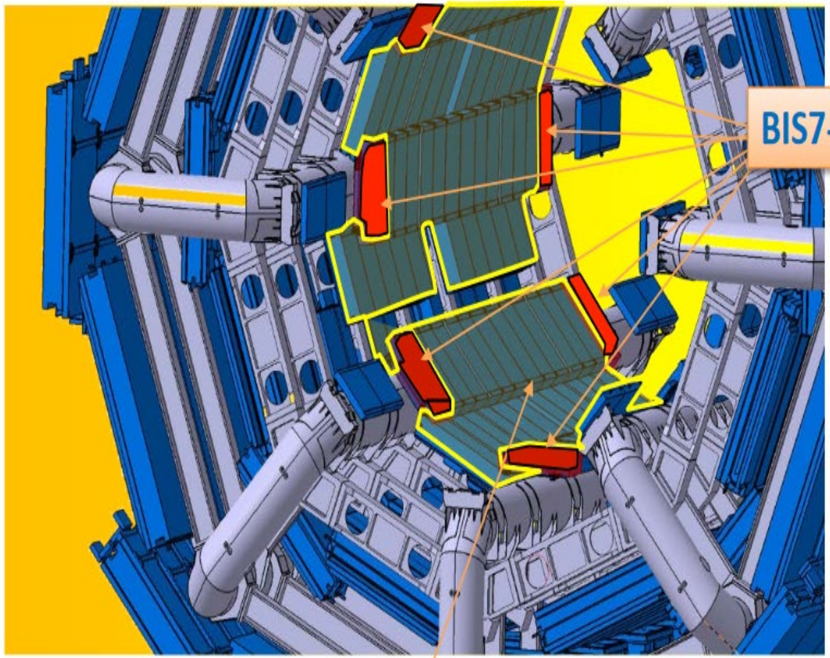
Main advantages for the BIS 7-8 location:

- This area is upstream of the cryostats where most of the fake muons are generated
- Solve the MDT rate problem
- Perfectly projective with the holes
- Robust against pileup
- Provides momentum selectivity

BIS78 project – BI pilot project

Replace the BIS MDT 7 and 8 chambers with an integrated new generation RPC + sMDT chamber in the same envelope

	Atlas Standard RPC	BIS78 RPC
Detector		
Gas Gap width	2 mm	1 mm
Electrode Thickness	1.8 mm	1.2 mm
Gas Mixture	95% TFE, 4.7% i-C4H10, 0.3% SF6	95% TFE, 4.7% i-C4H10, 0.3% SF6
Time Resolution	1 ns	~0.4 ns
Space Resolution	6 mm	1 mm
Gaps per chamber	2	3
Readout electronics	2D orthogonal	2D orthogonal



BIS7-8 in Phase-1/Run-3 2021

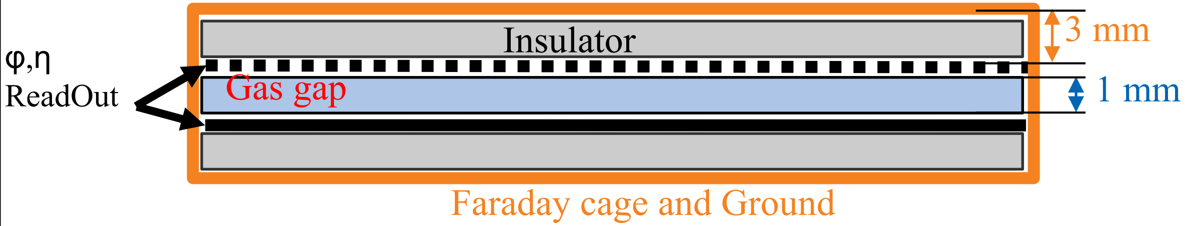
Full BI Layer for Phase-2/Run-4 2026

RPC BIS78 project:

- 16 BIS7 ≈1820 x 1180 mm^2
  16 BIS8 ≈1820 x 440 mm^2
- 3 independent layers measuring η and ϕ
- Total surface 150 m^2

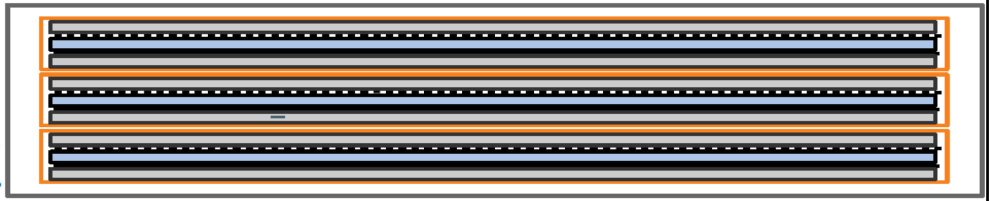
- In the ATLAS nomenclature RPC-BIS78 are considered a Small Project

RPC singlet layout



RPC triplet layout

- 3 independent singlets
- 3 x 64 φ FE chs
- 3 x 16/40 η FE chs



RPC detector and high-radiation environment

The **RPC rate capability** is mainly limited by the current that can be driven by the high resistivity electrodes.

$$V_{el} = V_a - V_{gas} = IR \quad \Rightarrow \quad V_{el} = \rho d \langle Q \rangle \Phi$$

$$V_{gas} = V_a - \rho \cdot \frac{d}{S} \cdot \langle Q \rangle \cdot S \cdot \Phi_{particles} = V_a - \rho \cdot d \cdot \langle Q \rangle \cdot \Phi_{particles}$$

$$RateCapability = \frac{\Phi}{V_{el}} = \frac{1}{\rho d \langle Q \rangle}$$

There are several possible ways to increase the detectable particle flux:

1. Decrease the electrode resistivity; large technological effort, with the risk of increasing the material cost of the detector and its operating current, causing a possible ageing problems due to the more current driven.

2. Reduce the electrode thickness; similar effect obtained with the reduction of the resistivity. The difference can be found in the bigger amplification of the induced signal and therefore in the improvement of the signal to noise ratio.

3. **Reduce the average charge per count Q.**

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$$RateCapability = \frac{\Phi}{V_{el}} = \frac{1}{\rho d \langle Q \rangle}$$

Reduce the average charge per count Q:

This method is the only one that permits to increase the rate capability while operating the detector at fixed current.

No further ageing test required

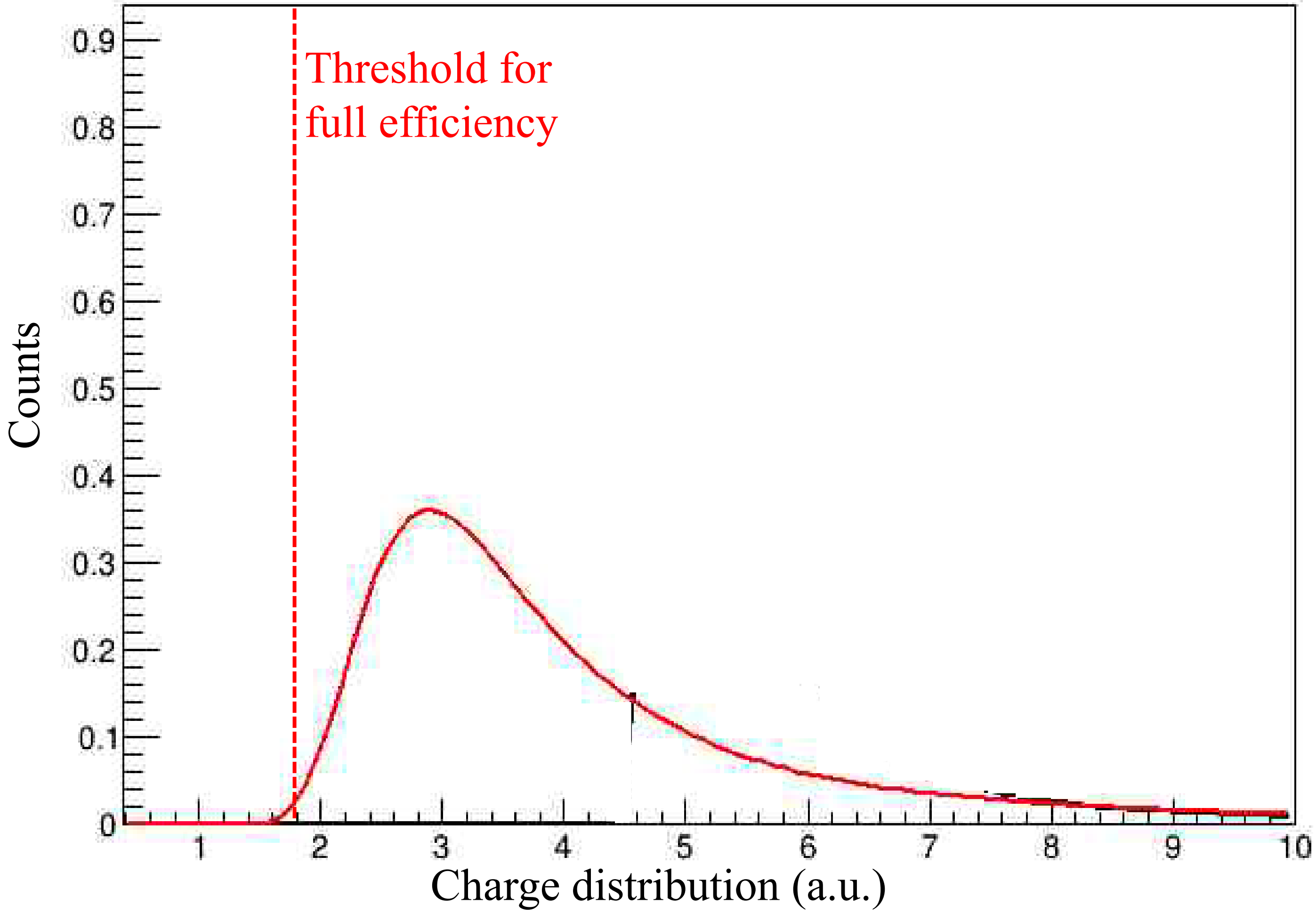
The main idea of this approach is to reduce the average charge per count moving part of the amplification from the detector to the Front-End electronics

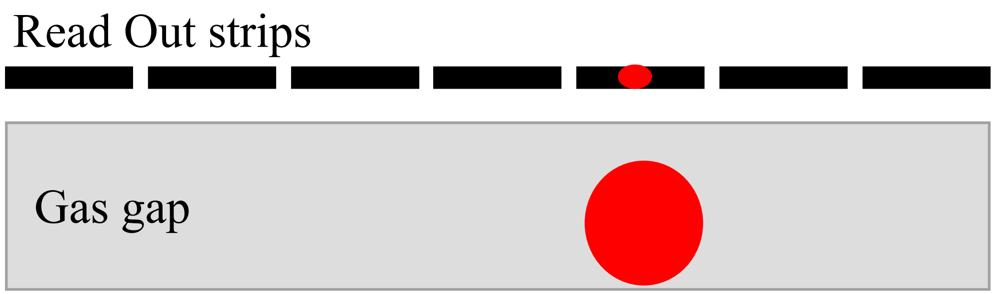
$\langle Q \rangle$ reduction requirements:

- Very sensitive FE electronics with an excellent signal to noise ratio
- High suppression of the noise induced inside the detector by the electronics and by external sources
- Very careful optimization of the chamber structure as a Faraday cage.

Front-End electronics threshold constraints

Sketch of the RPC charge distribution produced inside the gas gap



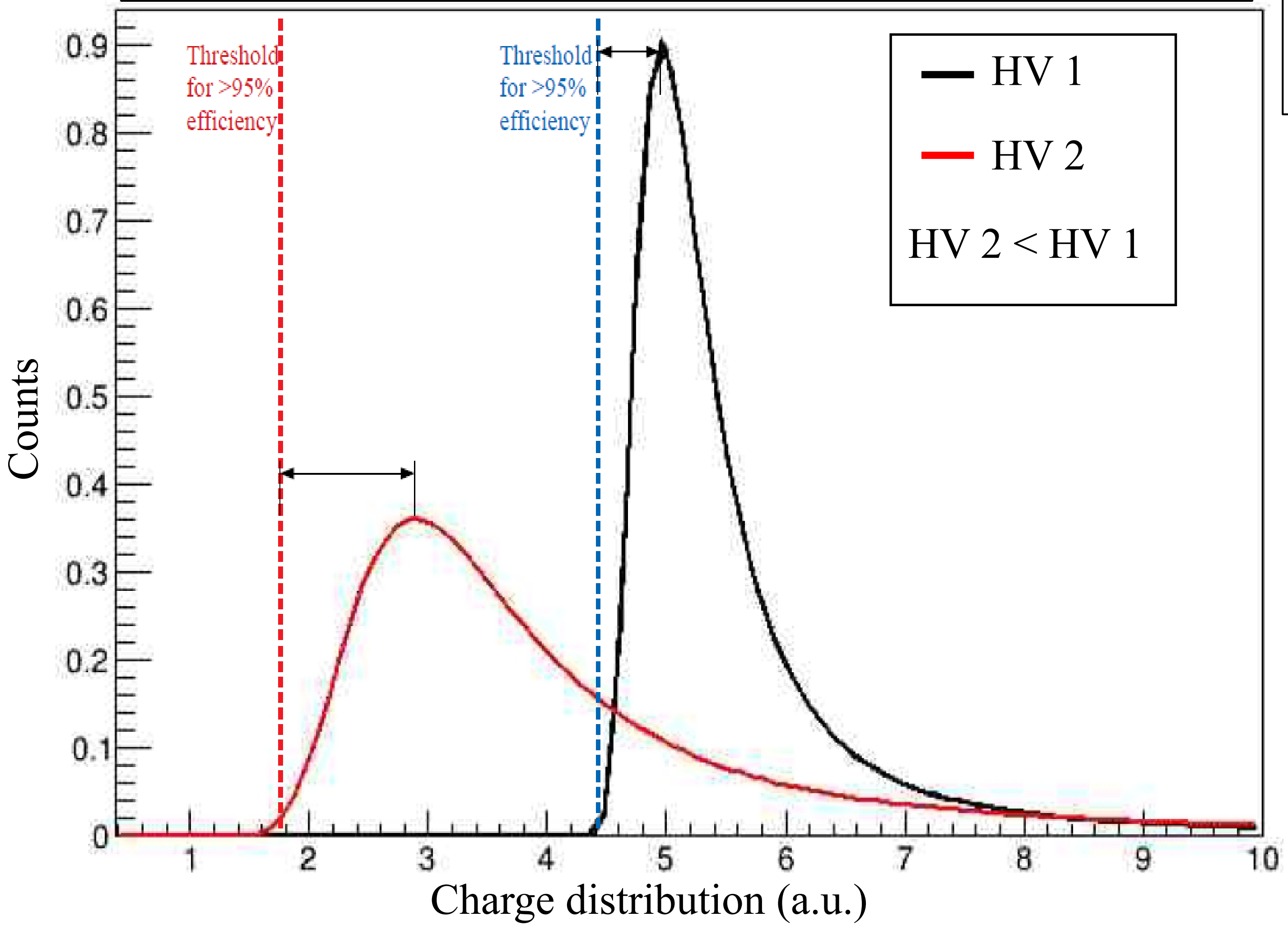


1. The quantity of charge induced on the readout panel is a factor 20-30 less with respect to the average charge per count produced inside the gas gap

2. In order to be full efficient the threshold must be set in order to be below most of the charge distribution

Front-End electronics threshold constraints

Sketch of the RPC charge distribution as function of HV



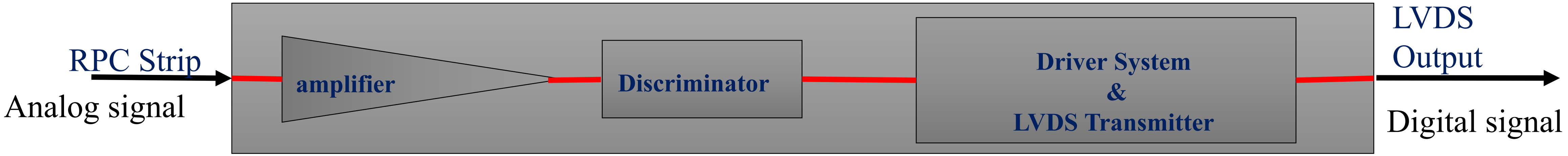
3. The approach chosen to increase the rate capability requires a reduction in the electric field

Reduction of the average charge per count (mean value of the charge distribution)

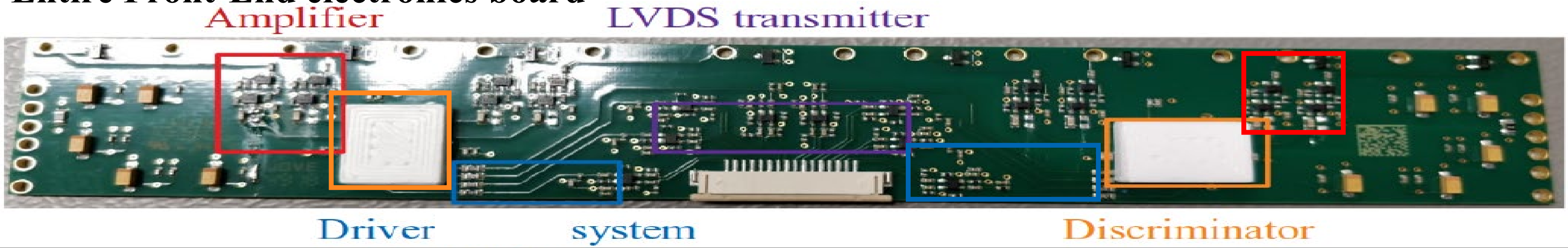
Charge distribution changes, spreading over a wider range

BIS78 - Front-End electronics

Single channel configuration:



Entire Front-End electronics board



Amplifier parameters

- Silicon standard components
- Gain: 0.2-0.4 mV/fC
- Power consumption: 1-5 V 1–2 mA
- Band-width: 100 MHz

Discriminator parameters

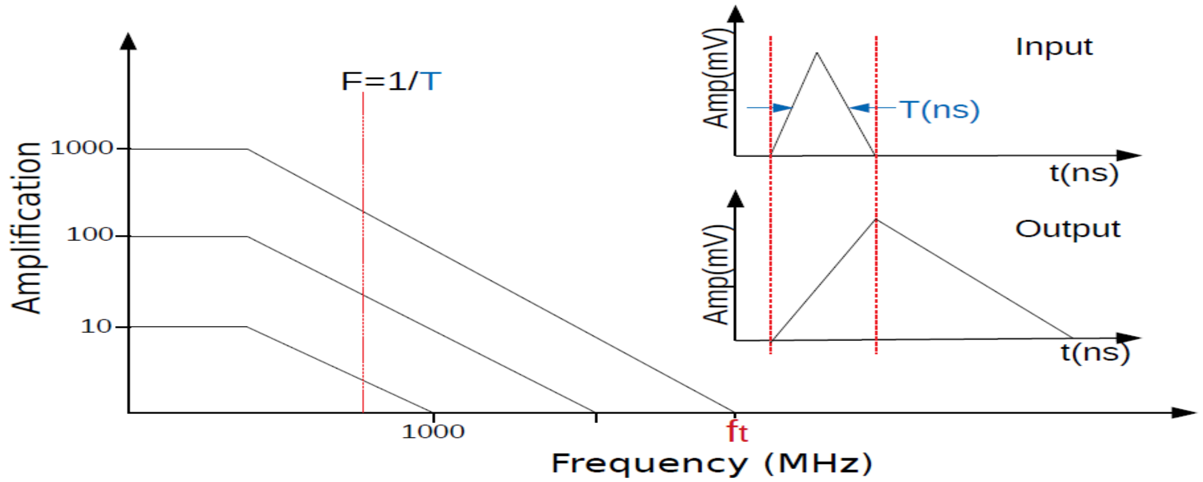
- SiGe full custom
- Power consumption: 2-3 V 4-5 mA
- Threshold: 0.5 mV
- Band-width: 100 MHz

1. Minimum Threshold of 0.3 mV
2. Detectable signal of *1-2 fC*

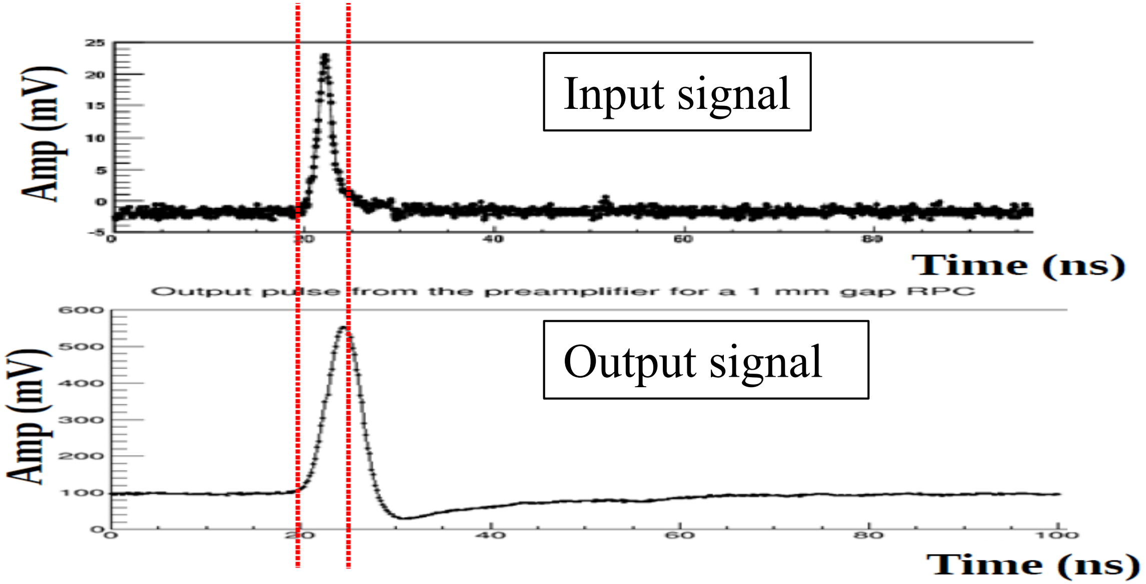
} Reduction of factor 5-10 in the charge produced inside the gas gap ⇒ **Rate capability up to some kHz/cm²**

Time-over-threshold measurement achievable directly within the Front-End

Front-End electronics – Amplifier



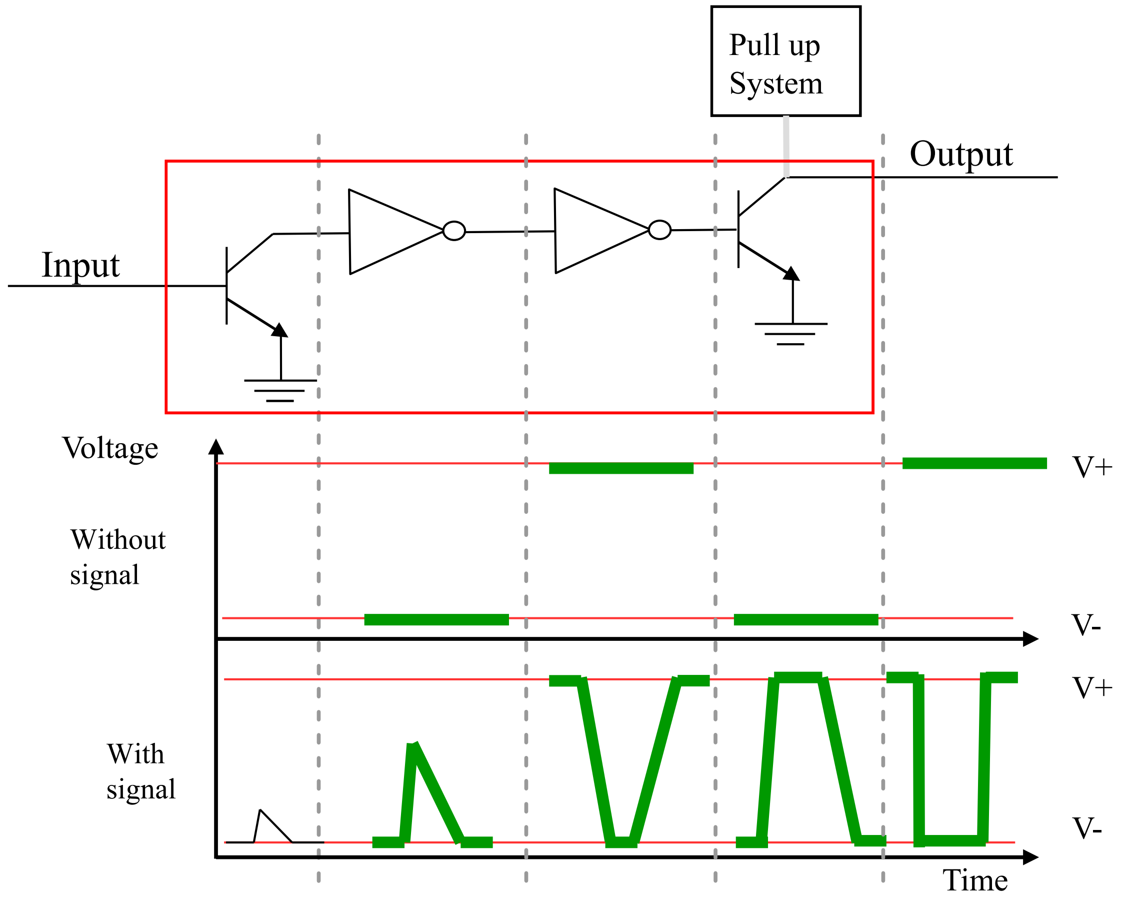
The new amplifier developed for the RPCs is made in **Silicon Bipolar Junction Transistor** technology. It is based on the transimpedance concept with a fast charge integration and the possibility to match the input impedance to a transmission line.



Preamplifier parameters	
Voltage supply	1-5 Volt
Sensitivity	0.2-0.4 mV/fC
Noise (up to 20pF input capacitance)	4000 e^- RMS
Input impedance	50-150 Ohm
BandWidth	10-100MHz
Power consumption	2-10mW/ch
Rise time $\delta(t)$ input	300-600 ps
Radiation hardness	1 Mrad, 10^{13} $n\ cm^{-2}$

Front-End electronics – Discriminator

The new full-custom discriminator circuit dedicated to the RPCs for high rate environment is developed by using **the Silicon-Germanium HBT technology.** The main idea behind this new discriminator is the limit amplifier. If the signal surpasses the threshold, it will be amplified until saturation giving as output a square wave.

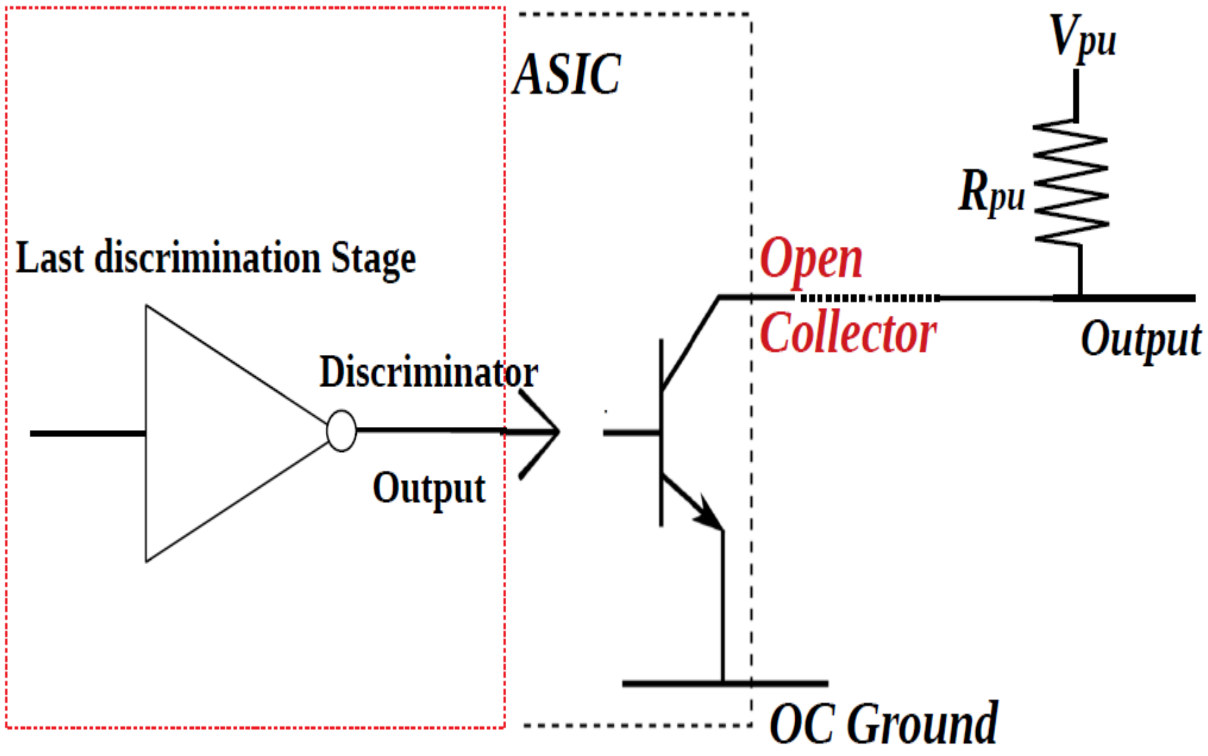


The principle of **SiGe heterojunction bipolar transistor (HBT**) is to introduce a Silicon-Germanium impurity in the base of the transistor. The advantage of this device is that the band structure introduces a drift field for electrons into the base of the transistor, thus producing a ballistic effect that reduces the base transit time of the carriers injected in the collector. The net effect is to improve the transition frequency and to introduce a directionality in the charge transport allowing a much lower value of B-C capacitance; hence a much higher charge amplification can be achieved.

Discriminator parameters	
Technology	Si-Ge BiCMOS 130 nm
Voltage supply	1-2.5 Volt
Minimum Threhsold	0.3 μV
Minimum input pulse width for threshold linearity	0.5 ns
BandWidth	10-100MHz
Power consumption	10mW/ch
Output Rise time $\delta(t)$ input	300 ps
Input impedance	100 Ω
Double pulse separation	1 ns
Radiation hardness	10 kGy, 10^{13} $n\ cm^{-2}$

Front-End electronics – PullUp system

An **open collector** is a common type of output found on many integrated circuits (IC), which behaves like a switch that is either connected to ground or disconnected. Instead of outputting a signal of a specific voltage or current, the output signal is applied to the base of an internal NPN transistor whose collector is externalized (open) on a pin of the IC. The emitter of the transistor is connected internally to the ground pin, while the polarization of this transistor is achieved, from outside the ASIC, by applying the desired voltage supply through the PullUp resistor.



Advantages of Open Collector circuit:

1) Interface different families of devices that have different operating voltage levels.

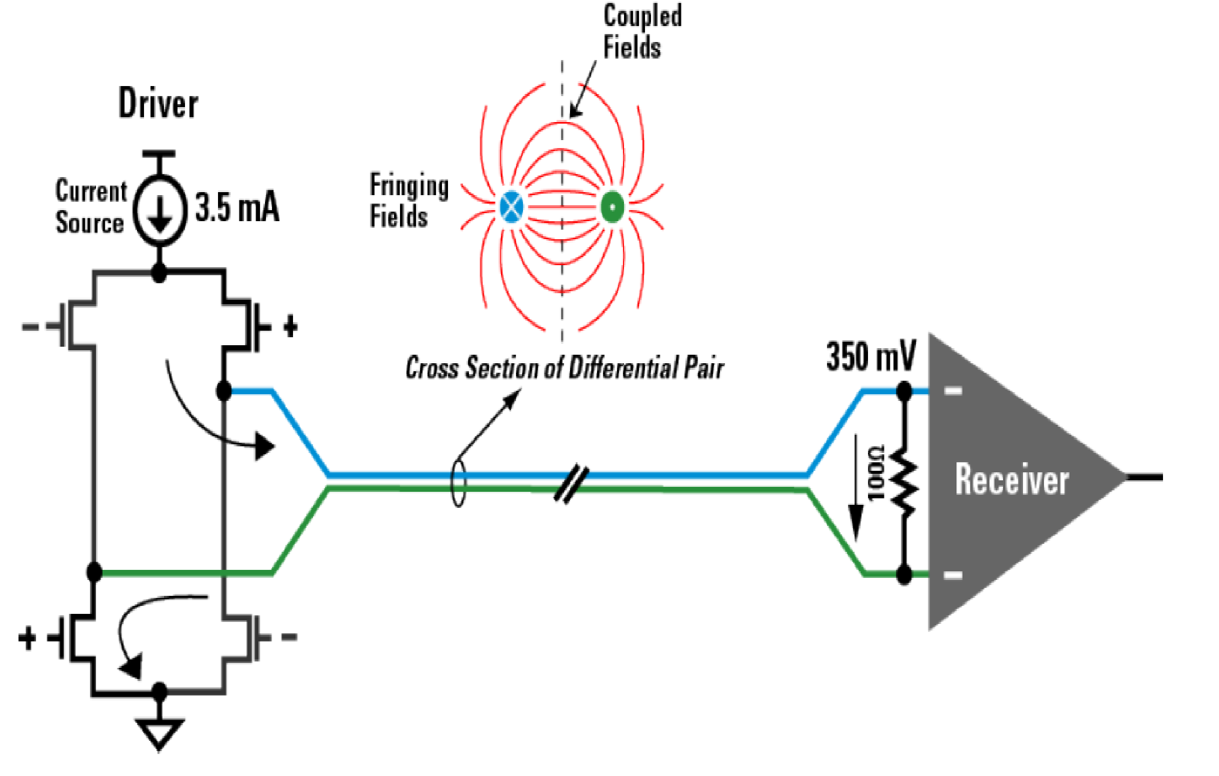
2) Withstand a higher voltage than the chip supply voltage.

3) Wired logic connection; more than one open-collector output can be connected to a single line.

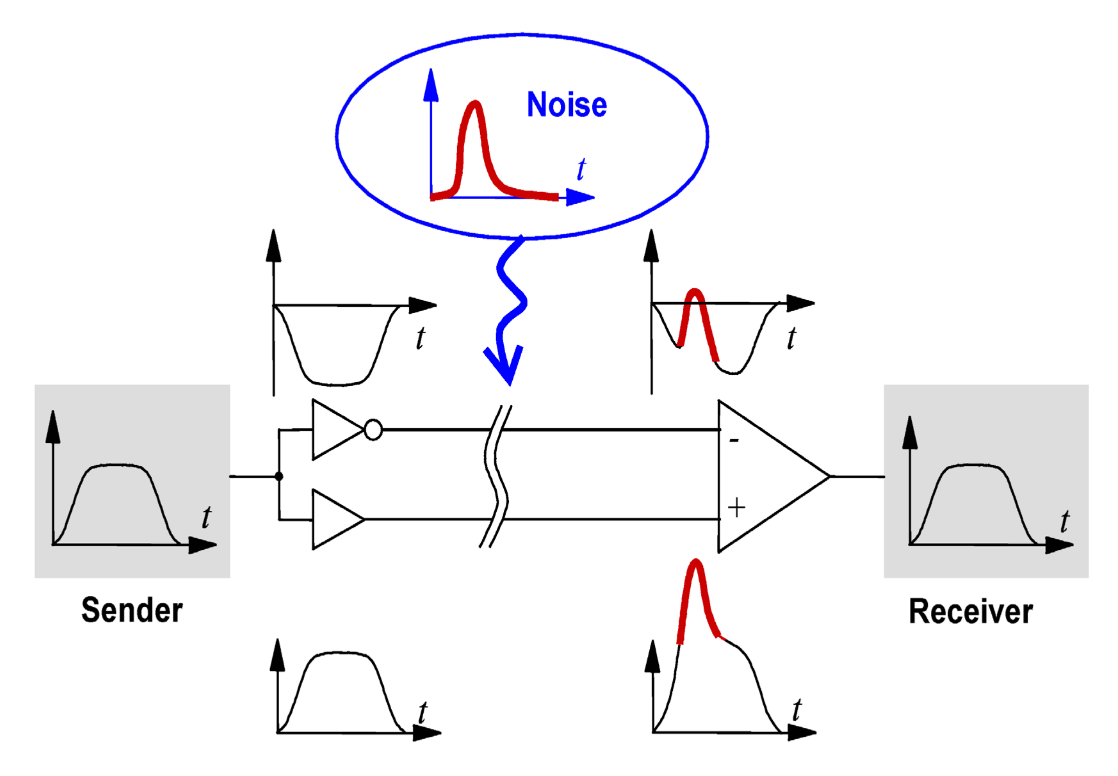
Front-End electronics – LVDS transmitter

The LVDS transmitter is a differential signaling system which transmits informations as the difference between the voltages on a pair of wires; the two wires voltages are compared at the receiver

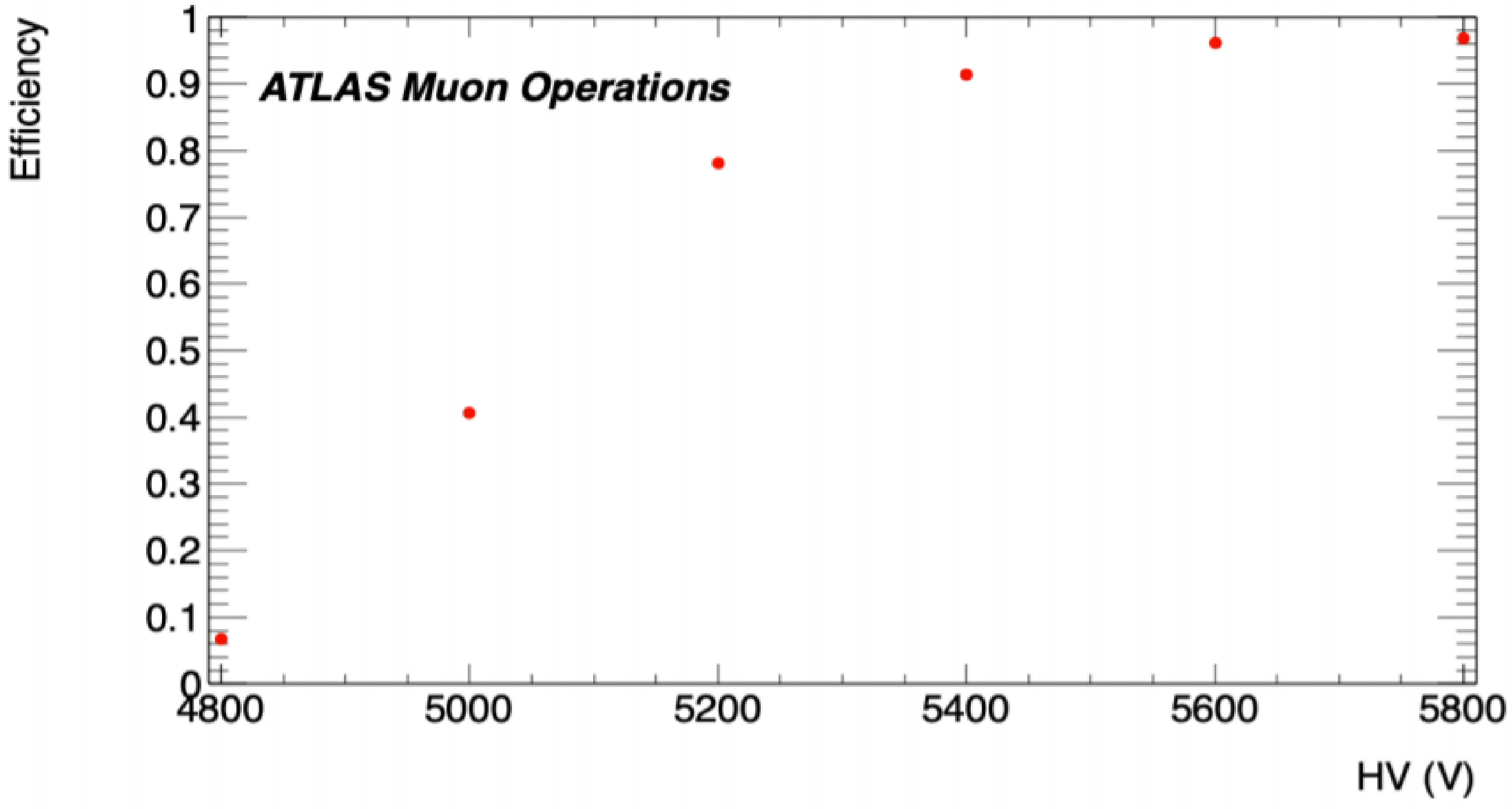
Sketch of the LVDS implementation



Main advantage of the differential transmission



BIS78 RPCs performance – Efficiency

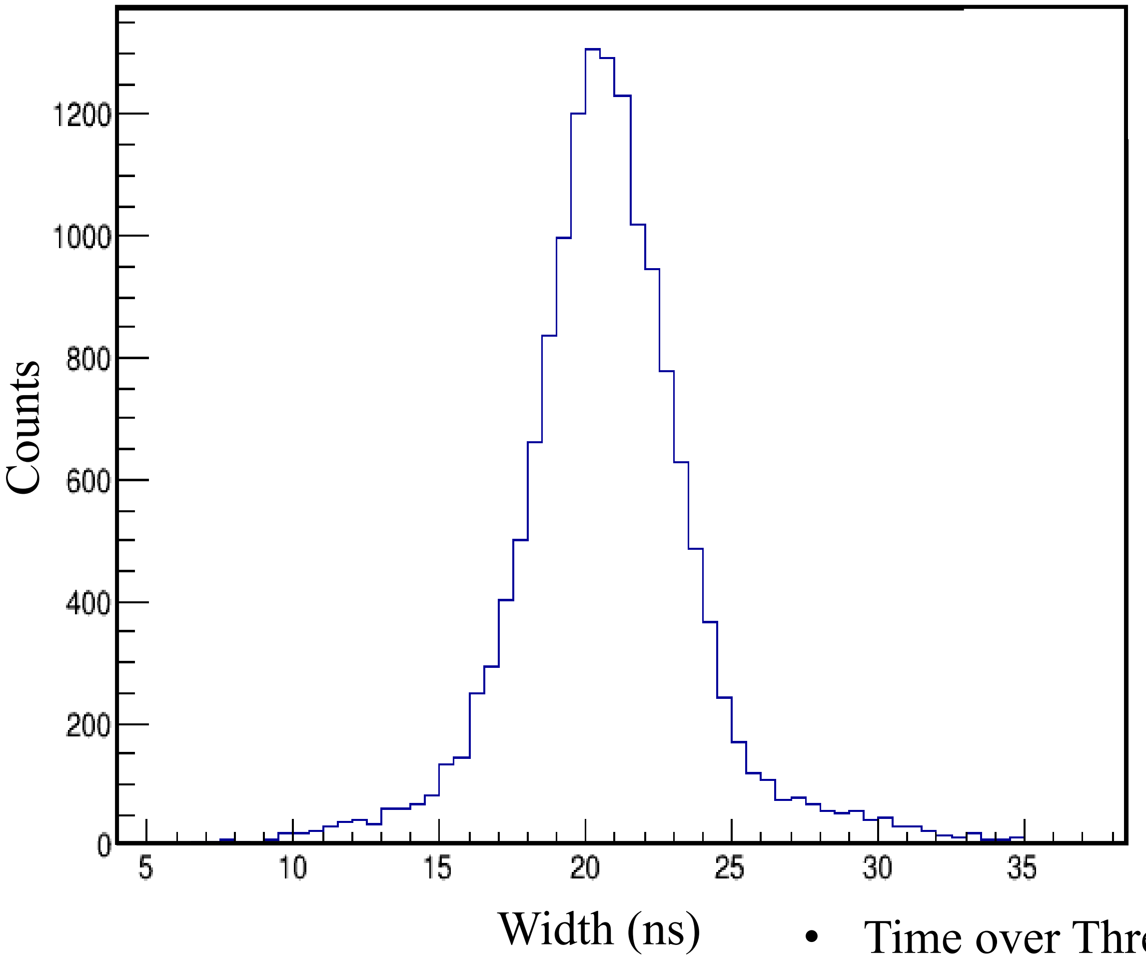


(η OR ϕ) singlet efficiency curve of a BIS7 module.
The chamber is operated with the PAD in broad self-trigger mode (just time coincidence without tracking). Two singlets are systematically kept at standard working point (5.8 kV) to provide a clean muon track ex post in the analysis in order to test the third one.
The curve is obtained considering the logical OR of the two read-out planes.
A conservative Front end threshold has been set. This threshold corresponds to 6 pC of average charge per count delivered inside the gas and allows to work with a very stable system even in high-noise environment. The possibility to use a lower threshold depends on the noise impact in UX15, which will be evaluated during the commissioning.

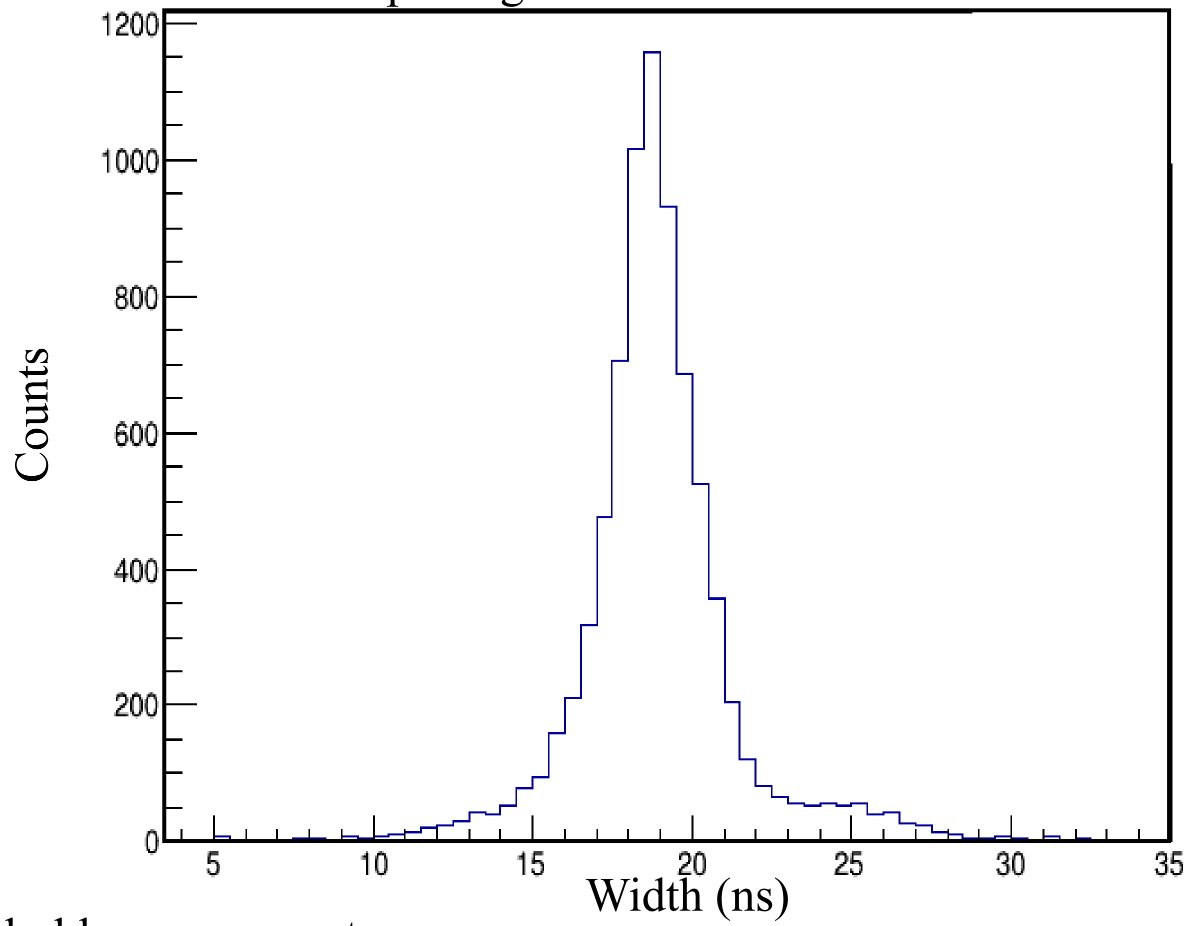
BIS78 RPCs performance – Time Over Threshold

Obtained by taking the width of the first signal of each cluster at HV=5.6 kV

η Output Signal Width distribution



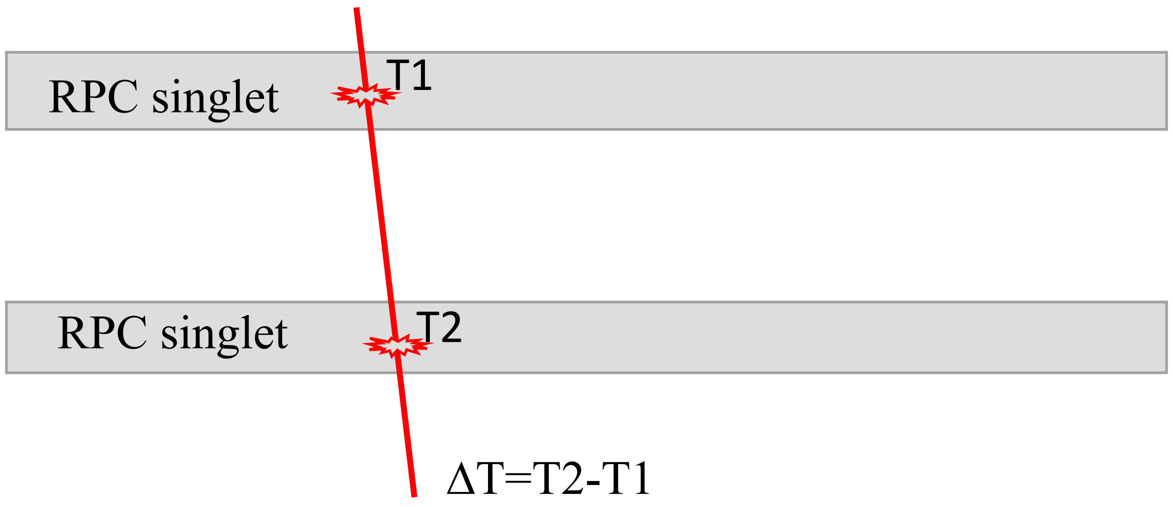
Φ Output Signal Width distribution



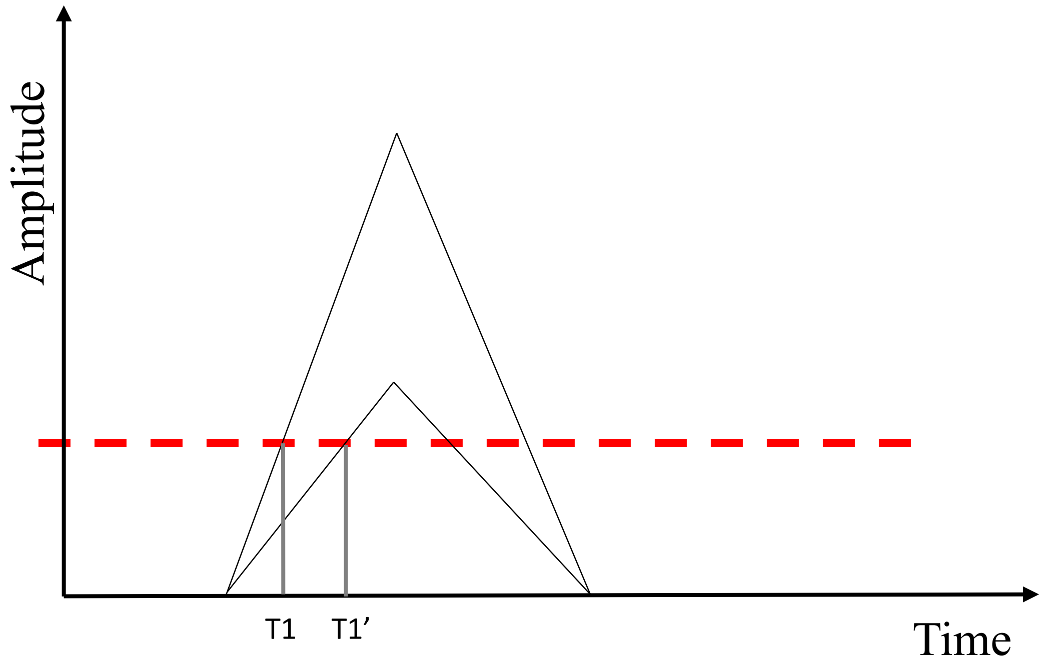
- Time over Threshold measurement
- Time walk correction for the time resolution

BIS78 RPCs performance – Time Of Flight and Time Walk

Time of Flight method for Time resolution calculation



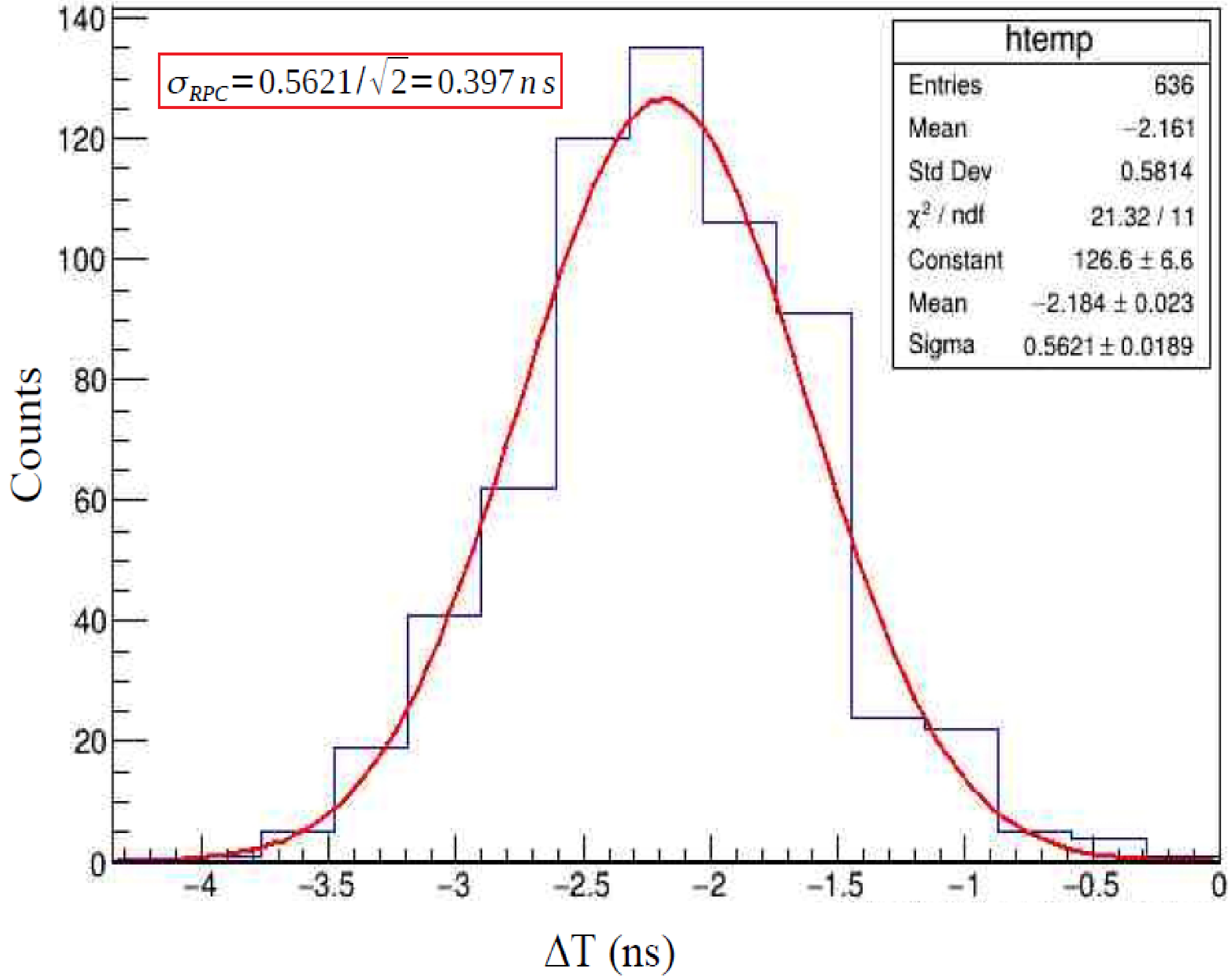
Time resolution calculated as the sigma of the gaussian fit over the distribution of the difference between the arrival time of the signals of the 2 singlets (ΔT)



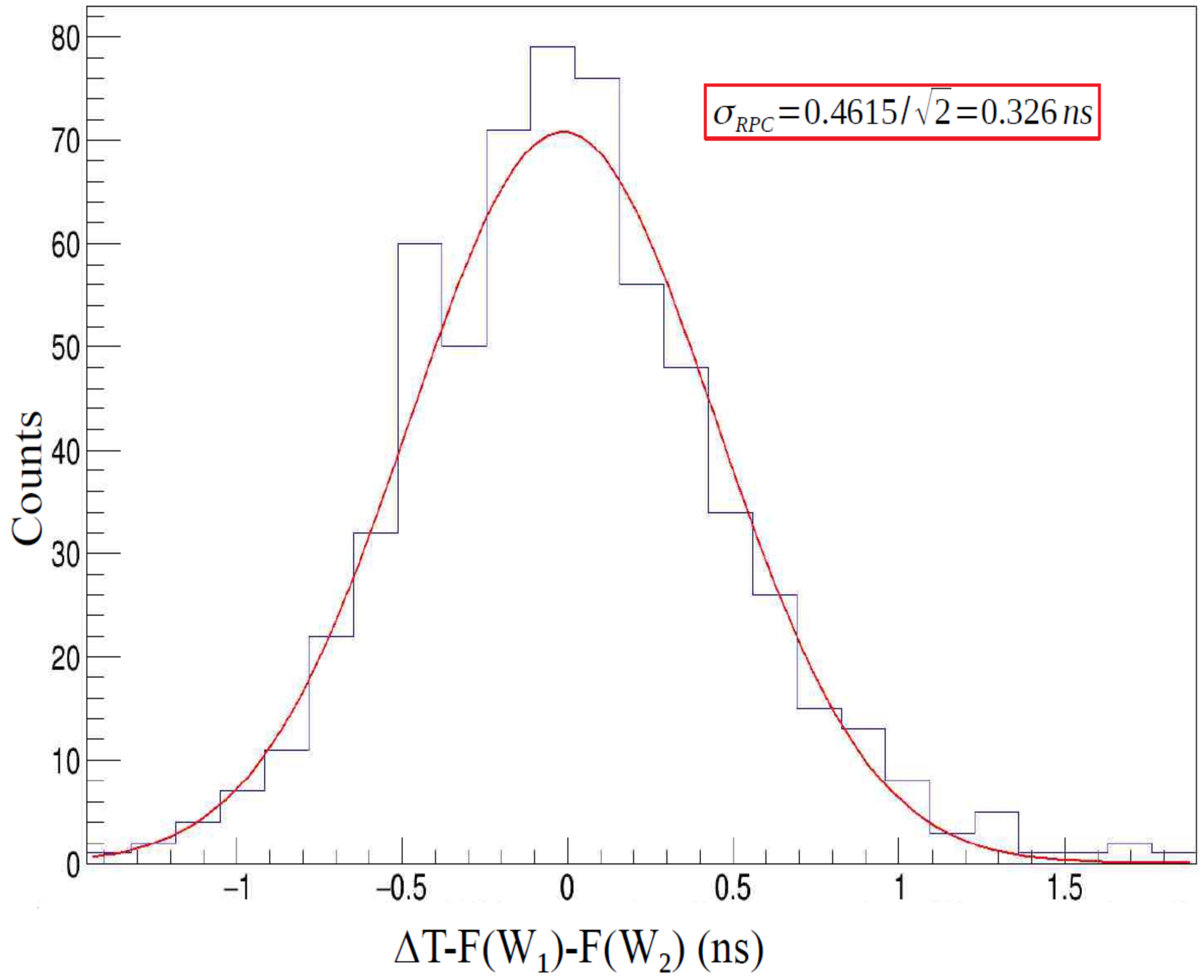
Time walk effect can be corrected by using the function F(Amplitude), which correlate the time when the signal passes the threshold and its amplitude

BIS78 RPCs performance – Time resolution

Raw time resolution without correction



Time resolution with time walk correction



Obtained at HV=5.6 kV

Conclusion

The newly developed Front-End electronics integrated with the BIS78 RPC detectors achieve the following:

1. Very low threshold of the order of few fC along with low noise and good stability

2. Huge performance uniformity in the entire detector

3. An order of magnitude in the rate capability with respect to the old ATLAS RPC

4. Raw time resolution of 400 ps and 330 ps considering the time walk correction

Thank you !