Electronics for timing detectors: the CMS PPS timing system

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on behalf of the CMS and TOTEM Collaborations

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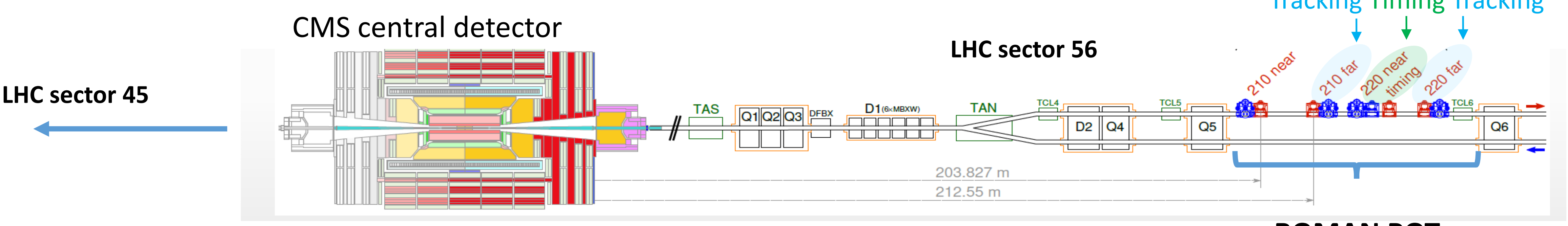
OUTLINE:

- Overview of PPS timing system
- Sensor characteristics
- FE integration and performance
- Readout with NINO+HPTDC
- Readout with SAMPIC
- Outlook and conclusions

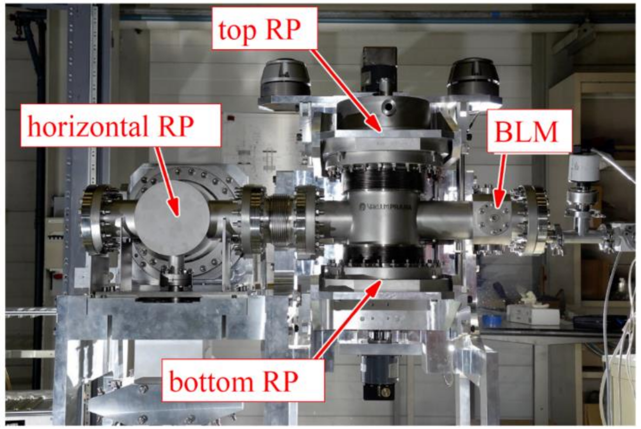
PPS detector

Symmetric experimental setup w.r.t. the interaction point to detect leading protons



- Standard RP units composed of 3 RPs (2 vertical, 1 horizontal)
- Hosted detector brought to few mm from the beam
- RP infrastructure from TOTEM

Detector operate in a vacuum



In 2017-2018 PPS RPs were inserted at
12 σ_{beam}+ 0.3 mm (~1.5 mm) from the LHC beams

Very high non-uniform irradiation field, with a **peak of ~5x10^{15} p/cm^2**(~ 2x10^{15} neq/cm^2)

Sensors in Run 2

Tracking (2 stations per sector)
2016: 2 TOTEM strip detector stations
2017: 1 strip and 1 3D pixel stations
2018: 2 3D pixel stations

Timing (1 station per sector)
2016: 4 single diamond planes (SD)
2017: 3 SD and 1 UFSD planes
2018: 2 SD and 2 double diamond (DD) planes

Another timing system, based on 4 planes of UFSD, was operated by TOTEM

Timing detectors

Average number of interactions per bunch crossing $\langle\mu\rangle$ in 2018 is ~ 35.
Beam longitudinal dimension $\sigma_z \sim 7.5$ cm.
Tracking system cannot reconstruct the primary vertex of detected protons.

Solution: measure the proton time of flight in the two sectors:

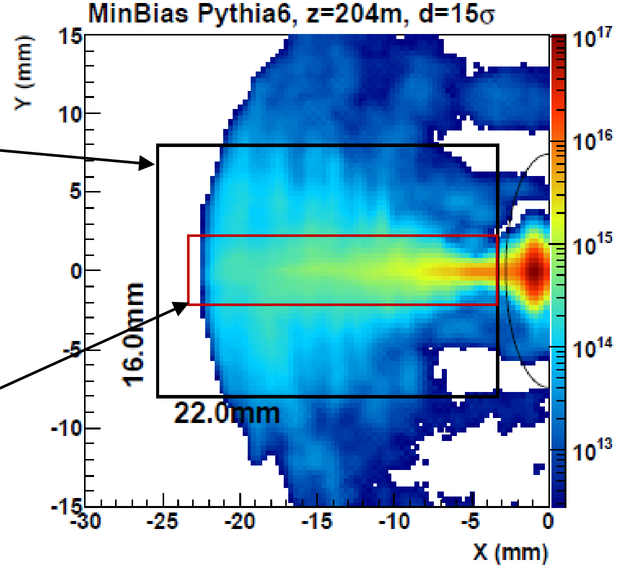
- $Z_{PP} = c\Delta t/2$
- Pile-up background reduction

PPS Detector requirements:

- Station resolution of 10-30 ps on MIP is the final goal.
- High efficiency for MIP detection
- High radiation hardness (up to $\sim 5 \cdot 10^{15}$ p/ cm^2 for $100\ \mathrm{fb}^{-1}$, highly non uniform)
- Low density/thickness detector (to fit more planes inside a RP and reduce material budget)
- Segmentation needed to avoid double hit on same pad
- Detector must operate in a vacuum

Area covered by tracking station

Area covered by timing station



Simulated particle flux for $100\ \mathrm{fb}^{-1}$ (full Run2)

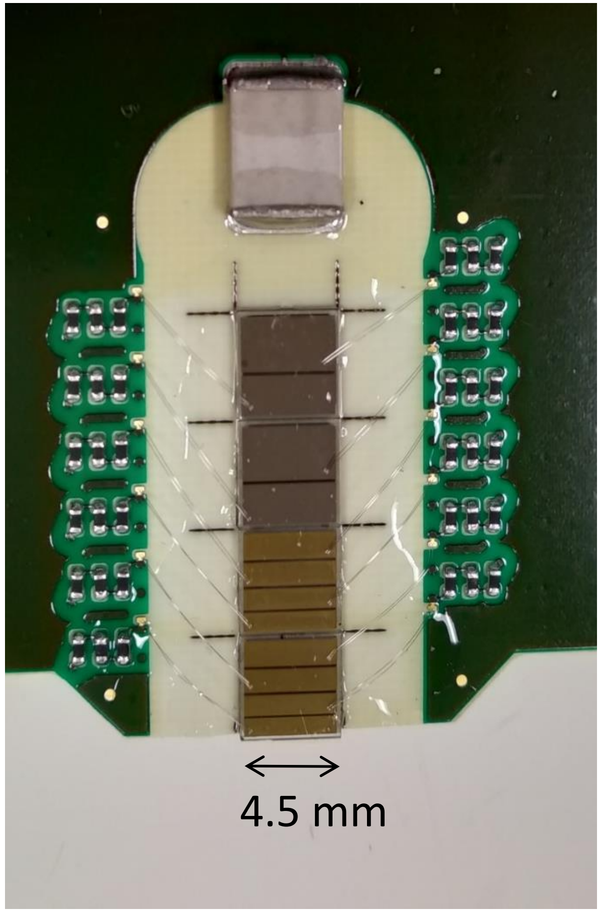
PPS diamond sensors

Originally designed for TOTEM , then used in PPS.

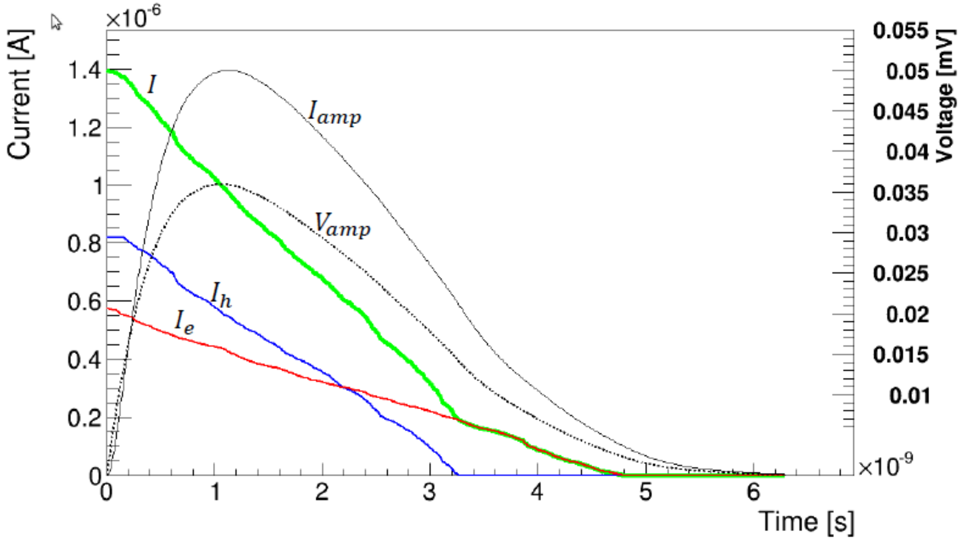
Sensor based on ultra pure single crystal CVD diamonds. Each crystal has dimensions 4.5x4.5x0.5 mm^3 , total area coverage $\sim 80\ \mathrm{mm}^2$.

Detector segmentation, optimized to reduce number of channels while keeping double hit probability low, is carried out in the metallization phase.

Pads are directly connected to pre-amplifier input to reduce input capacitance (~0.2 pF with 0.25 μm bonding wire diameter).



Sensor capacitance: 0.2-2 pF



Main signal characteristics:

- Fast intrinsic rise time (few ps)
- Very low noise (<nA) → Noise dominated by pre-amp input stage
- Low signal ~ 1 fC/MIP
- Electron/hole mobility nearly equal

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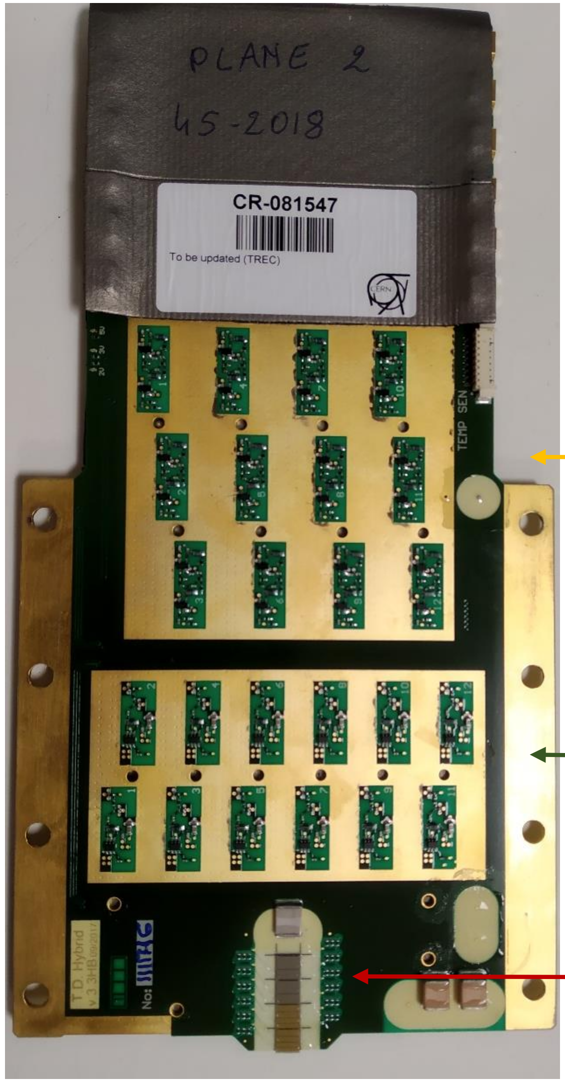
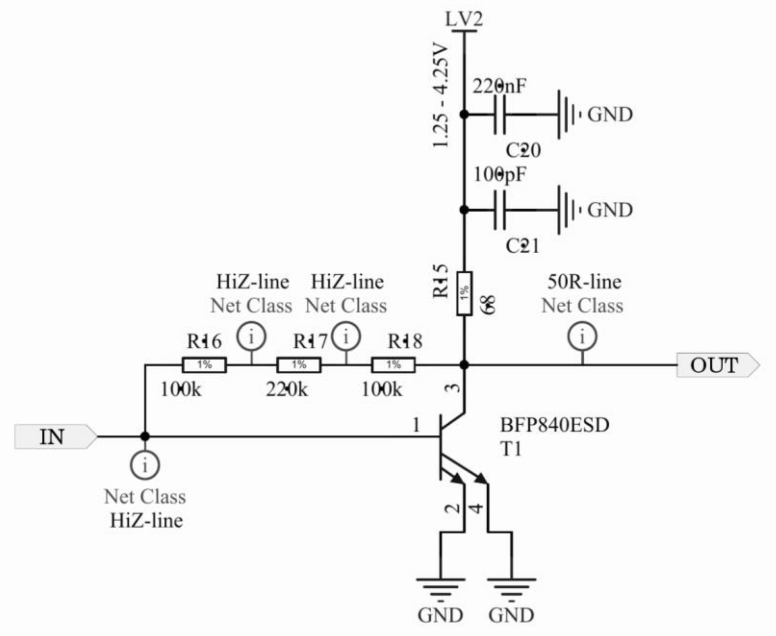
Diamond hybrid board



12 discrete amplification channels, with a design adapted from the HADES collaboration, on each hybrid board [JINST 12 (2017) no.03, P03007]

4 crystals (8 in DD configuration) are mounted on a custom hybrid board

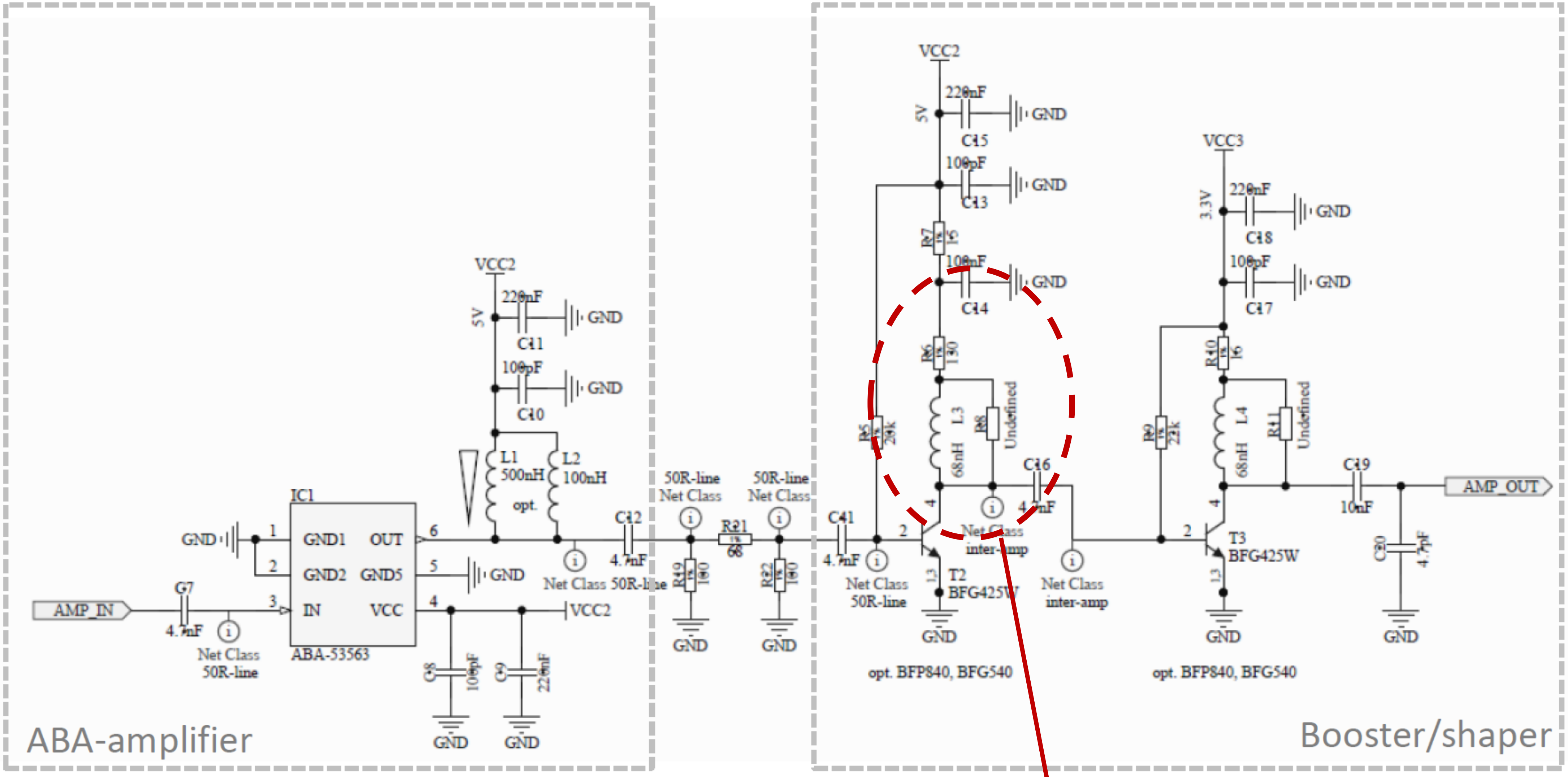


Shaper:
2xBFG425 Si BJT matched amplifier for shaping the signal

Amplifier:
Monolithic microwave integrated circuit ABA-53563, near linear phase, absolute stable amplifier

Pre-Amplifier:
stage BFP840 SiGe BJT with low-C feedback (~0.4 pF)

2nd & 3rd stage

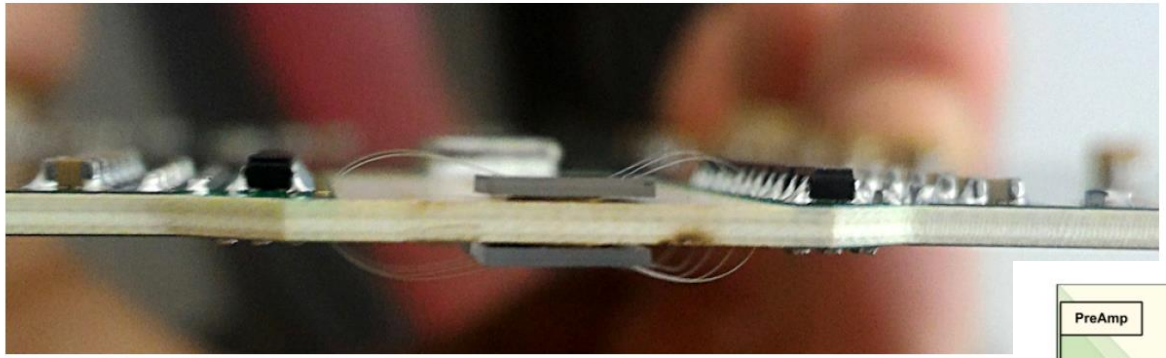


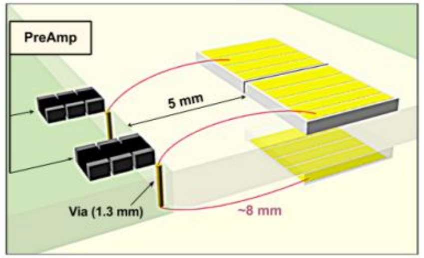
Definition of the shaping time -> ~1.5 ns for diamonds

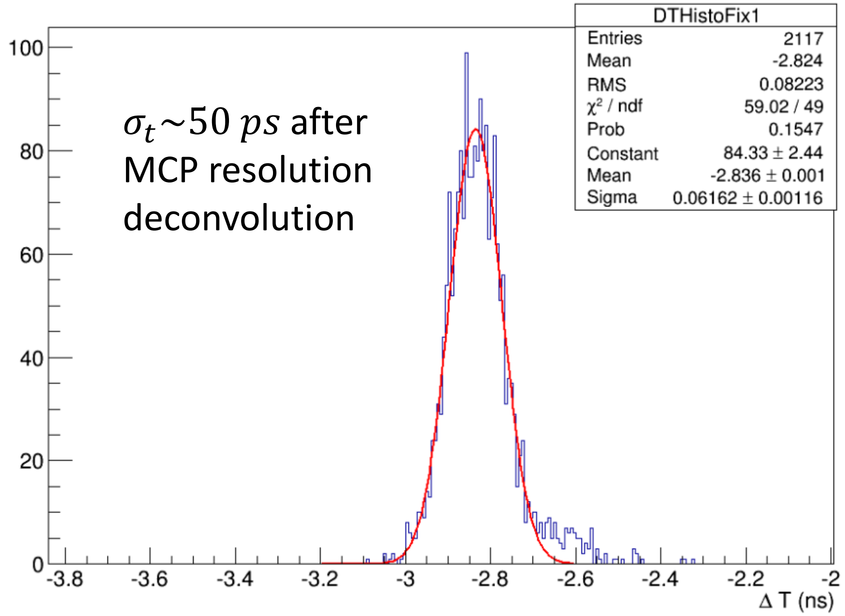
Double diamond performance

[JINST 12 (2017) no.03, P03026](https://doi.org/)

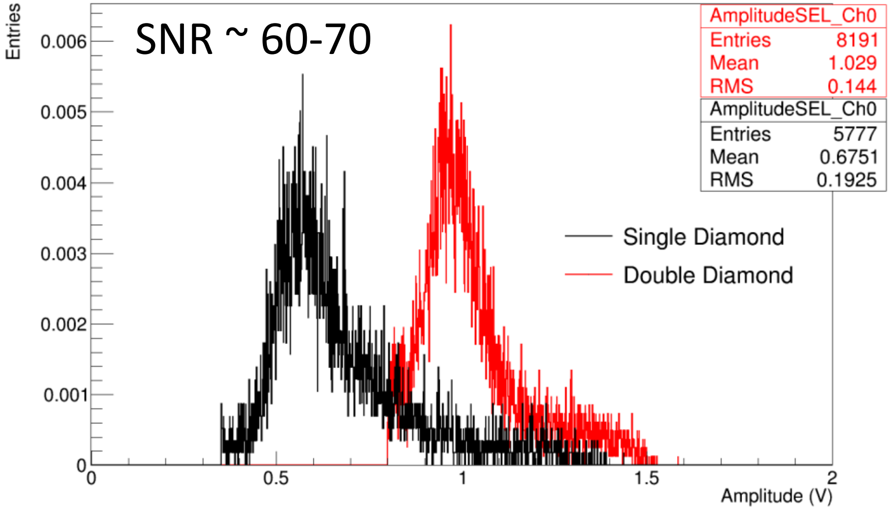
Sensor readout performed with oscilloscope. Actual sensor technology limit.







Time difference distribution between DD and reference MCP ($\sigma_{t,MCP} \sim 40\ ps$)



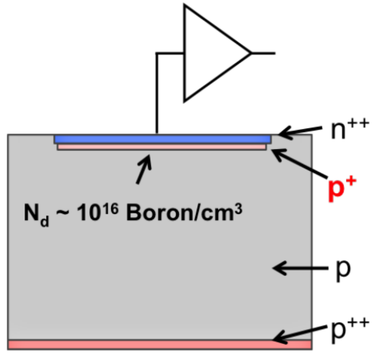
Signal amplitude comparison between DD and SD

Signal from corresponding pads is connected to the same amplification channel:

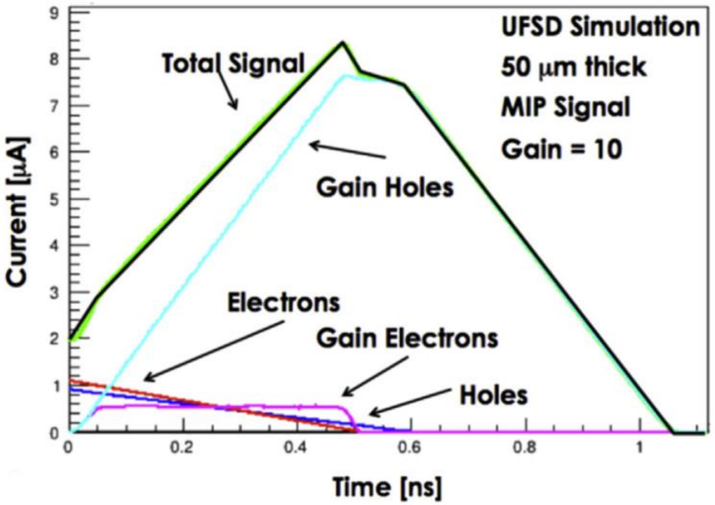
- Higher signal amplitude
- Same noise (pre-amp dominated) and rise time (defined by shaper)
- Higher sensor capacitance
- Need a very precise alignment

Better time resolution (factor ~1.7) w.r.t SD

UFSD sensors



Low gain avalanche detectors



UFSD are LGAD (Low Gain Avalanche Detector) optimized for timing:

- Reduced sensor thickness (~50 um)
- High (E~300 kV/cm in the multiplication region) and uniform electric field
- Small size to keep capacitance low

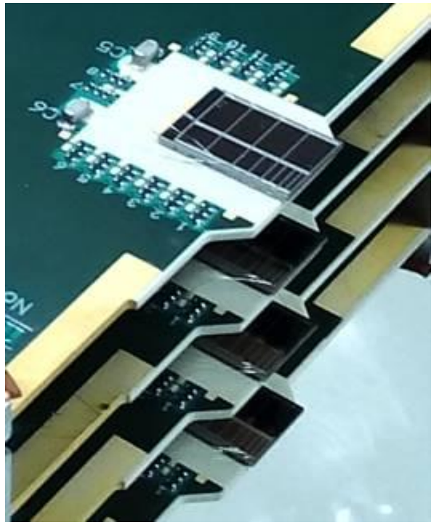
Surface [mm^2]	Capacitance [pF]	HV [V]	Time precision [ps]
1.8	3.1	180	32
2.2	4.4	180	33
3.0	6.0	180	38
7.0	14	180	57
14	28	180	102
2.2	4.4	140	49
2.2	4.4	160	41
2.2	4.4	180	33

JINST 12 (2017) P03024

UFSD detectors used in the TOTEM timing system and in PPS (1 plane in 2017).

Same hybrid board with modifications:

- ABA stage removed
- Pre-amp feedback reduced to maintain fast signal rise time with the larger sensor capacitance (~2 pF/mm2 @ 50um thickness)



Diamond timing sensors

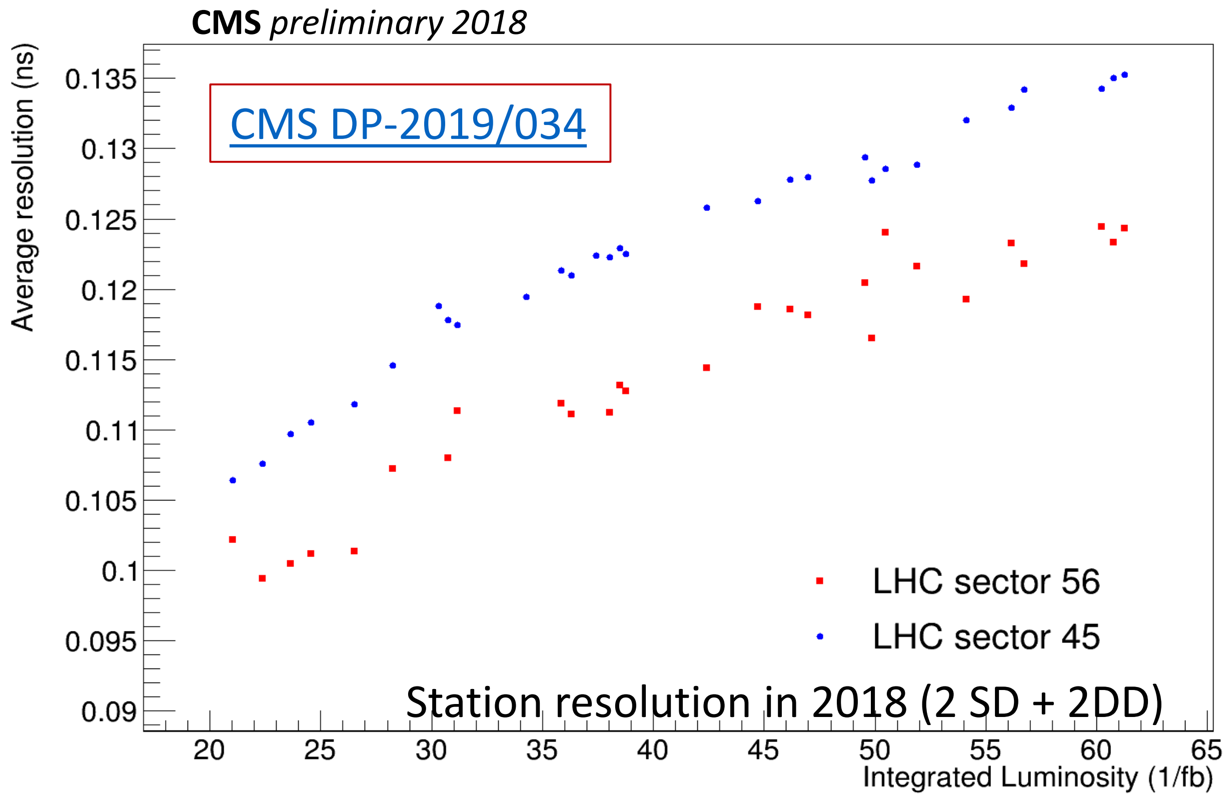
Some issues prevented exploiting the full potential of the detector:

- RF noise pickup inside RP -> reduced amplifier gain
- Beam induced HV discharges -> reduced HV
- Discrimination stage not fully optimized
- Digitization effect

The timing detector was operated during the full Run 2. In 2018 the first DD planes were installed:

- ➢ Very high detector efficiency
- ➢ Final vertex resolution ~2 cm
- ➢ Timing information (time and measurement precision) integrated in the reconstructed proton information
- ➢ Timing can be used in physics analysis to suppress pile-up background.

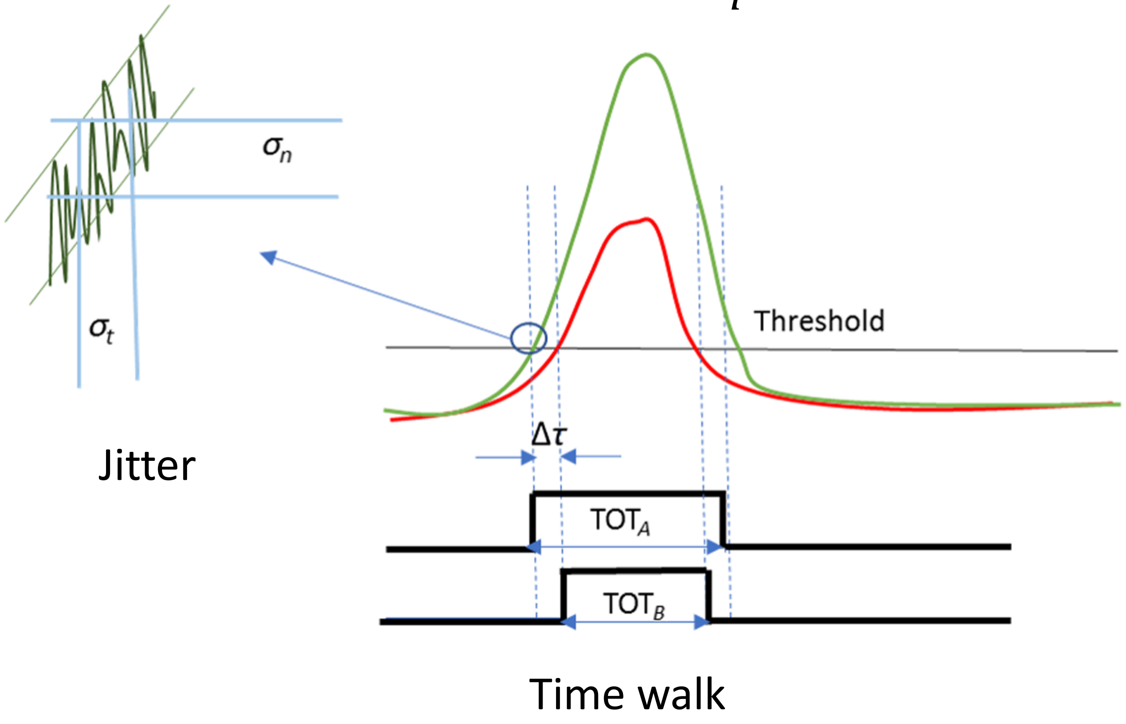
CMS DP-2020/046



Detailed studies on radiation damage to sensor and electronics available in CMS NOTE-2020/007. All timing planes dismounted and tested @ DESY.

Timing measurement

$$\sigma_t \approx \frac{RiseTime \ * NoiseRMS}{Amplitude}$$



$$\sigma_{tot}^2 = \sigma_{jitter}^2 + \sigma_{walk}^2 + \sigma_{digi}^2$$

Requirements for good timing:

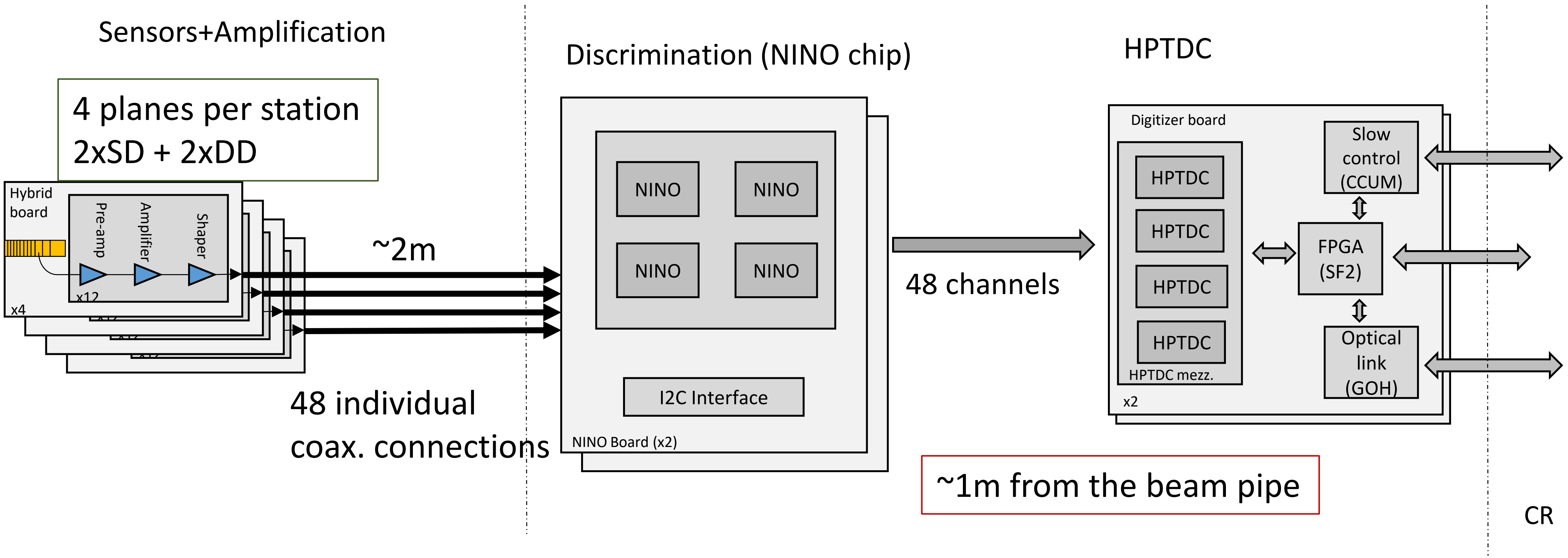
- High SNR and slew rate of the sensor signal
- Signal shape must be constant
- Possibility to perform time walk correction

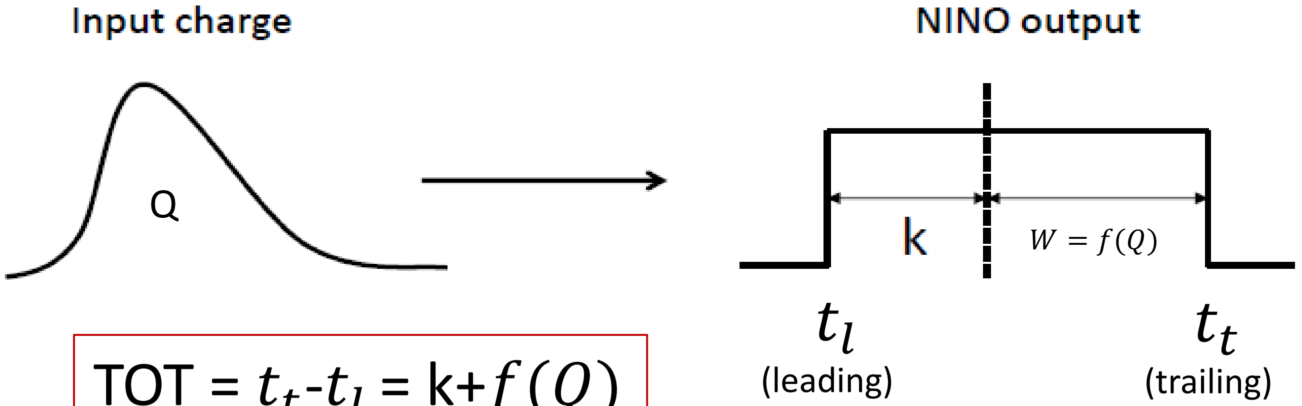
  - Time over Threshold
  - Constant Fraction Discriminator (CFD)
  - Signal charge measurement
  - Signal sampling

Rise time ~ 1-1.5 ns
SNR ~ 50-100
Amplitude ~ 300-700 mV

To cope with the high particle rate (~1MHz/channel) in the PPS application, a readout with a fast discriminator (NINO) and TDC (HPTDC) was chosen for the PPS timing system readout

Run 2 layout



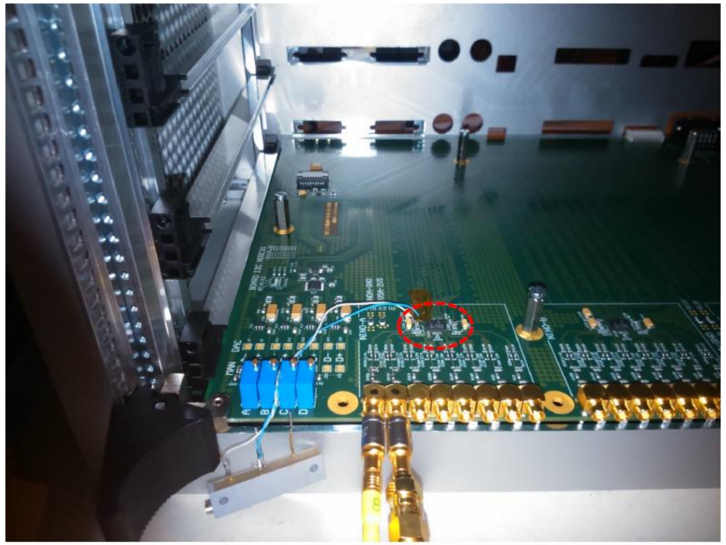


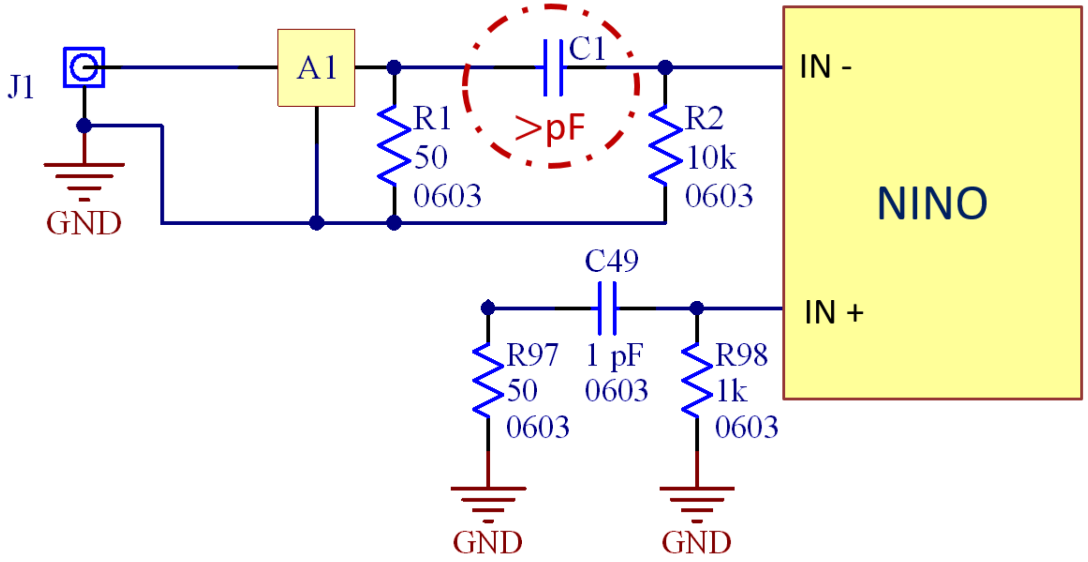
TOT = t_t-t_l = k+$f(Q)$

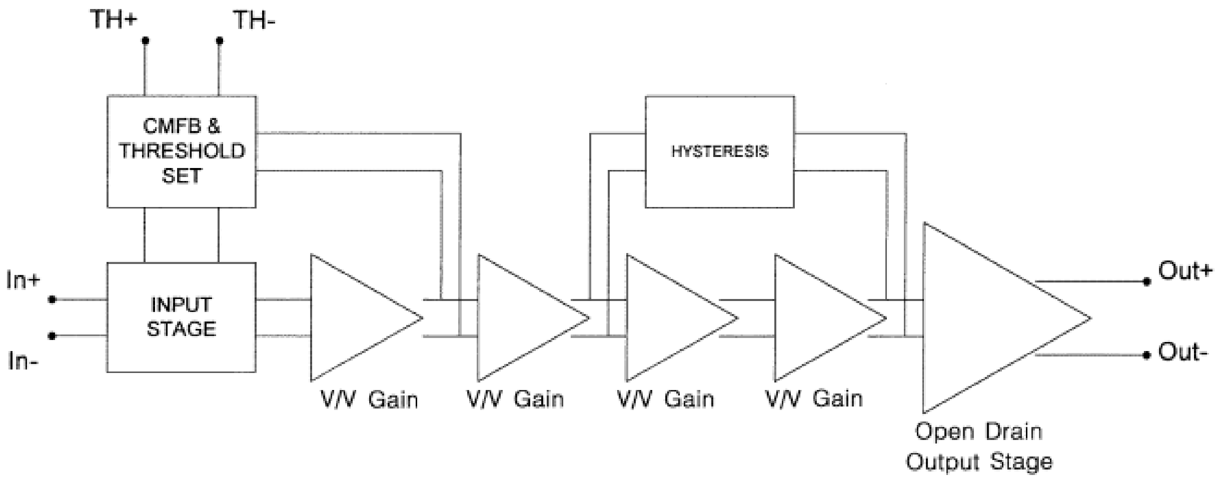
In Run 2 discrimination stage degraded timing performance by 30% (after time walk correction). Contribution of HPTDC (resolution <10ps) negligible.

Optimization ongoing for Run 3

NINO Discriminator

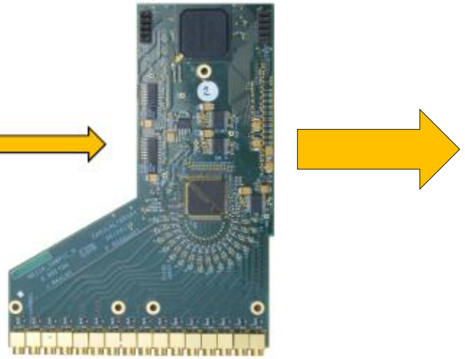


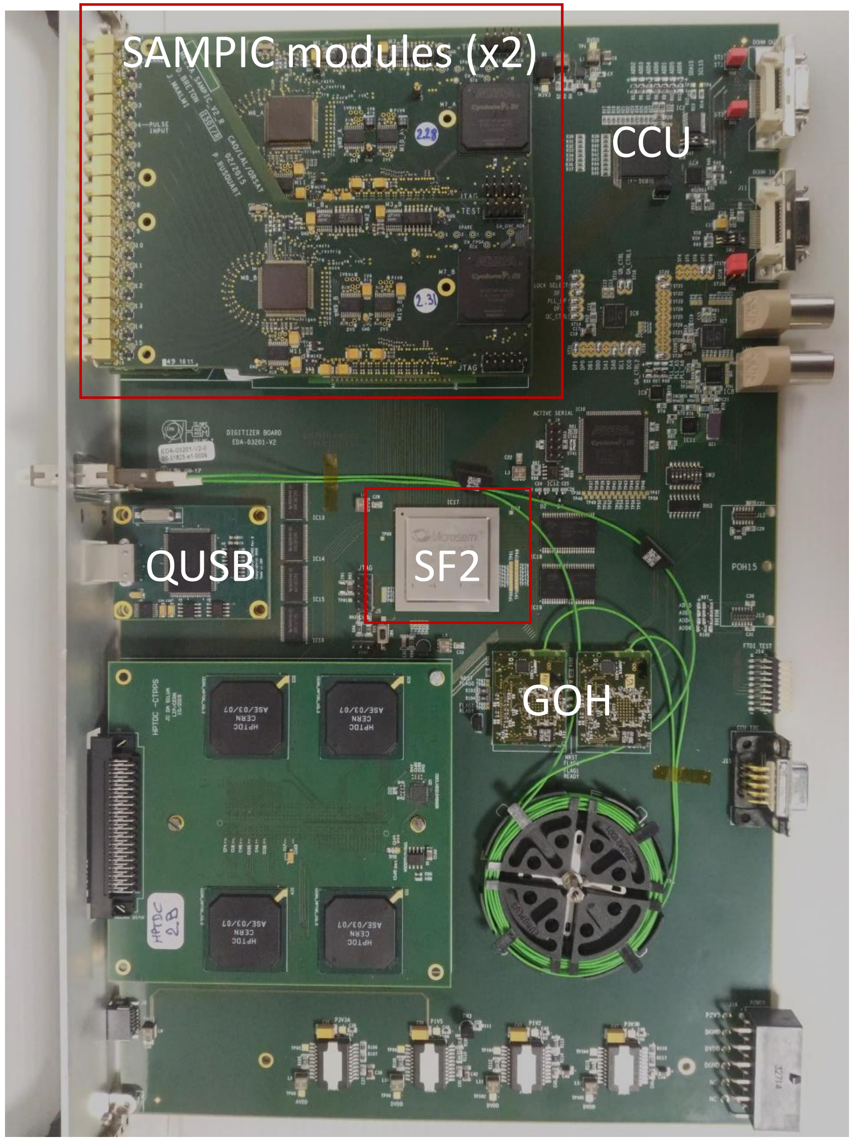




- Characteristic integration time ~500ps
- Test with pulser showed a resolution ~25 ps in SE configuration.
- Performance depends on input signal SNR
- Decoupling capacitor C1 can be used to tune the input charge
- Keep C1 above 1 pF, compensate with input attenuator
- Keep individual threshold values above 1.2V!

Readout with a sampler





SAMPIC chip:

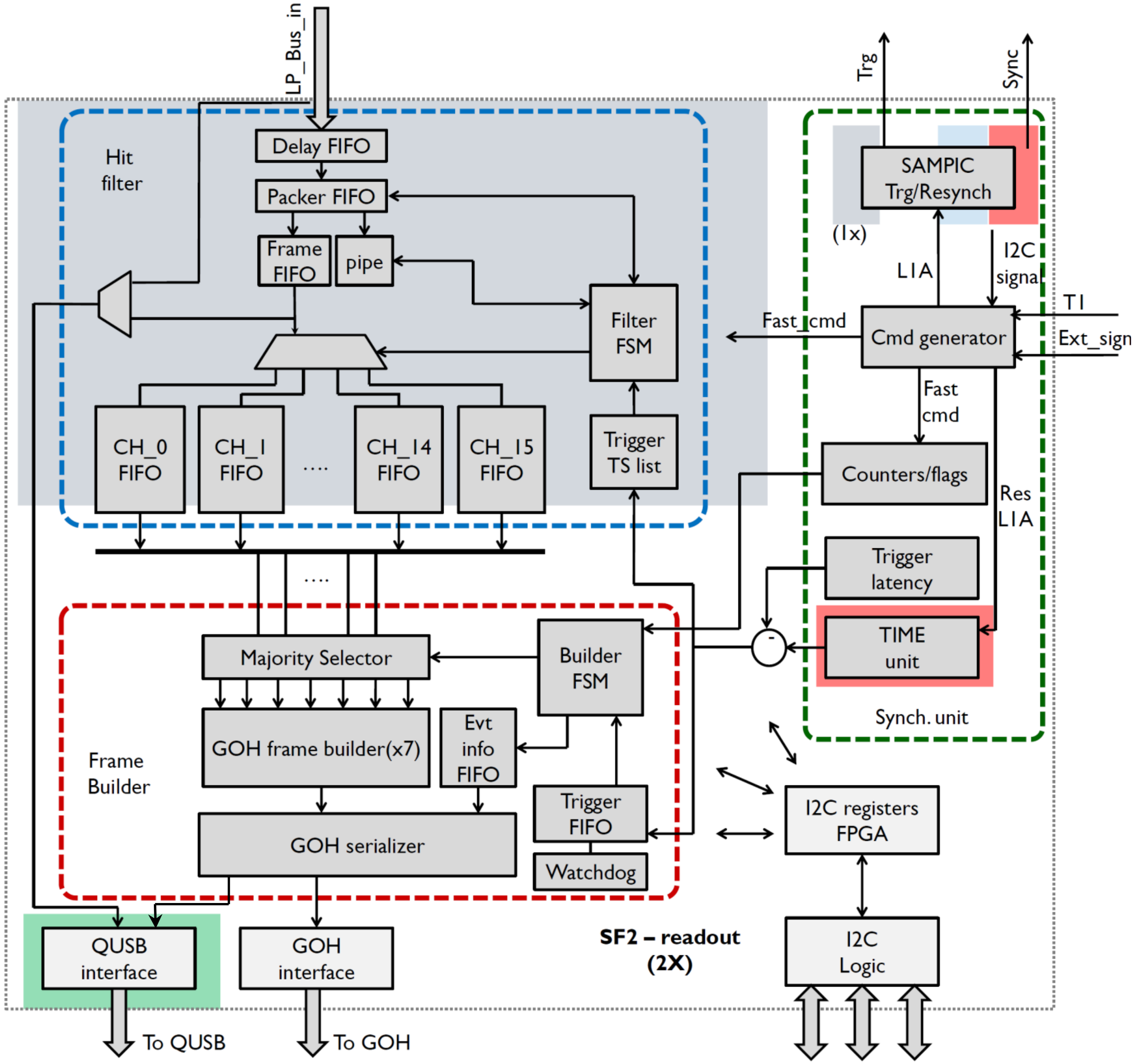
- 16 channel/chip
- Up to 64 sample/hit @ 10 GSa/s
- 1.5 GHz bandwidth
- 8-11 bit resolution
- 0.25-1.6 µs channel dead time

SAMPIC used as readout system for the TOTEM timing (UFSD) during the special TOTEM-CMS joint data taking in 2018.
Special optics -> Lower rate

To be used in TOTEM/CMS needs additional capability:

- Event buffering
- Event building
- Synchronization with central DAQ
- Zero suppression and data compression

Readout firmware



Trigger latency ~ 6 us
1 Frame for each trigger
No frame if no trigger
Max frame size ~ 350 B
Trigger rate up to 100kHz

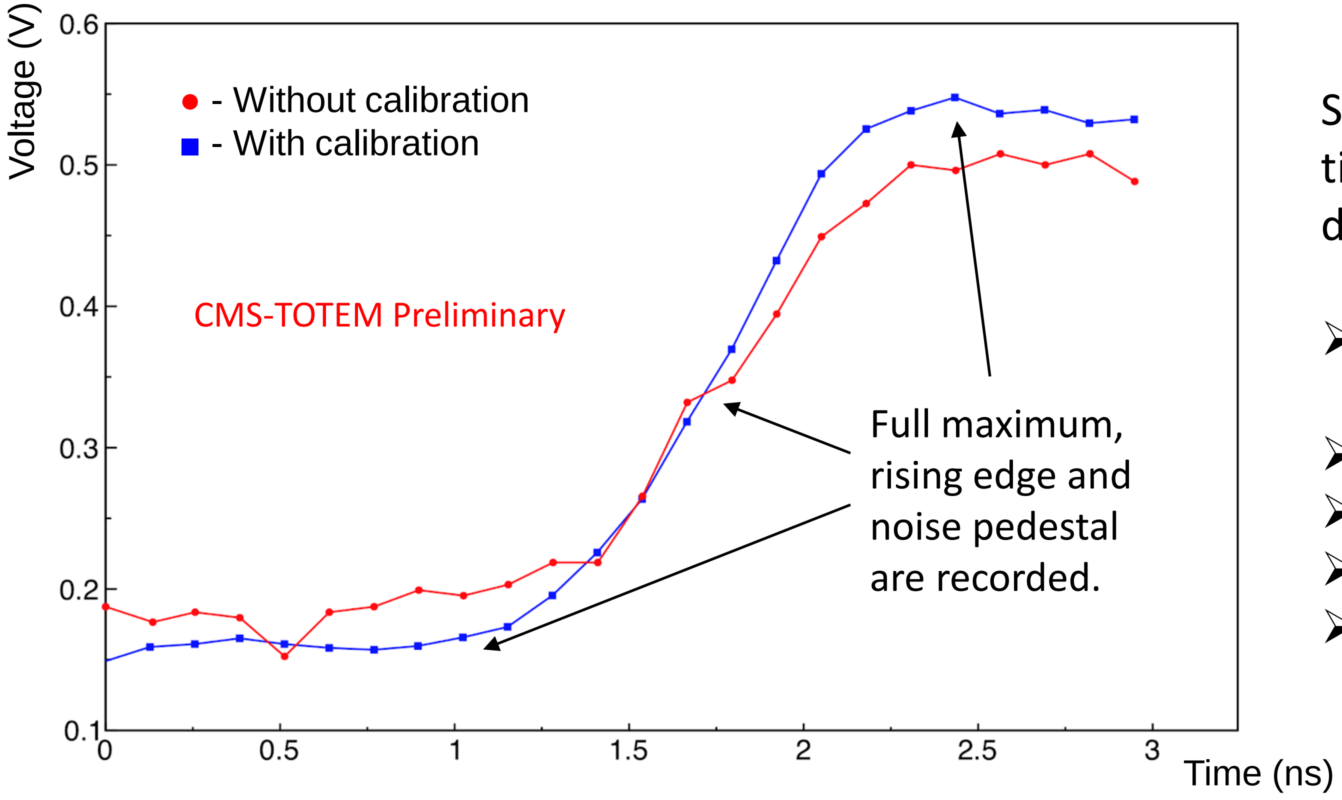
Hit selection, frame building and data reduction to be done inside Digitizer central FPGA (Microsemi SF2)

- Delay & synchronization of incoming waveforms
- Control of data frame integrity (header, trailer, WC)
- Waveform timestamp reconstruction and trigger matching logic (programmable tolerance)
- Large volume of data handled : event is built after ~100 us from trigger arrival to collect all SAMPIC waveforms
- Assembly of global event info
- Dynamic allocation of payload
- Selection of up to 7 matching channels
- Zero suppression
- USB readout & control available

Sampic experience in real data taking

SAMPIC operated at 7.8 Gsa/s, with 8 bit voltage resolution.
24 samples collected for each waveform (recording window of ~3.1 ns)

Example of waveform

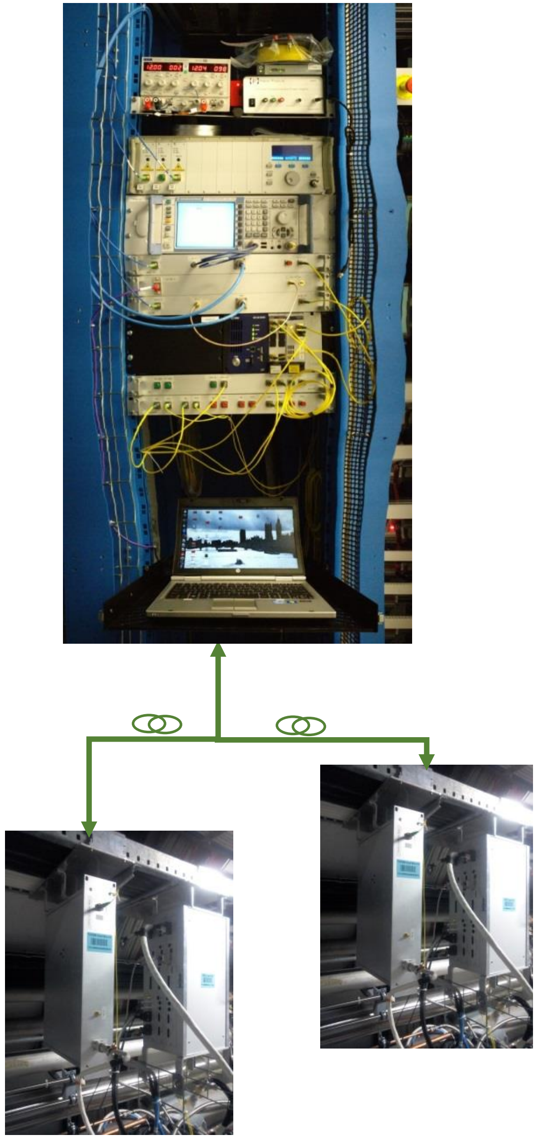


SAMPIC used as readout system for the TOTEM timing (UFSD) during the special TOTEM-CMS joint data taking in 2018:

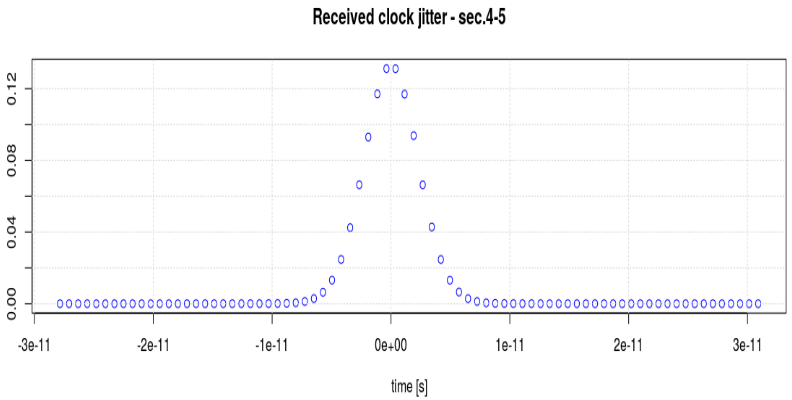
- Special run successfully performed during 6 days of continuous data taking (2-7 July)
- Very good quality of the collected waveform
- Operations with CMS DAQ fully stable
- Efficiency of the readout above 99%
- No sizable timing degradation introduced

PoS TWEPP2018 (2019) 137

Clock system



- LHC clock is derived from CMS TCDS (Timing Control Distribution System)
- System delay changes over optical path is constantly monitored -> 1 measurement every 10min.
- Data stored to files in csv format. File rotation system -> 1 file per day.
- Clock jitter measured at RP receiver <**2ps**



Clock source based on Silicon Lab 5344 chip:

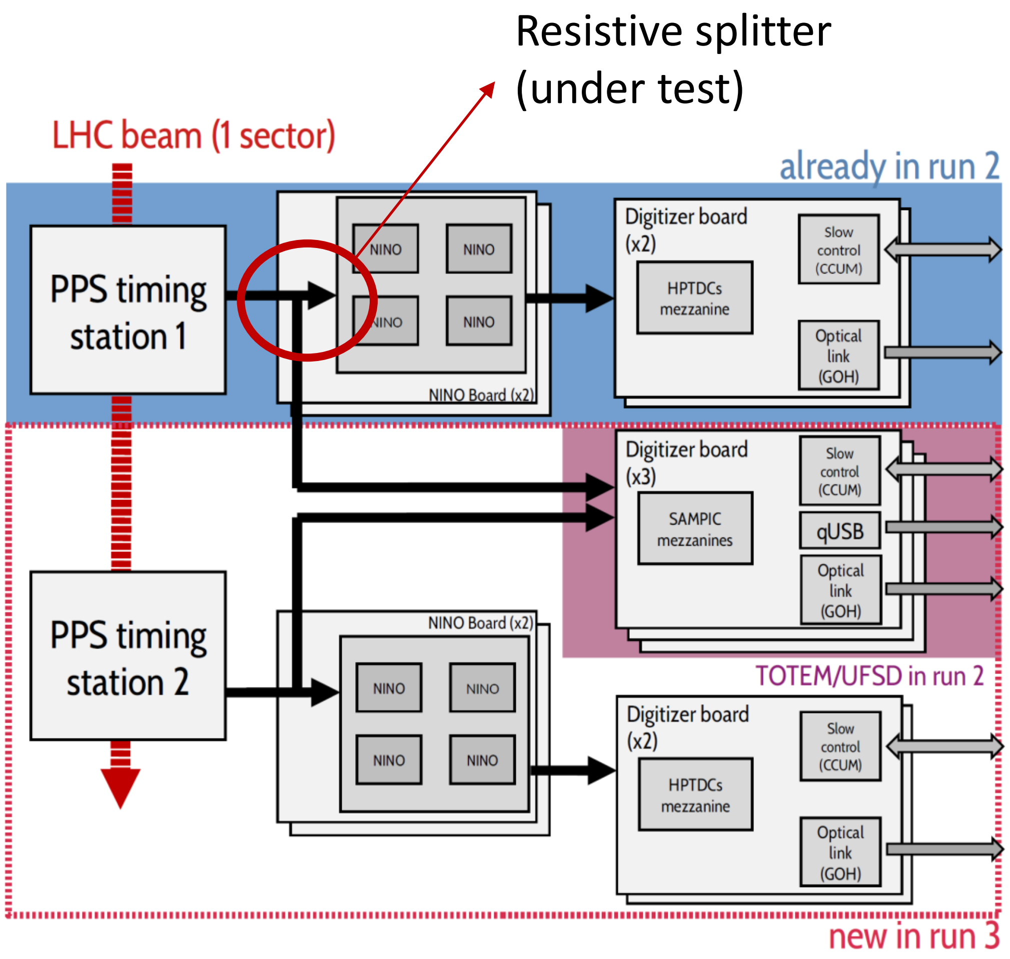
- Zero delay mode → constant phase delay between input and output
- Clock phase will be tuneable in ~18ps steps.

In 2017 PPS used also a clock distribution based on an RF connection.

Main run 3 upgrades (sensors & readout electronics)

Important upgrade program ongoing for the timing system:

- An additional timing station will be built and installed in each sector. Each station will be equipped with 4 DD planes (2SD +2DD in 2018) → 8 DD planes in each sector + 70 ps/plane (including digitization) → 25 ps/arm.
- New hybrid boards -> increase in amplification stability and HV isolation, further optimization of performance
- New NINO board -> reduce timing degradation in digitization phase and add secondary readout
- Sensor readout with SAMPIC chip (fast sampler @ 7.8 Gsa/s) will be available for commissioning phase and sensor monitoring (cannot sustain hit rate at nominal luminosity)



Conclusions

- The CMS PPS group has developed a timing system based on scCVD diamonds.
- Integration of the crystals and signal amplification is provided through a dedicated hybrid board, hosting 12 3-stage amplification channels.
- Test Beam data show that the sensor arranged in DD architecture can reach a precision of 50 ps.
- A similar hybrid has been used to amplify the signal of UFSD detector (best resolution achieved ~30 ps)

- The timing system was successfully operated in Run2 and provided timing information useful for pile-up suppression
- The PPS readout is based on the chain NINO+HPTDC, able to sustain the particle rate
- A readout with SAMPIC, successfully used in the special CMS-TOTEM data taking, will be added in Run 3 as a parallel readout system for sensor monitoring and calibration. Other upgrades are ongoing.

- A special clock distribution system has been developed to grant appropriate synchronization among detectors separated by ~400m.