

# Front-end and DAQ chain for cluster counting/timing of drift chamber signals

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# OUTLINE



- **dE/dx and Particle Identification (PID)**
- **Cluster counting/timing in drift chambers: what it is**
  - **cluster counting**: first approach and PID exp. results
  - **cluster timing**: second approach and cluster timing
    - spatial resolution improvement
    - background hit filtering
    - event time stamping
    - longitudinal coordinate improvement
- **Requirements for cluster counting/timing**
  - **front-end electronics**
  - **digitization and acquisition**

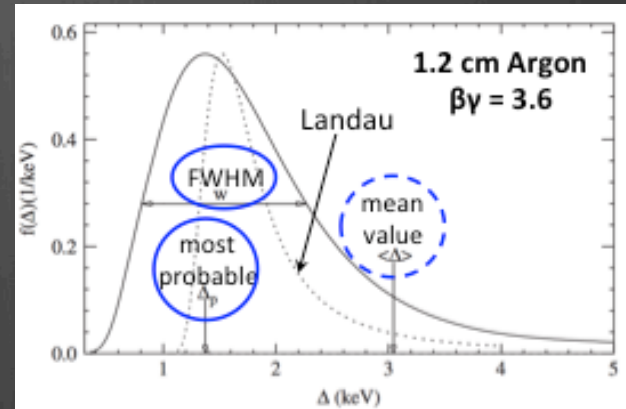
# PId with dE/dx: the task

straggling function



By definition, **the integral of a drift chamber charge signal** (described by the **straggling function**) is related to the **total number of electrons** liberated in the ionization process which, in turn, is a function of the **energy lost** by the charged particle crossing the **x** layer of material (**- dE/dx**).

By knowing the dependence of dE/dx on the velocity **β** of the crossing particle, given **p**, one can identify the **particle mass**.



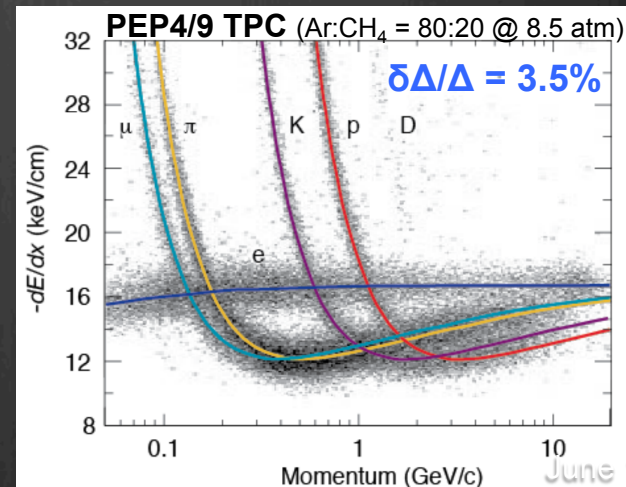
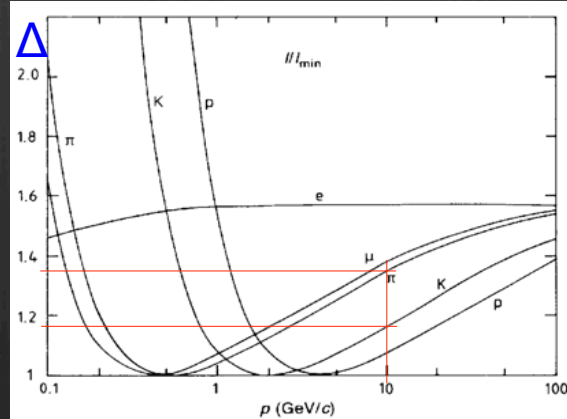
parameters describing the straggling function:  
most probable energy loss  $\Delta_p(x, \beta\gamma)$  and FWHM  $W(x, \beta\gamma)$

In the **relativistic rise** region:  
 $[\Delta(\pi) - \Delta(K)] / \Delta(\pi) \approx 10-15\%$

$\pi/K$  separation requires **resolutions**  
 $\delta\Delta/\Delta < \text{a few } \%$

Also, the **theory model description of the energy loss mechanism** needs to be accurate at  **$\approx 1\%$  level**

Cluster electronics



June 15, 2021

# Cluster counting

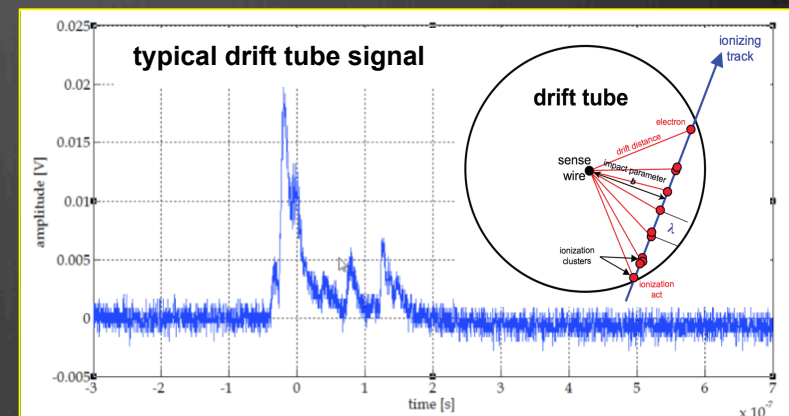
**Cluster counting** consists in identifying, in every recorded detector signal, **the isolated structures related to the arrival at the anode wire of the electrons belonging to each ionization act.**

In order to achieve this goal, special experimental conditions must be met: **pulses from electrons belonging to different clusters must have a little chance of overlapping in time** and, at the same time, **the time delay between pulses generated by electrons coming from the same cluster must be small enough to prevent over-counting.**

The fulfillment of both these requirements involves **incompatible time resolutions: the optimal counting condition can be reached only as a result of the equilibrium** between the fluctuations of those processes which forbid a **full cluster detection efficiency** and of the ones enhancing the **time separation among different ionization events.**

Cluster electronics

4



## Cluster counting/timing recipe for He based gas mixtures

- High front end bandwidth ( $\approx 1$  GHz)
- S/N ratio: as large as possible
- High sampling rate (2 GSa/s)
- $\geq 12$  bit

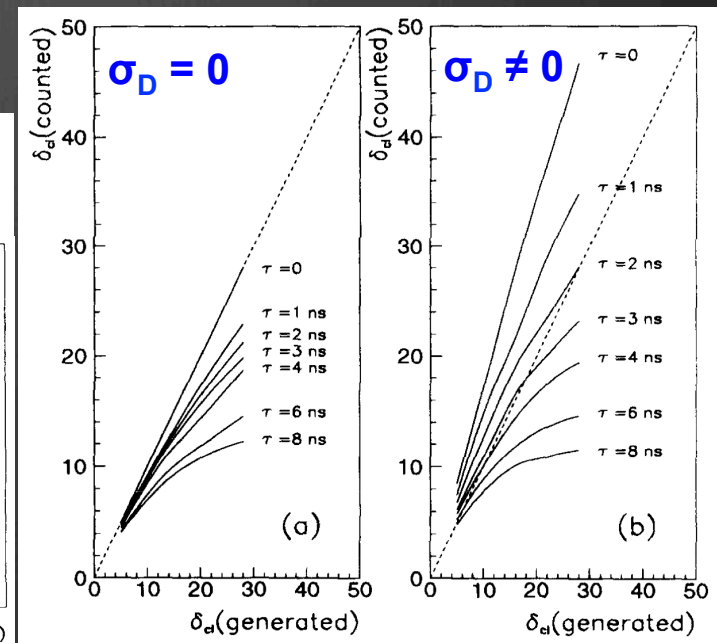
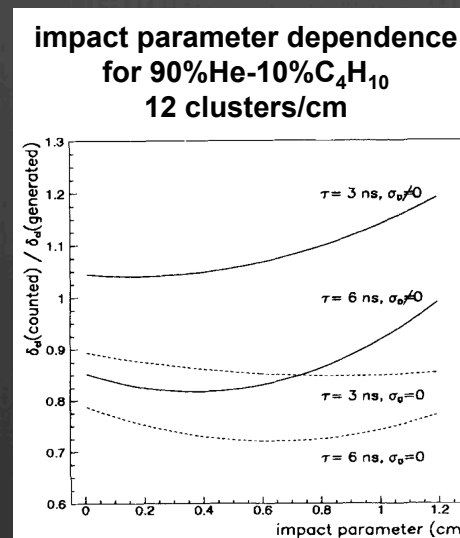
June 15, 2021



# Cluster counting: first approach



- The relevant parameters for a cluster counting measurement are **the resolving time  $\tau$**  and **the single electron diffusion  $\sigma_D$** .
- The ideal conditions, which guarantee a real Poisson distribution of the cluster counting, are met with a resolving time  $\tau = 0$ , in absence of diffusion,  $\sigma_D = 0$ .
- For the **90%He-10% $C_4H_{10}$**  gas mixture and a **2.5 cm drift cell**, the real optimal conditions are met with  **$\tau = 4$  ns**
- It should be stressed that the obtained result is strictly related to the **detector geometry** as it depends on the impact parameter and on the dimension of the drift cell for the given gas.
- **Corrections due to the track angle, impact parameter, saturation effects, attachment (for long drift) are necessary**

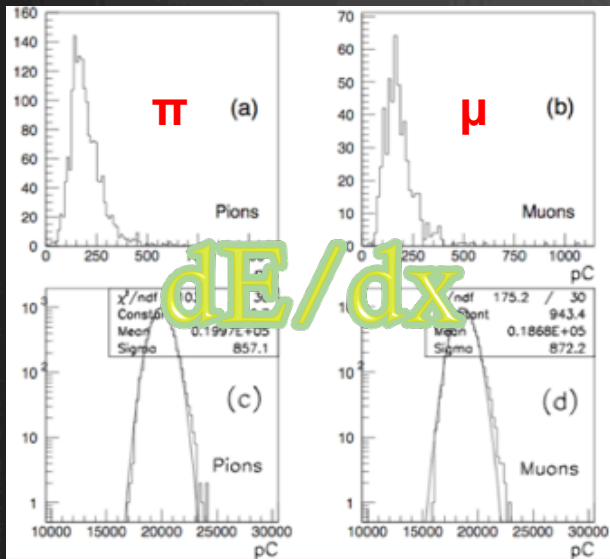


G. Cataldi, F. Grancagnolo, S. Spagnolo *Cluster counting in helium based gas mixtures* NIM A386 (1997) 458

# Cluster counting: PId exp. results



$\mu/\pi$  separation at 200 MeV/c in He/iC<sub>4</sub>H<sub>10</sub> – 95/5 100 samples 3.7 cm  
 gas gain  $2 \times 10^5$ , 1.7 GHz – gain 10 amplifier, 2GSa/s – 1.1 GHz – 8 bit digitizer



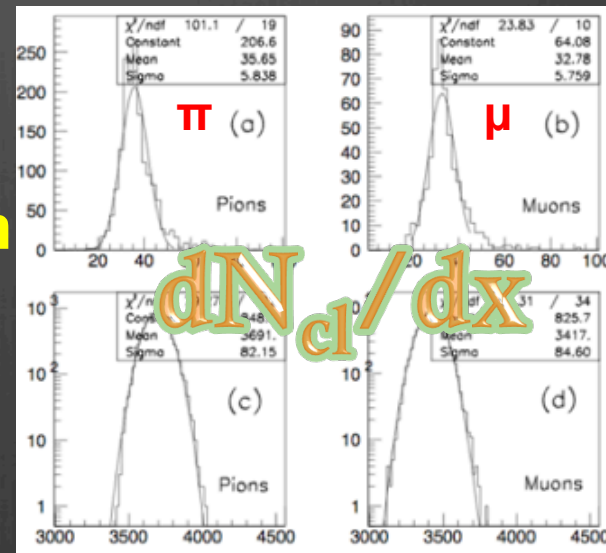
single sample  
(20% truncated mean)

test beam  
data

sum over  
100 samples

integrated charge  
 expected 2.0  $\sigma$  separation  
 measured 1.4  $\sigma$  separation

Cluster electronics



single sample

$\pi: \sigma/\sqrt{N_{cl}}=0.978$   
 $\mu: \sigma/\sqrt{N_{cl}}=1.006$

sum over  
100 samples

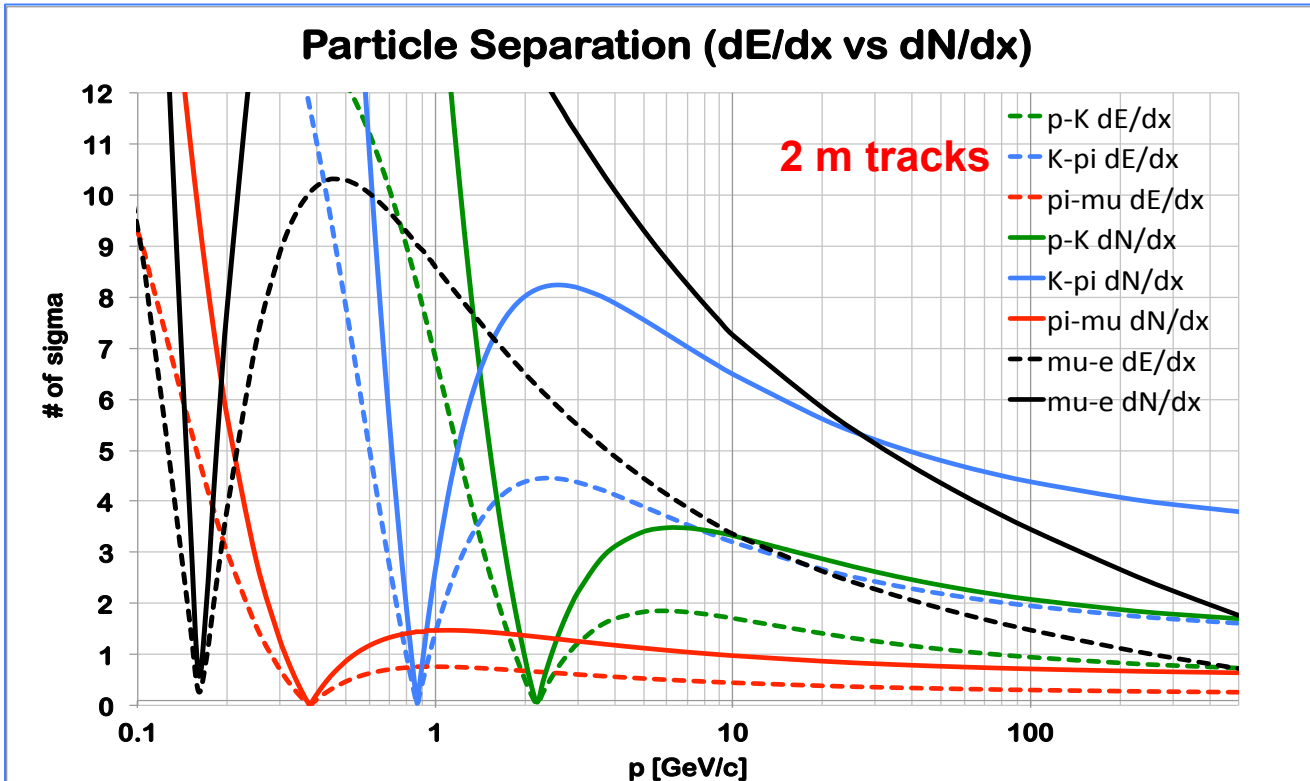
$\pi: \sigma/\sqrt{N_{cl}}=1.35$   
 $\mu: \sigma/\sqrt{N_{cl}}=1.45$

cluster counting  
 expected 5.0  $\sigma$  separation  
 measured 3.2  $\sigma$  separation

# dE/dx and dN<sub>cl</sub>/dx



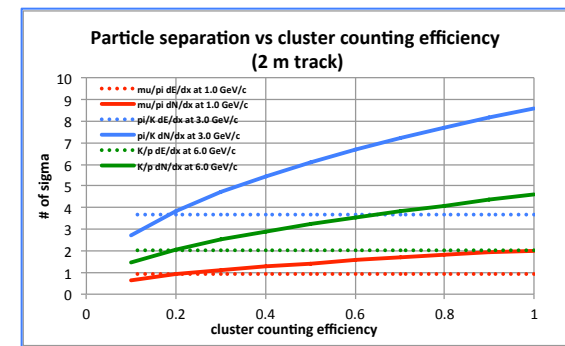
Expected from analytical calculation for the IDEA Drift Chamber at FCC-ee



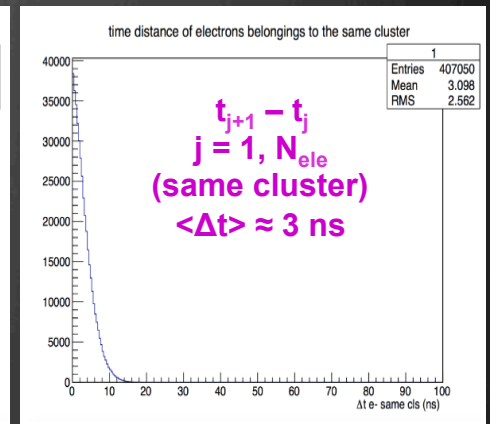
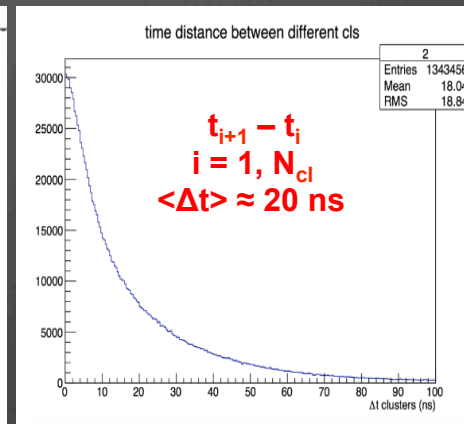
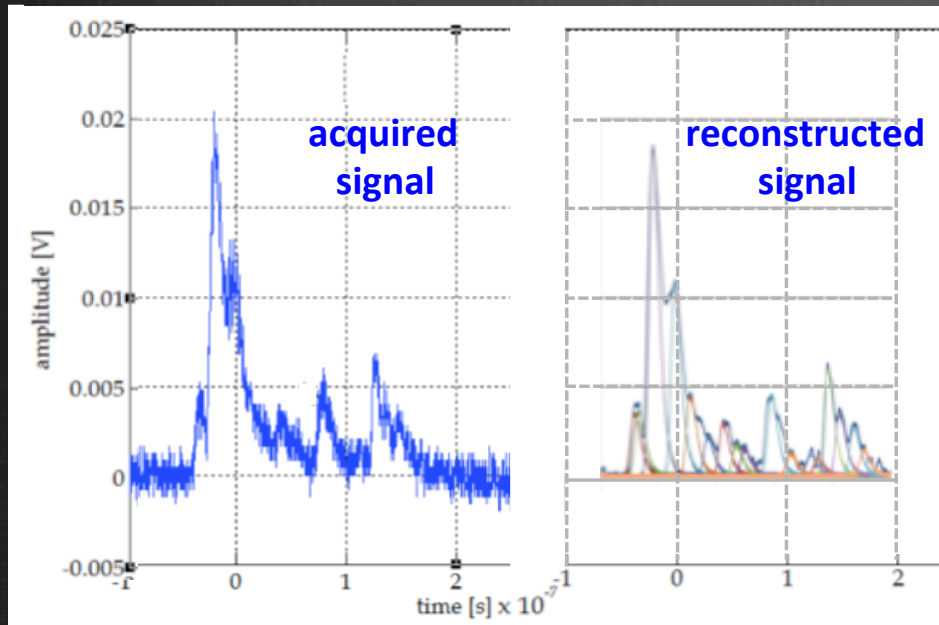
He/iC4H10 90/10  
 $\bar{\delta}_{cl} = 12 \text{ cm}^{-1} \text{ (mip)}$

$\sigma(dE/dx)/(dE/dx) = 4.3\%$

**80% cluster counting efficiency**

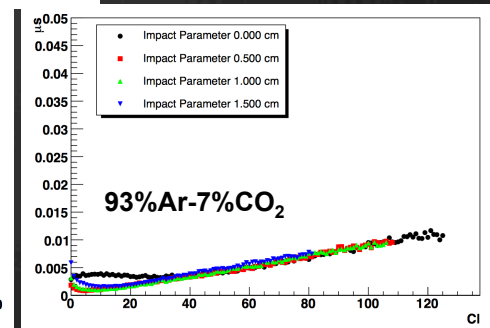
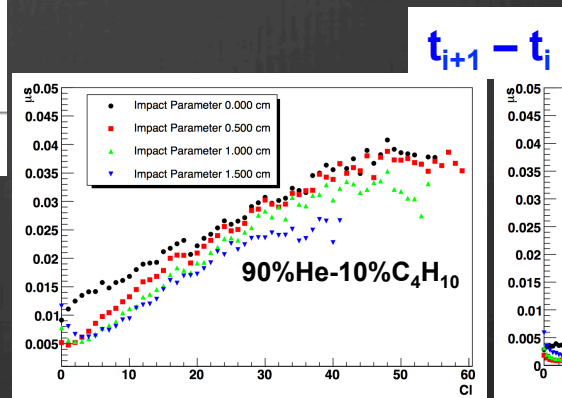


# Cluster counting: second approach



From the **ordered sequence of the electrons arrival times**, considering the average time separation between clusters and their time spread due to diffusion, one can reconstruct **the most probable sequence of cluster drift times**  $\{t_i^{cl}\}$ ,  $i = 1, N_{cl}$  and  $N_{cl}$ :

Cluster electronics

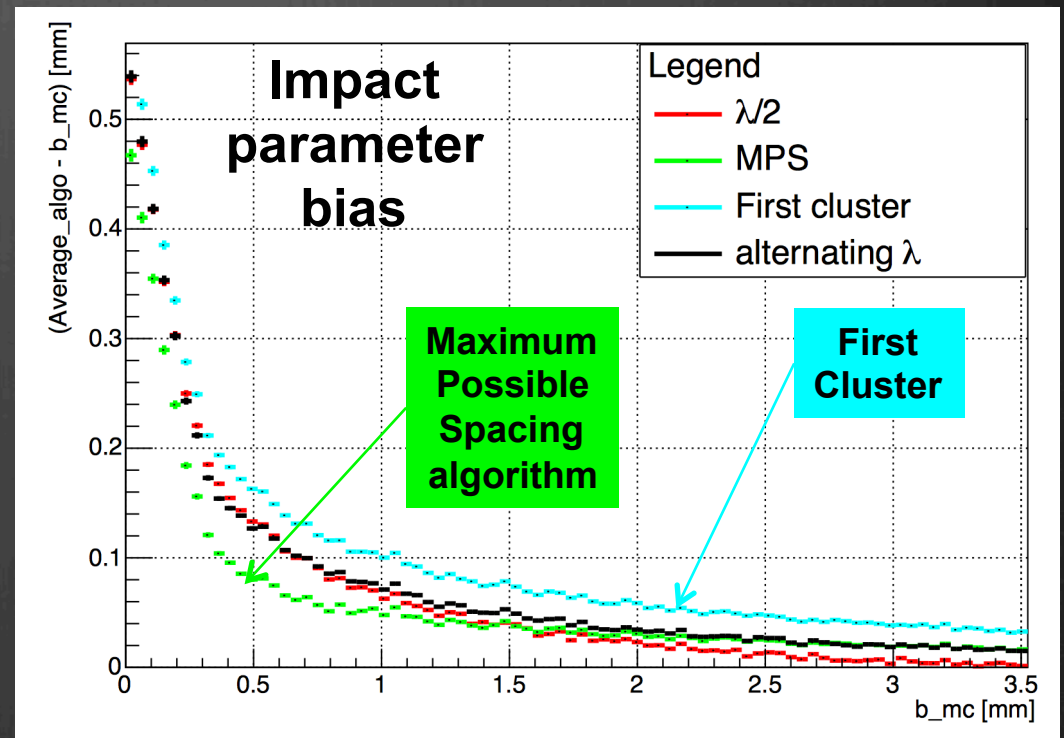


# Cluster timing: spatial resolution



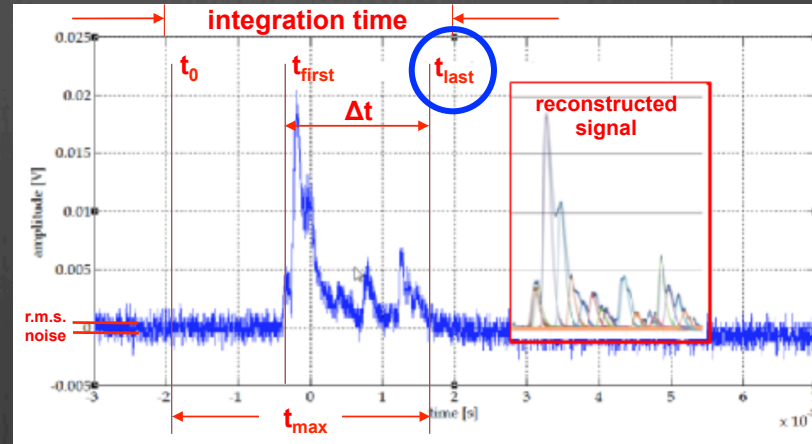
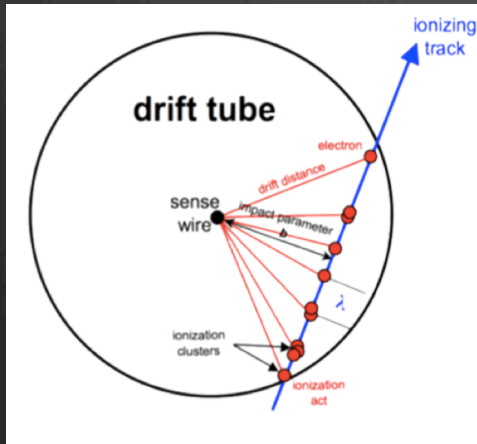
$$\{t_i^{cl}\}, i = 1, N_{cl}$$

For any given **first cluster (FC)** drift time  $t_1$ , the **cluster timing technique** exploits the drift time distribution of all successive clusters to statistically determine, hit by hit, the most probable **impact parameter**, thus reducing the **bias** and improving the average **spatial resolution** with respect to that obtained from with the FC method alone.





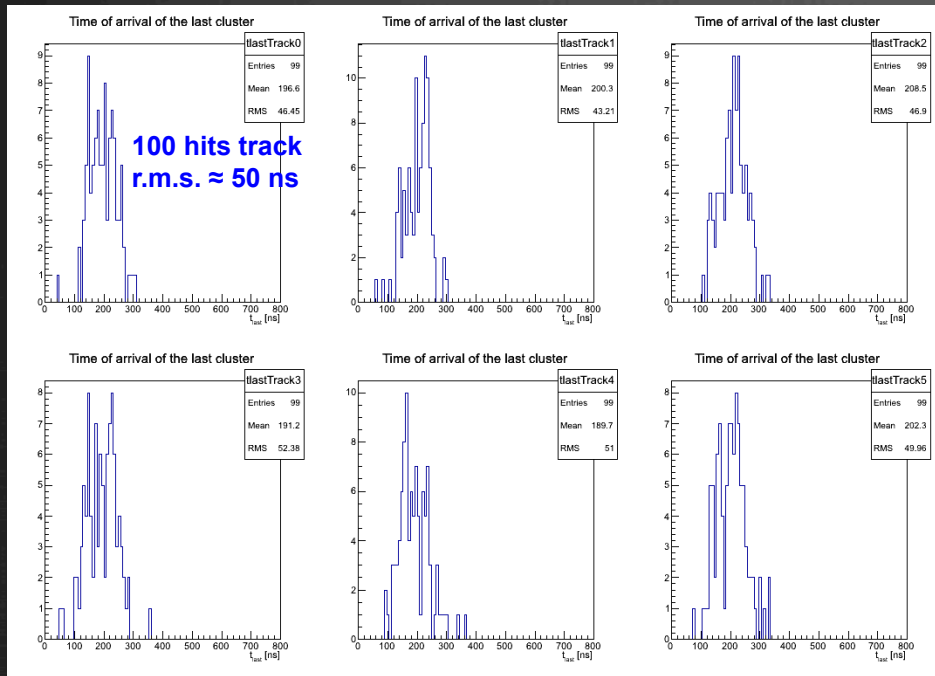
# Cluster timing: bkgnd hit filtering



Digitized signal  
(1 GHz, 2 GSa/s)

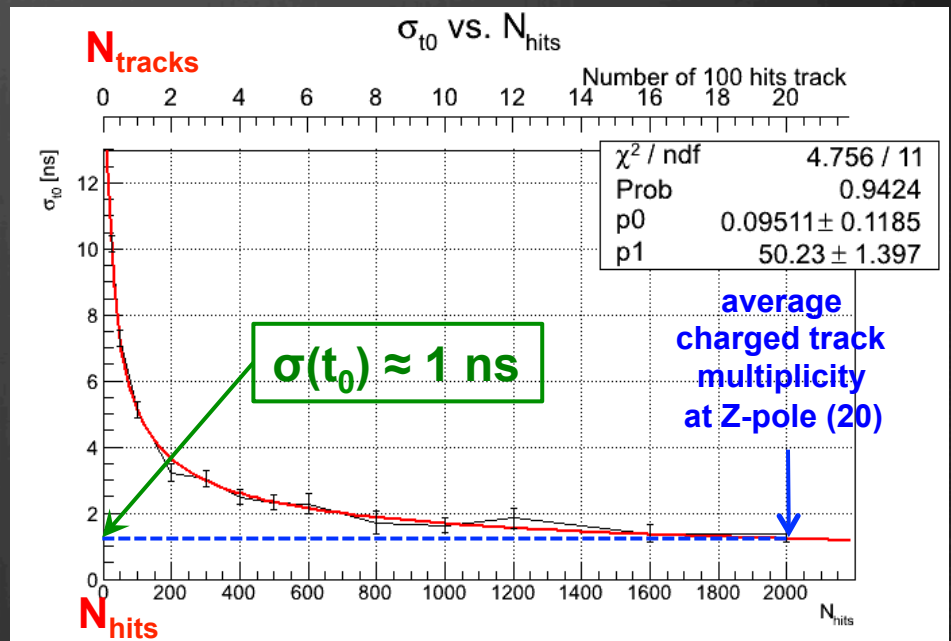
- $t_{i+1} - t_i \approx \text{a few ns}$  at small  $t_i$ ,  $t_{i+1} - t_i \approx \text{a few} \times 10 \text{ ns}$  at large  $t_i$
- $t_{\text{max}}$  **constant** in ideal case (slightly depending on track angle in drift cell case)
- $\Delta t \leq t_{\text{max}}$ , length of digitized signal, depends on impact parameter **b** ( $t_{\text{first}}$ )
- $N_{\text{cl}}$  depends only on  $\Delta t$  (or **b**, or  $t_{\text{first}}$ ) and on the track angle
- $t_{\text{last}}$  **constant** in the ideal case  $\Rightarrow$  defines the **trigger time**  $t_0 = t_{\text{last}} - t_{\text{max}}$

# Cluster timing: time stamping



100 hits track  
r.m.s.  $\approx$  50 ns

$\sigma(t_0)$  as a function of  $N_{\text{tracks}}$   
( $t_0 = t_{\text{last}} - t_{\text{max}}$ )

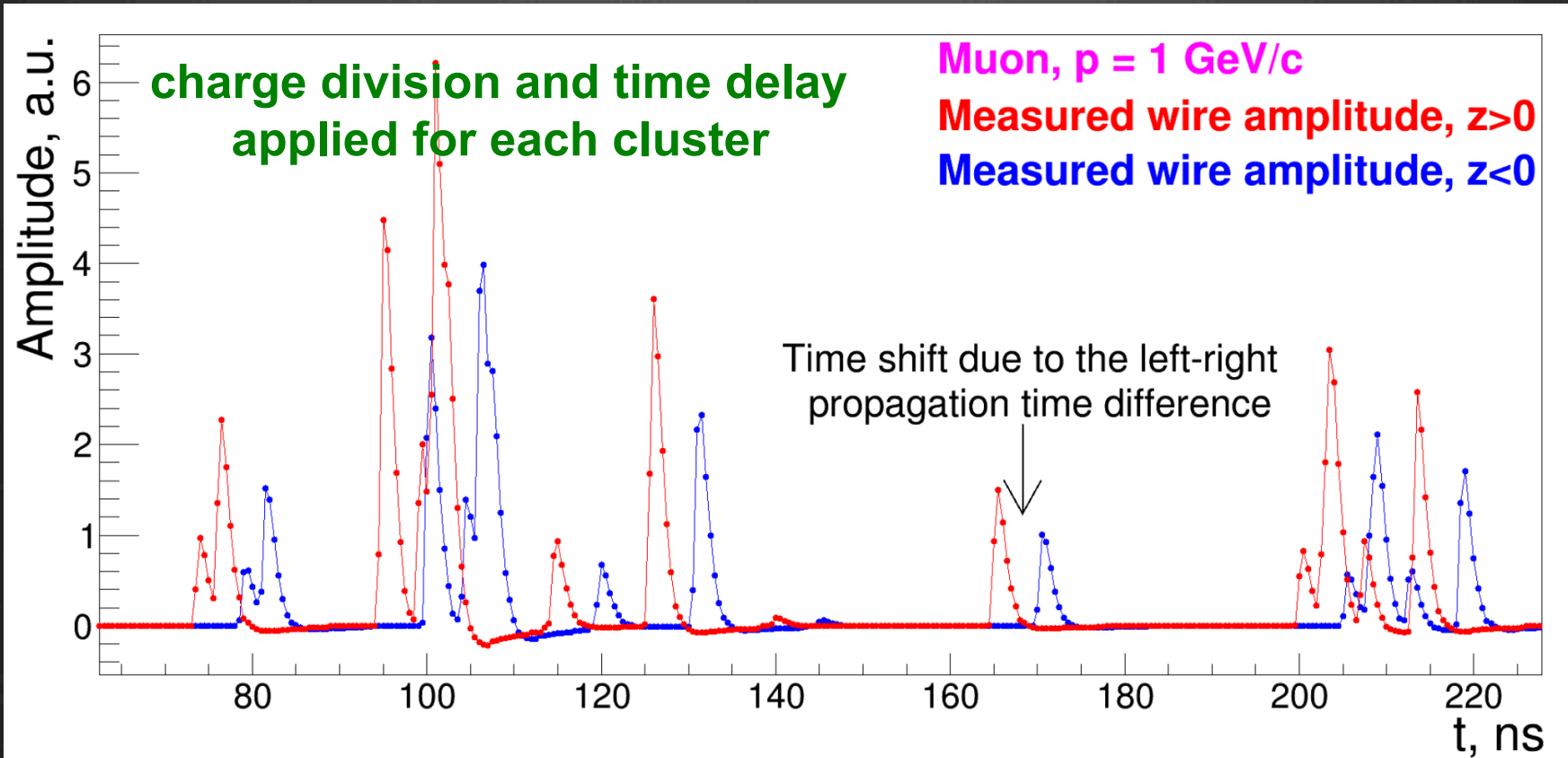


$t_{\text{last}}$  for a single 100 hits track

$\sigma(t_{\text{last}}) \approx 5 \text{ ns (r.m.s./}\sqrt{100})$

Cluster electronics

# Cluster timing: longitudinal coord.



# Cluster counting/timing requirements



## □ Helium-based vs Argon-based gas mixtures

	He/iC <sub>4</sub> H <sub>10</sub> = 90/10	Ar/iC <sub>4</sub> H <sub>10</sub> = 90/10	
primary and total ionization	12, 27 cm <sup>-1</sup>	30, 105 cm <sup>-1</sup>	} average cluster separation in time domain: He: tens of ns Ar: a few ns
average drift velocity	2 cm/μs	5 cm/μs	
longitudinal diffusion (0.5 cm)	110 μm (5 ns)	110 μm (2 ns)	multi-electron clusters
transverse diffusion (0.5 cm)	170 μm	260 μm	
ion mobility	5.1 cm <sup>2</sup> /s/V	1.37 cm <sup>2</sup> /s/V	affects signal formation
Townsend coeff. (10kV/cm)	35 cm <sup>-1</sup> (1/285 μm)	8 cm <sup>-1</sup> (1/1.25 mm)	higher gain
attachment coeff. (10kV/cm)	2.5 cm <sup>-1</sup> (4 mm)	3.5 cm <sup>-1</sup> (2.9 mm)	much lower attachment
density	0.42×10 <sup>-3</sup> g/cm <sup>3</sup>	1.86×10 <sup>-3</sup> g/cm <sup>3</sup>	
radiation length	1313 m	114 m	×4 smaller mult. scatt.

# Cluster counting/timing requirements



The DC drift cell should be considered as a transmission line with distributed parameters.

$C = 9 \text{ pF/m}$ ,  $L = 1.24 \text{ }\mu\text{H/m}$ ,  
 $Z_0 = 370 \text{ }\Omega$ ,  $R(20\text{ }\mu\text{m W(Au)}) = 1\text{K}\Omega/\text{m}$

This line must be matched so that there are no reflected pulses on the signal pickup side.

Signal shape (for single electron)

$$I(t) = \frac{Q_0}{2 \ln(R_0/r_0)} \frac{1}{t + t_0} \quad \text{for } 0 \leq t \leq t_{\max}$$

$$t_0 = \frac{r_0^2 \ln(R_0/r_0)}{2 \mu U_0}$$

$$\begin{cases} t_{\max}(\text{He}) = 170 \text{ }\mu\text{s} \\ t_{\max}(\text{Ar}) = 625 \text{ }\mu\text{s} \end{cases}$$

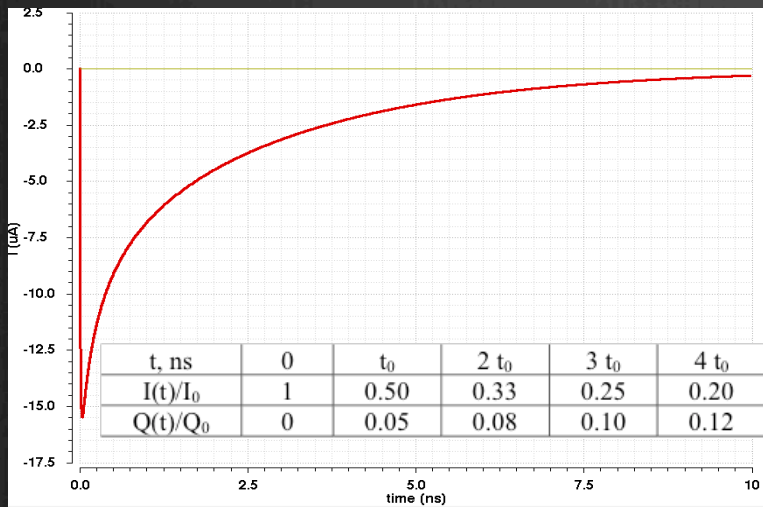
$$\begin{cases} t_0(\text{He}) = 0.5 \text{ ns} \\ t_0(\text{Ar}) = 2.0 \text{ ns} \end{cases}$$

$R_0 = 0.5 \text{ cm}$ ,  $r_0 = 10 \text{ }\mu\text{m}$ ,  $U_0 = 1500 \text{ V}$   
 and gas gain =  $5 \times 10^5$

$Q_0 = 8 \times 10^{-14} \text{ Coul}$

$I_0(\text{He}) = 16 \text{ }\mu\text{A}$  -  $I_0(\text{Ar}) = 4 \text{ }\mu\text{A}$

after  $t = 2t_0$  (= **1 ns for He**, **4 ns for Ar**)  
 only  $0.08 \times Q_0$  (= **6.5 fCoul**)  
 has flown to the external circuit  
 ( $6.5 \text{ fCoul} / 9 \text{ pF} = 7 \text{ mV per single } e^-$ )





# Data Transfer issues



## FCCee Physics running conditions

- **91 GeV** c.m. energy
- **200 KHz** trigger rate
  - **100 KHz** Z decays
  - **30 KHz**  $\gamma\gamma \rightarrow$  hadrons
  - **50 KHz** Bhabha (out)
  - **20 KHz** beam backgrounds

## DCH operating conditions

- drift cells: **56,000** , layers: **112**
- max drift time ( $\approx 1$  cm): **400 ns**
- cluster density: **20/cm**

## Cluster counting/timing conditions

- gas gain:  **$5 \times 10^5$**
- single  $e^-$  p.h.: **7 mV**
- r.m.s. electronics noise: **1 mV**
- $e^-$  threshold: **2 mV**; rise time  $< 1$  ns
- signal digitization: **12 bits at  $2 \times 10^9$  B/s**

## transferring all digitized data from DC

### Z decays

- $20 \text{ trks/ev} \times 130 \text{ hits/trk} \times 2 \text{ sides} \times 4 \times 10^{-7} \text{ s} \times 2 \times 10^9 \text{ B/s} \times 100 \text{ kHz} = \mathbf{400 \text{ GB/s}}$

### $\gamma\gamma \rightarrow$ hadrons

- $10 \text{ trks/ev} \times 130 \text{ hits/trk} \times 2 \text{ sides} \times 4 \times 10^{-7} \text{ s} \times 2 \times 10^9 \text{ B/s} \times 30 \text{ kHz} = \mathbf{60 \text{ GB/s}}$

### IPC background

- $1\% \text{ occupancy} \times 5.6 \times 10^4 \times 2 \times 4 \times 10^{-7} \text{ s} \times 2 \times 10^9 \text{ B/s} \times 100 \text{ kHz} \times 3 \text{ (SF)} = \mathbf{300 \text{ GB/s}}$

### Isolated peaks (noise above threshold)

- $2.5\% \times 5.6 \times 10^4 \times 2 \text{ sides} \times 4 \times 10^{-7} \text{ s} \times 2 \times 10^9 \text{ B/s} \times 100 \text{ kHz} = \mathbf{250 \text{ GB/s}}$

**$\geq 1 \text{ TB/s}$**

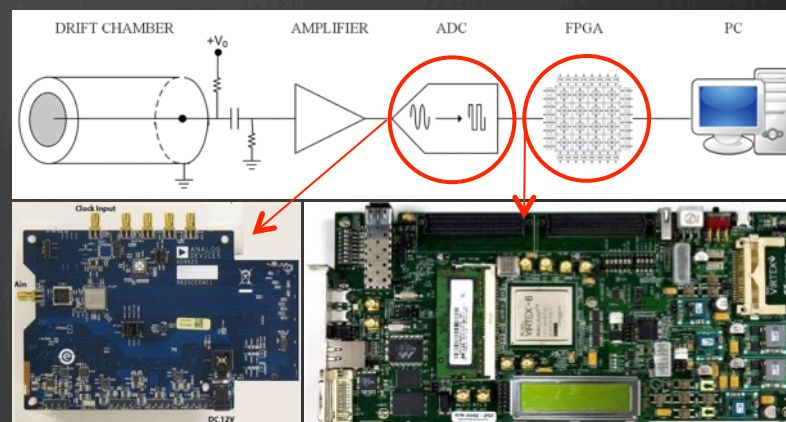
# The tested solution for a single channel



The solution consists in transferring, for each hit drift cell, **instead of the full spectrum of the signal**, only the minimal information relevant to the application of the cluster timing/counting techniques, i.e. **the amplitude and the arrival time of each peak associated with each individual ionisation electron**.

This is accomplished by using a **FPGA** for the real time analysis of the data generated by the drift chamber and successively digitized by an ADC.

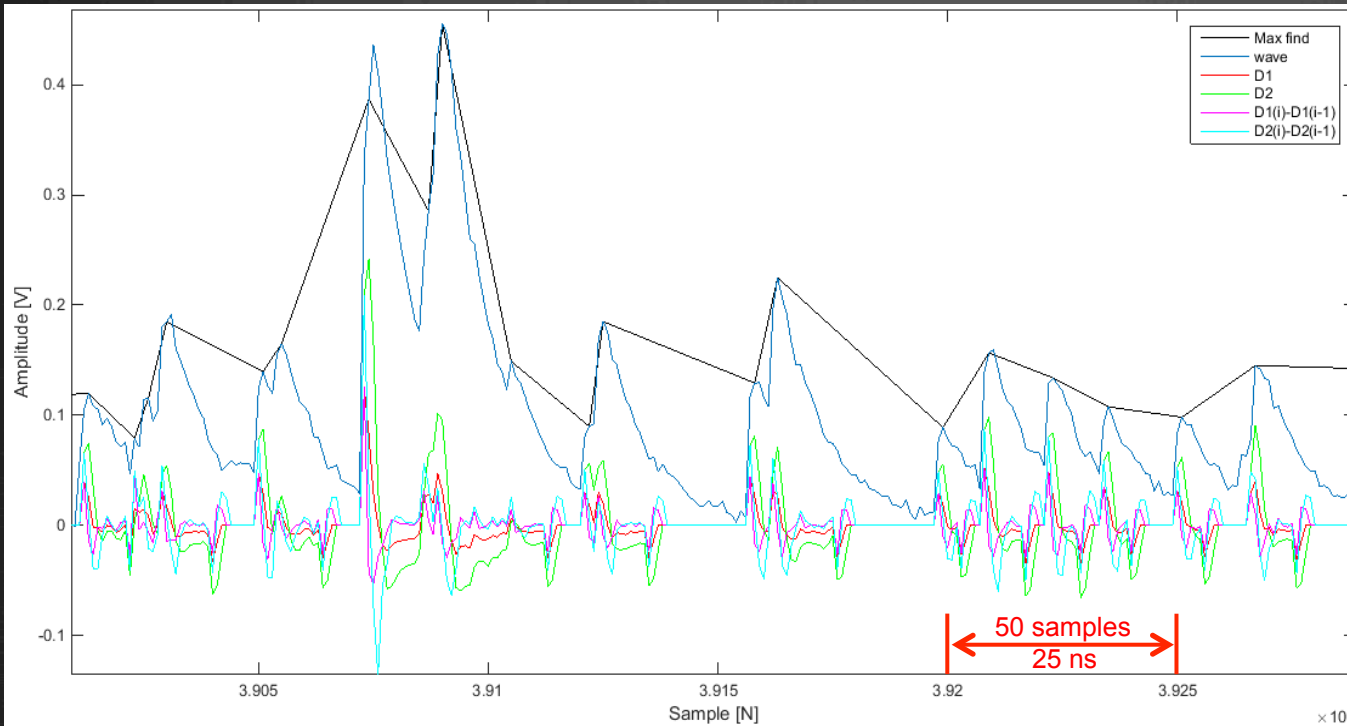
A fast readout algorithm (**CluTim**) for identifying, in the digitized drift chamber signals, the individual ionization peaks and recording their time and amplitude has been developed as **VHDL/Verilog** code implemented on a **Virtex 6 FPGA**, which allows for a maximum input/output clock switching frequency of **710 MHz**. The hardware setup includes also a 12-bit monolithic **pipeline sampling ADC** at conversion rates of up to **2.0 GSPS**.



AD9625-2.0EBZ  
Evaluation Board

Xilinx ML605  
Evaluation Board

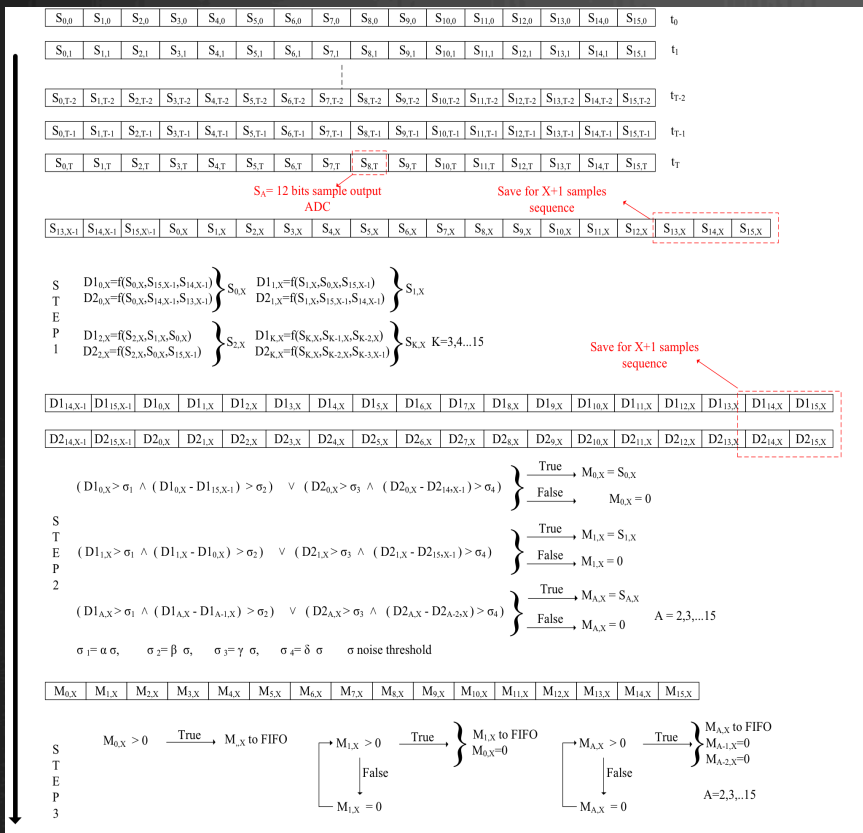
# The CluTim algorithm



At the beginning of the signal processing procedure, a counter starts to count, providing the timing information related to the signal under scrutiny. The determination of a peak is done by relating the  $i$ -th sampled bin to a number  $n$  of preceding bins, where  $n$  is related to the rise times of the signal peak. Once a peak is found, it is sent to pipeline memories which are continuously filled as new peaks are found. When a trigger signal occurs at time  $t_0$ , the reading procedure is enabled and only the data relative to the found peaks in the  $[t_0; t_0 + t_{\max}]$  time interval are transferred to an external device

*Portion of the input signal, values of the auxiliary functions and found peaks.*

# The CluTim algorithm



$S_{K,X}$ : 16 samples at 125 MHz to the FPGA input.

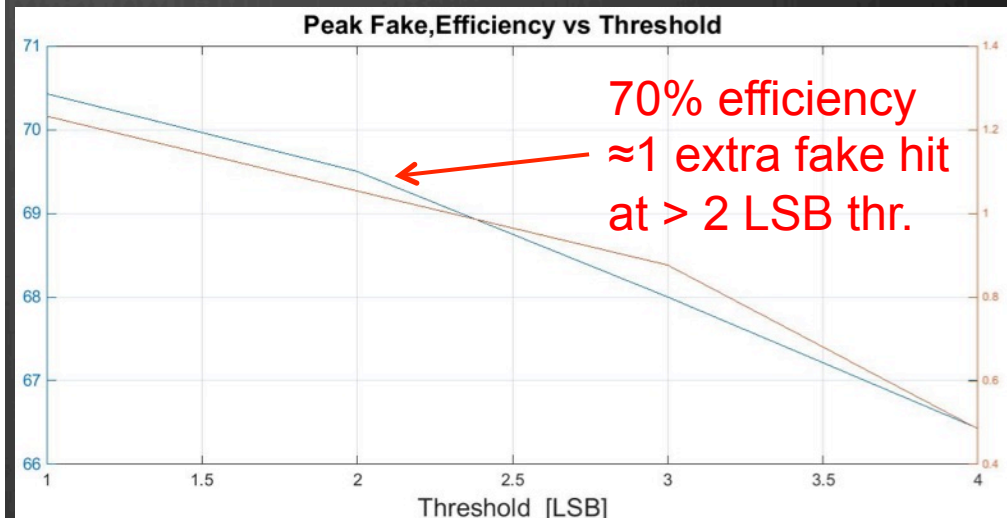
**STEP 1:** Of the 16 samples  $S_{K,X}$ , where K is the sample number among those available, and X is the time bin at which they are taken, the functions  $D1_{K,X}$  e  $D2_{K,X}$  are calculated as follows:

$$D1_{K,X} = ((2 * S_{K,X} - S_{K-1,X} - S_{K-2,X}) / 16) * 3$$

$$D2_{K,X} = ((2 * S_{K,X} - S_{K-2,X} - S_{K-3,X}) / 16) * 5$$

**STEP 2:** The values of  $D1_{K,X}$  and  $D2_{K,X}$  and the differences between  $D1_{K,X}$  and  $D1_{K-1,X}$  and between  $D2_{K,X}$  and  $D2_{K-1,X}$  are compared with the thresholds set according to the noise level in the input signal.

**STEP 3:** before transferring the data to memory, the last step checks that there are no adjacent peaks



# Data transfer reduction



## transferring all digitized data from DC

### Z decays

- $20 \text{ trks/ev} \times 130 \text{ hits/trk} \times 2 \text{ sides} \times 4 \times 10^{-7} \text{ s} \times 2 \times 10^9 \text{ B/s} \times 100 \text{ kHz} = 400 \text{ GB/s}$

### $\gamma\gamma \rightarrow \text{hadrons}$

- $10 \text{ trks/ev} \times 130 \text{ hits/trk} \times 2 \text{ sides} \times 4 \times 10^{-7} \text{ s} \times 2 \times 10^9 \text{ B/s} \times 30 \text{ kHz} = 60 \text{ GB/s}$

### IPC background

- $1\% \text{ occupancy} \times 5.6 \times 10^4 \times 2 \times 4 \times 10^{-7} \text{ s} \times 2 \times 10^9 \text{ B/s} \times 100 \text{ kHz} \times 3 \text{ (SF)} = 300 \text{ GB/s}$

### Isolated peaks (noise above threshold)

- $2.5\% \times 5.6 \times 10^4 \times 2 \text{ sides} \times 4 \times 10^{-7} \text{ s} \times 2 \times 10^9 \text{ B/s} \times 100 \text{ kHz} = 250 \text{ GB/s}$

**$\geq 1 \text{ TB/s}$**

## transferring only drift peaks from DC

### Z decays

- $20 \text{ trks/ev} \times 130 \text{ hits/trk} \times 2 \text{ sides} \times 50 \text{ peak/hit} \times 2 \text{ B/peak} \times 100 \text{ kHz} = 50 \text{ GB/s}$

### $\gamma\gamma \rightarrow \text{hadrons}$

- $10 \text{ trks/ev} \times 130 \text{ hits/trk} \times 2 \text{ sides} \times 50 \text{ peak/hit} \times 2 \text{ B/peak} \times 30 \text{ kHz} = 8 \text{ GB/s}$

### IPC background

- $1\% \text{ occupancy} \times 5.6 \times 10^4 \times 2 \text{ sides} \times \text{few peak/hit} \times 2 \text{ B/peak} \times 100 \text{ kHz} \times 3 \text{ (SF)} = 2 \text{ GB/s}$

### Isolated peaks (noise above threshold)

- $2.5\% \times 5.6 \times 10^4 \times 2 \text{ sides} \times \text{few peak/hit} \times 2 \text{ B/peak} \times 100 \text{ kHz} = 2 \text{ GB/s}$

**$\approx 60 \text{ GB/s}$**



# Current work on a 2ch board



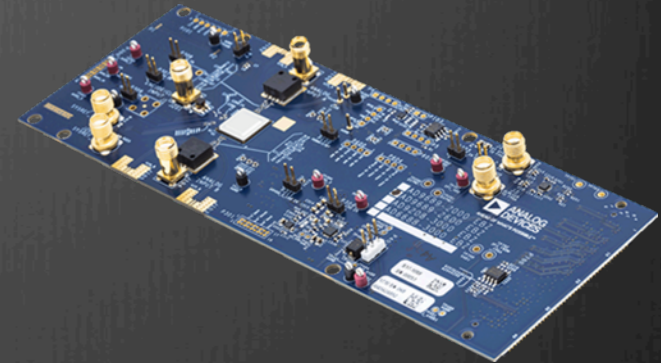
New hardware under test for a new **2ch board**

**Dual channel ADC: AD9689 - 2000EBZ**  
**FPGA: Xilinx Kintex UltraScale KCU105**

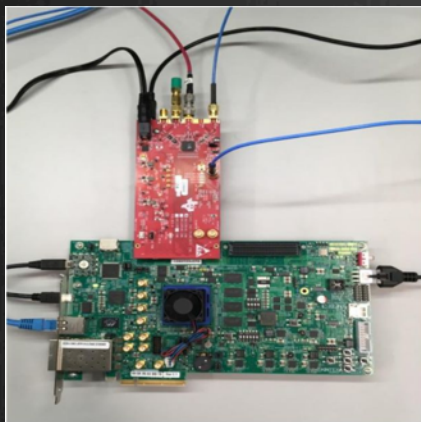
Considering also

**Dual-Channel ADC: ADC32RF45, 14-Bit, 3GSPS**  
from TEXAS INSTRUMENT directly compatible

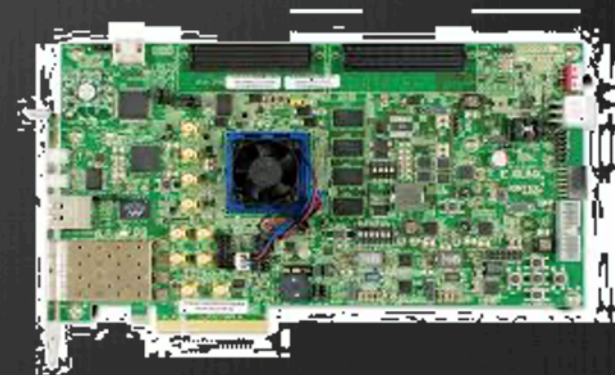
with **KCU105**, offering better performance in terms of noise, ENOB, channels isolation



Dual channel ADC: AD9689 - 2000EBZ



Cluster electronics



FPGA: Xilinx Kintex UltraScale KCU105

June 15, 2021

The aim of the activity is to be able to implement, within a **single FPGA board**, more sophisticated, more efficient and less fake-contaminated peak finding algorithms on **4 analog to digital conversion channels** for parallel real-time pre-processing of the signals generated by a drift chamber designed to operate at the next generation of lepton colliders.

The activity will be done in synergic collaboration with CAEN.

We will provide the experimental setups and elaborate the various peak finding algorithms. CAEN will provide the testing grounds for the produced firmware and design and build the electronic board.

Needless to say, this studies will pave the road to the engineering of a multi (128 or 256) channel board, to reduce costs and system complexity, to be ultimately implemented in large experiments where the number of channels can be of the order of several tens of thousand.

# Alternatives: ASoC



Nalu Scientific (the SiRead Chip manufacturers) is testing a new digitizer (**ASoC**) with better performance (4-channel) than **SiRead** and complying with our requests. After contacts with the Nalu Scientific, we have been promised a demo board at the conclusions of their quality tests (June 2021).

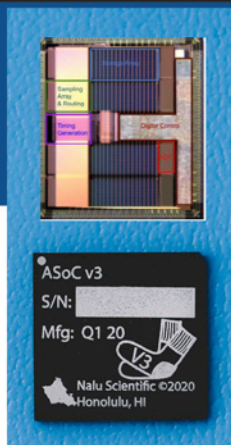
## ASoC V3 DESIGN DETAILS

Compact, high performance waveform digitizer

- High performance digitizer: 3+ Gsa/s
- Highly integrated
- Commercially available, low cost, patented design
- 5mm x 5mm die size

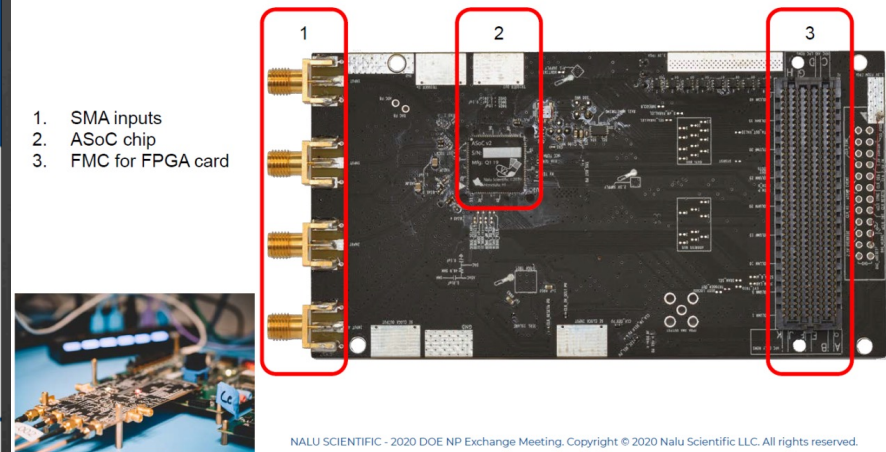
ASoC PARAMETERS	SPECIFICATION (MEASURED)
Sample rate	2.5 - 3.6 Gsa/s
Number of channels	4
Sampling depth	16 k Sa/channel
Signal range	0-2.5 V
Resolution	12 bits*, 10b ENOB
Supply Voltage	2.5 V
RMS noise	~1 mV
Digital Clock frequency	25 MHz
Timing resolution	1<25 ps***
Power /ch	50-125 mW/channel*
Analog bandwidth	950 MHz

- Integration/features:
- Calibration memory on chip
- PLL on chip
- Isolate analog/digital voltage rings
- Increase number of channels
- Implement serial interface
- Feature extraction on chip



## ASoC Eval Card

1. SMA inputs
2. ASoC chip
3. FMC for FPGA card



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# Alternatives: ASoC

Nalu Scientific  
better performance  
After contacts  
conclusions of

digitizer (**ASoC**) with  
our requests.  
demo board at the

ASoC PARAMETERS	SPECIFICATION (MEASURED)
Sample rate	2.5 - 3.6 GSa/s
Number of channels	4
Sampling depth	16 k Sa/channel
Signal range	0-2.5 V
Resolution	12 bits*, 10b ENOB
Supply Voltage	2.5 V
RMS noise	~ 1 mV
Digital Clock frequency	25 MHz
Timing resolution	1<25 ps***
Power /ch	50-125 mW/channel*
Analog bandwidth	950 MHz

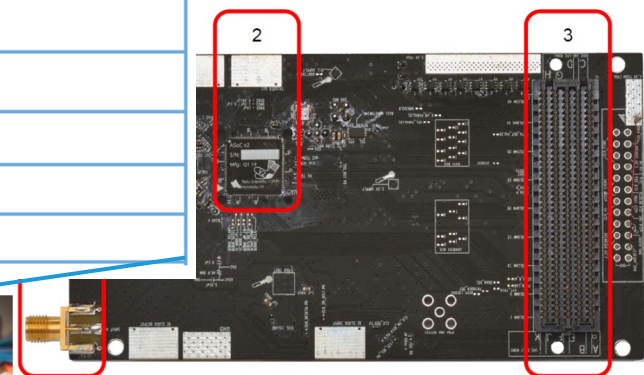
## ASoC V3 DESIGN

Compact, high performance

- High performance digitizer: 3+ G
- Highly integrated
- Commercially available, low cost
- 5mm x 5mm die size

ASoC PARAMETERS	SPECIFICATION (MEASURED)
Sample rate	2.5 - 3.6 GSa/s
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ASoC PARAMETERS	SPECIFICATION (MEASURED)
Sample rate	2.5 - 3.6 GSa/s
Number of channels	4

**Also, in preparation a 32 channel chip (HDSoc) to be packaged, board design, brought up and tested in the next few months.**

(private communication by Isar Mostafanezhad, founder and CEO of **NALU Scientific**)

ASoC  
Compact

- High p
- Highly
- Comm
- 5mm

ASoC PARAMETERS	SPECIFICATION (MEASU
Sample rate	2.5 - 3.6 GSa/s
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