Omega

ROC ASICs for timing

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Organization for Micro-Electronics desiGn and Applications

Timing optimization : common view

- Jitter due to electronics noise:

$$\sigma_t^J = \frac{N}{\frac{dV}{dt}}$$

- also presented as j = tr / (S/N)
- dV/dt prop to BW, N prop to √ BW => jitter prop to 1/√BW

⇒ « the faster the amplifier, the better the jitter ? »

⇒ « High speed preamps need to be low impedance (50 Ω or less) ? »

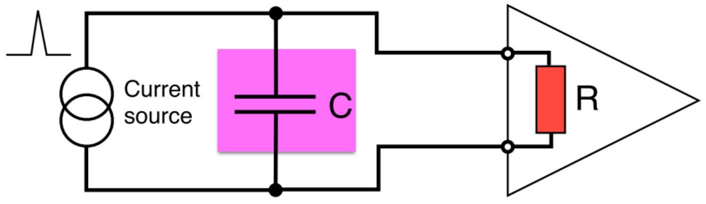
– minimize R_{PA} : small time constant R_{PA}.Cd « Minimize « charge time transfer »

NB : tr = $t_{10\text{-}90\%}$ = 2.2 tau.

f_{-3dB} = 1/2πtau = 0. 35 / $t_{10\text{-}90}$

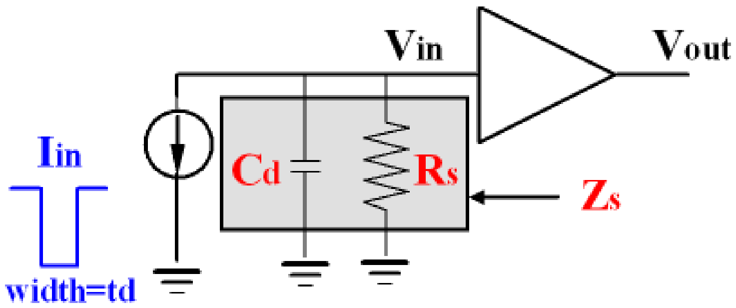
f_{-3dB} = 1 GHz <-> $t_{10\text{-}90\%}$ = 300 ps

1 ps = 300 µm in vaccum

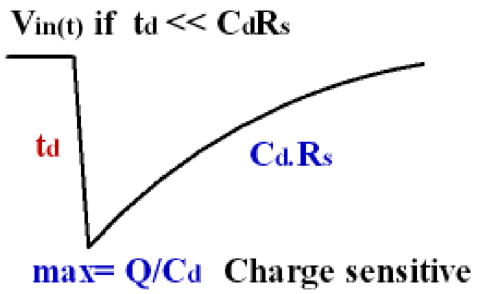


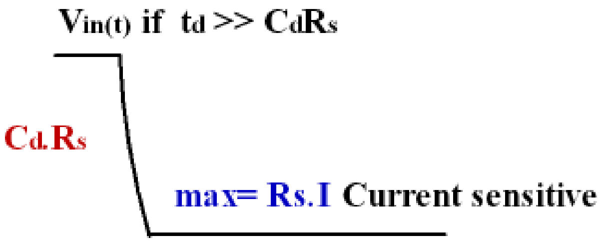
Detector impedance and input voltage

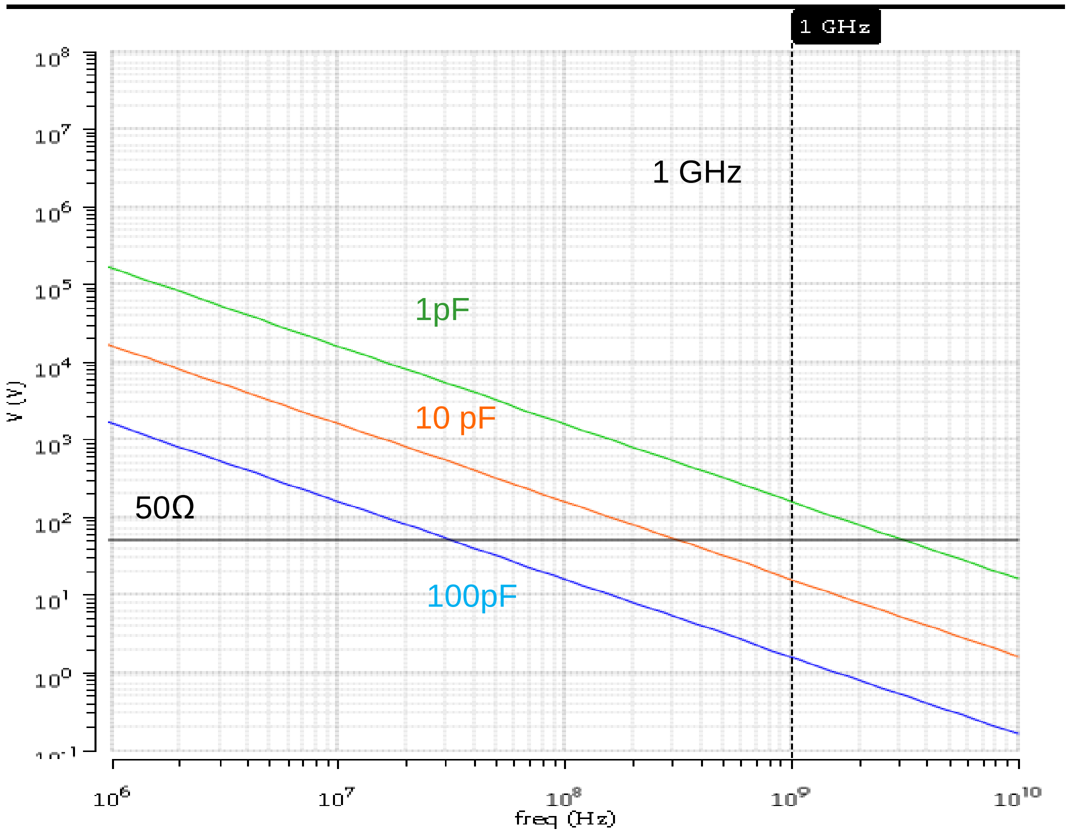
- 1 GHz, Cd=few tens of pF, input signal width <1ns
- Cd>1 pF, Zs@1GHz dominated by Cd
- Rise time: tr= td when td<< $R_S\,C_d$ and tr= $R_S\,C_d$ when td>> $R_S\,C_d$



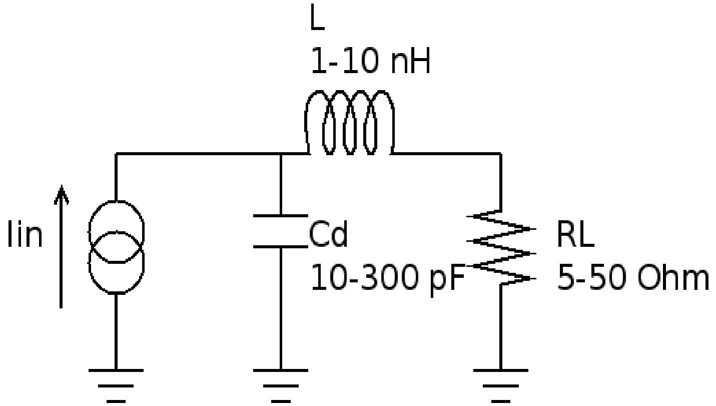
At HF : difficult to beat the capacitance => signal integrated on Cd

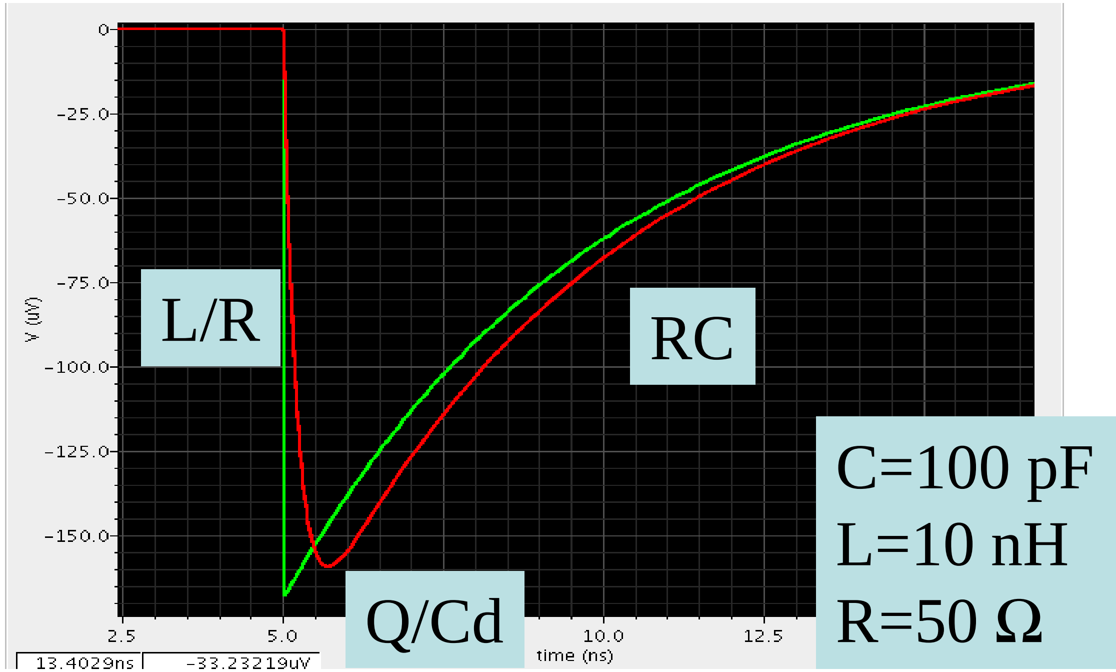


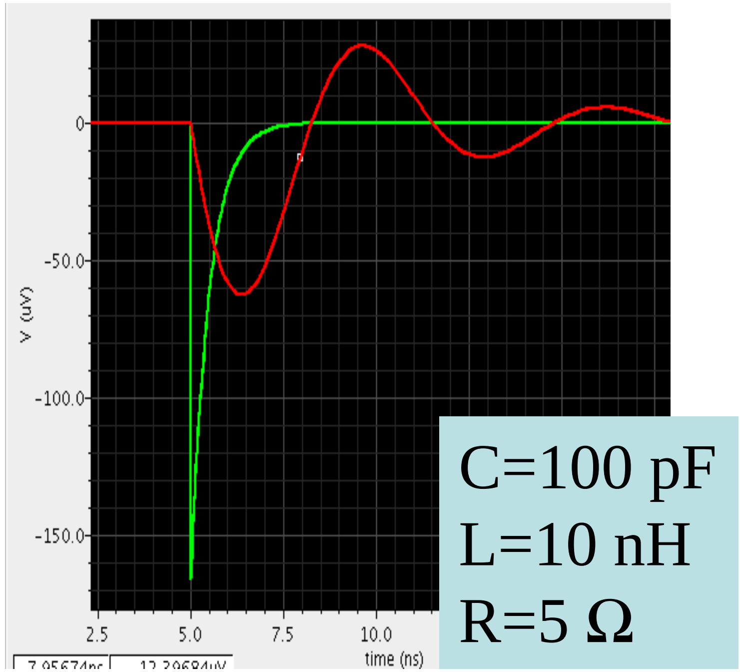




- SiPM pulse : Q=160 fC, Cd=100 pF, L=0-10 nH, R_{PA}=5-50 Ω
- Sensitivity to parasitic inductance
- Choice of R_{PA} : decay time, stability
- Small R_{PA} not necessarily the fastest
- Convolve with current shape… (here delta)

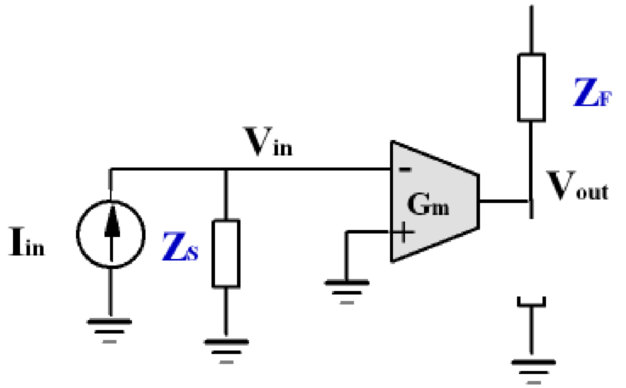




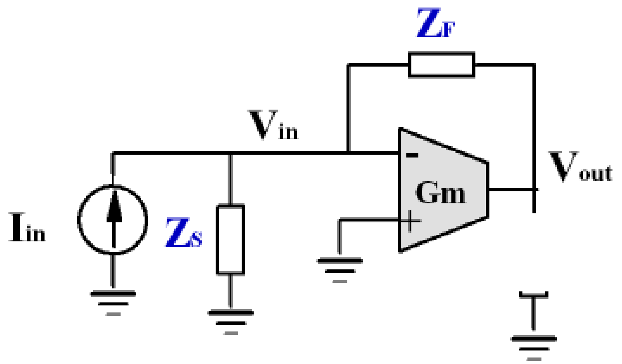


High speed amplifiers

- Response to very short pulse
- Broadband : voltage sensitive
  - Zin=Rs (50 Ohm)
  - Vin = Q/Cin
  - $V_{OUT} = -G_m R_F \frac{Q_{IN}}{C_d}$



- Transimpedance
  - Zin ~ Zf/G ~ 1/gm
  - $V_{OUT} = \frac{\frac{1}{G_m} - R_F}{1 + j\omega \frac{C_d}{G_m}} I_{IN} \approx -G_m R_F \frac{Q_{IN}}{C_d}$



- Same response at High Frequency
- For highest speed : go to broadband. Faster, less stability issues

Signal and noise in Broadband amplifiers

- Jitter is given by :

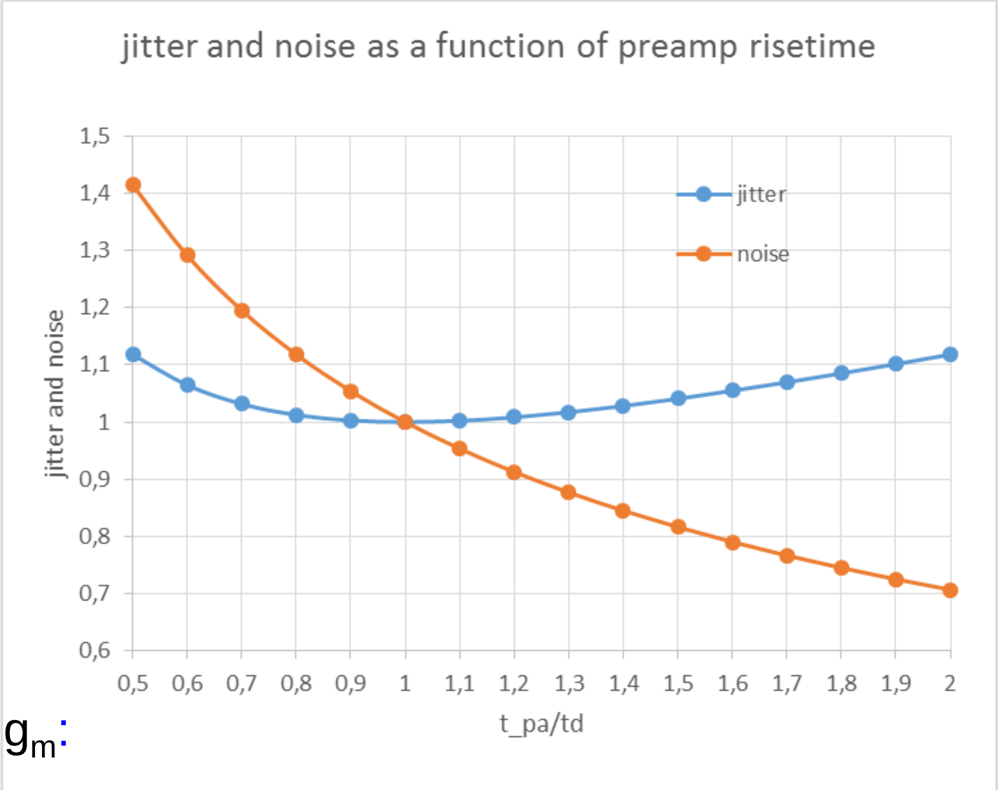
$$\sigma_t^{\ J} = \frac{N}{dV/dt} = \frac{e_n}{\sqrt{2t_{10-90\_PA}}} \frac{C_d\sqrt{t_{10-90\_PA}^2 + t_d^2}}{Q_{in}} = \frac{e_n C_d}{Q_{in}}\sqrt{\frac{t_{10-90\_PA}^2 + t_d^2}{2t_{10-90\_PA}}}$$

- Optimum value: $t_{10\text{-}90\_PA} = t_d$ (current duration)

Dominated by sensor
Electronics only gives en

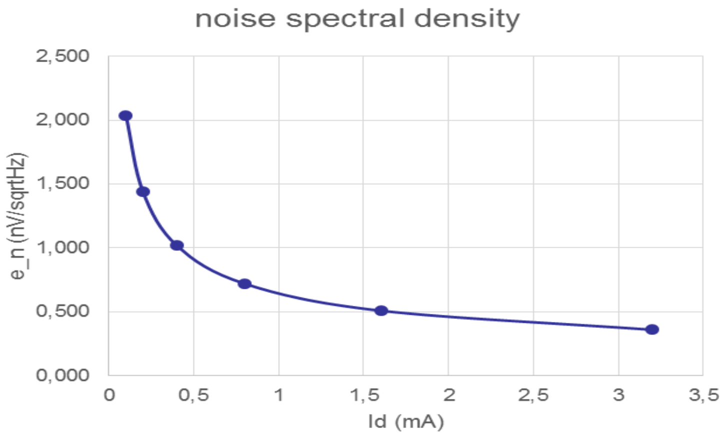
$$\sigma_t^{\ J} = \frac{e_n C_d}{Q_{in}}\sqrt{t_d}$$

Cd: detector capacitance
$t_{10\_10\_PA}$: rise time of the PA
t_d= detector current **duration**
e_n preamp noise density



- **Gives ps/fC** as scales with 1/Qin : « factor of merit »
- Electronics noise e_n given by the input transistor transconductance g_m:

$$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_D}}$$



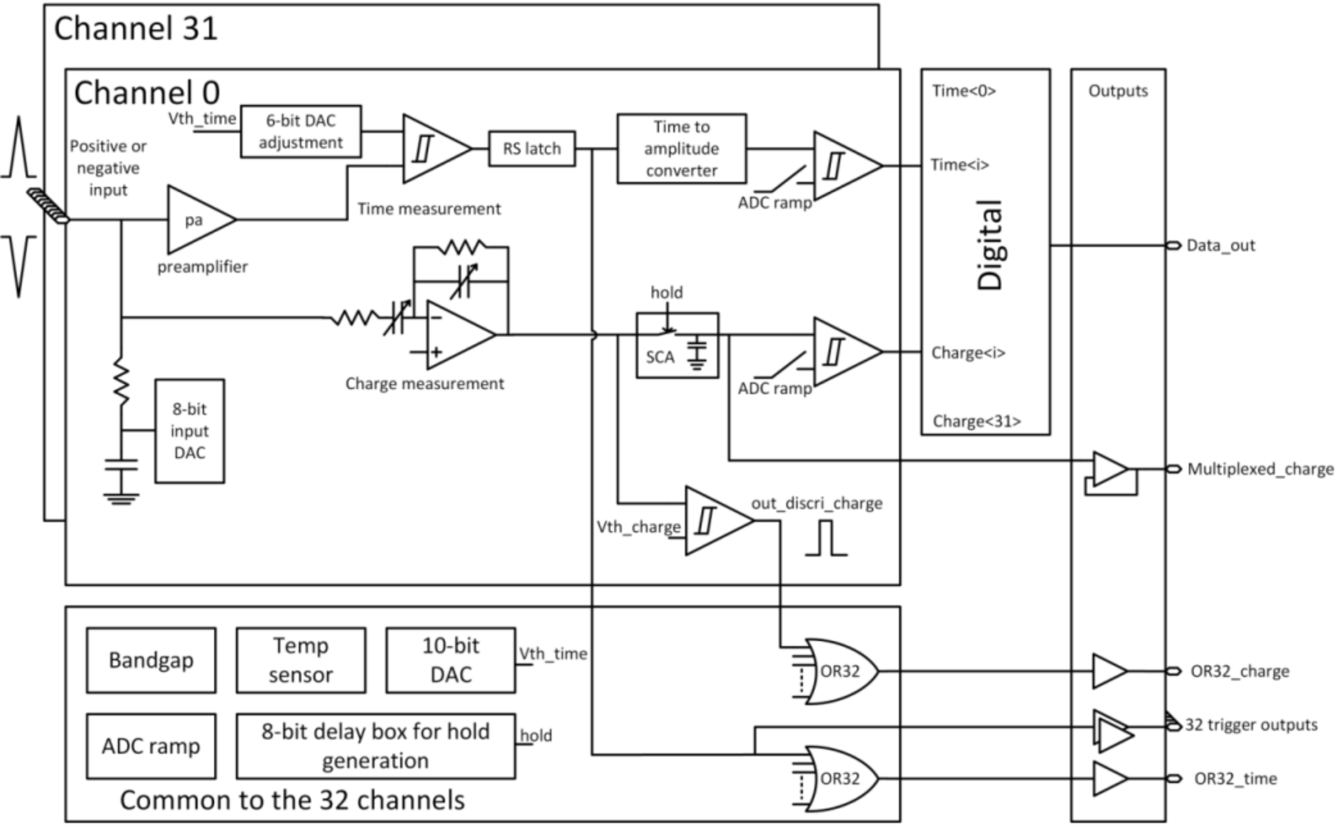
- Jitter optimum is rather shallow with preamp risetime
- But noise and minimum threshold goes up quickly with speed (as sqrt)

OMEGA timing chips

- See also prensentation by Stéphane Callier on Thursday (Hardroc et al.)

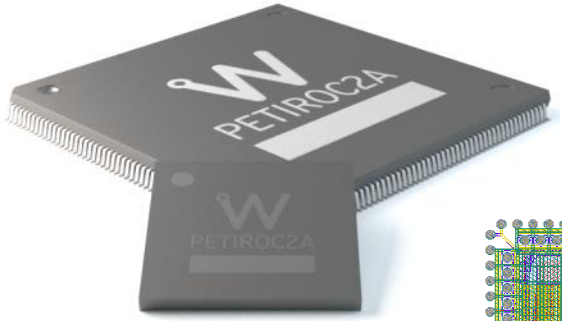
		sensor	polarity	BW	Zin	Cd	TDC	dyn range	FOM	min thresh	"@Cd="
PETIROC	VPA	SiPM/RPC	both	900 MHz	200	10-100 pF	25 ps			1 mV	
LIROC	VPA	SiPM/RPC	both	300 MHz	1k	10-100 pF	no	10fC-100 pC	2 ns/Q (fC)	40 fC	
ALTIROC	VPA/TZ	LGAD	neg	300-800 MHz	2k/200	1-10 pF	20 ps	0.1-50 fC	100 ps/Q(fC)	2 fC	5 pF
HGCROC	TZ	Si	neg	100 MHz	40	10-100 pF	25 ps	0.1 fC-10 pC	2 ns/Q (fC)	20 fC	50 pF
H2GCROC	CC	SiPM	pos	80 MHz	25	100p-1nF	25 ps	10 fC-200 pC			

PETIROC2A

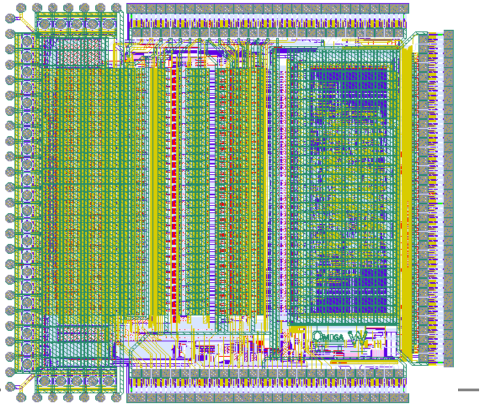


SiPM read-out for time-of-flight PET

SiGe 350 nm



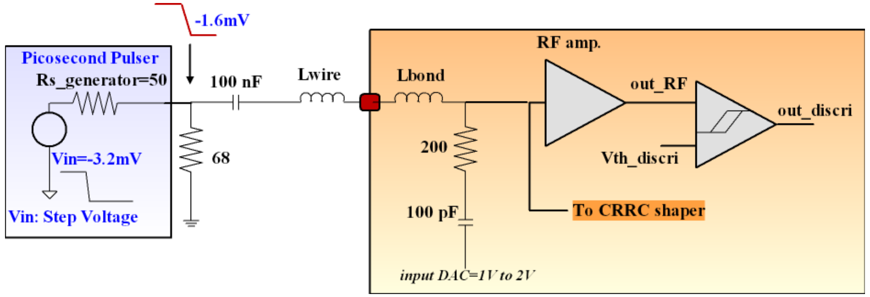
weeroc

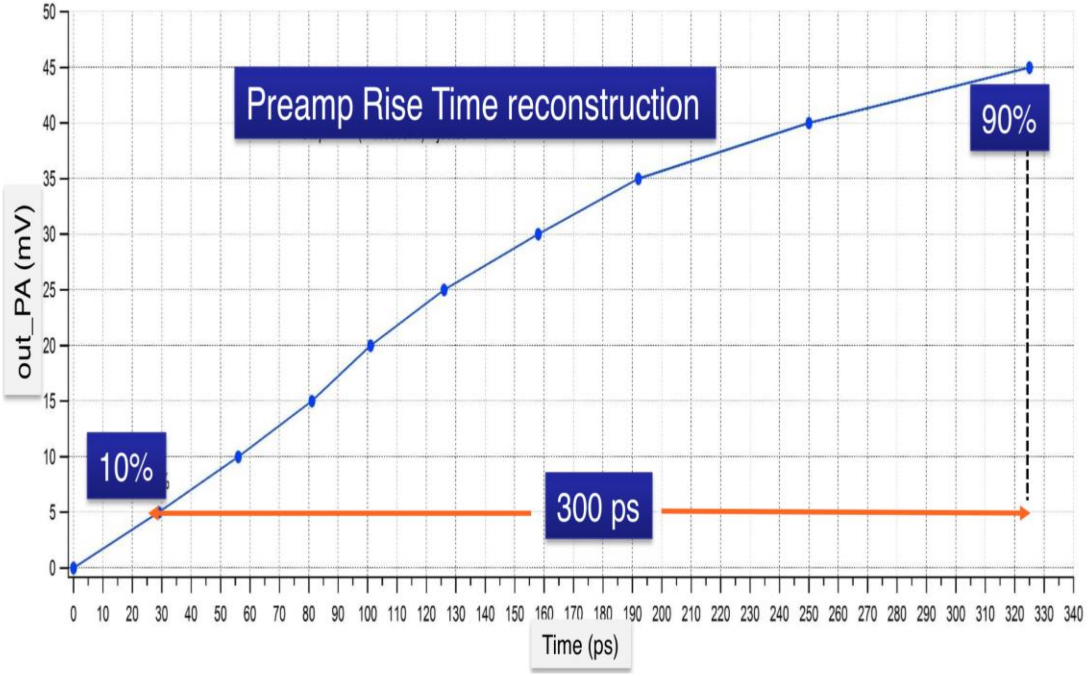


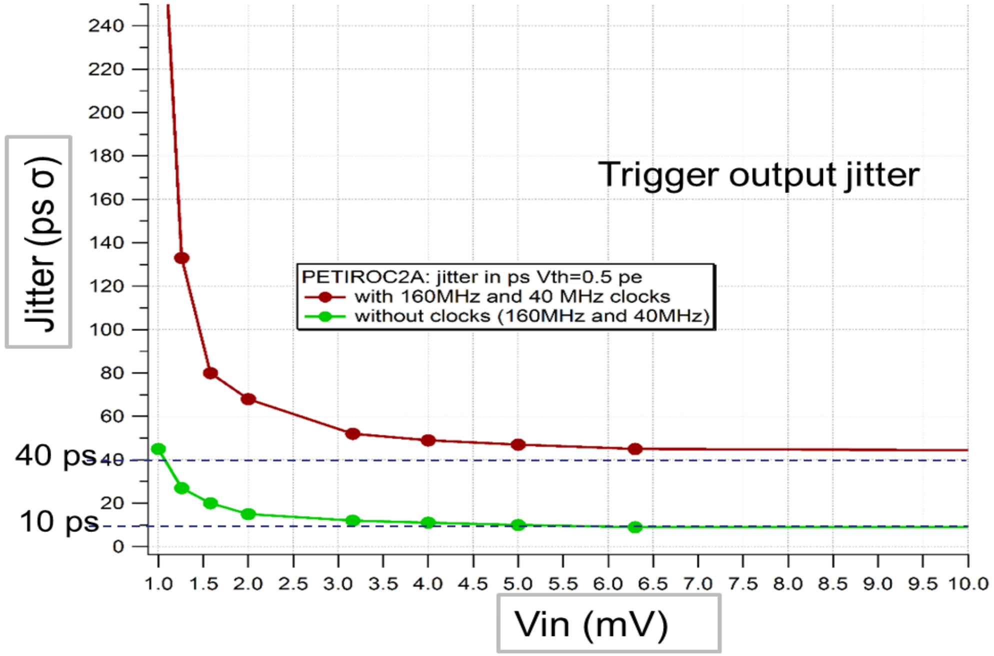
Detector Read-Out	SiPM, SiPM array
Number of Channels	32
Signal Polarity	Positive or Negative
Sensitivity	Trigger on first photo-electron
Timing Resolution	~ 35 ps FWHM in analogue mode (2pe injected) - ~ 100 ps FWHM with internal
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2500 ph-e
Packaging & Dimension	TQFP160 – TFBGA353

Petiroc2A bandwidth measurement

- Preamp + discriminator bandwidth
- reconstruction of pulse by discriminator
- **tr 10%-90% = 300 ps,**
- **BW = 0.35 / tr ~ 0.9 GHz**
- can also use BW = 0.1 / ($t_{50\%}$ - $t_{10\%}$)

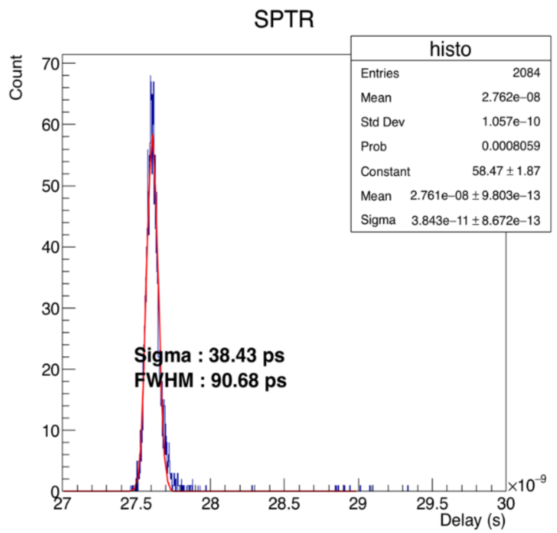


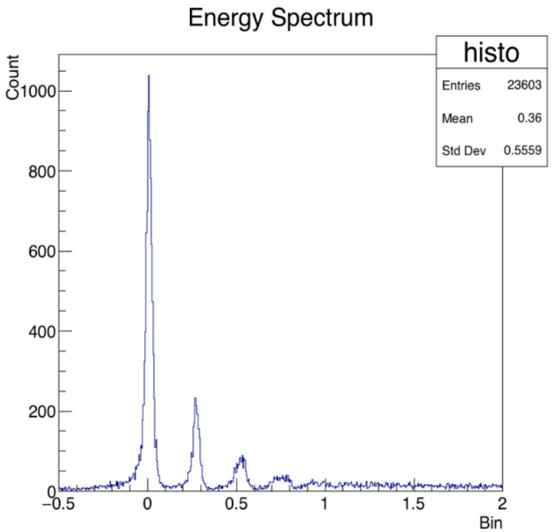




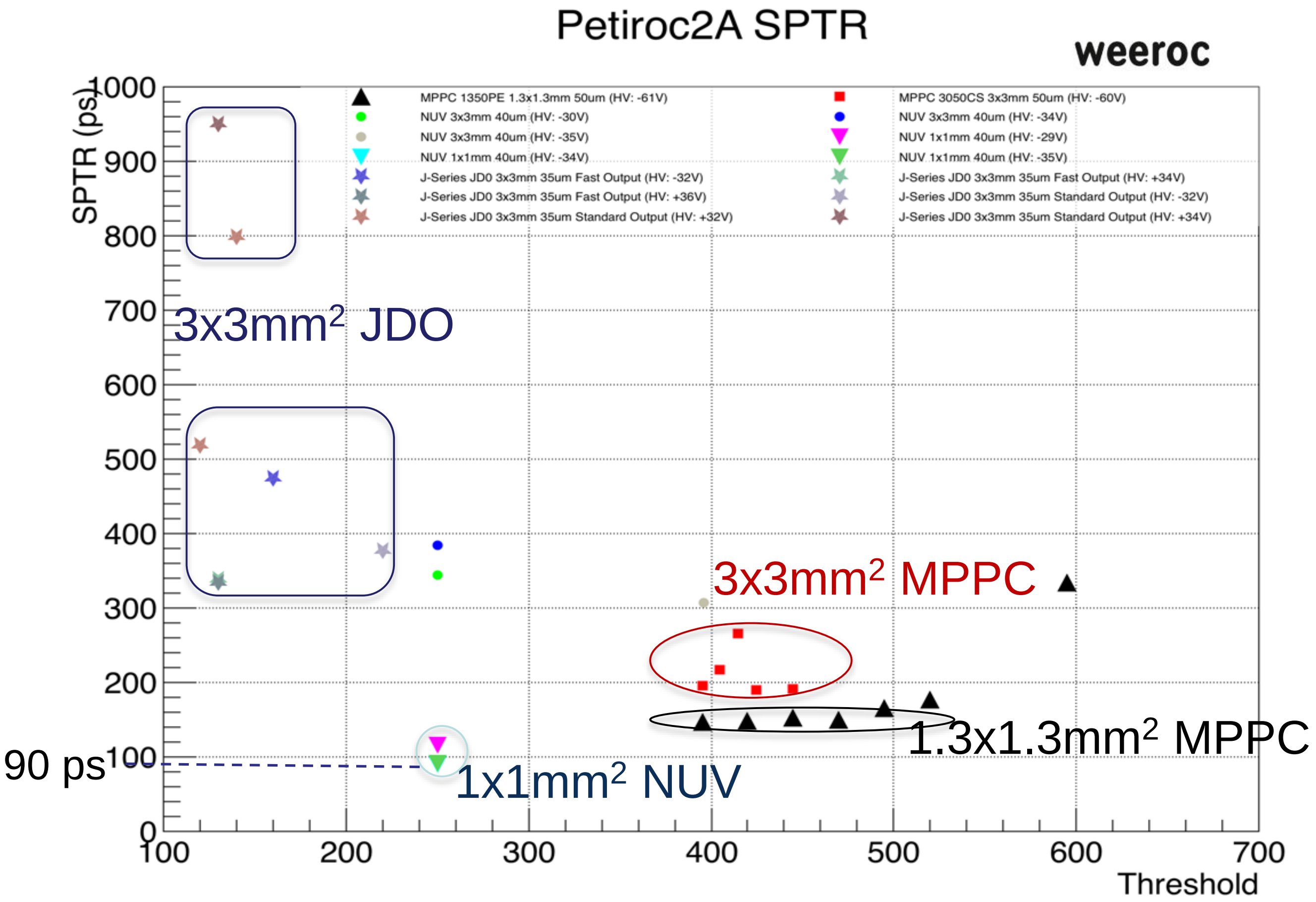
SPTR measurement : Petiroc2A trigger outputs

- SPTR : 90 ps FWHM (40 ps rms)



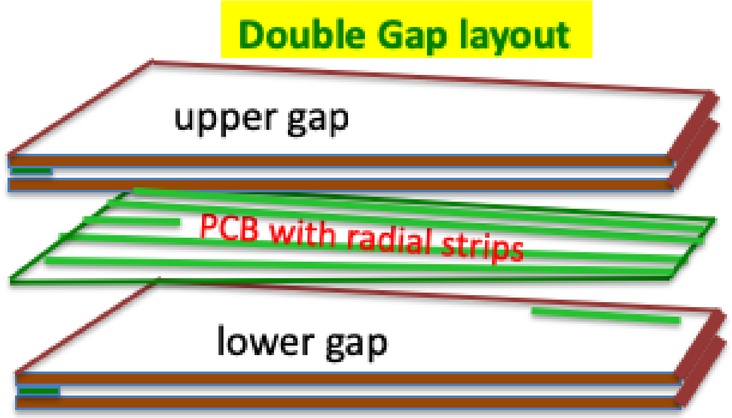


FBK NUV 1x1 mm^2 : 90.7 ps FWHM

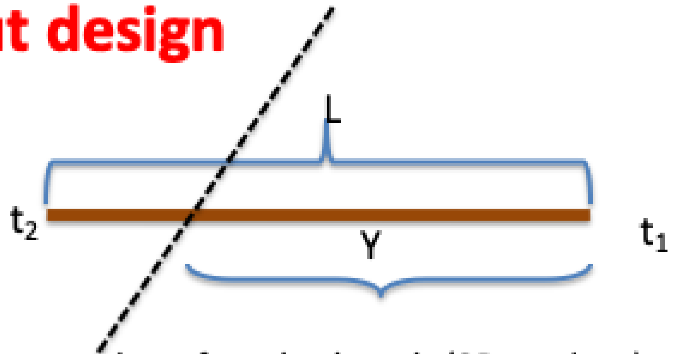


Source : Laser
SiPM : Various model (FBK, Hamamatsu, Sensl)
HV : Various value

CMS iRPC readout design



Dimensions: 165 cm x (63-114) cm

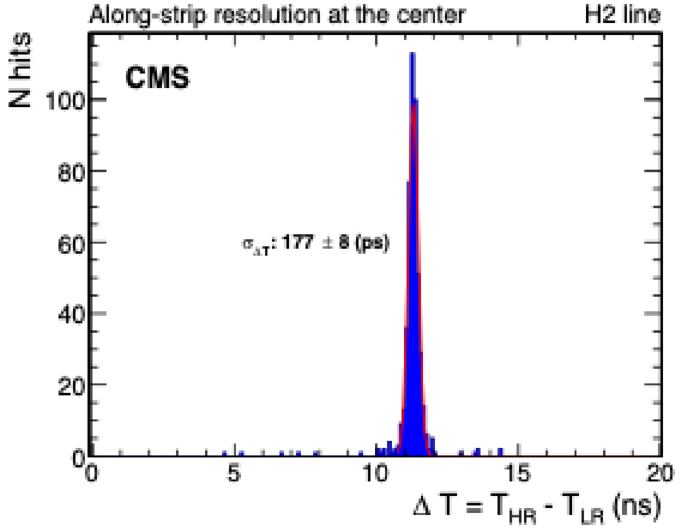


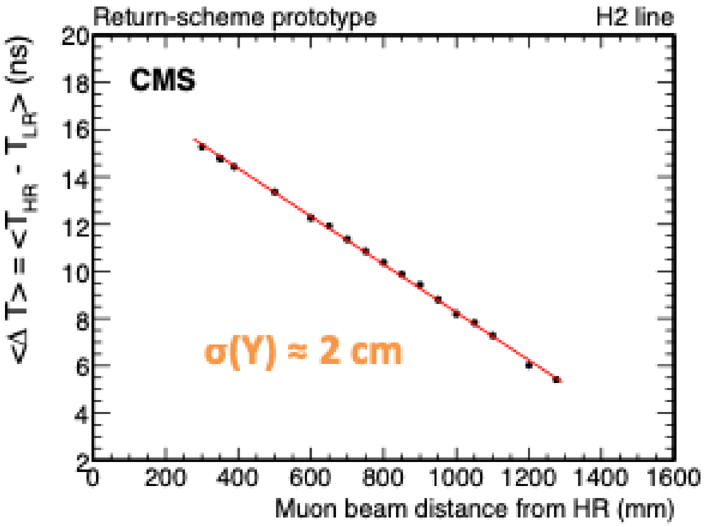
The strips are read out from both ends (2D readout) with good timing FEB.

→ Better Y determination

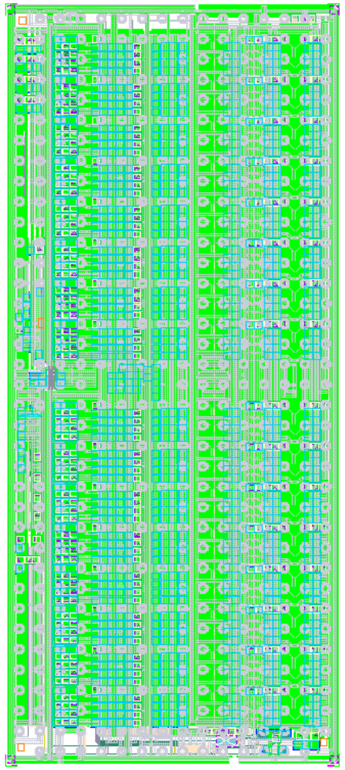
$Y = L/2 - v^*(t_2 - t_1)/2 \rightarrow \sigma(Y) = v^* \sigma(T_2 - T_1)/2$

→ Good absolute timing

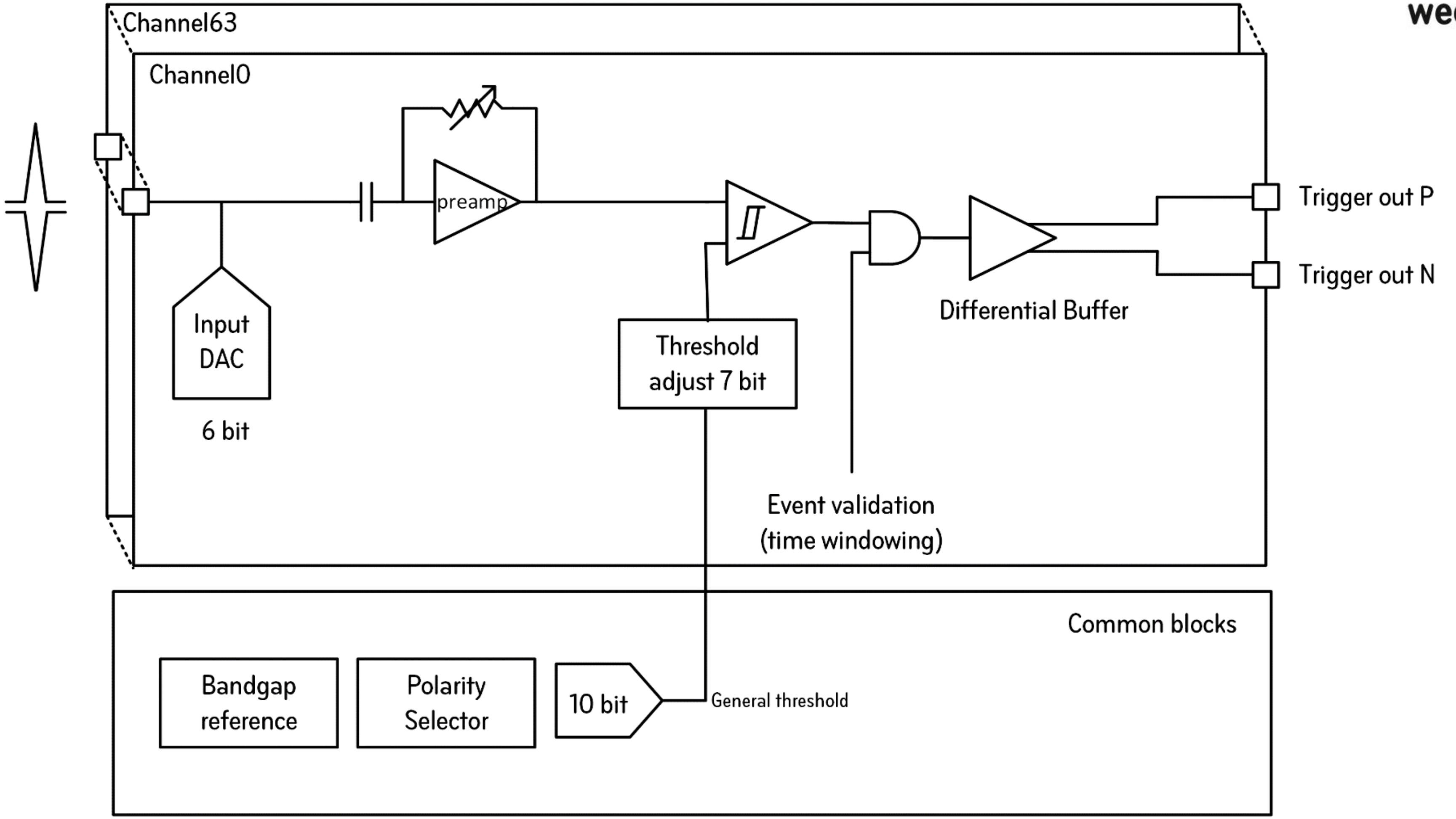




LIROC : SiPM read-out for Lidar



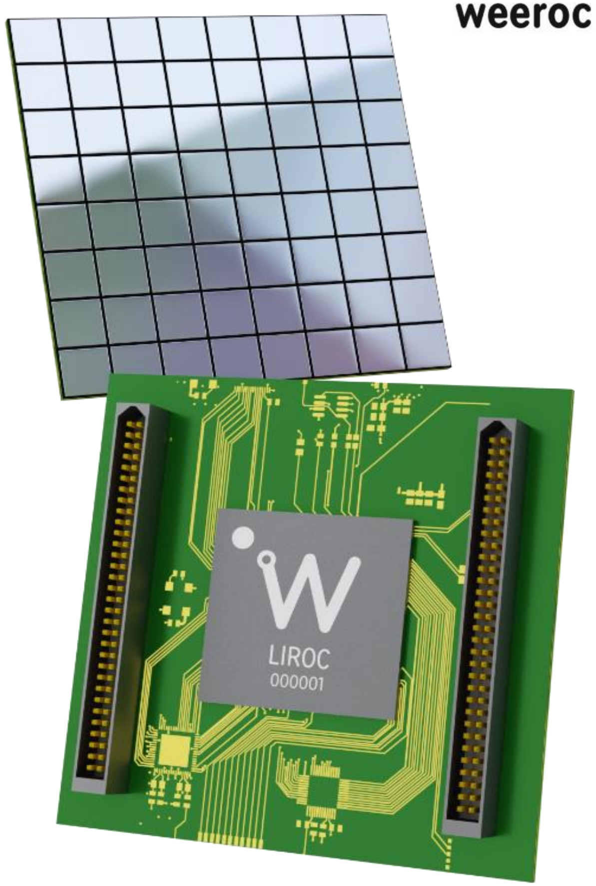
SiPM read-out for LIDAR
TSMC 130 nm



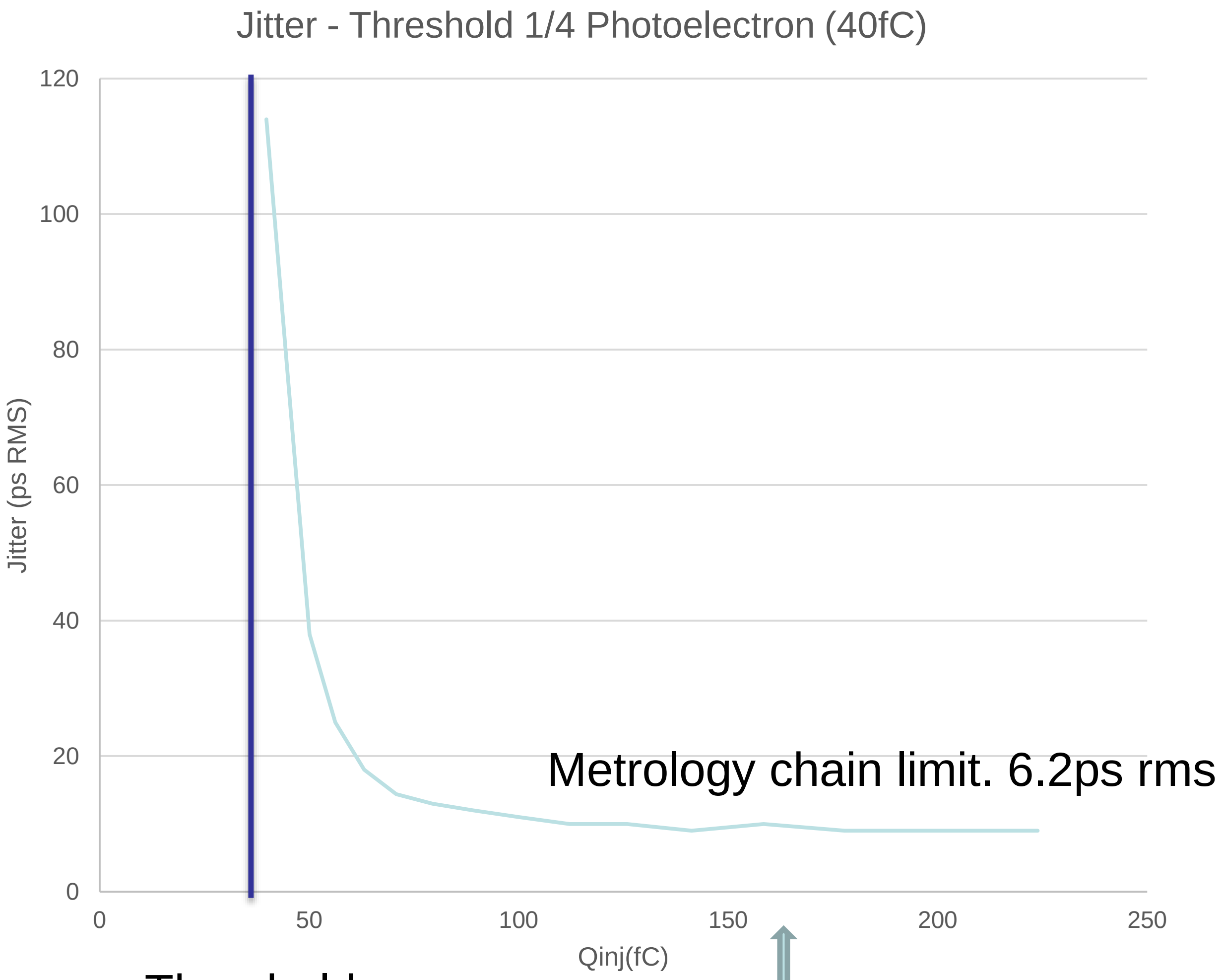
Collaborative design between Weeroc & Omega
Funding from ATTRACT EU H2020 Research & Innovation Program

Parameters & Performances

Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive or Negative (selectable ASIC-wise)
Sensitivity	Trigger on 1/3 of photo-electron
Timing Resolution	Better than 20 ps FWHM on single photo-electron Better than 5ns double-peak separation on single photo-electron
Dynamic Range	Over 100MHz photon counting rate
Packaging & Dimension	BGA 20x20 mm^2 Flip-Chip low inductance packaging technology
Power Consumption	210mW – Supply voltage : 1.2 V
Inputs	64 analogue inputs with independent SiPM HV adjustments
Outputs	64 low-common-mode LVDS triggers (CLPS) – compatible with CERN picoTDC and all LVDS FPGA I/Os
Internal Programmable Features (I^2C)	64 HV adjustment for SiPM (64 x 6 bit), trigger threshold programming (10bits), 64 x 7 bit channel-wise threshold adjustment, ASIC-wise polarity selector, preamp pole-zero cancellation adjustment, individual trigger masking and cell powering.

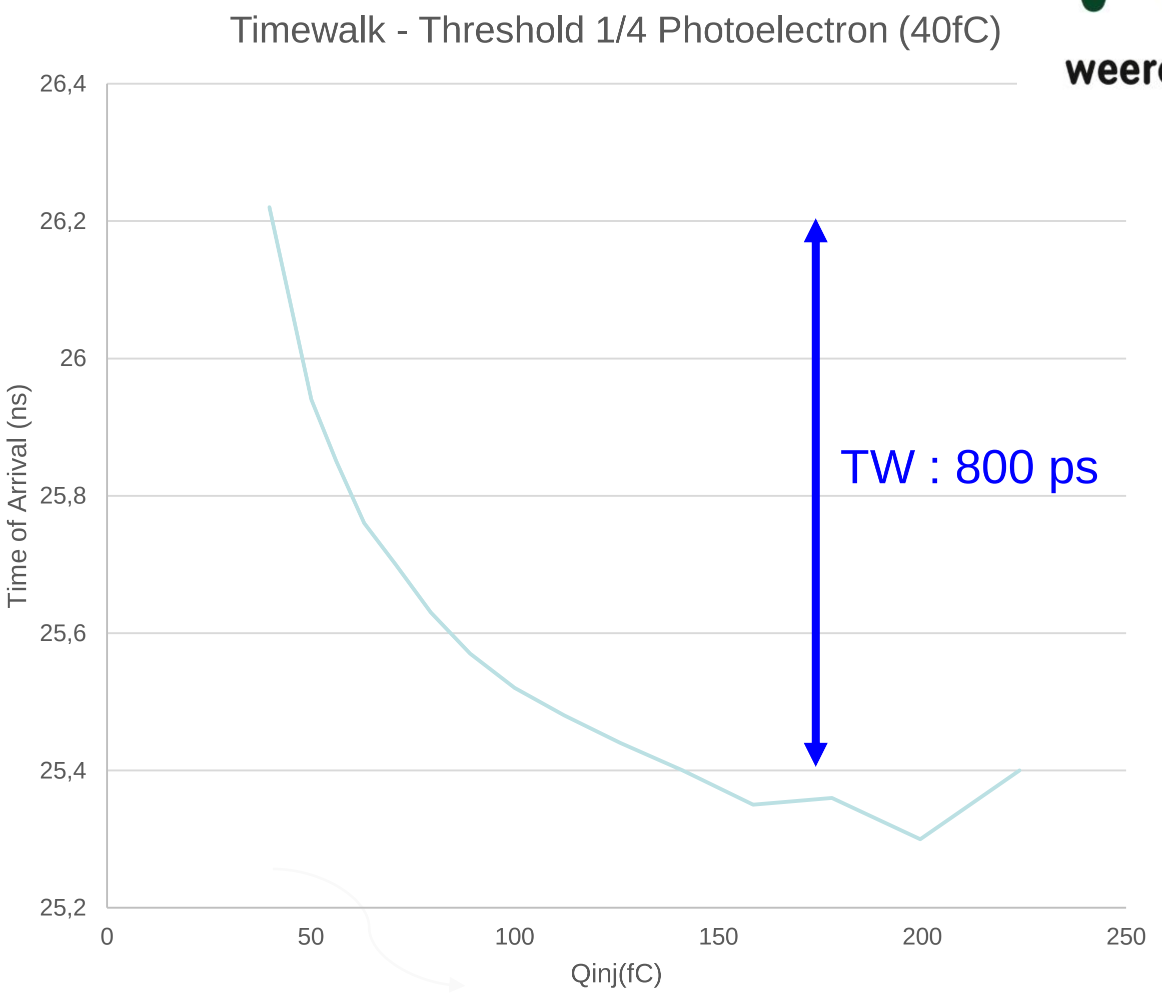


Jitter and timewalk

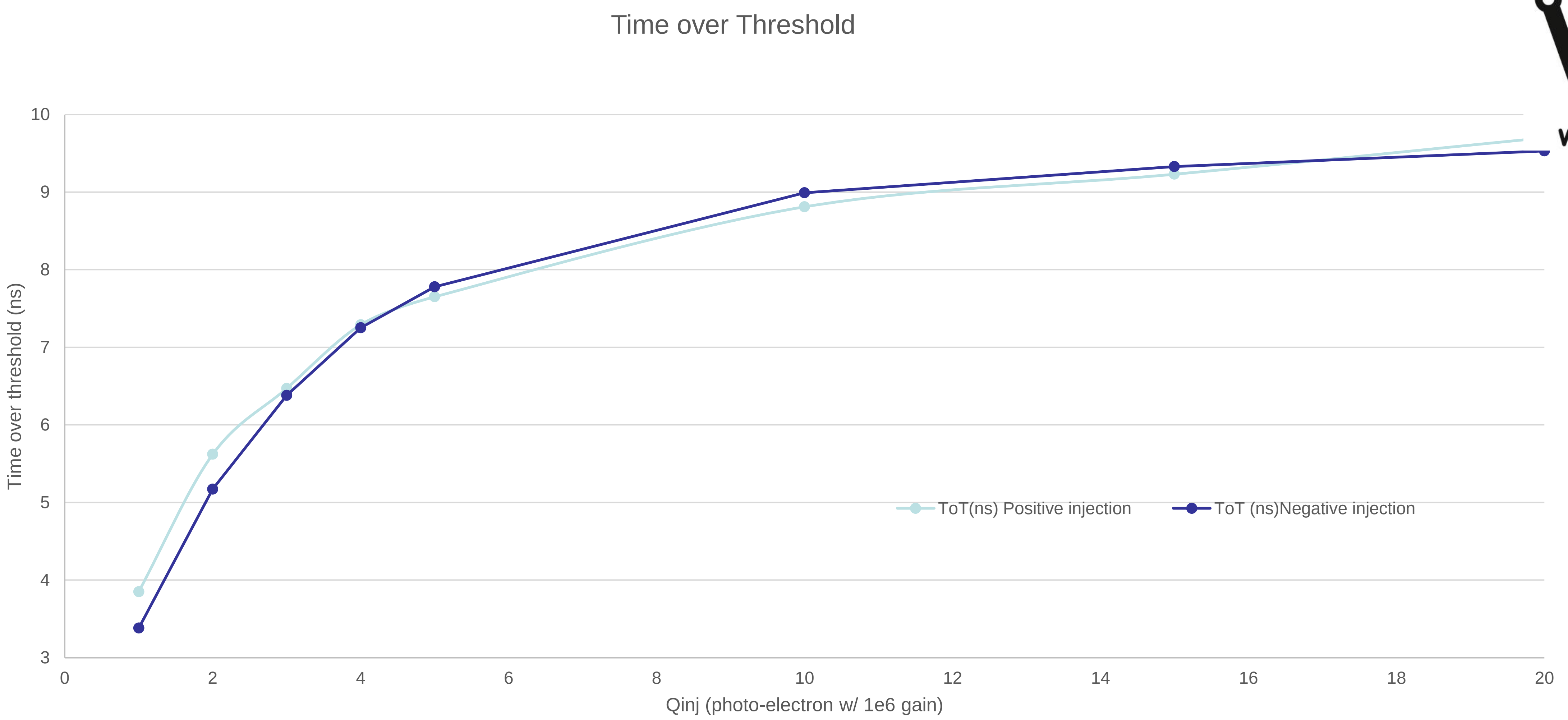


Threshold:
40 fC

1 photoelectron - Gain 10^6



Time Over Threshold – Measuring amplitude

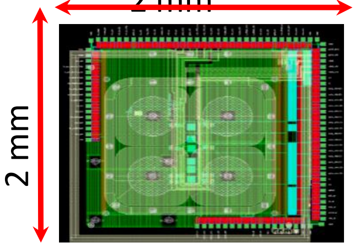


Trade-off beetween double peak separation (see consecutive photons) and time over threshold. Tuneable. Optimized for double-peak separation in that measurement (3ns separation measured)

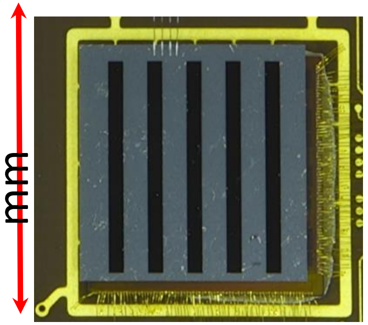
ALTIROC : ATLAS LGAD ReadOut Chip for HGTD

- **ALTIROC0 (2017) :** contains only PA + discriminator – for 2x2 1x1 mm2 sensors
  - 4 channels VPA and 4 channels TZ analog readout optimized for Cd=2pF
  - Bandwidth tunable (0.3-0.8 GHz)
  - Power : 2 mW/ch   TSMC 130 nm

Altiroc0

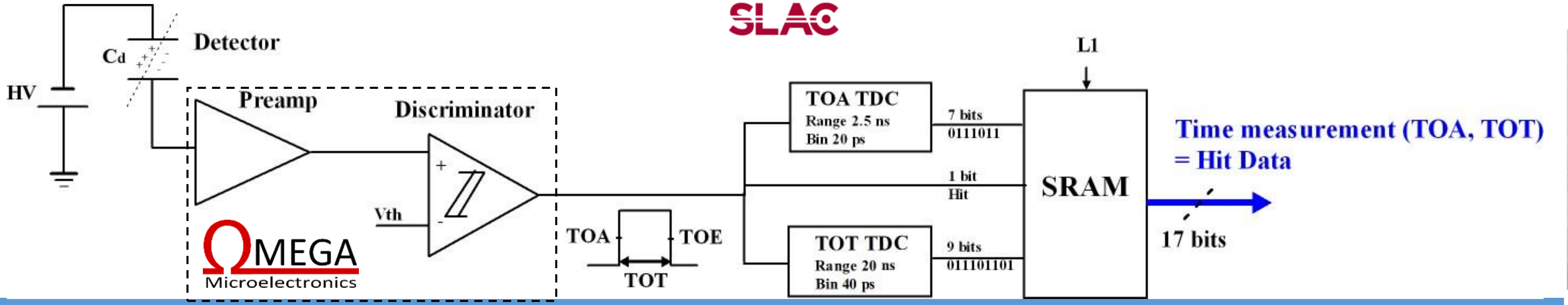


- **ALTIROC1 (2018) :** 5x5 complete readout channels (PA, discri, TDC, SRAM) to readout 1.3 x 1.3 mm2 LGAD pixels , 15 channels with VPA, 10 with Transimpedance amplifier (TZ)



- **ALTIROC2 (2021) : 1**5x15 final size and functionnality

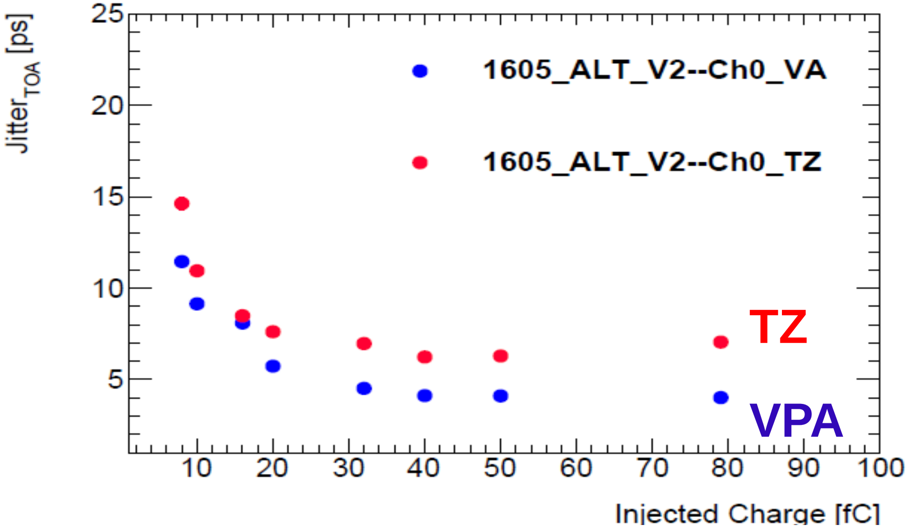
SLAC

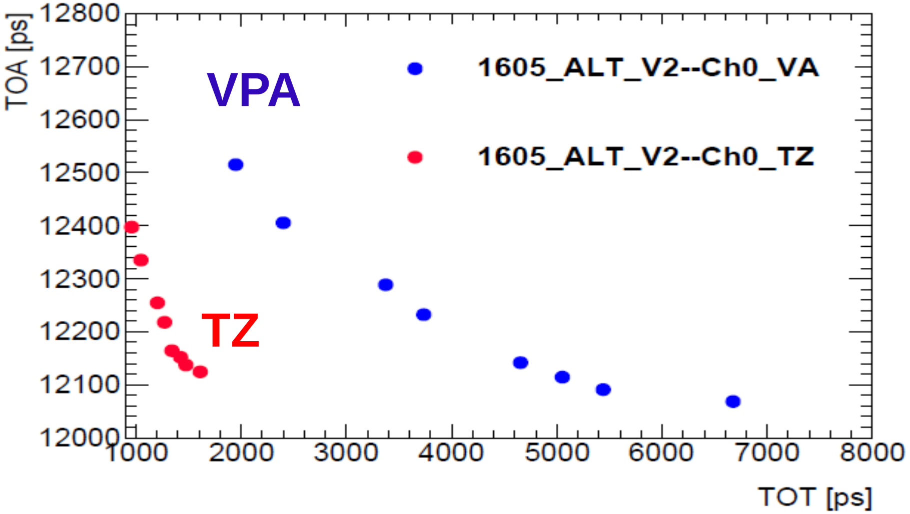


ATLAS HGTD

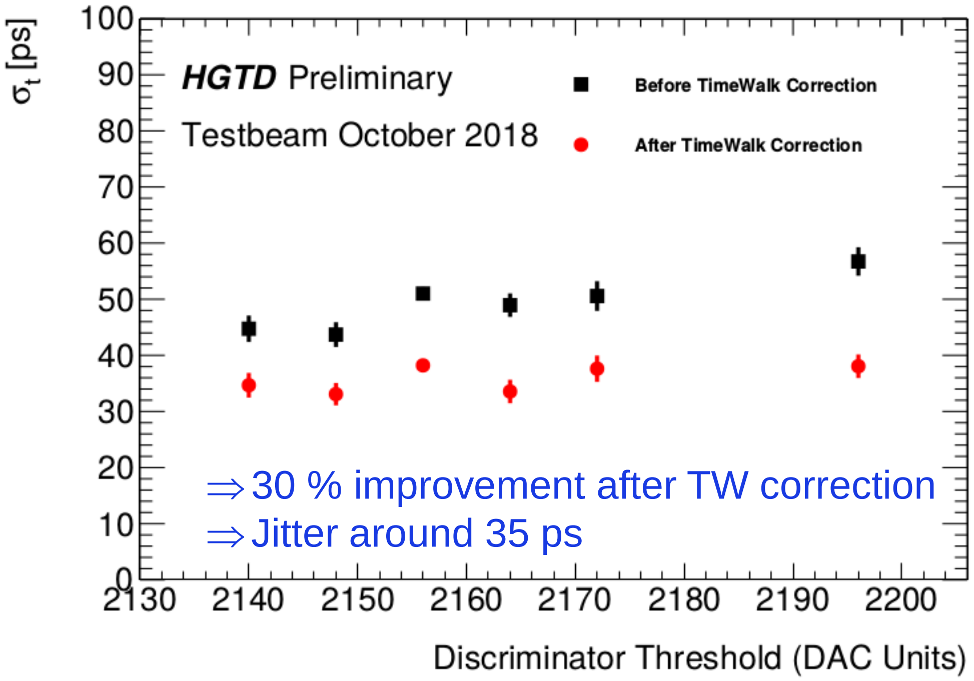
ALTIROC0 measurements

- Testbench (left) and testbeam (right) measurements





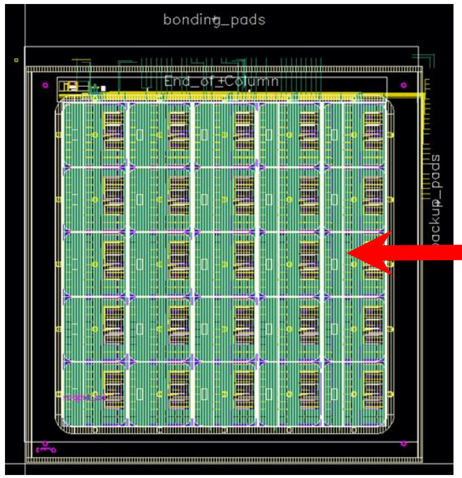
- ALTIROC0_V2
- Time resolution of a 2x2 x1x1 mm2 LGAD array bump bonded on an Altiroc0 ASIC as a function of the discri threshold (DAC Units) before (black points) and after TW correction (red points)

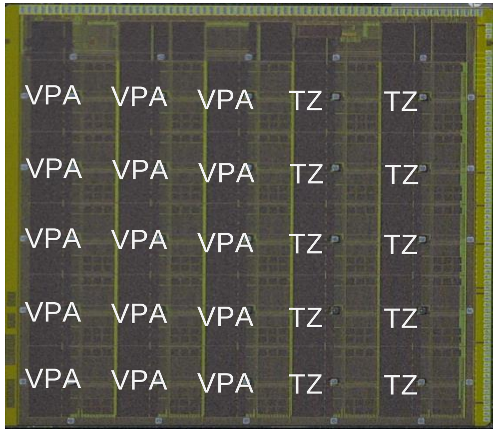


ALTIROC1

Altiroc1 layout

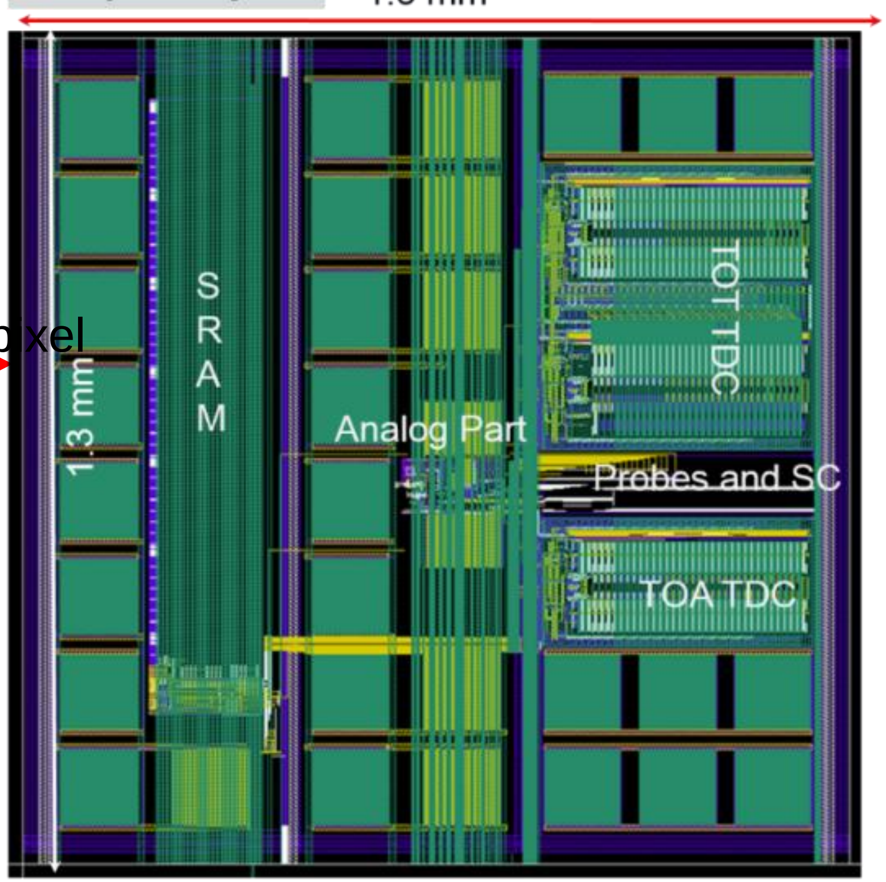
~ 8 mm





ZOOM of one pixel

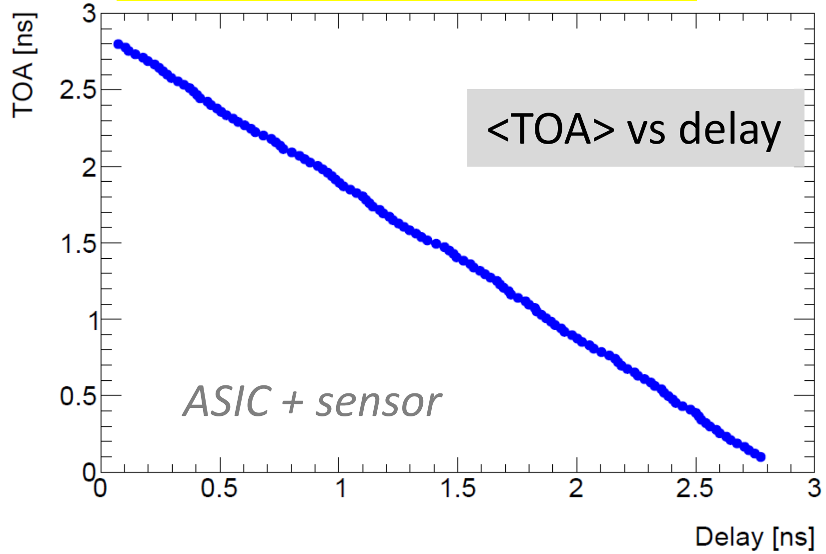
One pixel layout



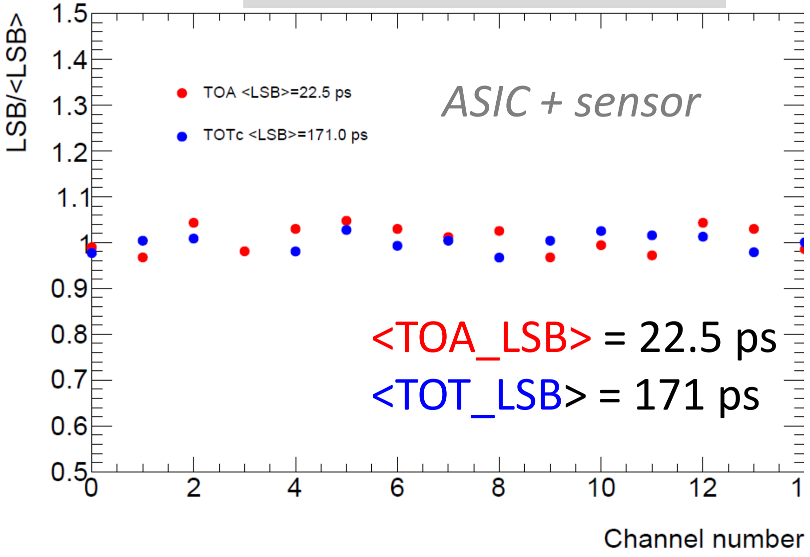
VPA: Voltage preamp
TZ: Transimpedance preamp

ALTIROC1_V2 - TDC performance

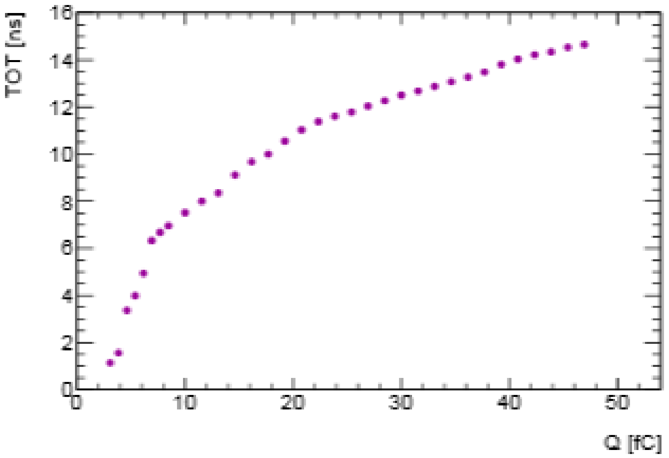
Specifications:
TOA: 20 ps ± 10%, range 2.5 ns



LSB /<LSB> vs channel



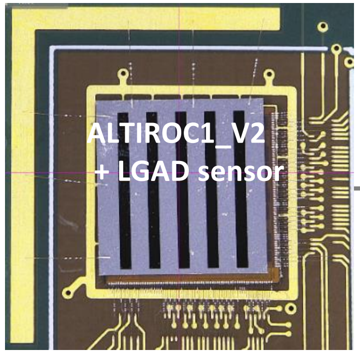
Specifications:
TOT: 160 ps ± 10%, range 20 ns



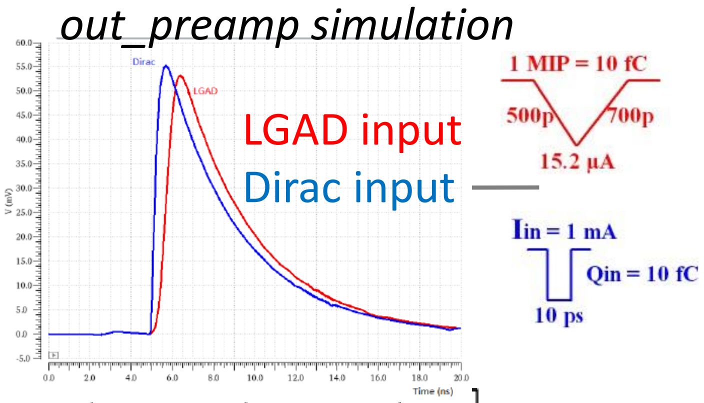
- TOA_LSB and TOT_LSB can be adjusted to 20 ps and to 160 ps (respectively) using per channel Slow Control parameters
- Some of the DLLs don’t lock properly => use of external R to set control voltages of the TDC
- <TOA> vs delay: Small discontinuities due to LSB bin size that can be calibrated with Random Programmable Generator

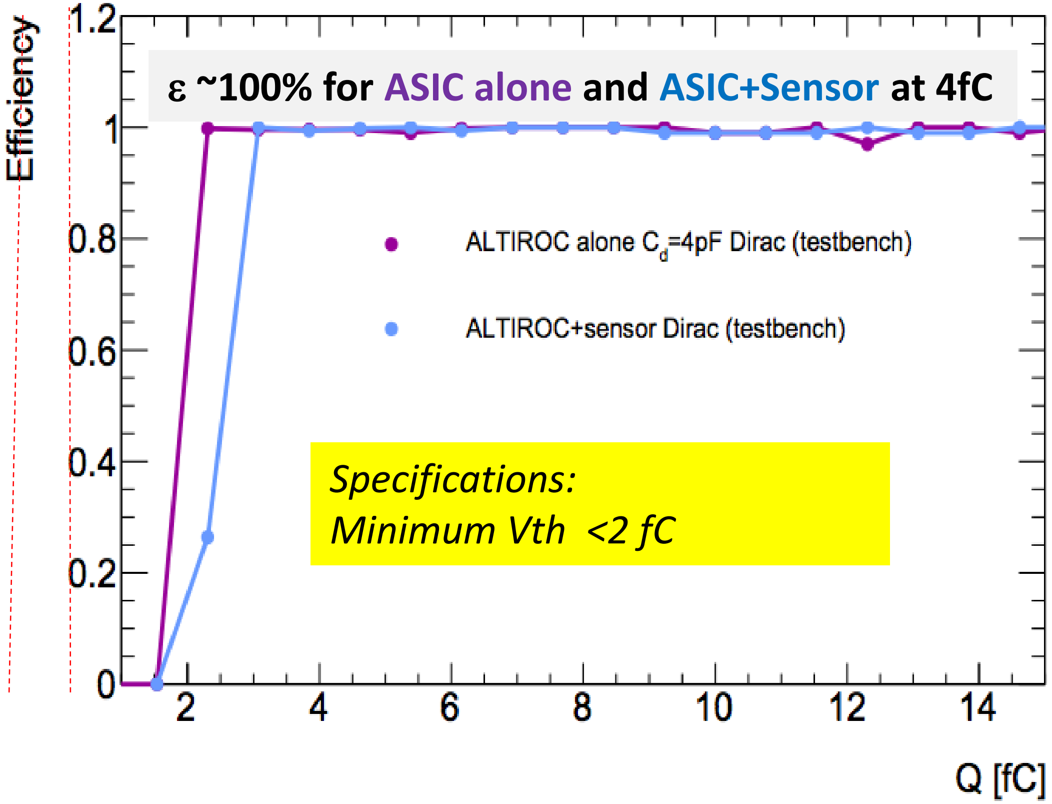
=> Altiroc1_V3: integrates a Random Programmable Generator

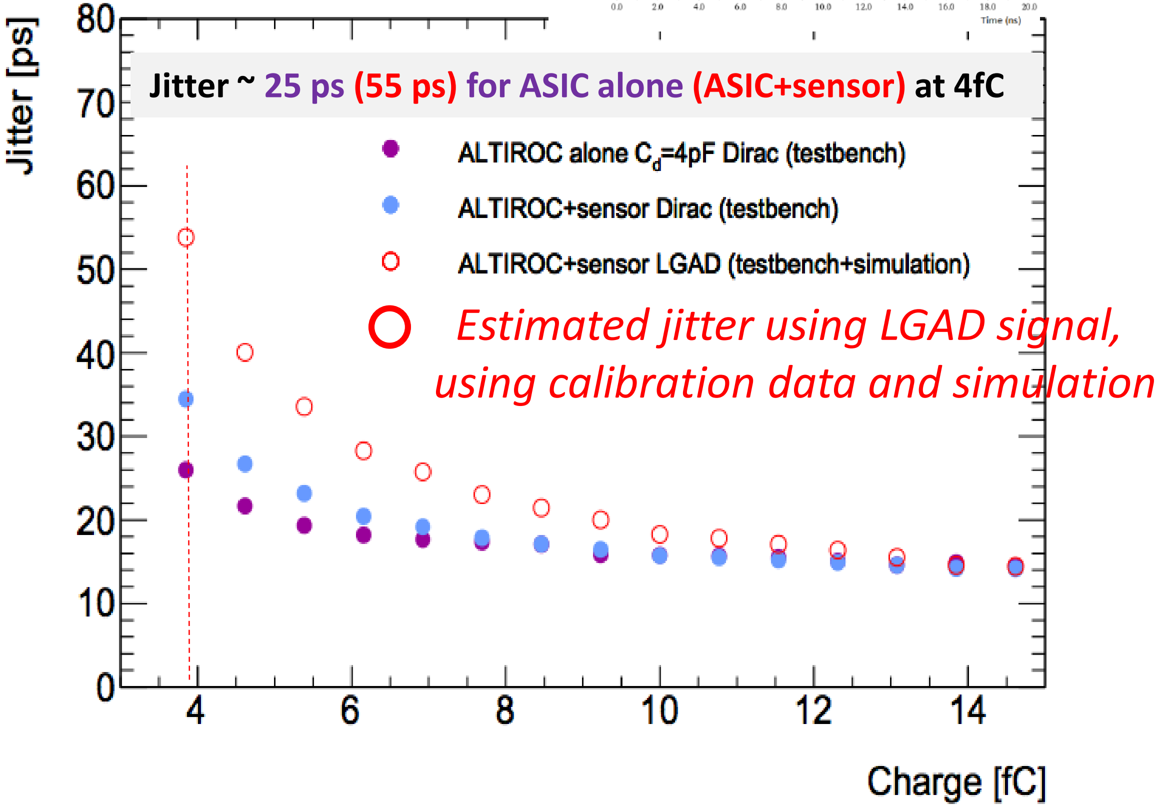
ATLAS
HGTD



ALTIROC1_V2- performance at system level







HGCROC2 : CMS HGCAL readout chip

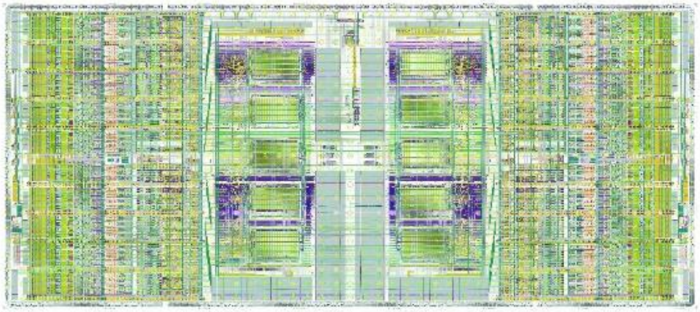
Overall chip divided in two symmetrical parts
- 1 half is made of:
  - 39 channels: 18 ch, CM0, Calib, CM1, 18 ch (78 channels in total)
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

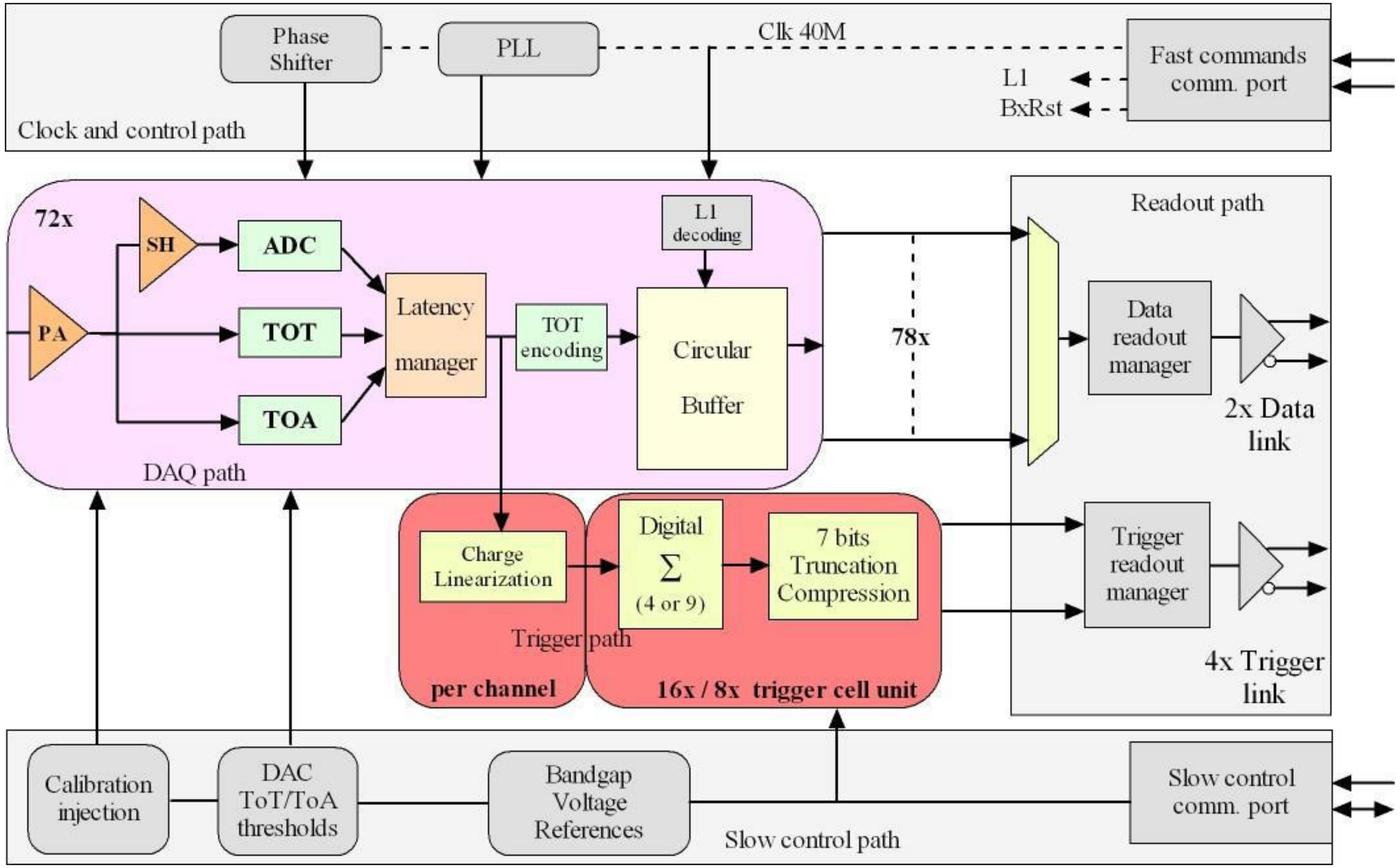
Measurements
- Charge
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.4 fC resolution. TOT: 2.5 fC resolution
- Time
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

Two data flows
- DAQ path
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links

Control
- Fast commands
  - 320 MHz clock and 320 MHz commands
  - A 40 MHz extracted, 5 implemented fast commands
- I2C protocol for slow control

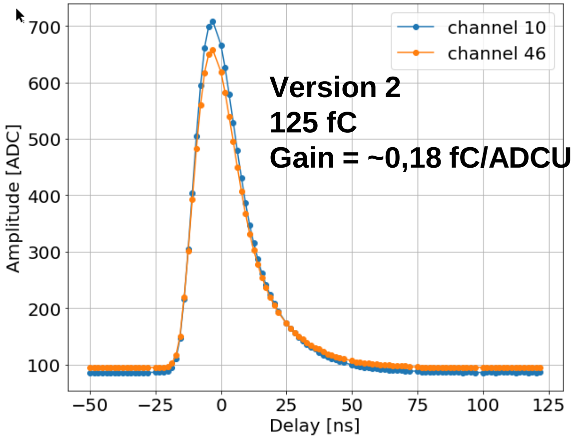
Ancillary blocks
- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain



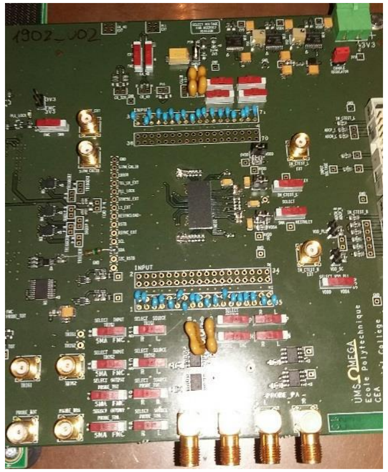


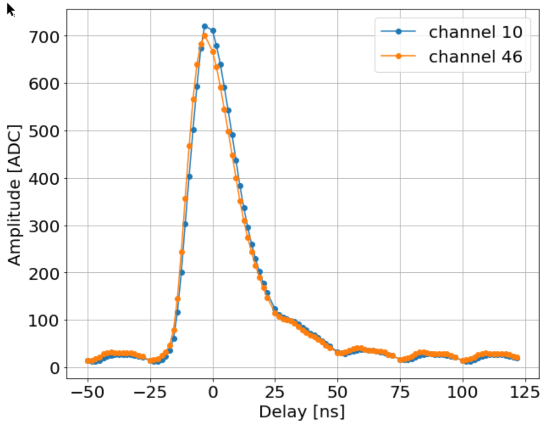
Test boards and signal

Flip-Chip on mezzanine

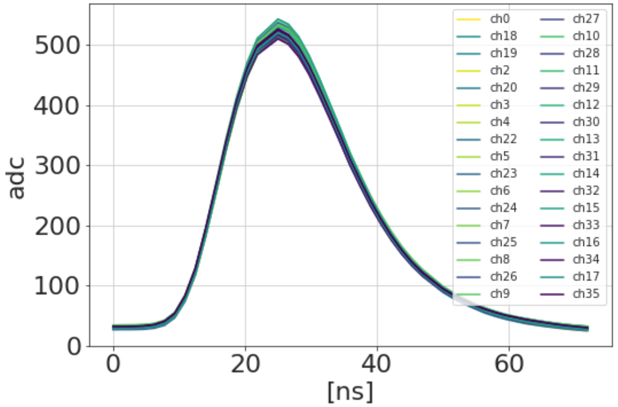


HD BGA board





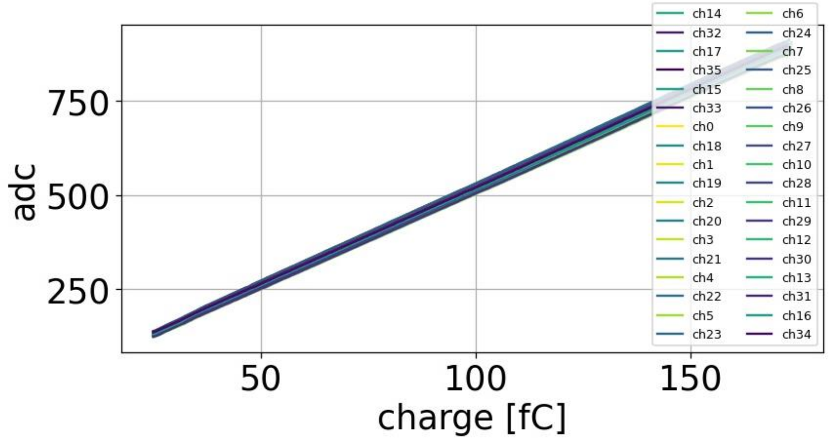
HD BGA on mezzanine

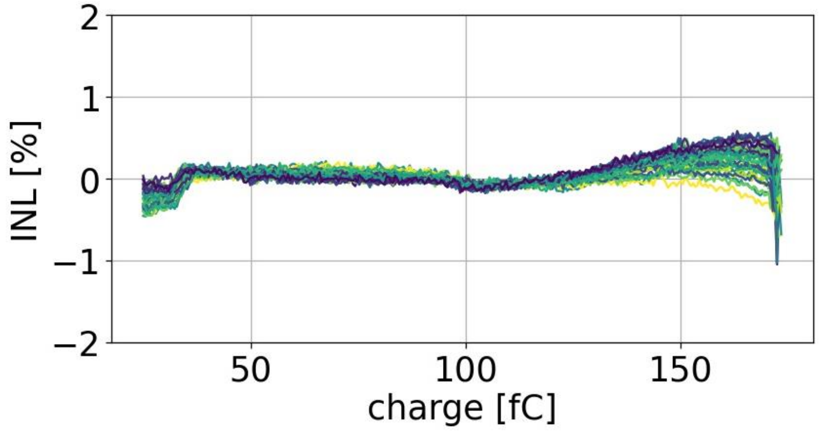


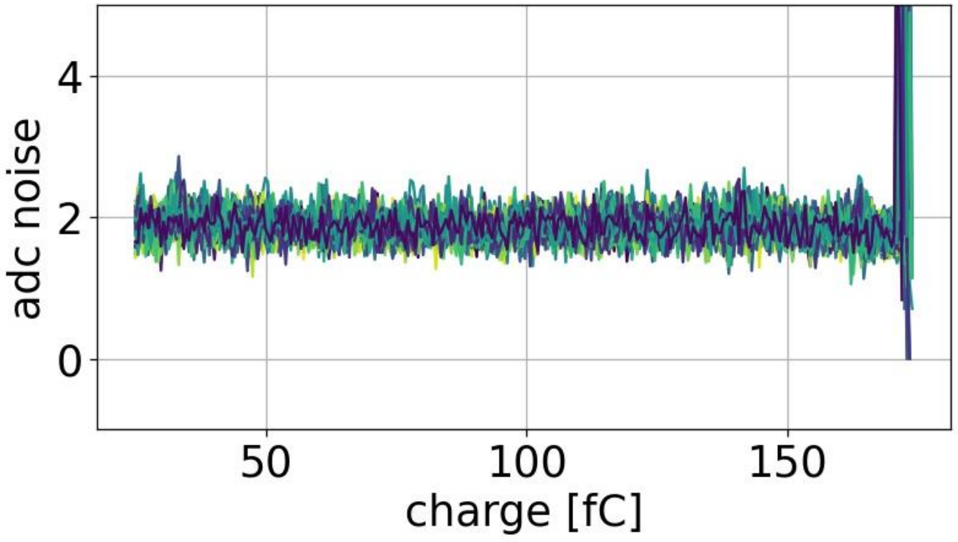
- Separates effects from the BGA substrate and PCB
- Rising time (10-90 %): ~ 15 ns
- Falling time (10-90 %): ~ 30 ns, < 20 % at BX+1
- Good uniformity over the channels
- Digital 40 MHz clock coupling on the analog signal on the HD BGA board: digital noise (slide 11)

Charge ADC (0 – 160 fC)

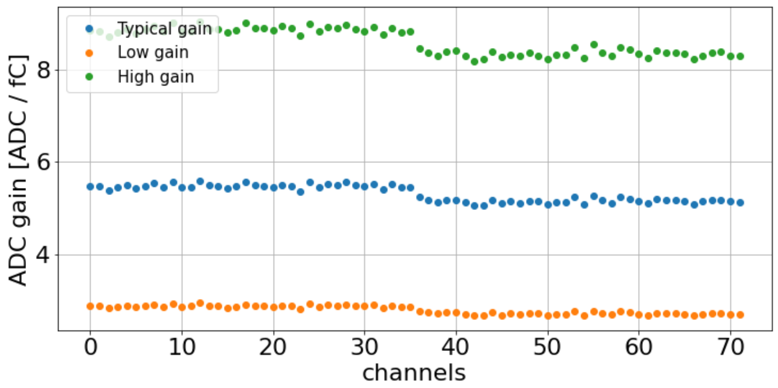
- Two 10b-DAC to globally set the pedestal to a wanted level
- 5b-DAC to reduce dispersion per channel
  - From ~ 100 ADCu dispersion to ~ 5 ADCu
- Good linearity within +/- 0.5%
  - 1.6 fC (~1 MIP) linearity for the typical gain
- ~ 0.3 fC resolution with 50 pF input capacitor







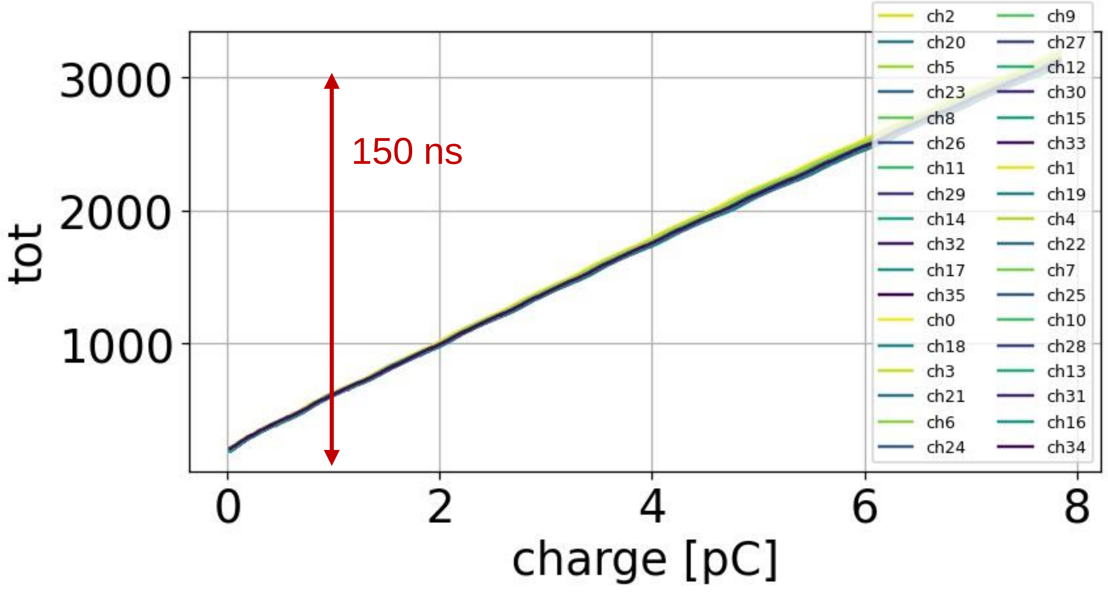
~ 0.3 fC

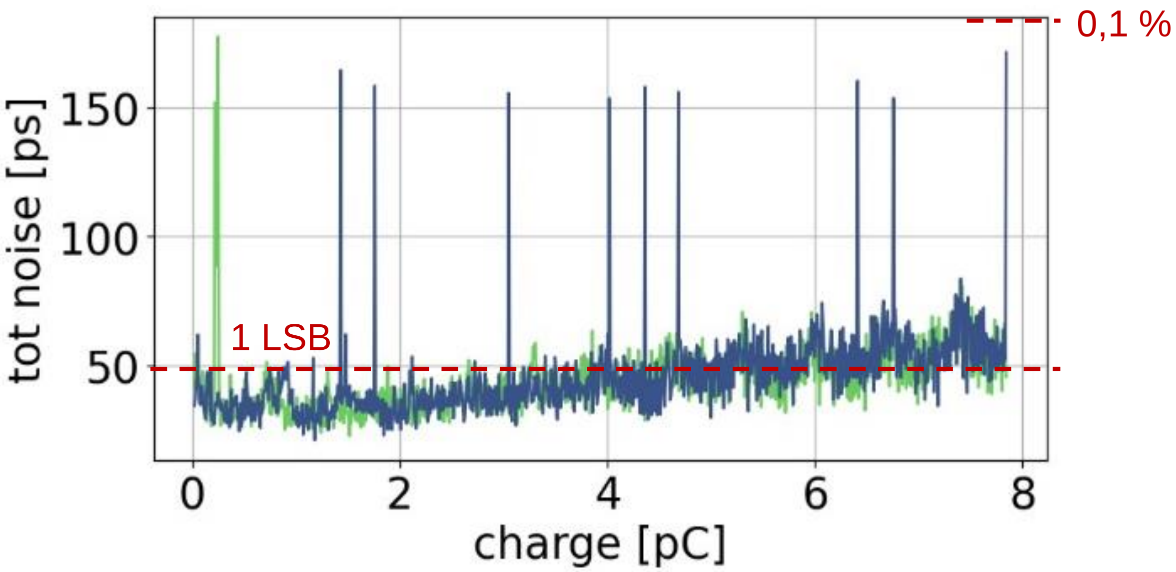


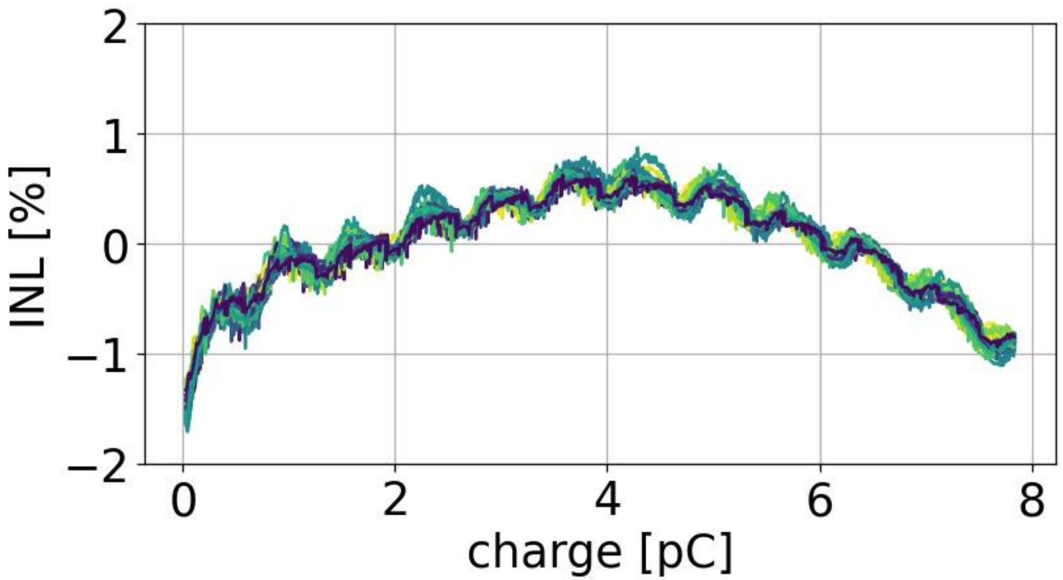
Charge: TOT range (160 fC – 10 pC)

Charge measurement from TOT when preamplifier saturates

- 160 fC to 10 pC (for the typical preamplifier gain)
  - 12 bits over 200 ns
  - 50 ps binning
- Linearity
  - < 2% linearity
  - Better with input capacitor (as expected)
  - Small residual wiggles on TOT due to digital noise on preamplifier input
- Resolution around the LSB (~ 50 ps)
  - Some peaks due to outliers (understood and fixed)







Noise

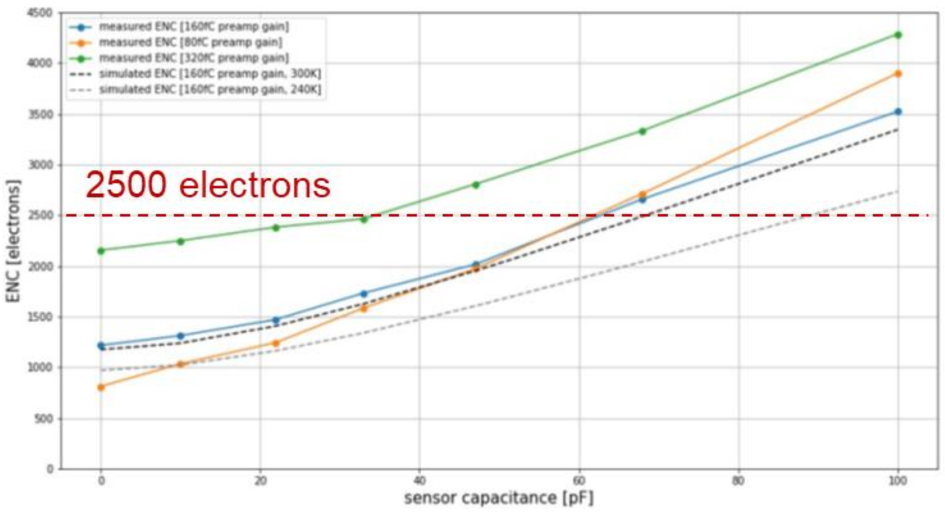
- Measured noise with 50 pF input cap = 0.3 fC (~ 2000 electrons) (0.7 nV / √Hz)
- Very low correlated noise contribution: ~ 0.1
- Coherent noise extracted by comparing direct and alternate sums on n channels (n = 72):

$$DS = \sum ped[i] \; ; \; AS = \sum(-1^{i})ped[i]$$

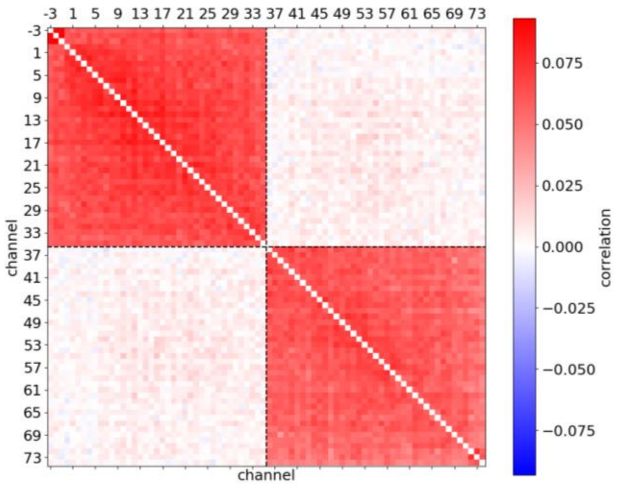
  - Incoherent noise $IN = rms(AS)/\sqrt{n}$
  - Coherent noise CN = $\sqrt{var(DS) - var(AS)}/n$

	0 pF Cdet	47 pF Cdet	68 pF Cdet
High gain ENC	900 electrons	2000 electrons	2750 electrons
Typical gain ENC	1250 electrons	2000 electrons	2700 electrons
Low gain ENC	2200 electrons	2800 electrons	3400 electrons
TOA FOM (1)	NA	2.5 ns/fC (FlipChip) 3 ns/fC (BGA)	3 ns/fC (FlipChip)
TOA noise floor (1)	20 ps	25 ps (FlipChip) 25 ps (BGA)	25 ps (FlipChip)
TOA Time-Walk	0.8 ns (FlipChip) 4 ns (BGA)	2.5 ns (FlipChip) 6.5 ns (BGA)	4 ns (FlipChip)

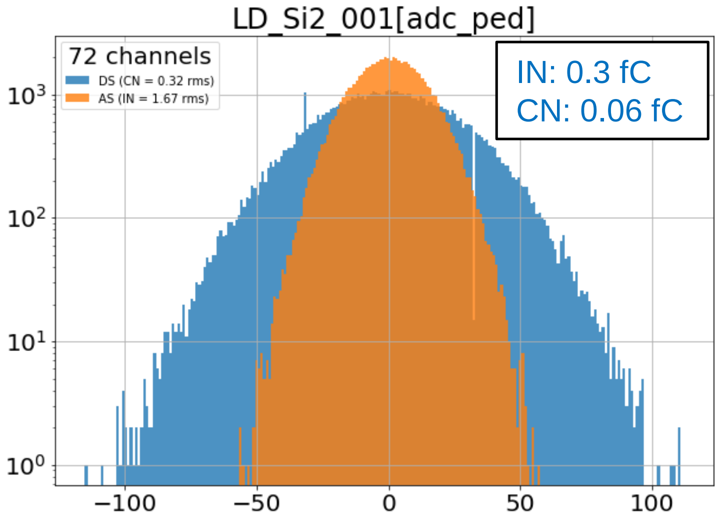
Equivalent Noise Charge wrt. sensor capacitance



Correlation matrix

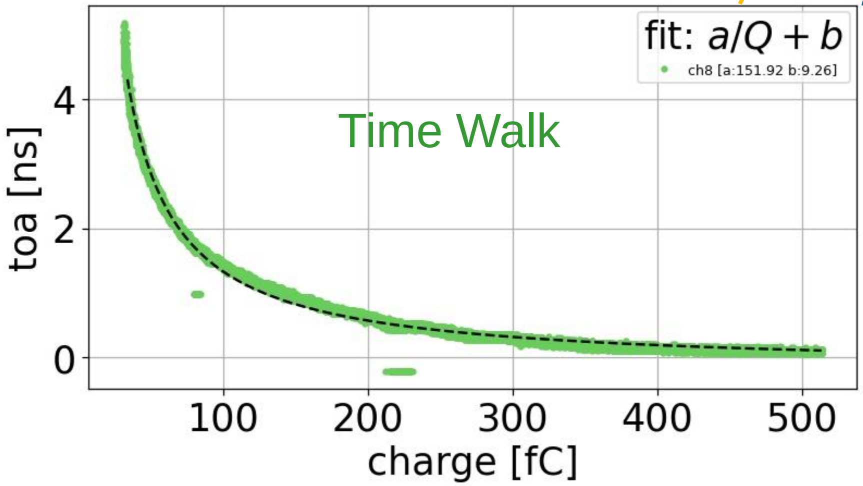


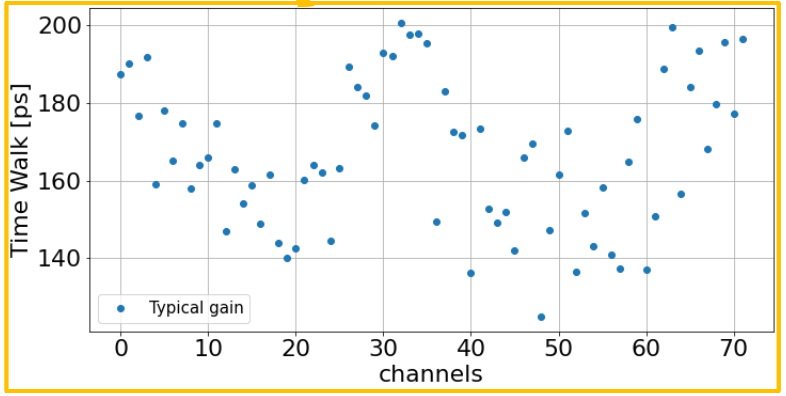
Coherent vs. incoherent noise

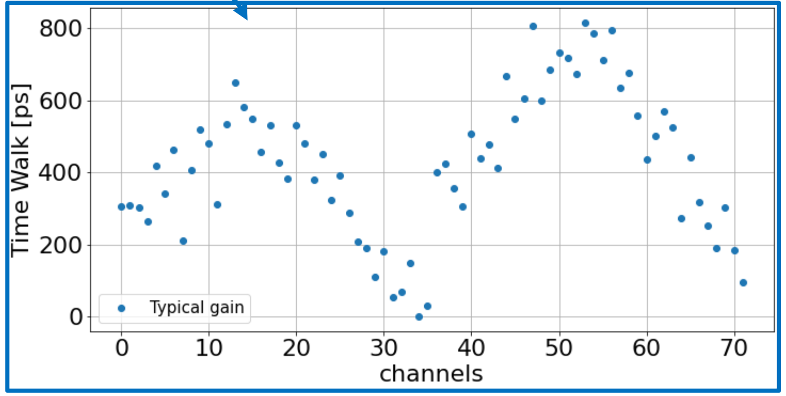


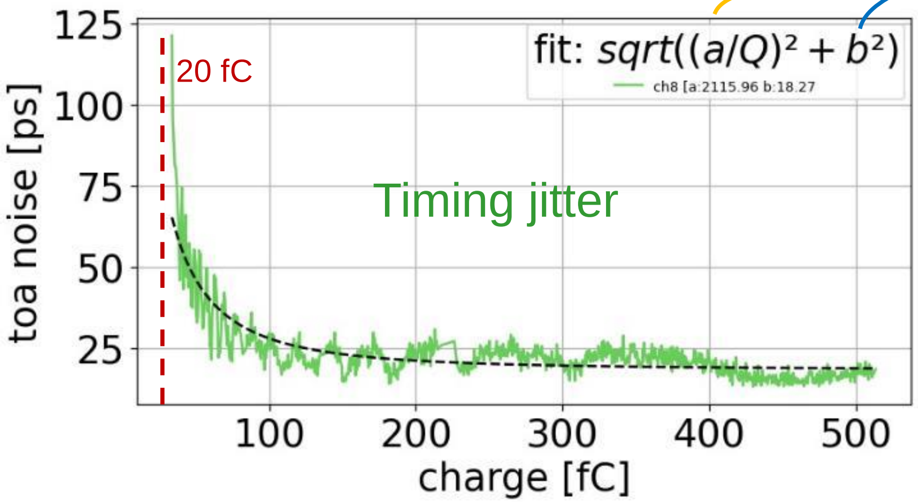
Timing performance

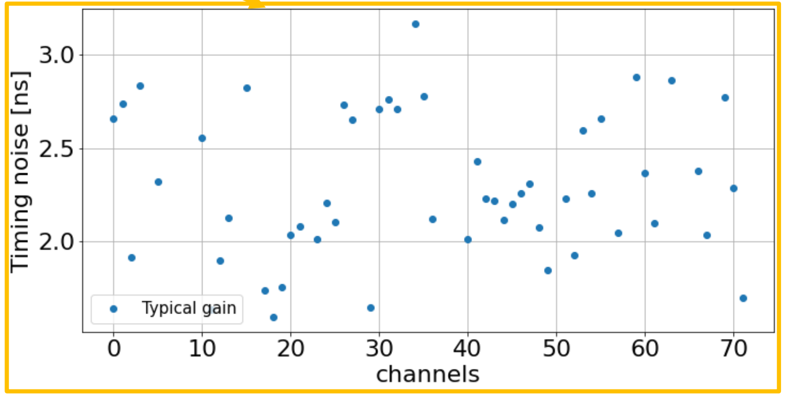
- Minimum Charge providing a TOA measurement is 20 fC, limited by the digital coupling
- $Time\ Walk = \frac{170\ [ps]}{Q\ [fC]} + 400\ [ps]$: 2.5 ns w/o detector cap., ~ 5 ns with 50 pF input capacitor
- $Jitter = \frac{2[ns]}{Q[fC]}\ (+)\ 22\ [ps]$

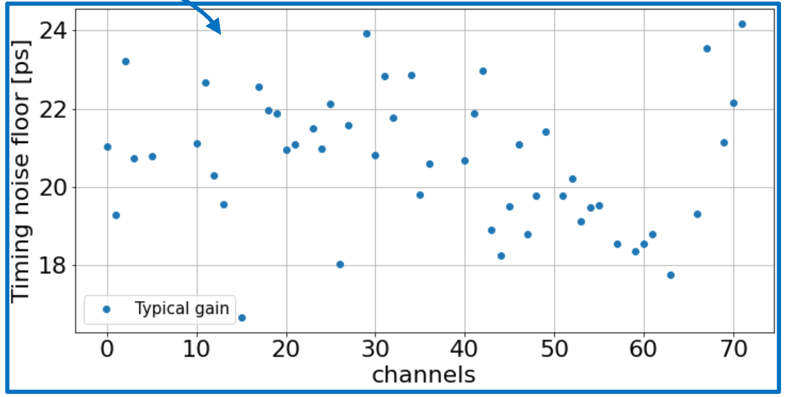






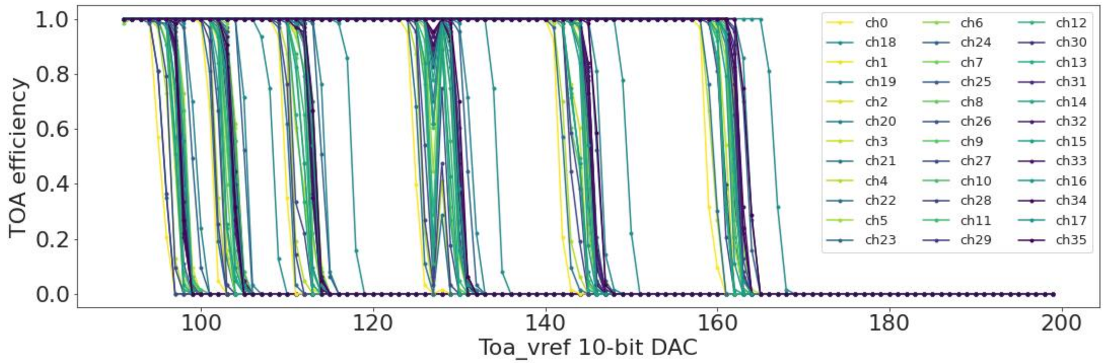


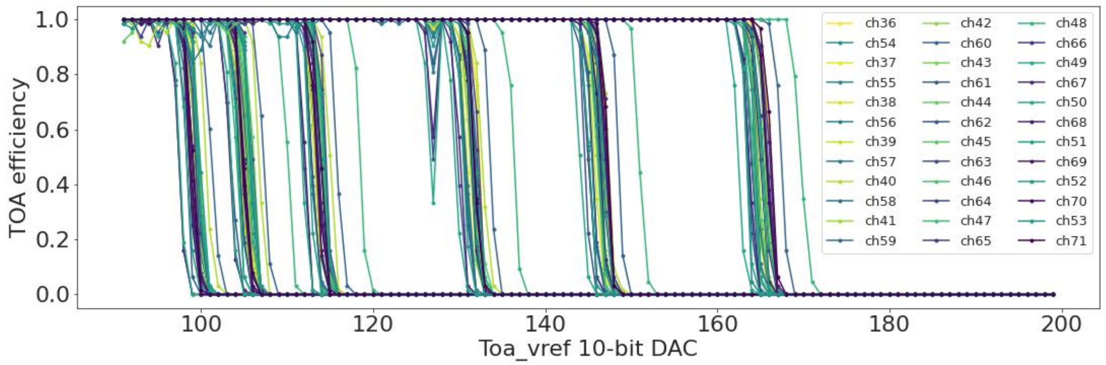


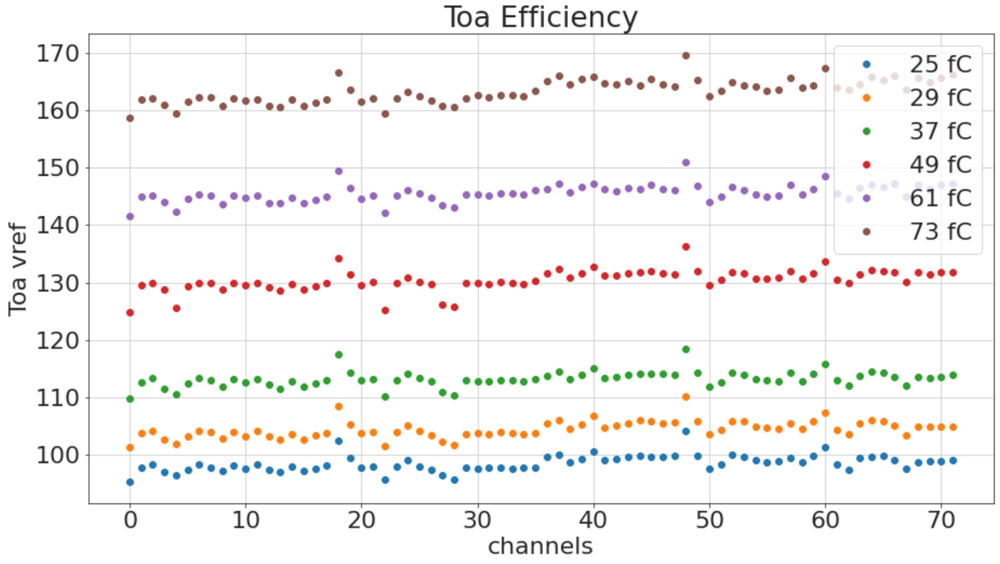


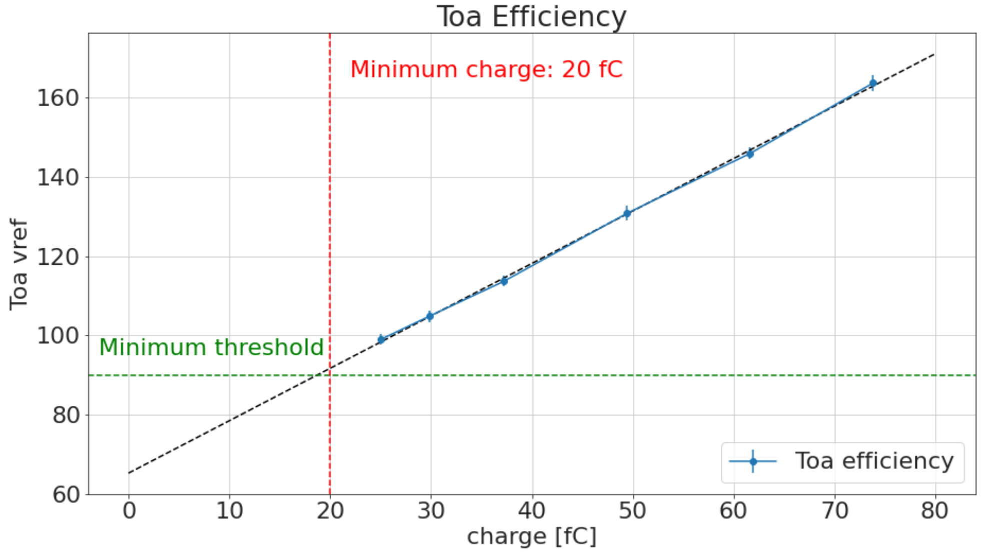
Timing performance – S-curve

- S-curves show the ToA efficiency as a function of the charge
- Minimum charge providing ToA events is 20 fC
  - Limited by the digital coupling



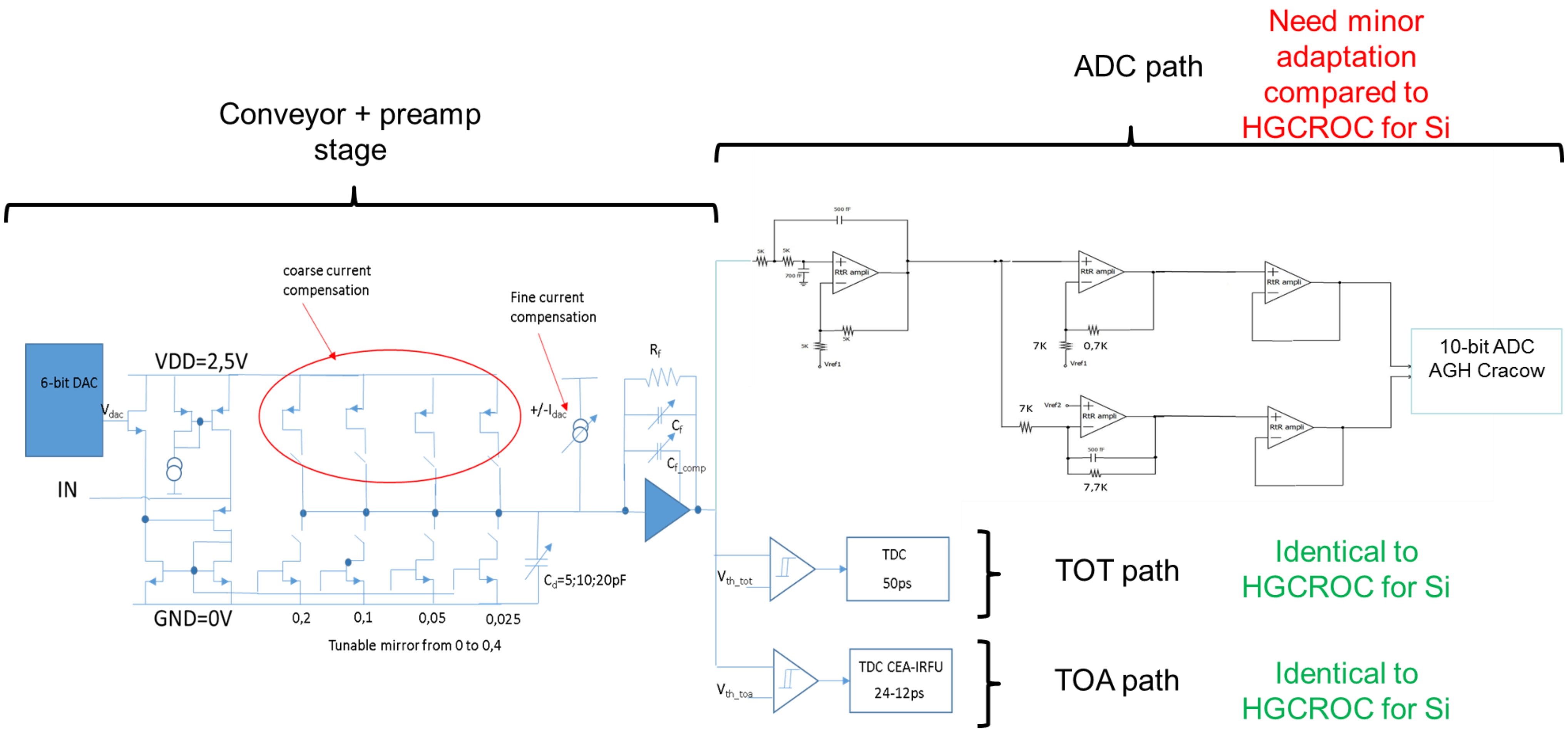






Analog Channel Overview: SiPM version

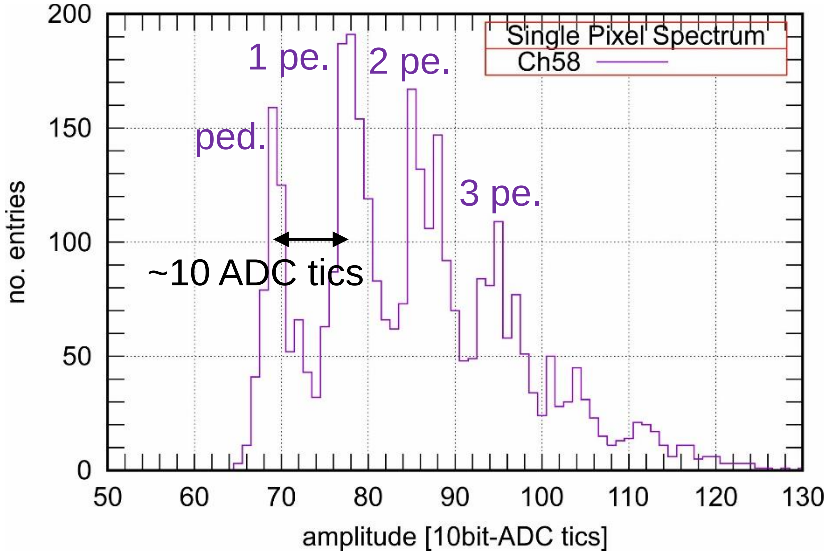
- H2GCROC2 (SiPM version) = HGCROC2 + input current conveyor
  - Heidelberg university design
- 2.5 V input stage for overvoltage adjustment

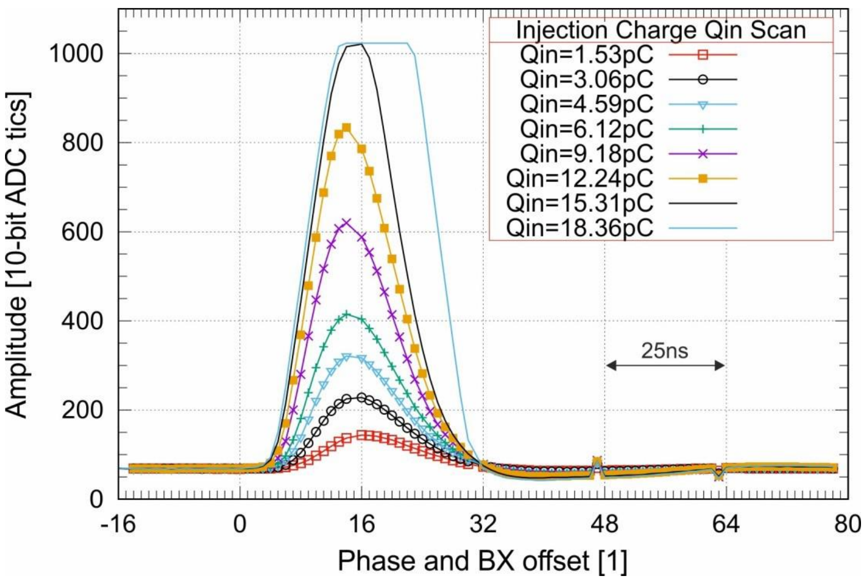


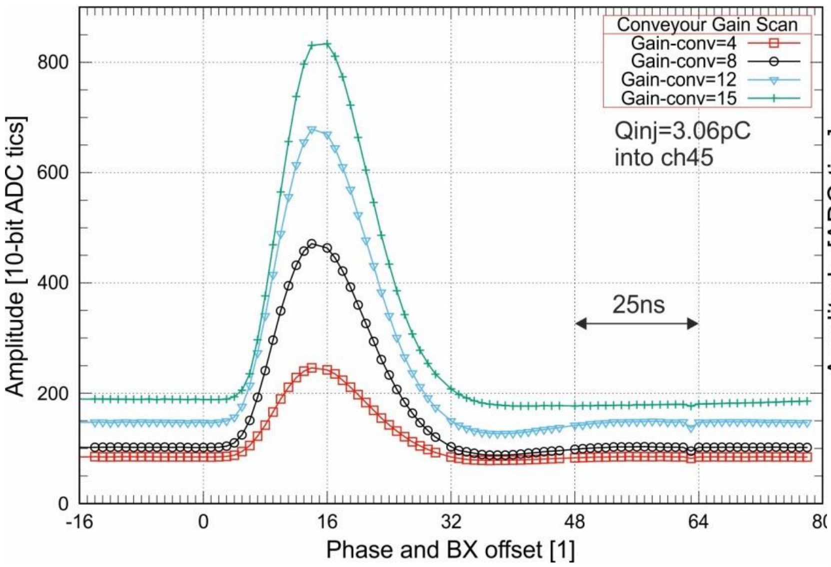
H2GCROC2 measurements:

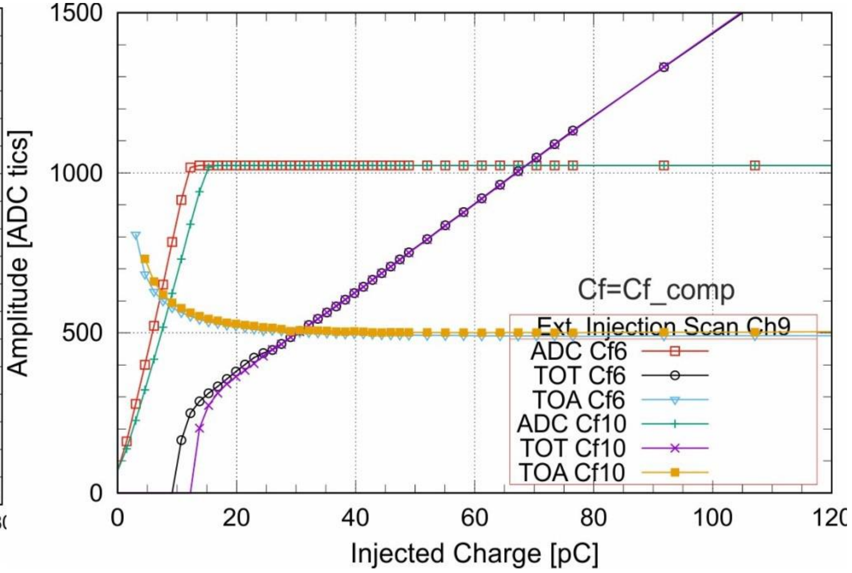
- Good shape as expected
- Adjustable conveyor gain
- Dynamic range as expected: TOT (12bit) – 300pC aimed

- Single-Photon Spectra (SPS):
  - 4V overvoltage, conveyor gain = 12
  - Gain: ~ 10 ADC counts









Conclusion

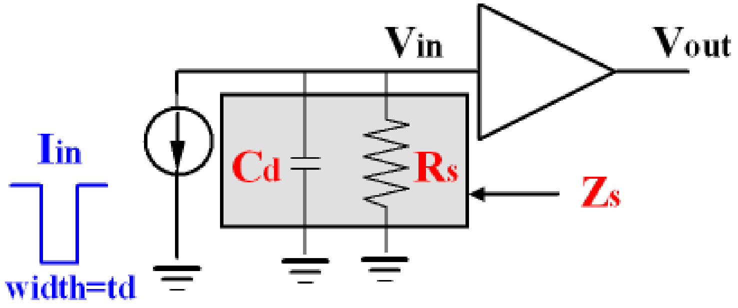
- Lots of interest for ~10 ps timing resolution
- Most of our work (so far) focused on Si, LGADs and SiPMs
- Studies of PETIROC and LIROC with MGRPCs by Imad et al.

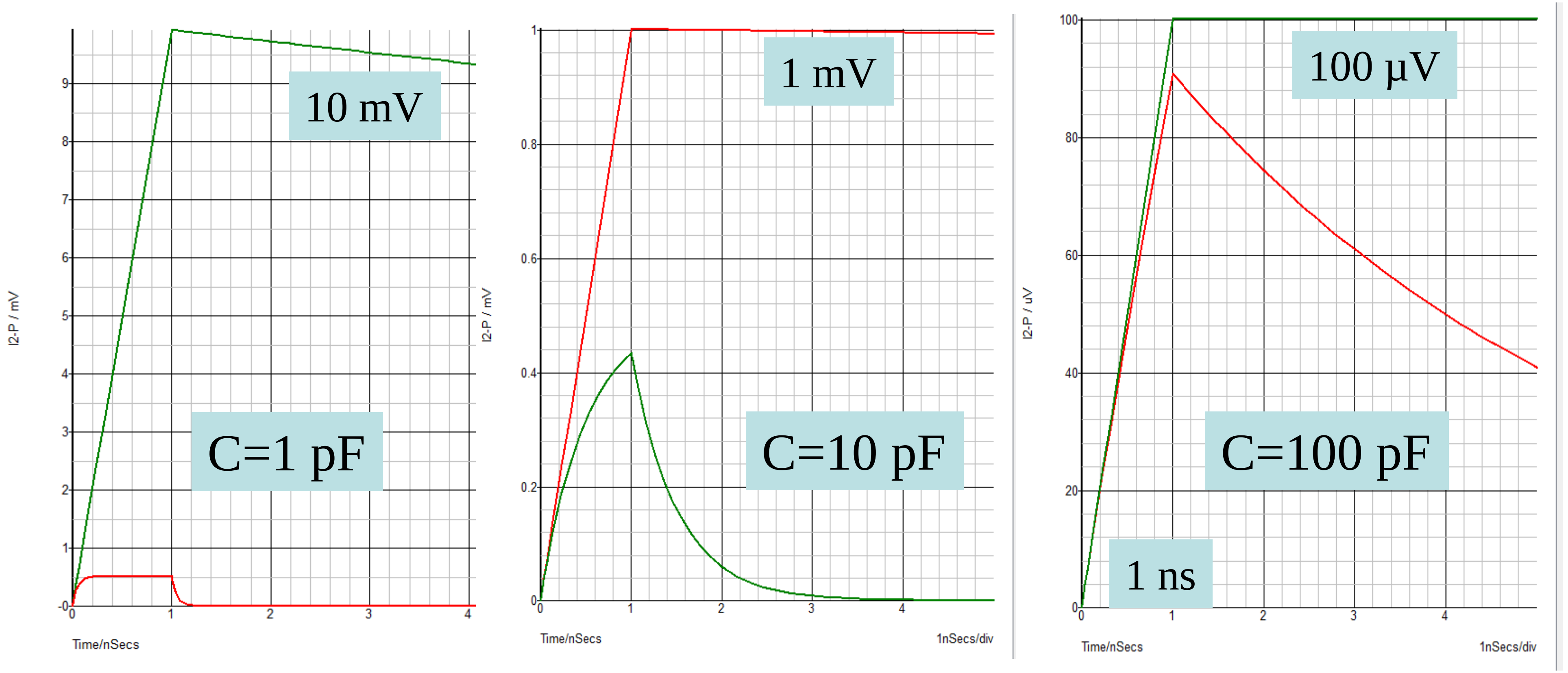
		sensor	polarity	BW	Zin	Cd	TDC	dyn range	FOM	min thresh	"@Cd="
PETIROC	VPA	SiPM/RPC	both	900 MHz	200	10-100 pF	25 ps			1 mV	
LIROC	VPA	SiPM/RPC	both	300 MHz	1k	10-100 pF	no	10fC-100 pC	2 ns/Q (fC)	40 fC	
ALTIROC	VPA/TZ	LGAD	neg	300-800 MHz	2k/200	1-10 pF	20 ps	0.1-50 fC	100 ps/Q(fC)	2 fC	5 pF
HGCROC	TZ	Si	neg	100 MHz	40	10-100 pF	25 ps	0.1 fC-10 pC	2 ns/Q (fC)	20 fC	50 pF
H2GCROC	CC	SiPM	pos	80 MHz	25	100p-1nF	25 ps	10 fC-200 pC			

backup

voltage vs current sensitive

- *Example* : 10 fC – 1 ns => i = 10 uA
- signal from 1-10-100 pF sensors into 50 Ω (current) or 50k (voltage) preamp



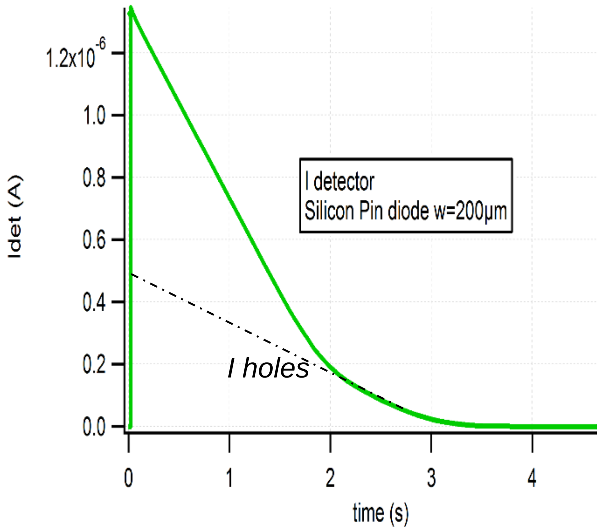


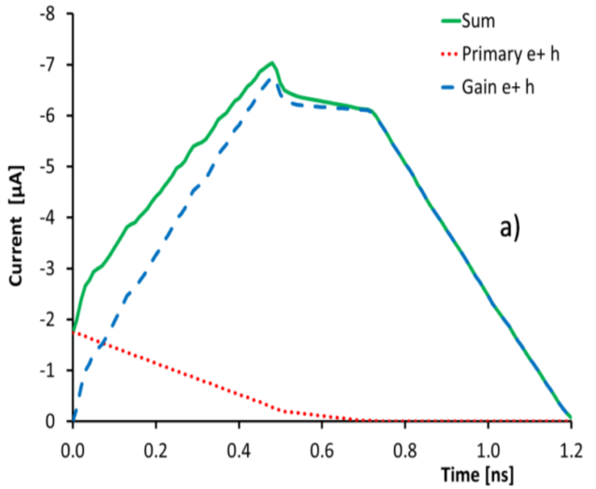
Signal : detector current

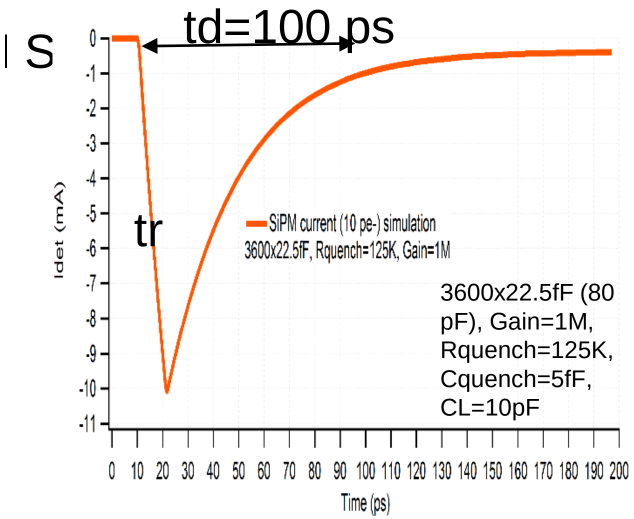
- PN diode w =200µm
- Very short rise time : tr~10ps
- Relatively long «drift time» : td~2ns

- LGAD sensor w =50µm
- rise time : tr~500ps
- Decay time» : td~700ps

- SiPM detector (10pe-)
- very short rise time : tr~10 ps
- Short duration : td~100ps),





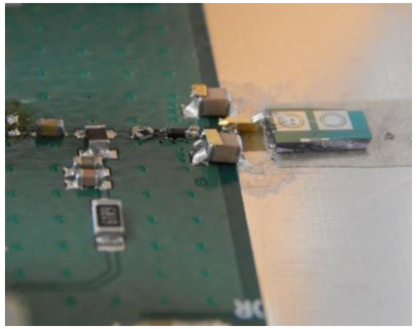


© Harmut Sadrozinski (Santa Cruz) "the beautiful risetime of the detector is spoilt by the electronics"

Examples [measurements from testbeam studies]

$$\sigma_t^J = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

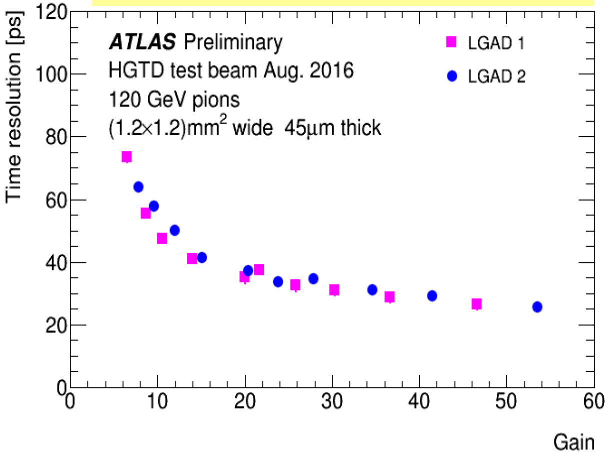
- NA62 tracker : PIN diode thickness 300 µm A=0.09 mm²
  - C_d = 0.1 pF e_n = 11 nV/√Hz t_d = 3 ns σ = 60 ps/Q(fC)
  - 1 MIP = 3 fC => σ = 20 ps/#MIP (~60-200 ps measured)



- CMS HGCAL : PIN diode thickness 300 µm A=25 mm²
  - C_d = 8 pF e_n = 1 nV/√Hz t_d = 3 ns σ = 420 ps/Q(fC)
  - 1 MIP = 3.8 fC => σ = 110 ps/#MIP (~200 ps measured)

- ATLAS HGTD : LGAD diode thickness 50 µm A= 2 mm² G = 10
  - C_d = 2 pF e_n = 2 nV/√Hz t_d = 0.5 ns σ = 50 ps/Q(fC)
  - 1 MIP = 5 fC (G=10) => σ = 10 ps/#MIP (~40 ps measured

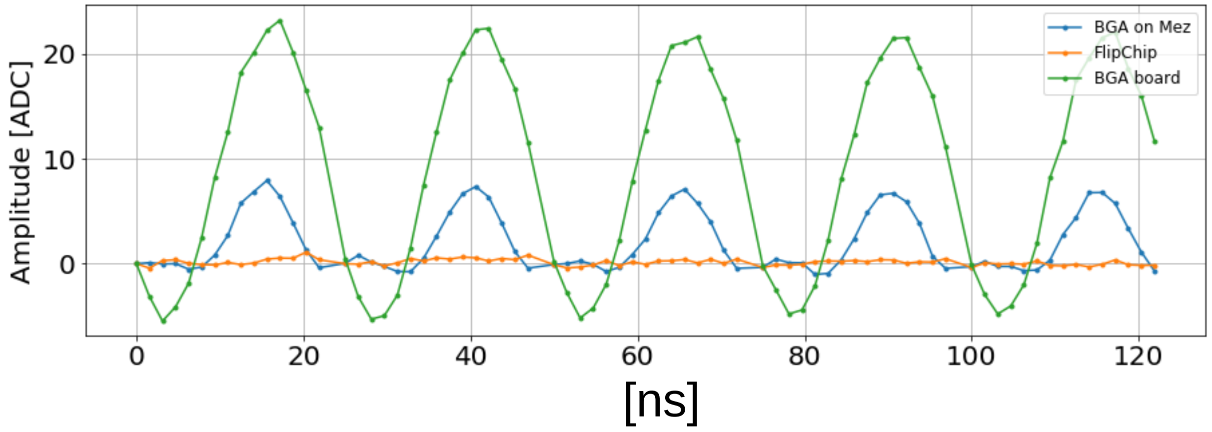
SiGe preamp © N. Spencer (UCSC)



- SiPM G = 1E6
  - C_d = 300 pF e_n = 1 nV/√Hz t_d = 100 ps σ = 3 ns/Q(fC)
  - 1 pe = 160 fC => σ = 20 ps/#pe (~60 ps measured)

Digital noise

- A 40 MHz modulation is visible on the analog signals
  - Comes from digital current spikes on preamp ground node
    - 10 µV on ground give 1 ADC count
  - BGA worse than flip chip
  - BGA substrate optimised, improvements made by optimizing decoupling & the pcb ground impedance
  - Further improved by removing decoupling caps !
    - Reduces digital current spikes (inductance)



- This provides recommendations for the Hexaboard design
  - Very delicate design!