Design of a Front-End ASIC for the New Small Wheel

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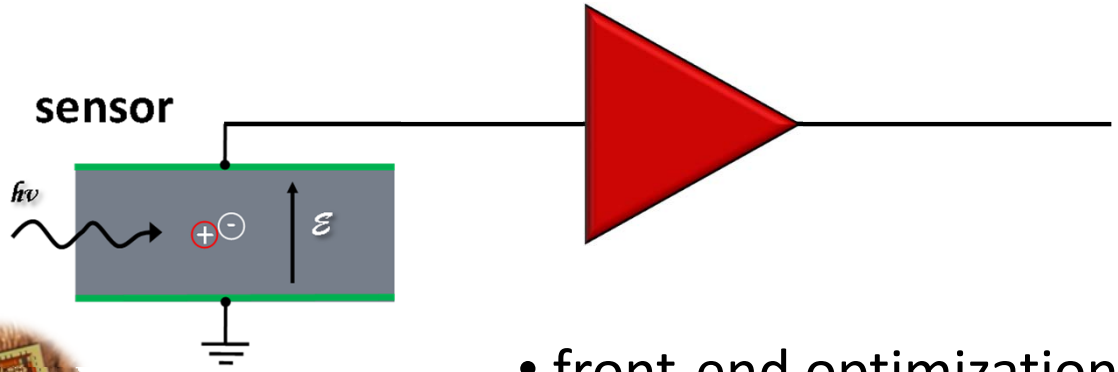
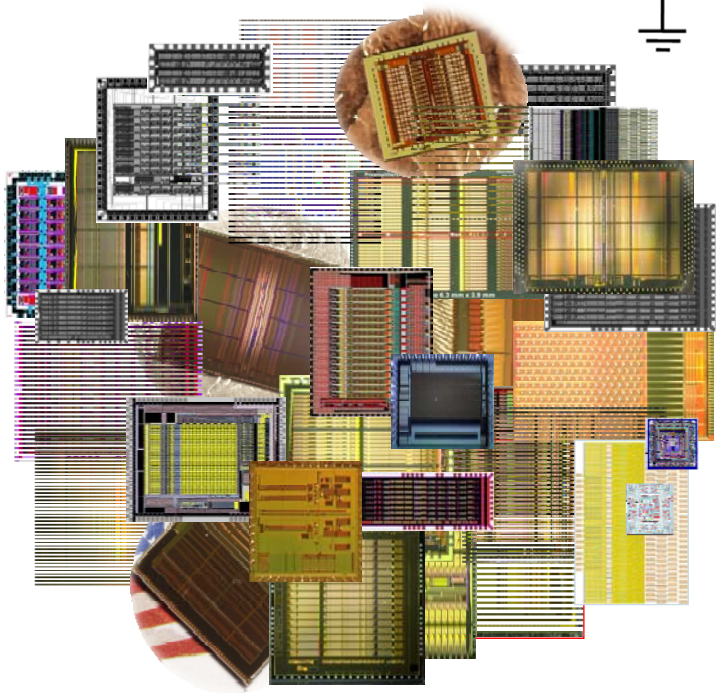
RD51 Collaboration Meeting and Topical Workshop, June 14-18 2021

Outline

- Front-End Design in CMOS
  - input MOSFET optimization
  - reset and charge amplification
- Overview of VMM3a
- Prospects in FE ASIC Design

Front-End Microelectronics

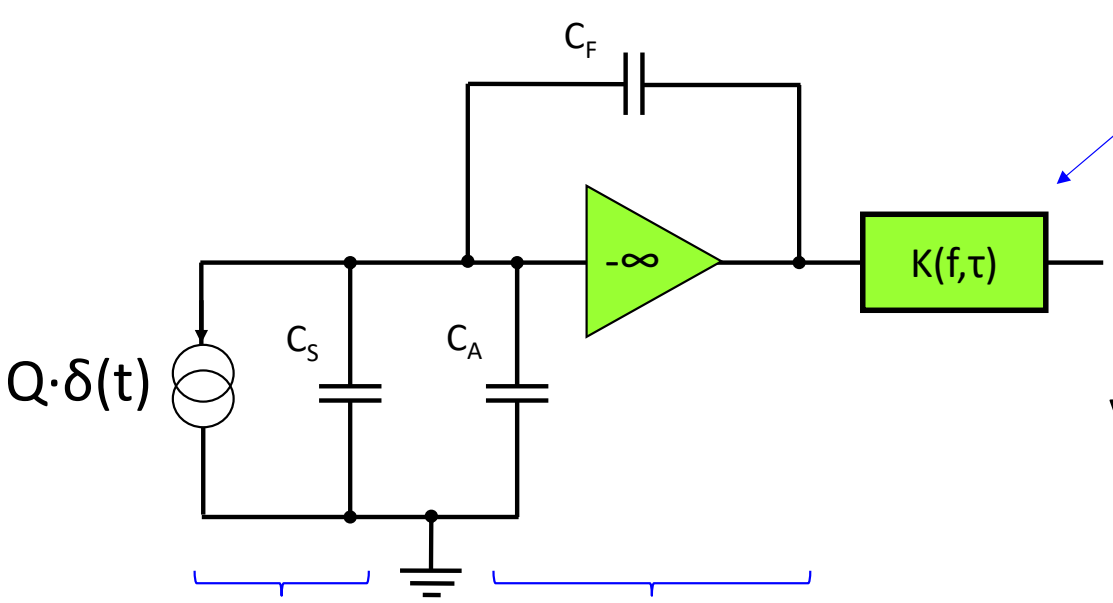




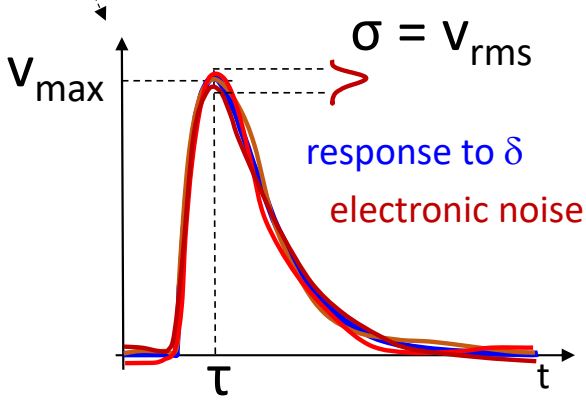
- front-end optimization for resolution
- small physical size, low parasitics
- low power consumption
- high functionality and programmability
- high channel density
- low production cost per channel
- extreme environment

becoming the only option for modern detectors

Charge Amplifier



filter
- time-invariant
- time-variant
- anti-aliasing (DSP)

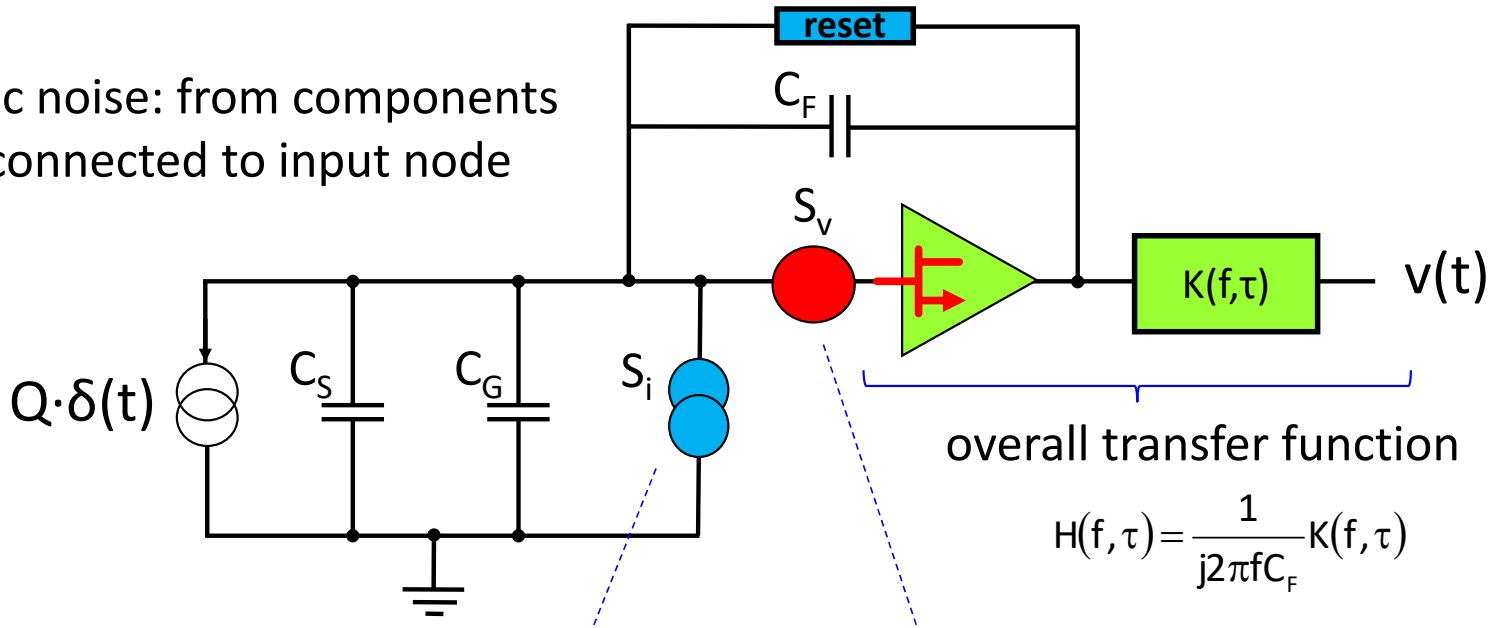


$$\text{gain} = \frac{v_{max}}{Q} \quad [\text{ mV/fC }] \qquad \text{ENC} = \frac{v_{rms}}{\text{gain}} \quad [\text{ fC }] \text{ or } [\text{ electrons }]$$

Equivalent Noise Charge

Noise Sources

Electronic noise: from components directly connected to input node

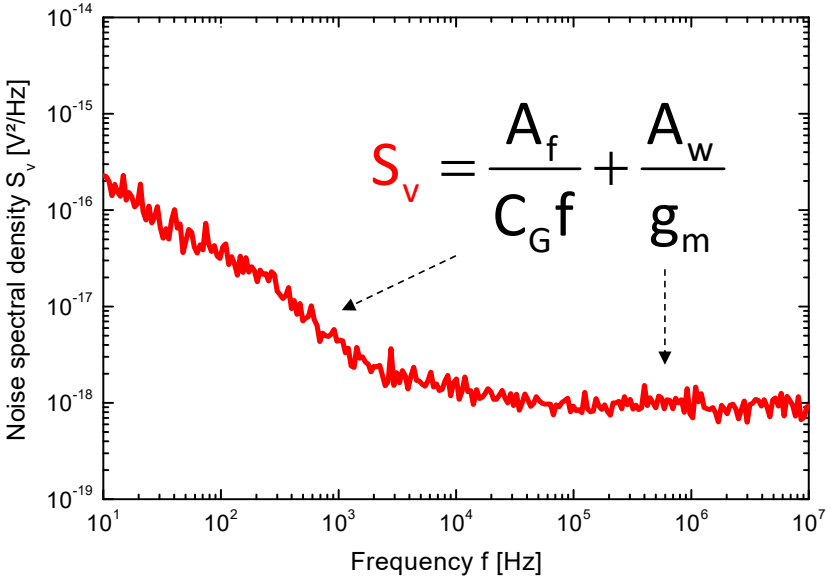


$$H(f,\tau)=\frac{1}{j2\pi f C_F}K(f,\tau)$$

$$ENC^2 \cong \frac{\int_0^\infty S_i\left|H(f,\tau)\right|^2 df + \int_0^\infty S_v\omega^2\left(C_S+C_G\right)^2\left|H(f)\right|^2 df}{\left|h(t)\right|^2_{max}}$$

need minimum 2 poles in H(f,τ)

Input Transistor



C_G = gate capacitance
g_m = transconductance

} proportional to transistor size

transistor sized for
$C_G = C_S$ (capacitive matching)

From S_V : $$ENC_v^2 = a_f A_f \frac{(C_S + C_G)^2}{C_G} + \frac{a_w}{\tau} \underbrace{\frac{A_w}{g_m / C_G}} \frac{(C_S + C_G)^2}{C_G}$$

f_T (max current density)
(depends on V_{GS})

$C_G \rightarrow$ ~ 1fF/µm
$I_D \rightarrow$ ~ 100µA/µm

For C_S=1pF
1mm, 100mA !

Low-Power Input Transistor

white noise contribution $ENC_{vw}^2 \approx \frac{a_w}{\tau} \frac{A_w}{g_m(I_D)/C_G} \frac{(C_S + C_G)^2}{C_G}$

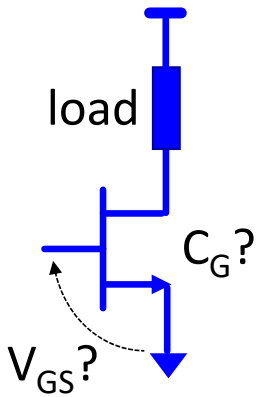
fix power → fix drain current I_D

$V_{GS} >> V_{th}$ (strong inversion)

$g_m(I_D) \approx \sqrt{\frac{2\mu c_{ox}}{n} \frac{W}{L} I_D} \propto \sqrt{\frac{C_G I_D}{L^2}}$

↓

$ENC_{vw}^2 \propto \frac{L}{\sqrt{I_D}} \frac{(C_S + C_G)^2}{\sqrt{C_G}}$



$V_{GS} << V_{th}$ (weak inversion)

$g_m(I_D) \approx \frac{I_D}{nV_T} \propto I_D$

↓

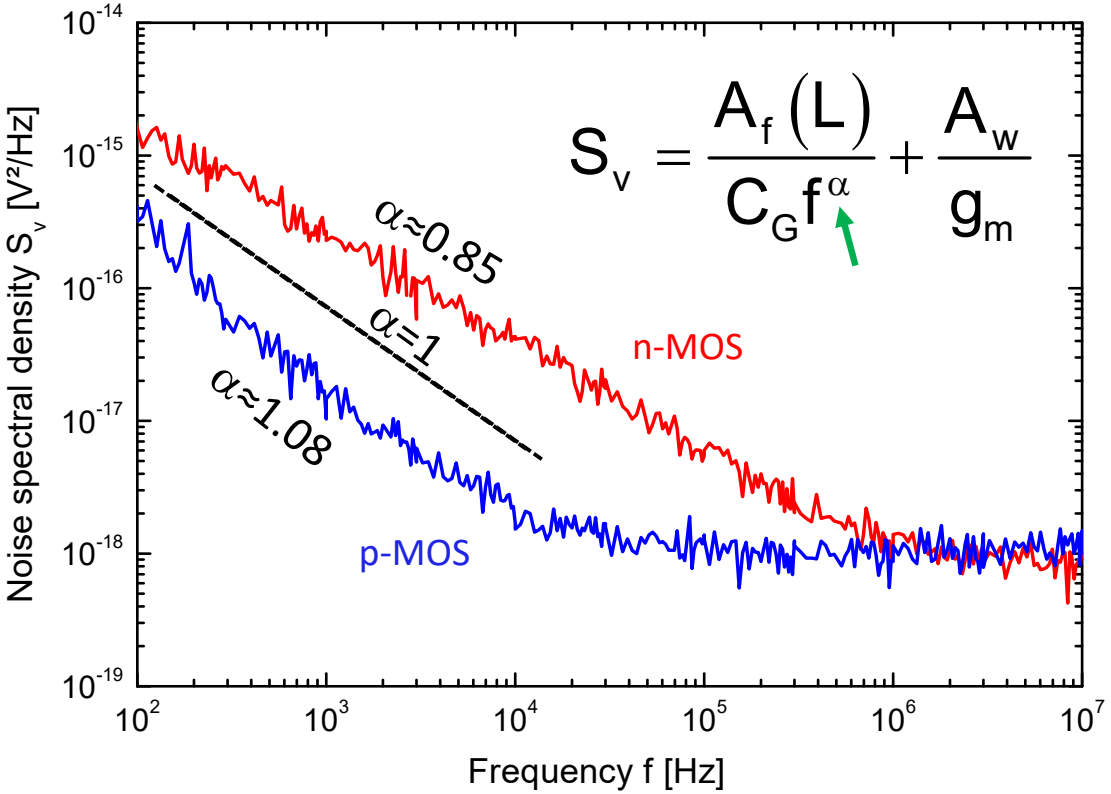
$ENC_{vw}^2 \propto \frac{(C_S + C_G)^2}{I_D}$

- minimum L
- $C_G = C_S/3$

- independent of L
- $C_G = 0$ pushes back towards strong inversion

→ $V_{GS} \approx V_{th}$ (moderate inversion), $C_G << C_S$

Low-Frequency Noise



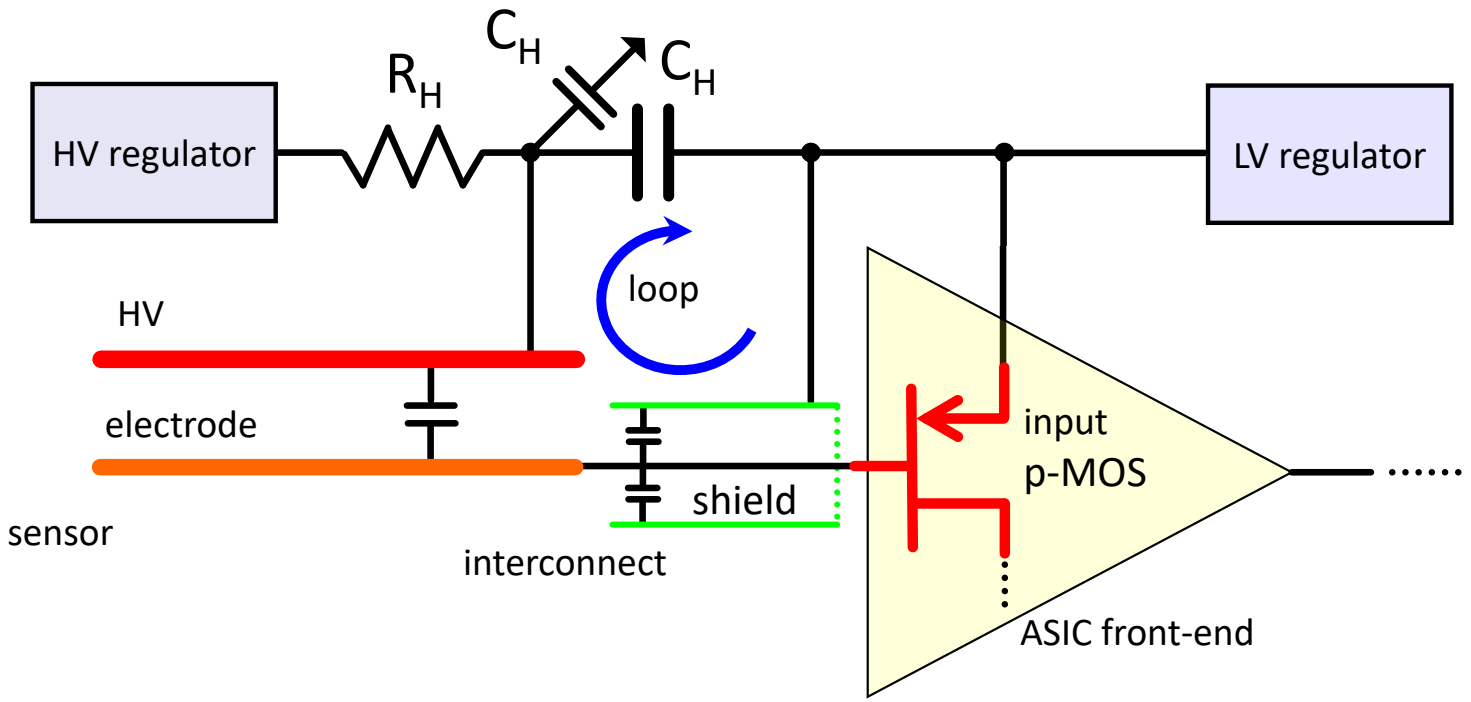
low-freq. noise contribution

$$ENC_{vf}^2 = a_f(\alpha)\frac{A_f(L)}{\tau^{1-\alpha}}\frac{(C_S + C_G)^2}{C_G}$$

depends on τ !

VMM3a → p-MOS, L=180nm, W=10mm, I_D=2mA, C_G=10pF

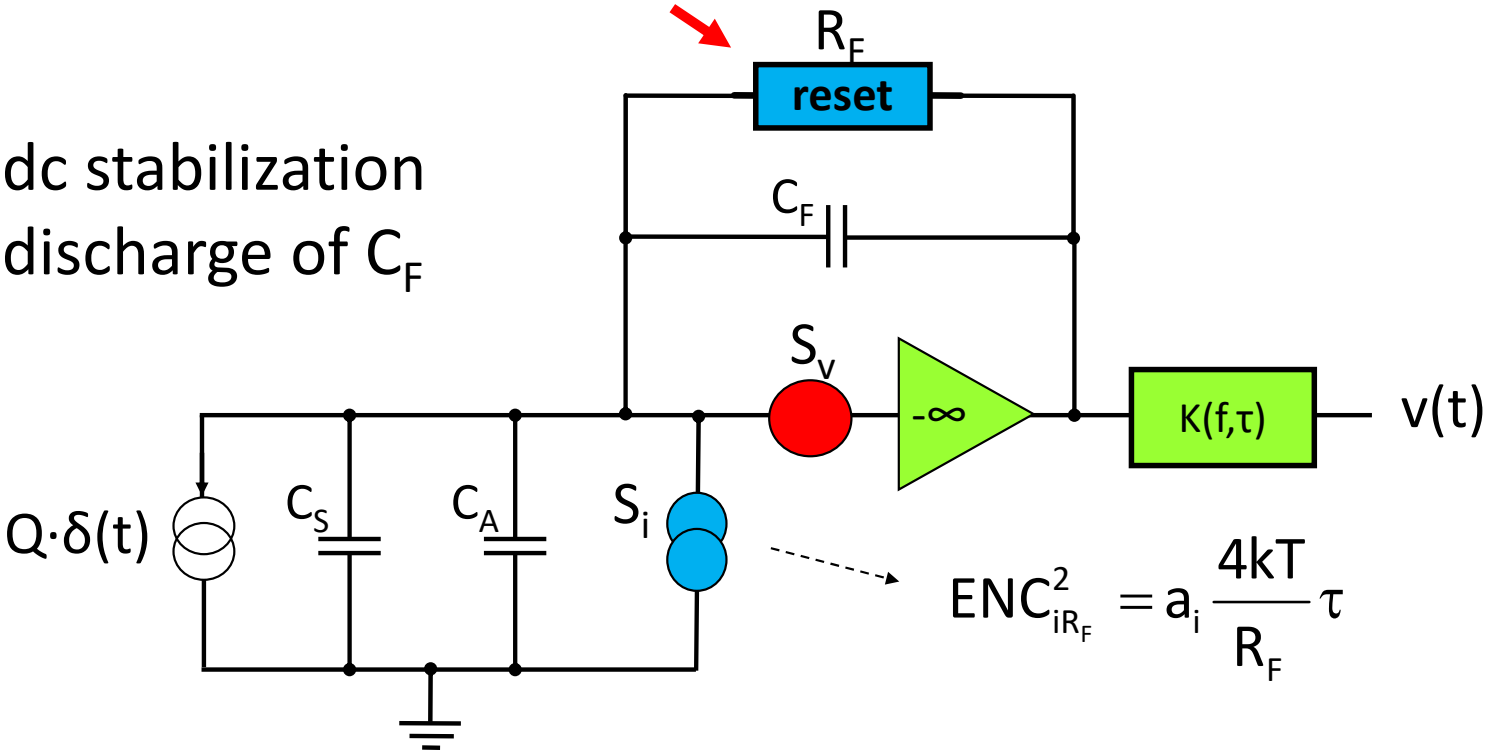
Input Loop with PMOS



- decouple sensor supply to p-MOS supply
- decouple input shield to p-MOS supply
- minimize length and area of input loop

Charge Amplifier "Reset"

- dc stabilization
- discharge of C_F



$$ENC^2_{iR_F} = a_i \frac{4kT}{R_F}\tau$$

$$\frac{4kT}{R_F} << 2qI_S \quad \rightarrow \quad R_F I_S >> \frac{4kT}{2q}(\sim 50mV)$$

"50mV rule"

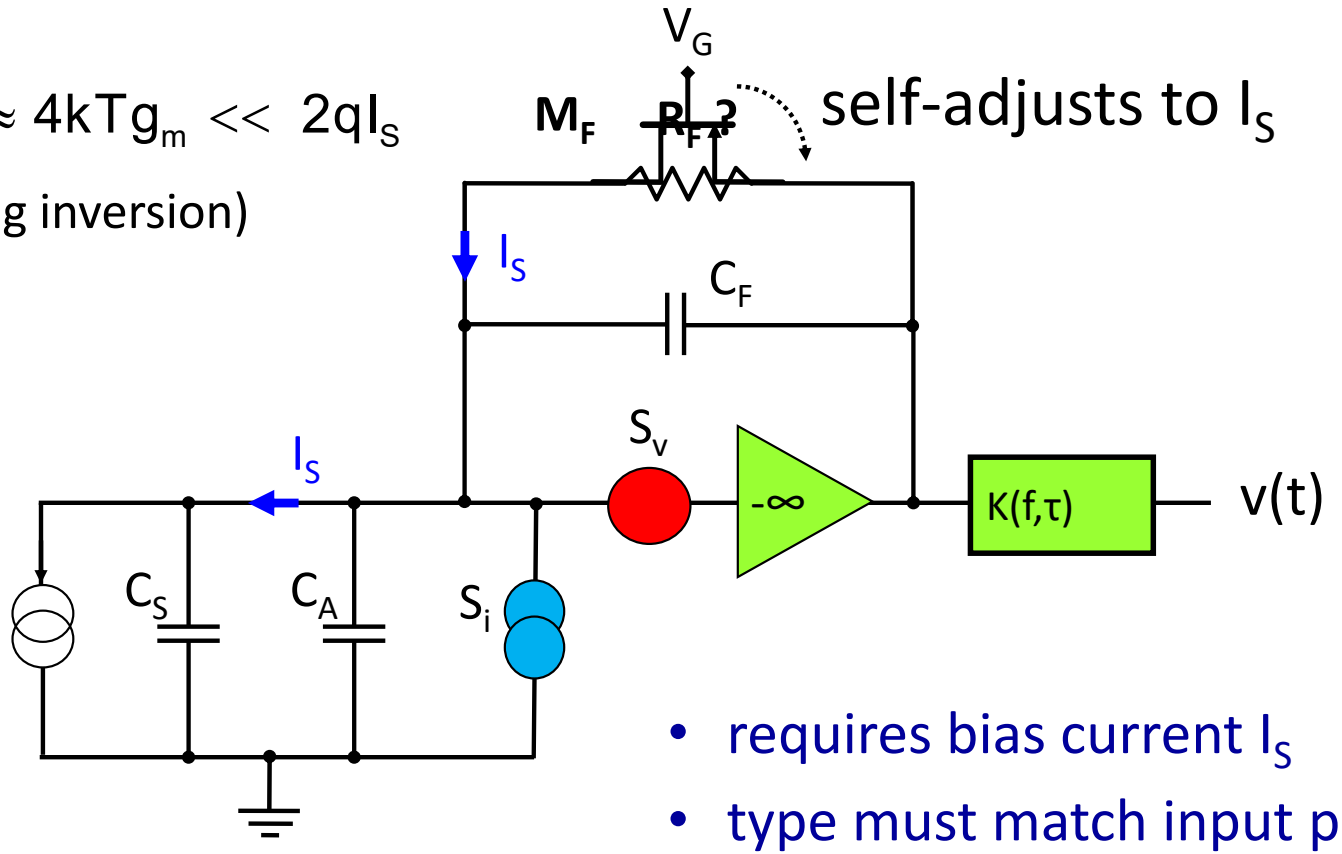
sensor shot noise from leakage current I_S

examples
- CZT: I_S = 1nA → R_F >> 50 MΩ !
- Si: I_S = 1pA → R_F >> 50 GΩ !

Reset in CMOS

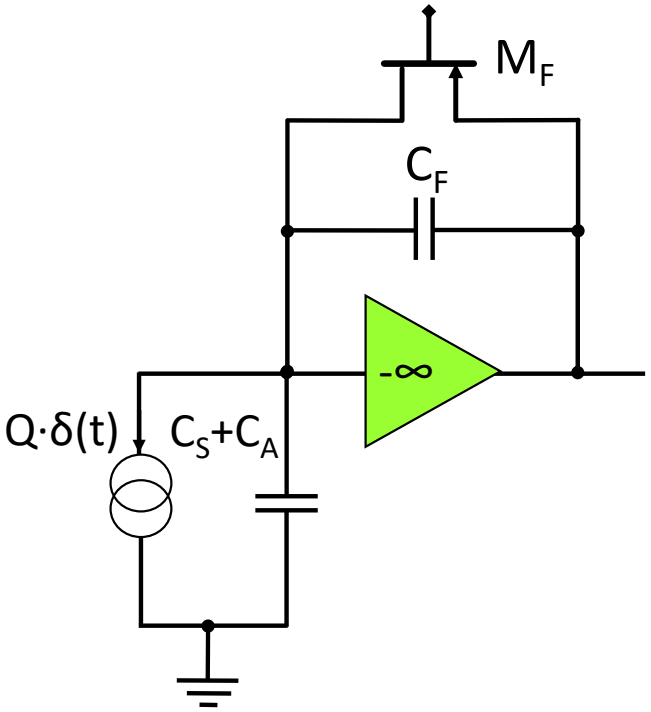
M_F noise: $S_{iM_F} \approx 4kTg_m << 2qI_S$

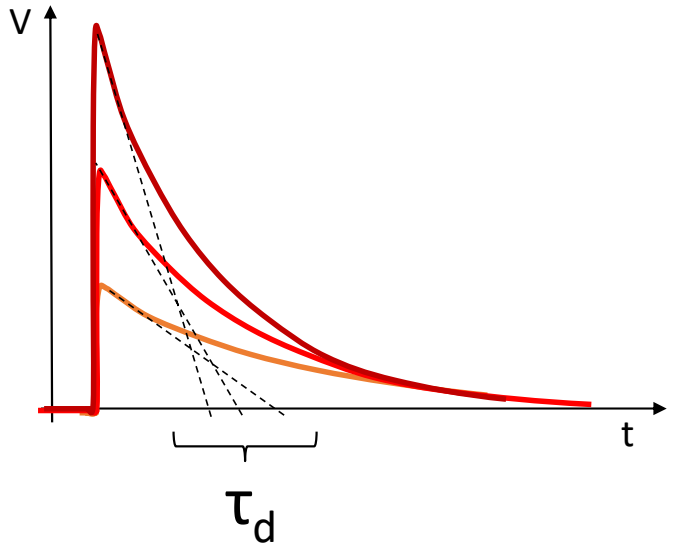
if $V_{GS} >> V_{th}$ (strong inversion)



- requires bias current I_S
- type must match input polarity
- adds noise increase at discharge

Reset Non-Linearity

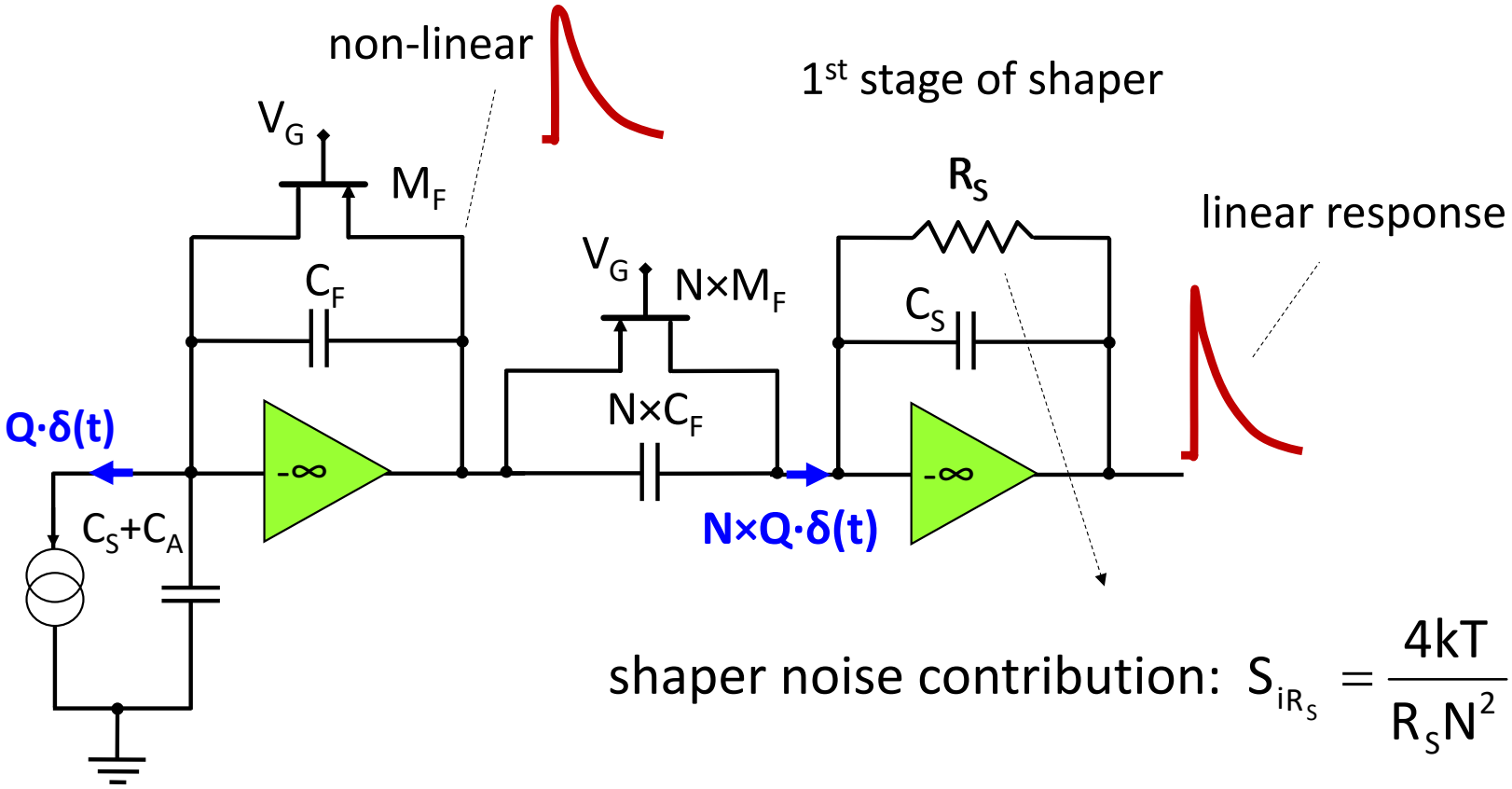




τ_d depends on amplitude and affects linearity

How to realize a linear configuration?

Reset Linearization

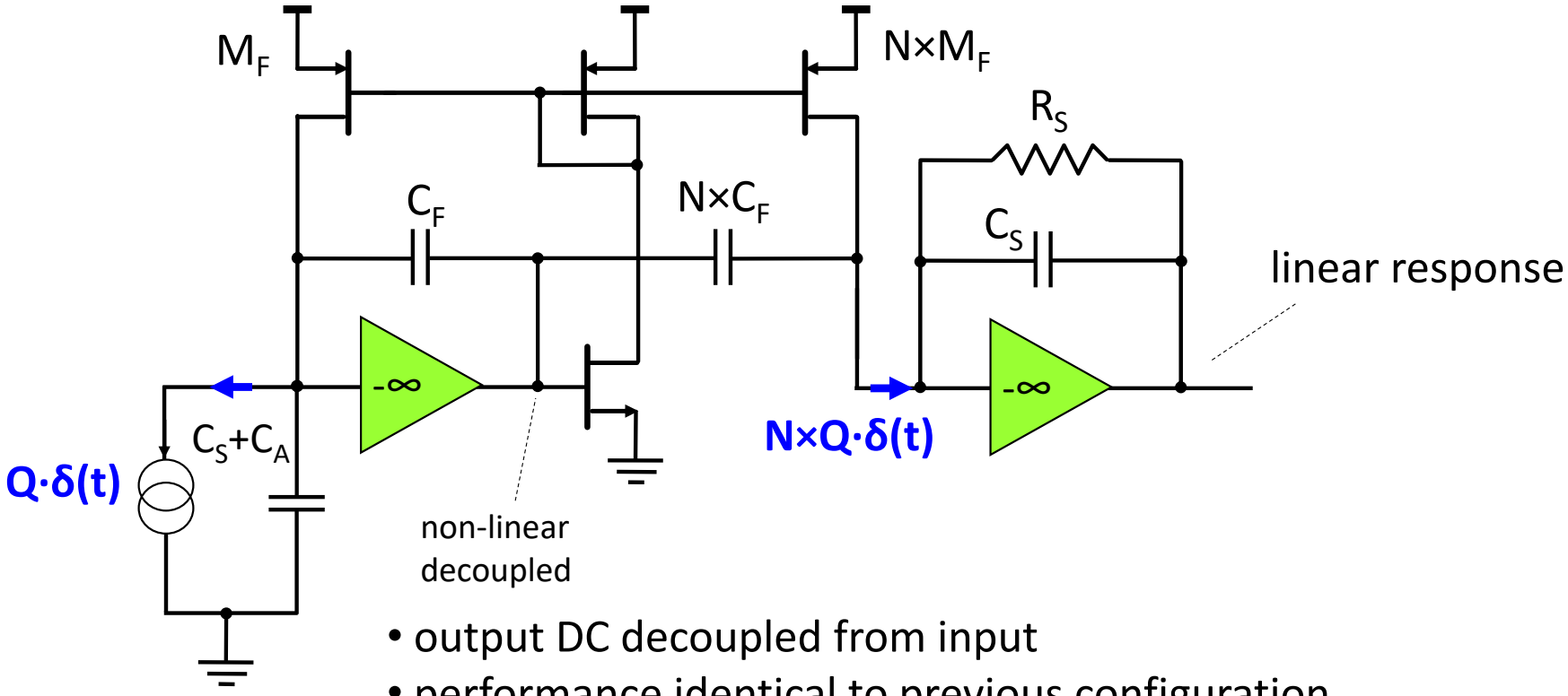


shaper noise contribution: $S_{iR_S} = \frac{4kT}{R_S N^2}$

Effective linear "**charge amplification**" by N

De Geronimo, IEEE TNS 47, 2000

Mirror Reset

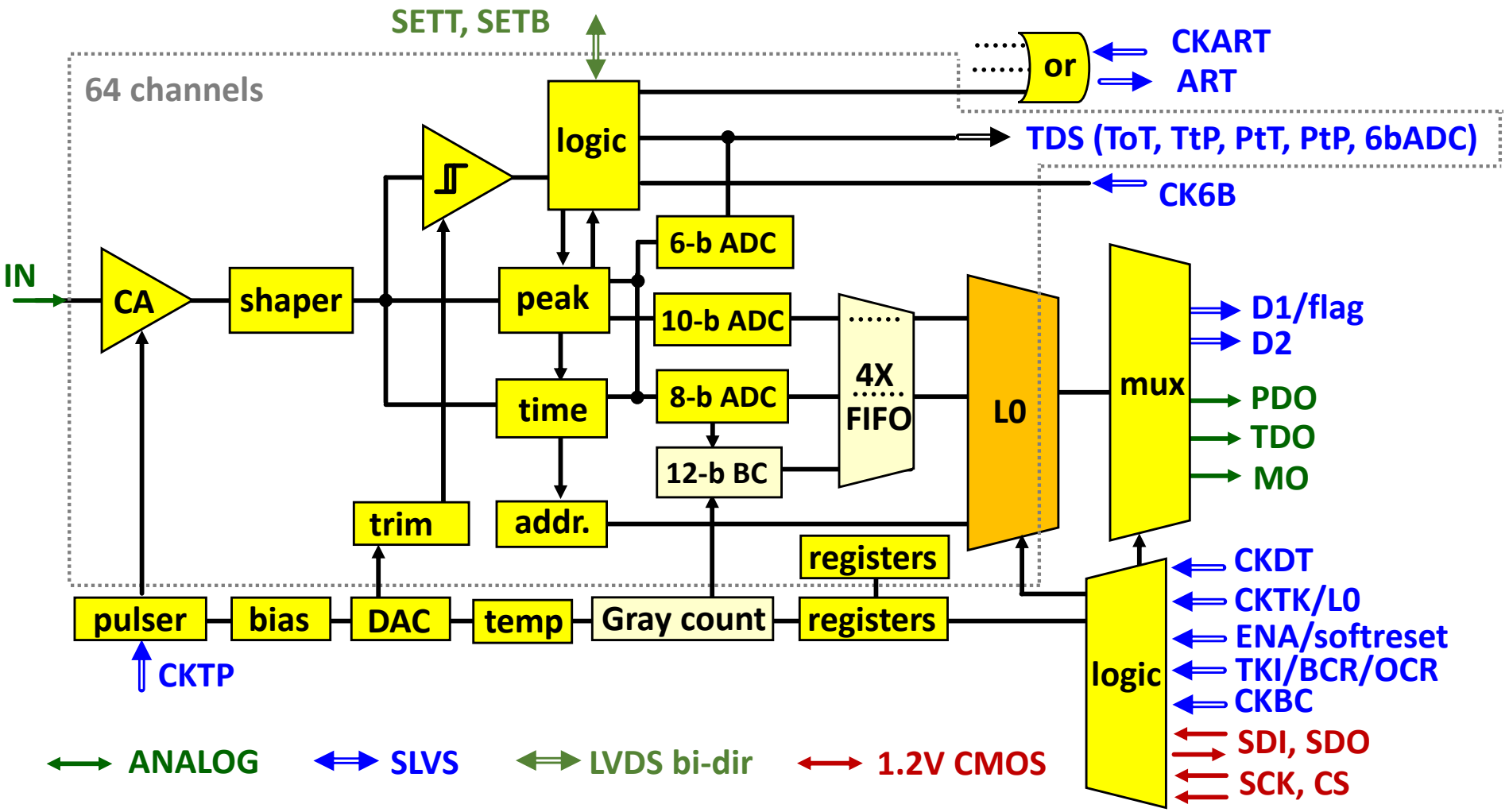


- output DC decoupled from input
- performance identical to previous configuration

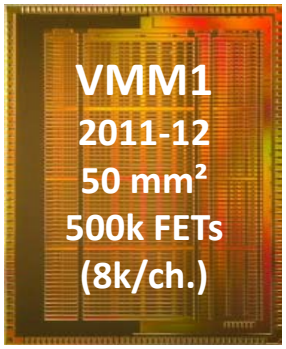
CMOS reset

- Requires input bias current **VMM3a** → adjustable
- Adjust type according to signal polarity **VMM3a** → adjustable
- Cascade stages for high charge amplification **VMM3a** → 3 prog. stages

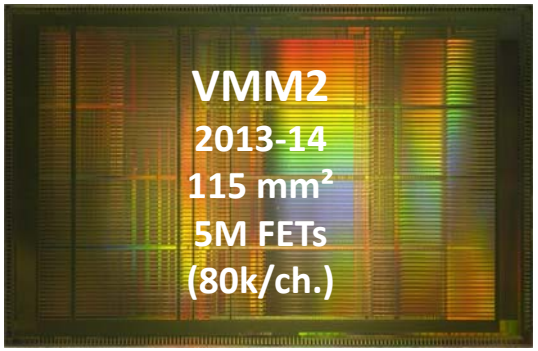
VMM3a Architecture



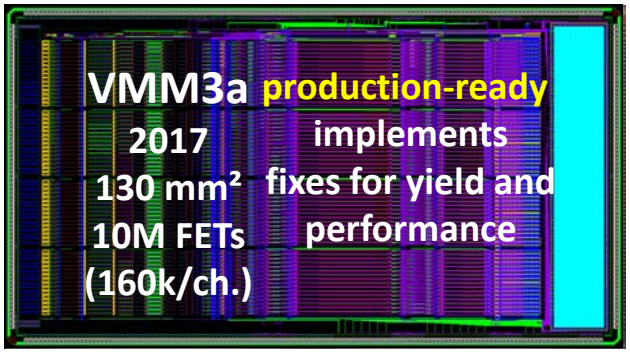
VMM3a Development Stages



- mixed-signal
- **2-phase** readout
- peak and timing
- **neighboring**
- sub-hysteresis
- few timing outputs



- mixed signal
- **continuous** fully-digital readout
- current-output peak detector
- increased range of gains
- three **ADCs** per channel
- FIFOs, **serialized** data with DDR
- serialized **ART** with DDR
- additional timing modes
- 64 **direct outputs**
- additional functions and fixes

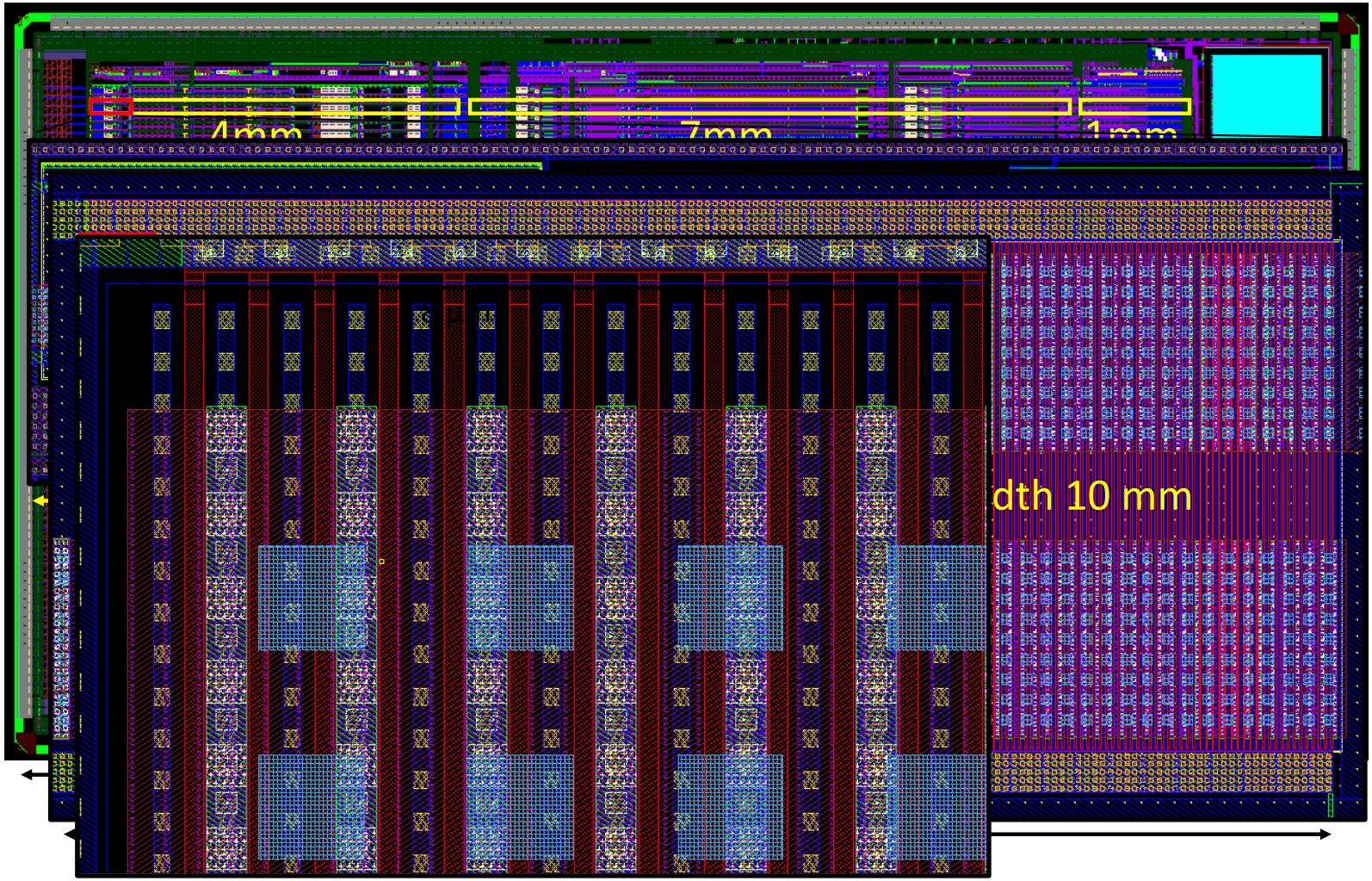


- mixed signal + pure digital core
- continuous simultaneous readout
- **SEU**-tolerant logic
- deeply revised front-end for **TGC**
  (2nF, 50pC, fast recovery, ...)
- **L0** handling digital core
- **SLVS** and new configuration interface
- new **reset** control and fast reset
- **timing** at threshold
- timing ramp optimization
- pulser range extension
- ART synchronization
- 32-channel skip
- additional functions and fixes

Designers: G. De Geronimo & Sorin Martoiu (L0)

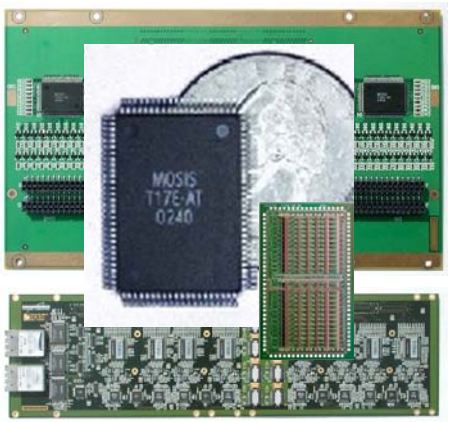
Residual issues: - baseline yield (modeling + manufacturing)
- ADC accumulation (requires redundancy)

VMM3a Physical Layout

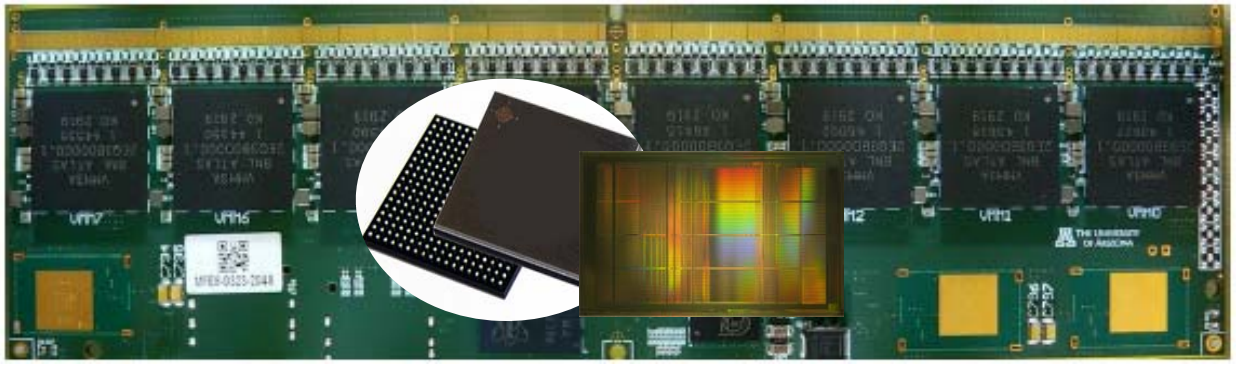


64 channels, 6M transistors, 426 bonding pads, 13.3 x 8.4 mm²

Progress in NSW Front-End Electronics



2005 - ASM

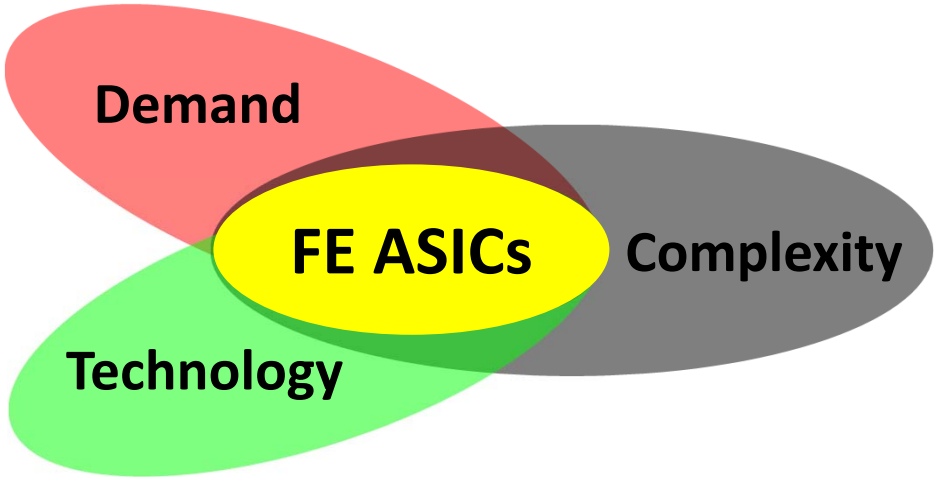


2015 - **VMM**

- 60x sensing elements, 10x element density, 3x power dissipation
- Front-end ASIC (**VMM**)
  - data-driven, trigger primitives, peak, timing, ADCs, direct outputs
  - multiple detector types, broad range of signal charge and input capacitance
  - high programmability, dedicated L0 digital core

Front-end ASICs are becoming systems-on-chip

Prospects in Front-End ASICs



- Rapidly increasing concentration of design and review expertize
- Frequently in critical path; increasing risk of missing some specs

Progress in detectors tightly coupled to progress in FE ASICs

Organizational and design resources must keep increasing

Conclusions

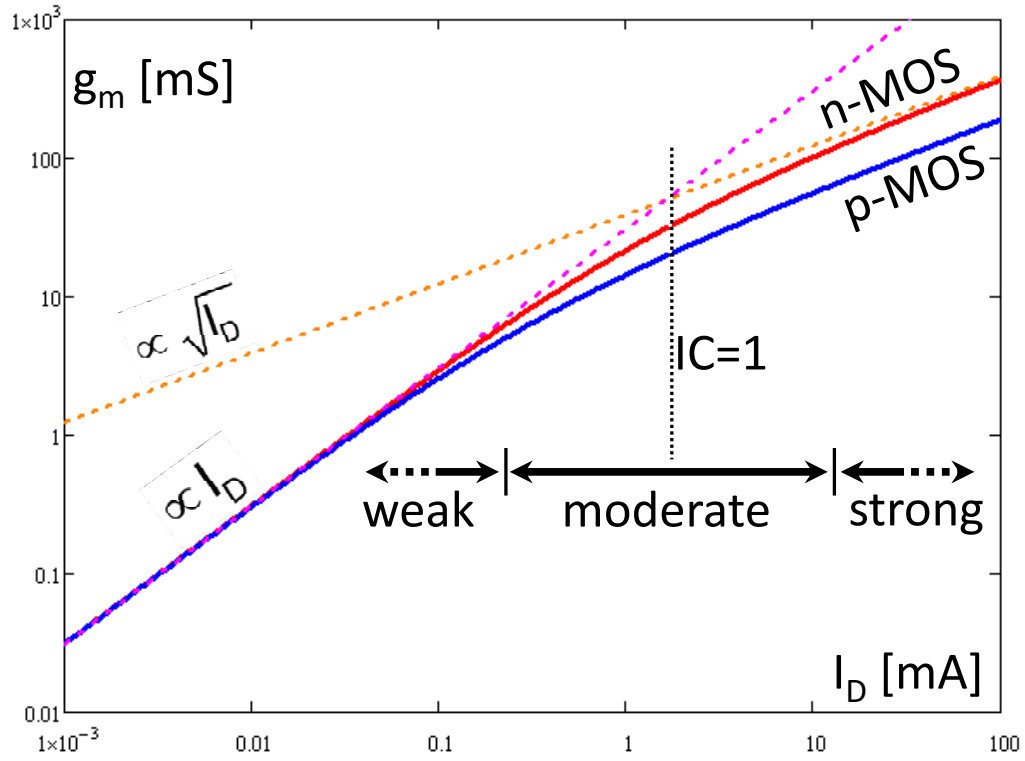
- Input MOSFET operates in **moderate inversion**, far from capacitive matching
- Charge amplification in CMOS requires **active reset, biasing** and **linearization**
- Progress in radiation detectors **tightly coupled** to progress in front-end ASICs
- Front-end ASICs
  - rapid increase in **demand, functionality, programmability, and complexity**
  - increase in **risk of failures** with consequent need to **accept trade-offs**
  - require continuous increase in **organizational and design resources**
  - main front-end ASIC enemies: "perfection" and "general purpose"

Acknowledgment

Vinnie Polychronakos: leadership and support
George Iakovidis: measurements, debugging and documentation
Sorin Martoiu: L0 digital core design
NSW community

Backup

Transconductance g_m in Moderate Inversion

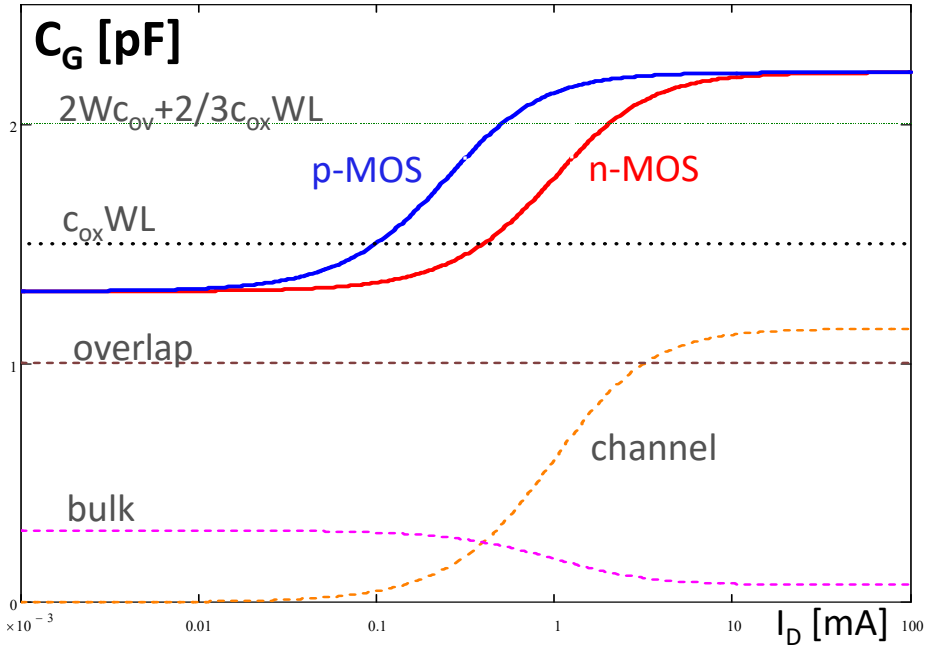


From EKV model $$g_m(I_D) \approx \frac{I_D}{nV_T} \frac{\sqrt{1+4\cdot IC}-1}{2\cdot IC}$$

$$IC = \frac{L}{W} \frac{I_D}{2nV_T^2 \mu c_{ox}}$$ inversion coefficient

De Geronimo, IEEE TNS 52, 2005

Gate Capacitance C_G in Moderate Inversion



$\propto C_{ox}WL$

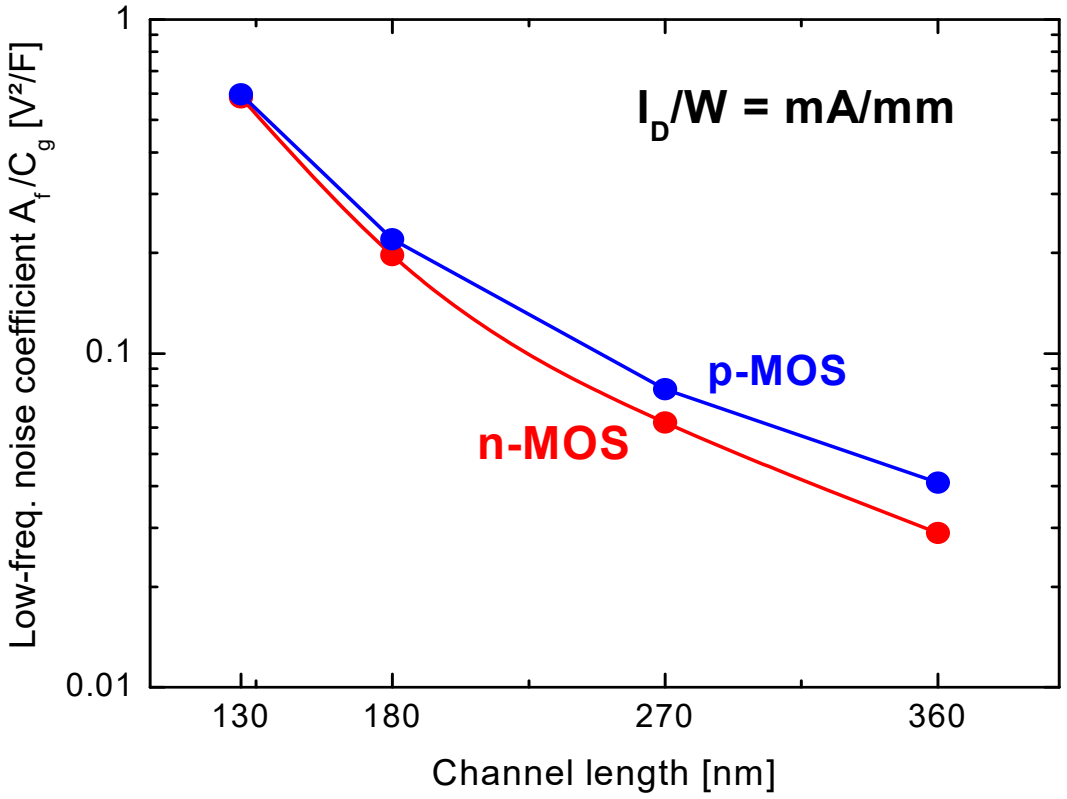
$$C_G(I_D) \approx 2c_{ov}W + C_{ox}WL\left(\gamma_C(IC) + \frac{n-1}{n}\left[1-\gamma_C(IC)\right]\right)$$

$$\gamma_C(IC) \approx \left(\frac{3}{2} + \frac{1}{3}\frac{\sqrt{1+4\cdot IC}+1}{IC^2}\right)^{-2/3}$$

Both g_m and C_G push towards n-channel and L = L_{min}

De Geronimo, IEEE TNS 52, 2005

Low-Frequency Noise vs L

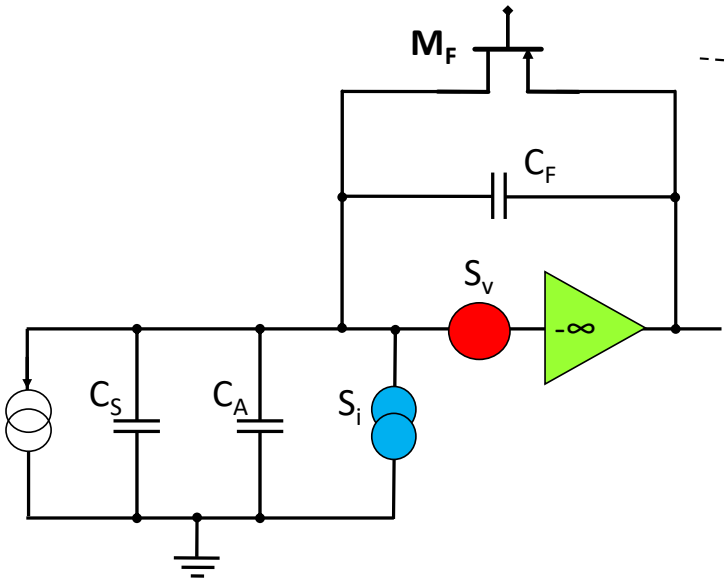


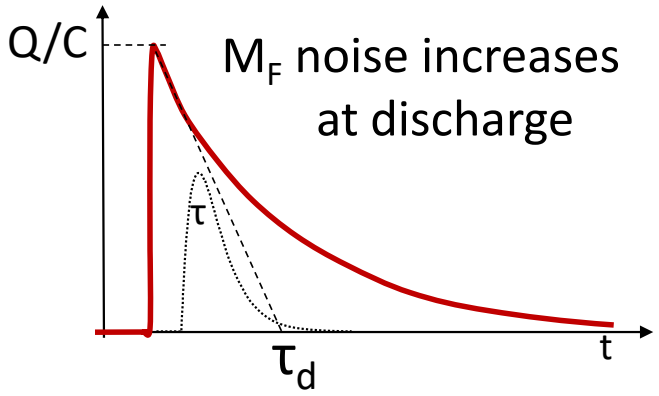
A_f/C_G decreases more rapidly than 1/L

$$S_v = \frac{A_f(L)}{C_G f^{\alpha}} + \frac{A_w}{g_m}$$

Low-frequency noise pushes towards p-channel and $L > L_{min}$

Reset Discharge Noise



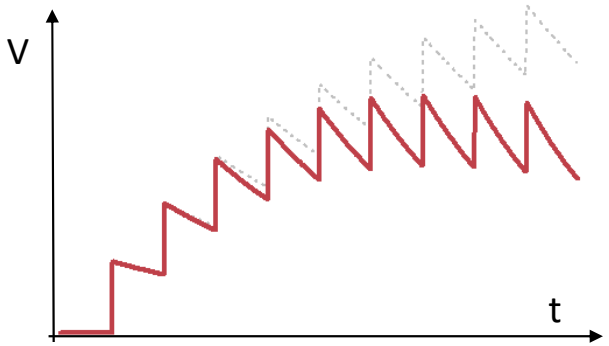


M_F noise increases at discharge

$$\delta ENC_{id}^2 \le \frac{a_i}{2} 2qQ \frac{\tau}{\tau_d}$$ use large τ_d/τ

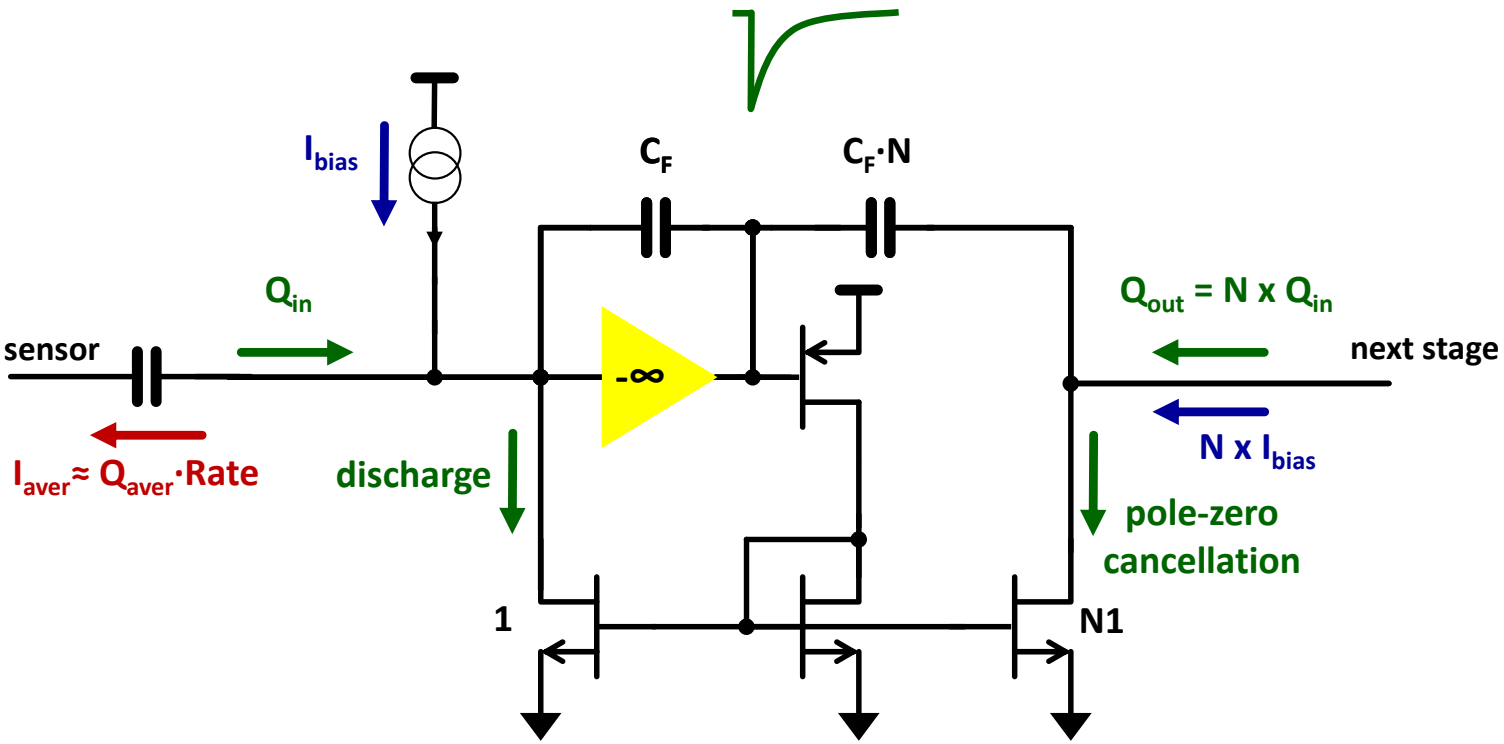
De Geronimo, NIM A 421, 1999

At high rate ρ
$\overline{\tau}_d$ decreases



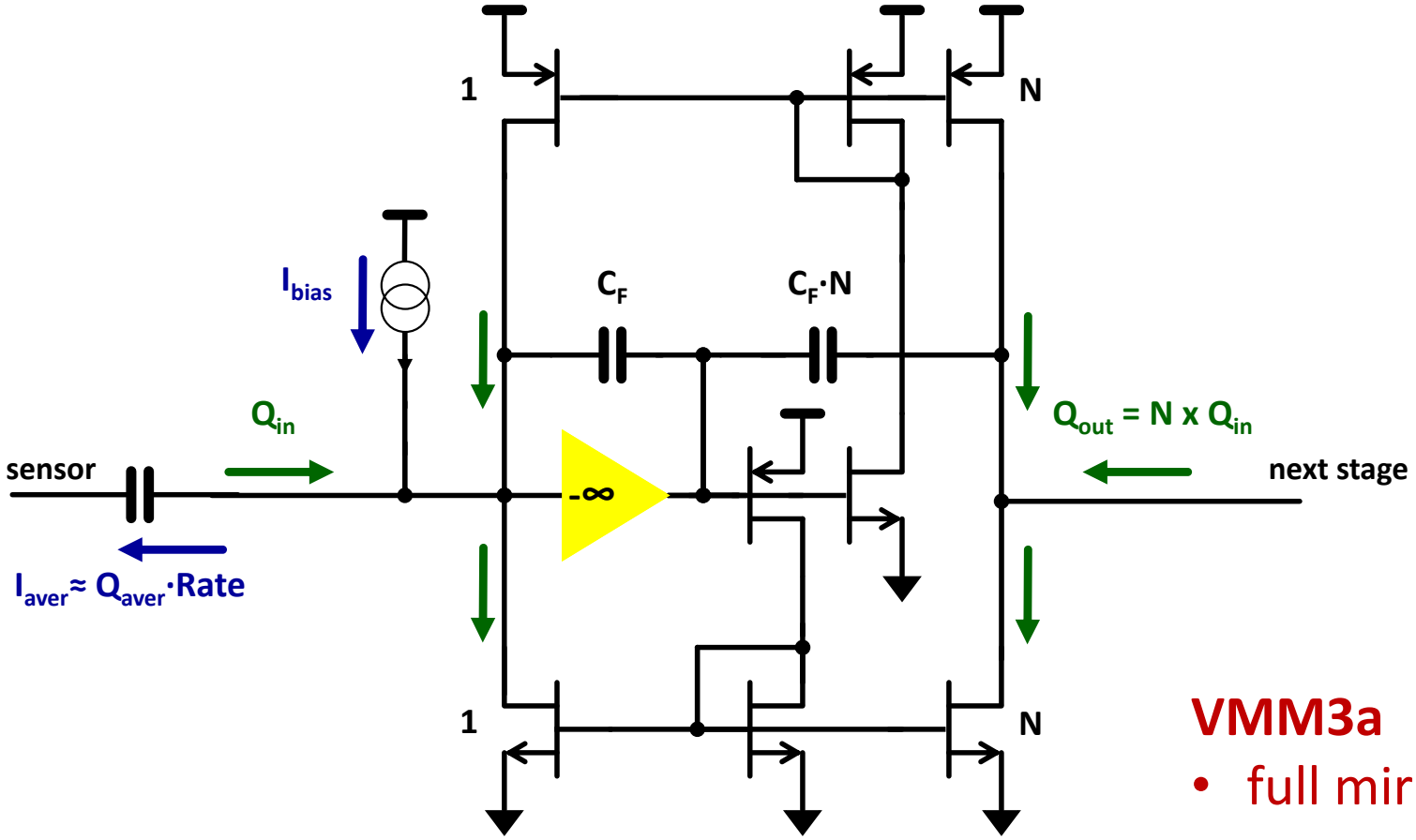
$$\delta ENC_{idr}^2 \le \frac{a_i}{2} 2qQ\rho\tau$$

AC Coupling



$I_{aver} > I_{bias}$ → amplifier shuts down → dead time

Full Mirror Reset

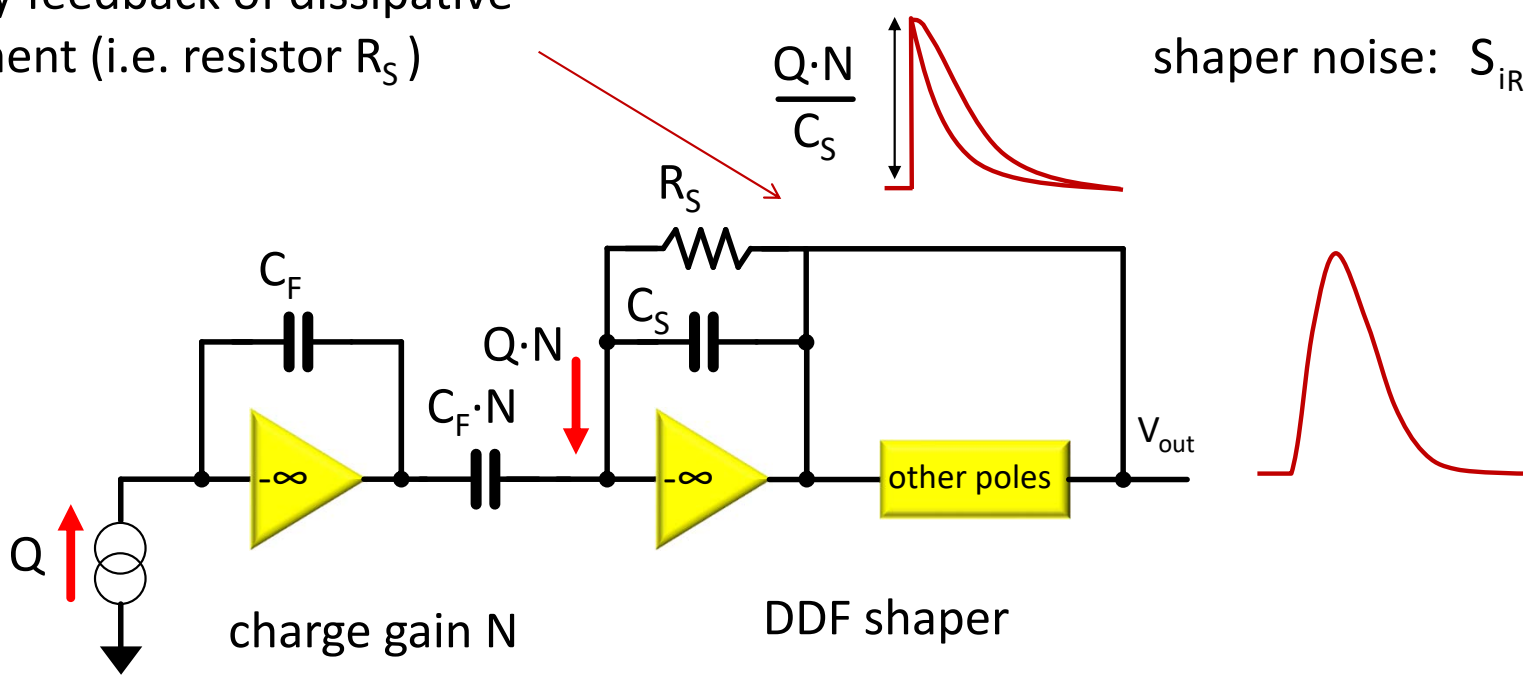


VMM3a

- full mirror enable

Shaper in Delayed Dissipative Feedback

delay feedback of dissipative element (i.e. resistor R_S)

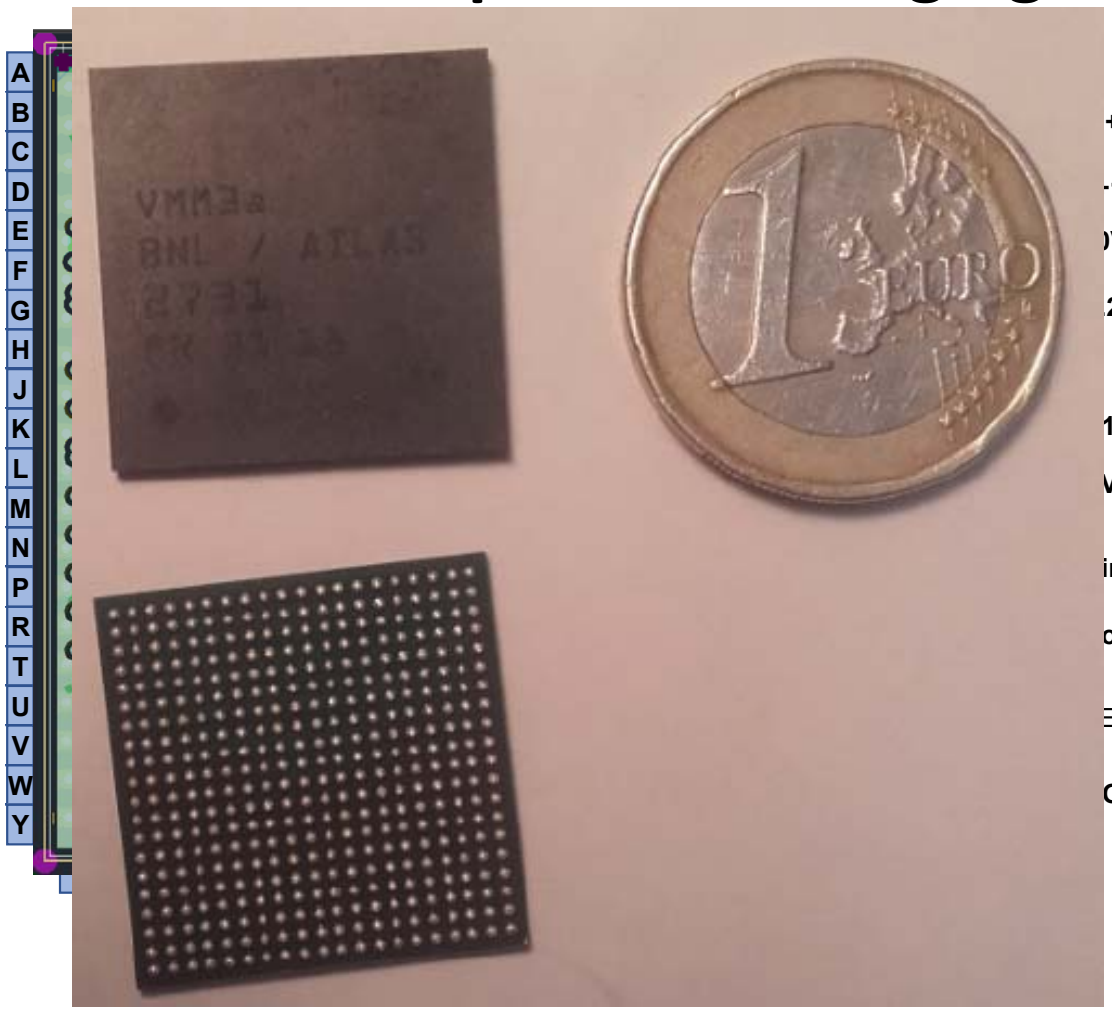


shaper noise: $S_{iR_S} = \frac{4kT}{R_S N^2}$

high analog dynamic range $DR_a \approx \frac{Q_{max}}{ENC_{ca}+ENC_{sh}}$

De Geronimo, IEEE TNS 58, 2011

VMM3a Optional Packaging



BGA 400 pin, 21 x 21 mm, pitch 1 mm