International meeting on "Tracking detectors for particle colliders - present and future"





Tracking detectors for CMS upgrade

Ashok Kumar University of Delhi

Queen Mary University of London October 28, 2021

Foreword

•The potential for new physics in running the LHC without a significant luminosity increase may be negligible.

•The run time necessary to reduce the statistical error in the measurements will be more than 10 years.

•LHC need to have a decisive increase on its luminosity in the coming years.

•The CMS detector will be upgraded to maintain the high level of performance for better precision and improved physics output required for upcoming discoveries.



we are here

CMS in the High-Luminosity LHC Era

Running conditions for LHC to HL-LHC

- Pileup (PU) would be enormous $(30 \rightarrow 200)$
- Increase in Hit rate from 0.58 to 3.2 GHz/cm²
- Radiation: shall be efficient up to ~ 4000 fb⁻¹

forces stringent requirements on the tracking detectors of the CMS, such as

- Maintaining detectors performance high in terms of
 - Efficiency
 - Resolution
 - Background rejection
- High pileup (~ 200) scenario demands
 - Improved granularity e.g. 1200 tracks / unit of eta (at or below the percent level)
- High integrated luminosity (radiation)
 - Replacement of Tracker and Endcap Calorimeter
- Reduced material budget for improving tracking performance
- Huge amount of data (computing and storage)
 - Overhauled Trigger and DAQ systems



CMS Average Pileup (pp, vs=13 TeV)



Upgrade of the CMS Si Tracker

New silicon tracker would be installed in LS3 (2025-2027)

- Outer Tracker (OT) replaces legacy silicon strip tracker
- Inner Tracker (IT) replaces legacy silicon pixel detector

Design goals

- Tracker operate efficiently and withstand HL-LHC luminosity
- Compatibility to deal with higher data rates expected for an instantaneous luminosity of 7.5 x 10³⁴cm⁻²s⁻¹
 - Improved two-track separation, to resolve tracks in high-pT jets
- Trigger latency $(3.2 \ \mu s \rightarrow 12.5 \ \mu s)$
- Increased radiation-hardness
- Higher granularity, low material budget
- Increased forward acceptance for Inner Tracker, up to $|\eta| = 4$
- Tight FE power requirements:
 8 W (+ 1.4 W Sensor) for the PS module, 5 W (+ 1 W Sensor) for the 2S module
- Contribution of Outer Tracker to Level-1 trigger, < 750 KHz

Radiation Environment



Layout of Si Tracker upgrade

Inner Tracker: 4 barrel layers, 8 small disks, 4 large discs per side Pixel size options: 50 x 50 μ m²,25 x 100 μ m²

Outer Tracker: 6 barrel layers, 5 discs per side

9.5 million channels, 44M strips + 174M macropixels



Track Trigger

- CMS uses a 2-level trigger system: L1 (Hardware) trigger and High Level Trigger (HLT)
- Presently only muon & calorimeter contributes in L1 trigger Tracker used at the HLT
- L1 Trigger Challenges: High rates, high pileup environment, Selection algorithms become inefficient

Improved L1 trigger rate: 750 kHz, L1 trigger latency: 12.5 µs

- For reducing trigger rates → increase momentum/energy thresholds:
 - This can obviously hurt physics potential
 - Insufficient at HL-LHC rates
 - Without tracking, L1 output would be ~4000 kHz at 200 PU

Track Trigger

- The use of tracker in L1 trigger
 - A powerful alternative
 - Allow the exploitation of information on track
 - Improve the p_T resolution of various objects at L1 (e.g. jets, muons)
 - Better e/γ/τ identification
 - Contribute to the mitigation of pileup





Design Concept

- L1 trigger is one of the main motivation for the OT Design
 - Impossible to transfer all data off-detector for decision logic at BC rate
- A reduction of data on the module itself is required
 → Exploits p_T dependent bending of tracks in B
- Compare pattern of hits in contiguous sensor elements → Each module has 2 sensor planes
 - → Select Hit Pairs → STUBS
- Primarily depends on separation
 - Increasing separation worsens fake combinations
- $p_T > 2 \text{ GeV} \rightarrow$ a data volume reduction of roughly one order of magnitude
- Stub efficiency is reduced for high η in flat barrel geometry due to impossibility to correlate hits between left half of lower and right half of upper sensor → motivation for tilted TBPS





2S Module

- Electrically, the basic building block is the module no common service boards
- Each module contain
 - Front-end hybrids (FEH): readout and concentrator ASICs
 - Service hybrids (SEH): power and opt. comm.
 - AICF-bridges: high thermal conductivity and similar CTE as silicon
 - HV isolation and HV connection



2S Module

- Strip-Strip layout
- 2×1016 strips ~ $5 \text{ cm} \times 90 \mu \text{m}$ per side
- 90 cm² active area
- In region 60 < r < 120 cm
- Spacing 1.8 mm and 4.0 mm

2S ROC

- CMS Binary Chip (CBC) ASIC
 130 nm CMOS, 254 strips (127 from top+bottom sensor)
- Bump bonded to hybrid, hybrid wire bonded to strip sensor
- Input hit array from both sensor planes

Cluster and correlate to create stubs.

- Two data formats passed to 65 nm Concentrator Integrated Circuit (CIC)
 - L1 hits Send full event clusters along single SLVS line Cluster = x centroid, width
 - Stubs Send stub info along 5 SLVS lines
 Stub = x centroid, bend



PS Module

- Electrically, the basic building block is the module no common service boards
- Each module is connected with 3 wires and 2 fibers directly to the back-end



PS Module

- Pixel-Strip layout
- 2×960 Strips ~ 2.5 cm × $100 \,\mu$ m
- 32×960 macro-pixels ~ 1.5mm × 100μ m
- 45 cm² active area
- In region 20 < r < 60 cm
- Spacing 1.6 mm, 2.6 mm and 4.0 mm



PS ROC

- 65 nm CMOS Short-Strip ASIC (SSA) 120 strips (100 μ m)
- Bump bonded to hybrid, hybrid wire bonded to strip sensor
- Two data formats passed to MPA
 - L1 hits Send full event clusters along single SLVS line
 - Stub preliminary Send strip centroids along 8 SLVS lines
- 65 nm Macro-Pixel ASIC (MPA) 120 x 16 pixels (100 μm x 1446 μm)
- Bump bonded to pixel sensor, wire bonded to hybrid
- Perform clustering and stub association using data passed along stub lines

0 0		10 10 10 10	9 9 9	0 0 0			10 - 10 - 10	0 0 0	0 0			8 8	10 00 00			10 10 TO	0 00	0 0 0		8	10 IO IO	10 II	a			0 (0 (0	9 9	9 9 9	0 0				6 0 a	9 9	8 8 8	0 00 00	0 0 0	0 0			0 0	10 (P	9 9	0 0 0	0 0	0 0 0	
ł			H		U,		ų,	H				ł.				Į.			H.		H	i li	R	H		H.		<u>î</u>			TI.	Т									ġ.	H.			10	- b	
Range Table		8	14 MG		Ħ							雷		iii											00						34		10.1			100					ä		Ŧ		100 101		
h	H	녩	轀									쁥	1				电		4		ų	ł				H	4	1	1					ł							h.	÷			붱		
i.	h	÷,	÷		a,	w	ė		τų		M	è				÷.		en e	w		di.	10	÷			÷	uu:	÷	di.	w		•••	į.	÷	÷.	w	e e e e e e e e e e e e e e e e e e e				ŵ		÷.	ųπ,	÷	÷	
			÷							1		H.									Į,														H			1					-				
	ł																					14												詯		Π.				1			İ				
		1	11			<u>12</u>		-8			-			-						4	2				-	4	4					-			11	ŧΨ	1			44	148			4		-	
		5	łł.			i i	А.	2	1	100		q.	H	H	14	2	8	1	1	S FC	2	18			1	2	167	1		ET I			î.	61	a.	G	1	1	14		2	е,	3			2	ł



Inner (Pixel) Tracker

- Reduction in pixel area by factor of 6 compared to earlier CMS Pixel Detectors →enabling low occupancy and improved two track separation
- n in p type Si sensors of thickness 150 µm thickness segmented into pixel sizes of 25 x 100 μ m² (long side along z in barrel and along r in endcaps) or 50 x 50 μ m² for better resolution







Two options

- 1 x 2 modules (with 2 chips) in inner 2 layers of TBPX and inner 2 rings of TFPX and TEPX.
- 2 x 2 modules (with 4 chips) • in outer 2 layers of TBPX and outer 2 and 3 rings of TFPX and TEPX



TBPX : 4 Barrel cylindrical layers (2.9 cm, 7 cm, 11.8 cm, 15.7 cm)

- TFPX : 8 small Double Discs at each end (25 cm, 32 cm, 41 cm, 52 cm, 67 cm, 85 cm, 110 cm, 140cm)
- TEPX : 4 large Double Discs at each end (175 cm, 198.5 cm, 225 cm, 255 cm)



TEPX Disk 4 Ring 1 is dedicated to lumi measurements, independent readout and control

Inner (Pixel) Tracker Electronics

65 nm C-ROC developed as variant of the RD53B chip

- Linear front-end, 432 x 336 pixel array
- Binary readout plus time-over-threshold and serial powering features.
- Preliminary versions tested up to 1 Grad (high dose rate)

Serial powering up to 12 modules / chain

- ROCs share constant input current
- Generate the necessary operational voltage



RD53B on single-chip test card

Serial powered chain of 2x2 digital modules



Modules connected with up to 1.6m electrical links to port cards at periphery

- ~ 6 electrical up-links @1.28 Gb/s per module to LpGBT
- 1 electrical down-link
 @160 Mb/s per module
 from LpGBT
- ~ 6 e-links at 1.28Gb/s per LpGBT (AC-coupled)
- 28 DTC (Data, Trigger, Control) boards required for CMS IT



Occupancy < 0.1%

Inner (Pixel) Tracker assembly

- Readout chips (ROCs) bump bonded to sensor
- High density interconnect (HDI) on top collects the data & distributes signals & power
- ROC based on RD53 development: Pixel chip in 65 nm CMOS →Hit rates of upto 3 GHz/cm²
- No active components
 - HDI wire bonded to the ROC
 - Base strips with high thermal conductivity support the module, also facilitate handling & mounting
 - Electrical cables (e-links) connect modules with LpGBT boards
- All modules rectangular, two types
- Double-discs formed by 4 "dees"
 →modules arranged hermetically on 4 layers
- Structures supported by Carbon Fiber cylinders





Phase-2 Muon tracking stations

Legacy Muon stations

- (DT, CSC, and RPC detectors)
- DT and RPC: new readout with improved z and time precision
- CSC forward: new readout at high bandwidth
- shielding to reduce neutron background on top part of detector

New Muon stations

- iRPC: RE3/1 and RE4/1 Short electrode recovery, reduction in total charge produced in a discharge
- GEM based GE1/1 and GE2/1 Improved L1 µ trigger in endcap
- GEM based ME0 detector
 Extension in eta coverage to |η| = 2.8
 (7° w.r.t beam axis)





Expected Performance

Upgraded muon system will maintain physics performance at the HL-LHC

- Much better resolution
- Much better rate capability

Muon trigger and reconstruction

- Increased trigger efficiency
- Lower trigger rate
- Extended eta coverage
- Better redundancy

Physics improvements

- Increase in Higgs (4μ) signal strength (7%)
- Improved weak angle measurement
- Top quark mass in
 - t \longrightarrow J/ ψ (µµ)µ + X decays



Stations with new detectors

GE1/1 (Installed in LS2, Commissioning ongoing)

- ✓ 36 superchambers (SC) per endcap
- ✓ 2 triple GEM detectors per SC
- 🖌 10° in φ
- ✓ $1.5 < \eta$ < 2.0

GE2/1 (installation during LS3)

- ✓ 18 superchambers (SC) per endcap
- ✓ 2 triple GEM detectors per (SC)
- 🗸 20° in φ
- $\checkmark 1.6 < \eta \ < 2.4$

ME0 (installation during LS3)

- 18 stacks per endcap
- ✓ 6 layers of triple GEM detectors per stack
- 🗸 20° in φ
- $\checkmark 2.0 < \eta < 2.8$

RE3/1, RE 4/1 (installation during LS3)

- ✓ 72 new RPC chambers
- ✓ 20° in φ
- $\checkmark 1.8 < \eta < 2.5$







GEM - CSC Trigger

- Adding GEM chambers significantly increases the local lever arm for the segment reconstruction with respect to the CSC-only system (by factor of > 2).
- There are no iron yoke elements in between the GE2/1 and ME2/1 chambers, the multiple scattering is small.
- The additional local lever arm is important for displaced vertices, for which the vertex constraint cannot be exploited. Here two independent direction measurements, in endcap stations 1 and 2, allow a standalone momentum measurement in the muon system in the Level-1 trigger.





Summary

- The HL-LHC upgrade offers a large improvement to the instantaneous luminosity alongwith new challenges for detector technology
- The CMS outer tracker has been completely redesigned for high radiation environment and sufficient granularity
- Typical tracking accuracy: spatial precision O(100) micron, and time resolution less than few ns are achievable.
- Muon (outer) tracking stations coverage is going to be extended and new technologies improvises position resolution, rate capability and radiation susceptibility under harsh environment.
- CMS would maintain the excellent performance of the CMS muon system within large geometrical acceptance in more challenging data-taking conditions

- Electronics use programmable search window to accept high-pT tracks & form stubs (hit position + bend info)
- "Stubs" sent to the back-end at 40 MHz \rightarrow track reconstruction \rightarrow L1 trigger decision
- On receipt of a L1 trigger, the complete event information is read out at 750 kHz



Layout of Si Tracker upgrade

Inner Tracker: 4 barrel layers, 8 small disks, 4 large discs per side

Pixel sizes: 50 x 50 μm^2 , 25 x 100 μm^2

Outer Tracker: 6 barrel layers, 5 discs per side

9.5 million channels, 44M strips + 174M macropixels

