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40 picoseconds time resolution analysis from test beam of monolithic pixel sensors.

Théo Moretti on behalf of the MONOLITH team

10th Beam Telescopes and Test Beams Workshop – Lecce

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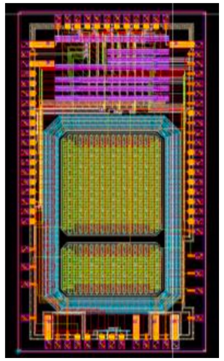
Introduction

2016

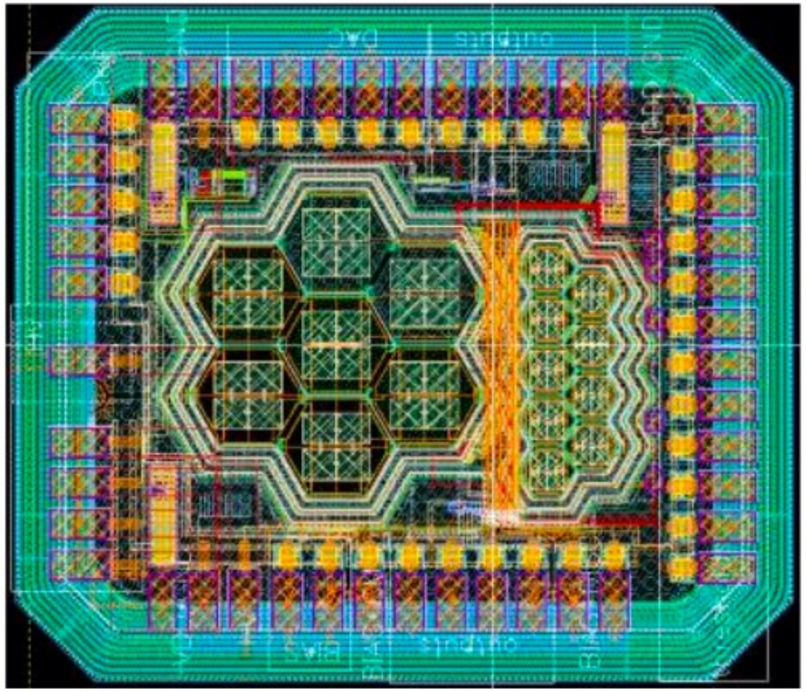


200 ps

2017

100 ps

2018



50 ps time resolution

2018 prototype:

- Hexagonal pixels: 65 µm side (100 µm pitch)
- Discriminator output
- High discrimination threshold
- Time Over Threshold (TOT) used for Time Walk Correction

Ref: https://iopscience.iop.org/article/10.1088/1748-0221/14/02/P02009
Ref: https://iopscience.iop.org/article/10.1088/1748-0221/13/04/P04015
Ref: https://iopscience.iop.org/article/10.1088/1748-0221/14/11/P11008

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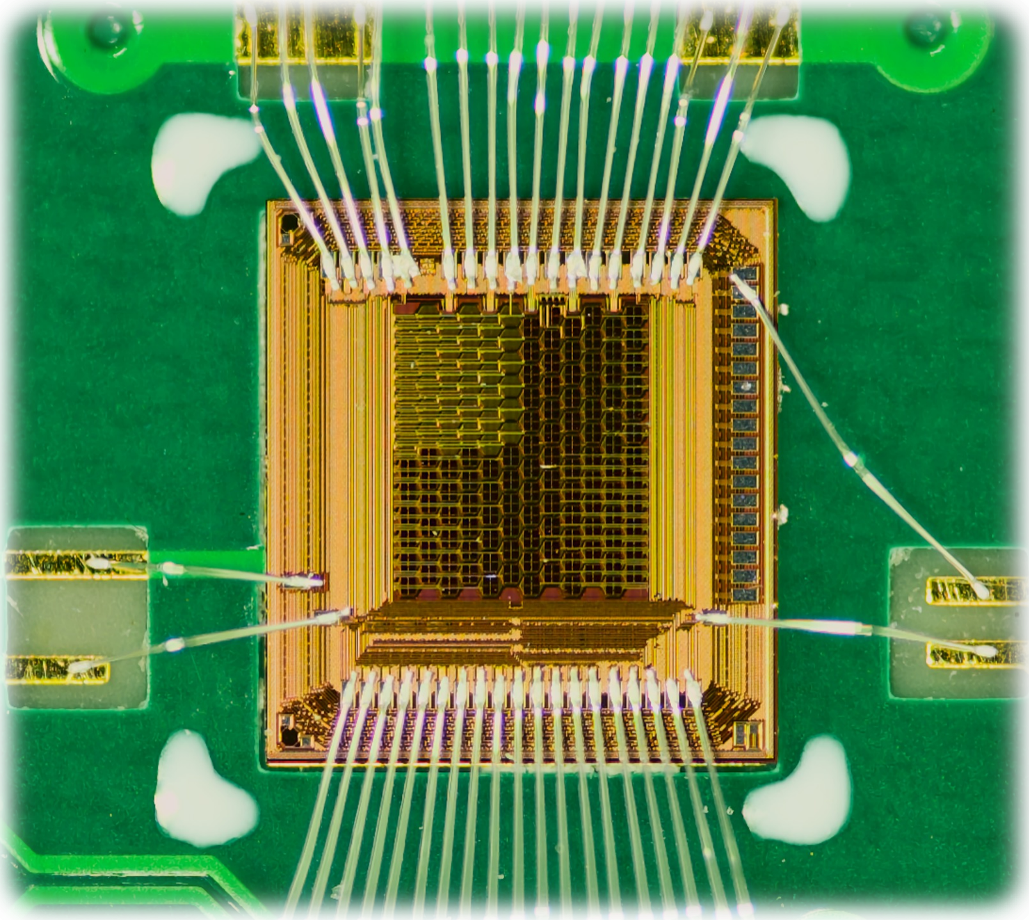
Outline

- **Monolithic SiGe BiCMOS pixel sensor**
  - SiGe BiCMOS technology
  - Sensor characteristics
- **Test Beam measurements**
  - The FEI4 telescope and experimental setup
  - Efficiency
  - Correcting for time walk
  - Time resolution
- **Summary and Outlook**



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SiGe BiCMOS front end technology

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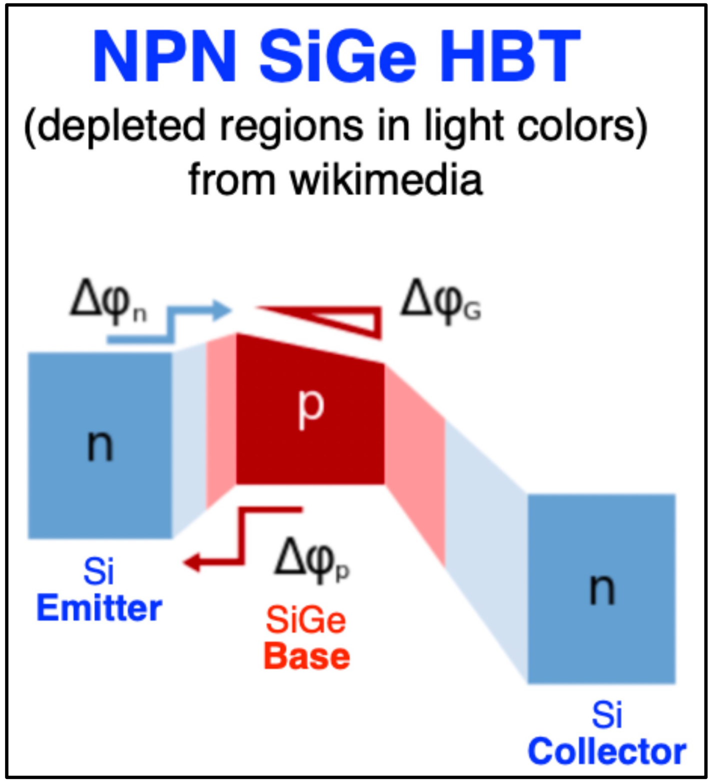
Recipe for timing: ultra-fast, low noise and high gain amplifier



SiGe Hetero Bipolar Transistor (HBT) = Bipolar Junction Transistor (BJT) with Germanium in base material:

- **Reduced base resistance R_b**

Grading of Germanium doping in base:

- **Higher current gain β**
- **Charge transport via drift**

Reduced Equivalent Noise Charge (ENC):

$$ENC_{Series\ Noise} \propto \sqrt{k_1 \frac{C_{tot}^2}{\beta} + k_2 R_b C_{tot}^2}$$

Leibniz Institute for high performance microelectronics

IHP SG13G2, 130nm process.

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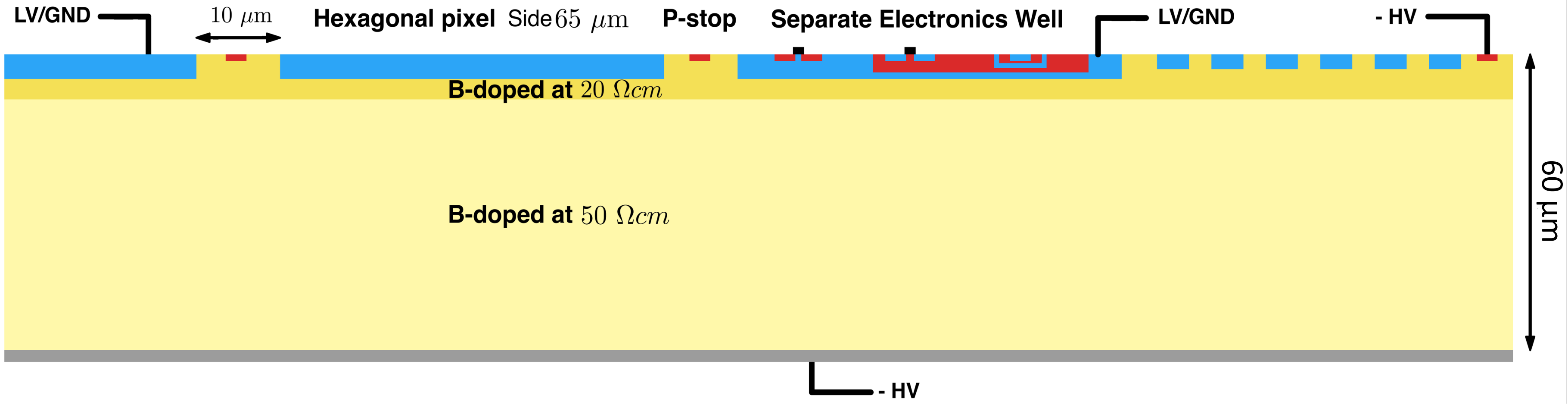
Sensor design

Hexagonal pixels with large collection electrode:

- 65 µm side (100 µm pitch) + 10 µm interpixel with P-stop.
- Heavily Boron-doped (p-doped) substrate and standard low resistivity wafer

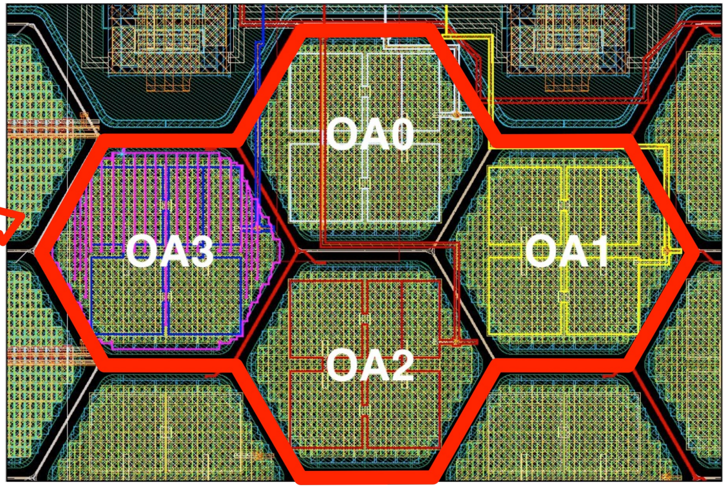
- Negative HV to substrate from backside and from top.
- Pixels and electronics in deep n-well at positive low voltage

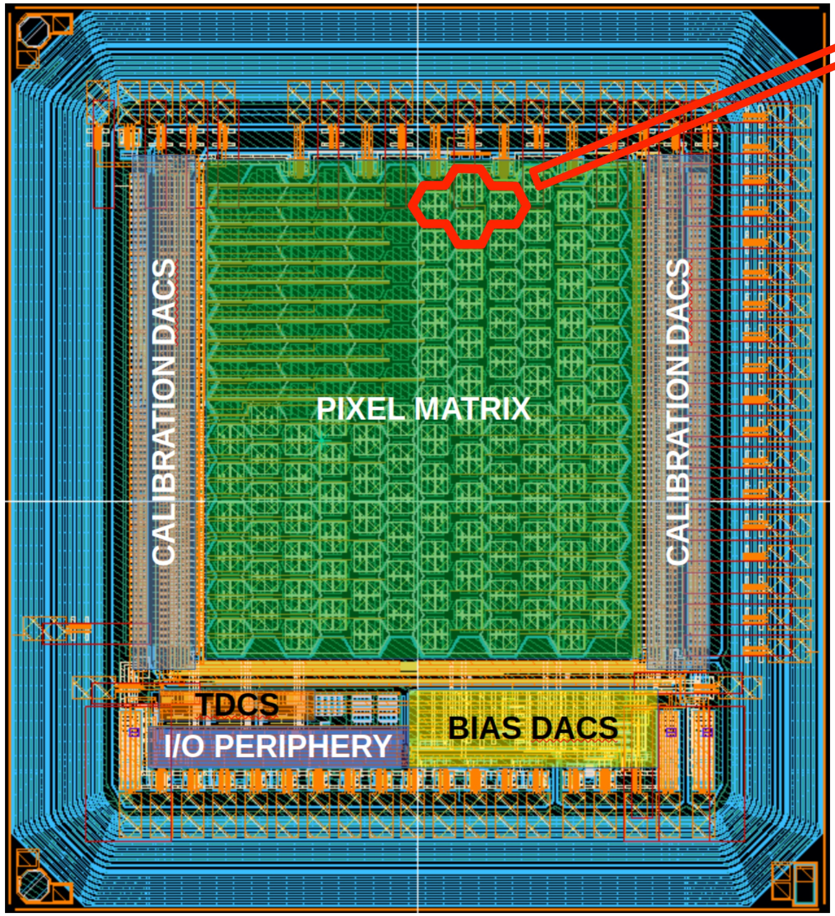


Typical HV = -140 V:

- Depletion layer: 24 µm.
- Typical signal charge for MIP: ~1500 electrons.

The "ATTRACT" prototype





Four pixel with analog channels including:

- HBT pre-amplifier
- Two HBT Emitter Followers to 500 Ω resistance on pad

Test performed on analog channels to investigate HBT and sensor performance.

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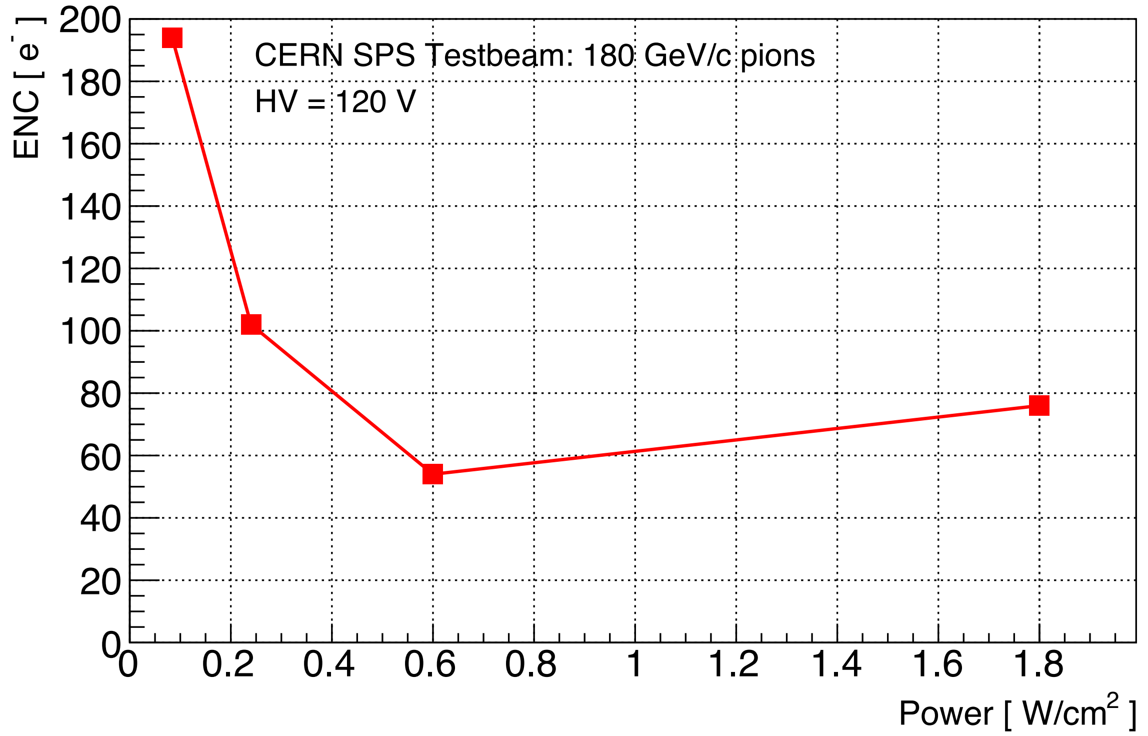
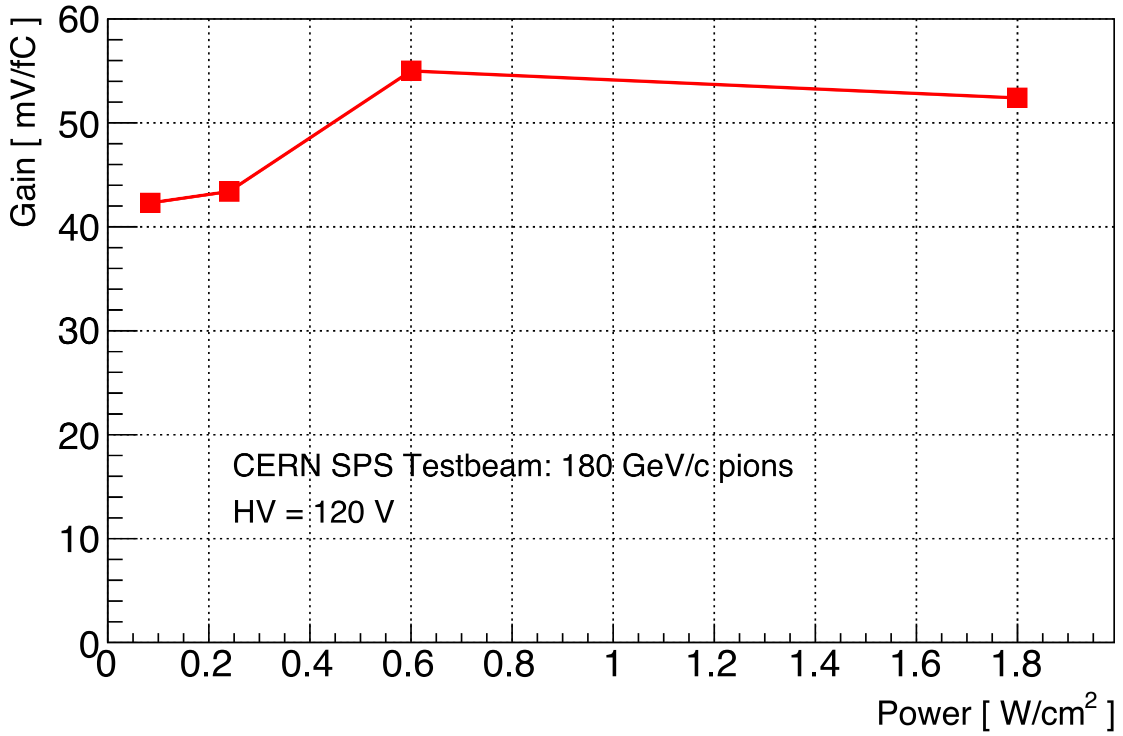
Sensor characteristics

Gain and ENC measurement of the electronic gain (pixel + pre-amplifier + driver) as a function of power consumption:

- Performed using ^{109}Cd source, two X-rays with E_1 = 22.2 keV and E_2 = 24.9 keV.
- Separate noise from electronic chain and oscilloscope following:

$$ENC = \frac{\sqrt{\sigma_V^2 - \sigma_{scope}^2}}{A_q}$$





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Test Beam Set-Up

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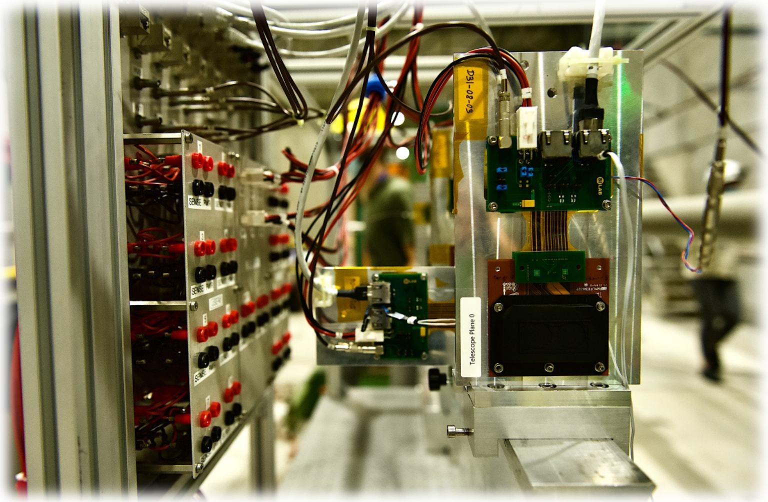


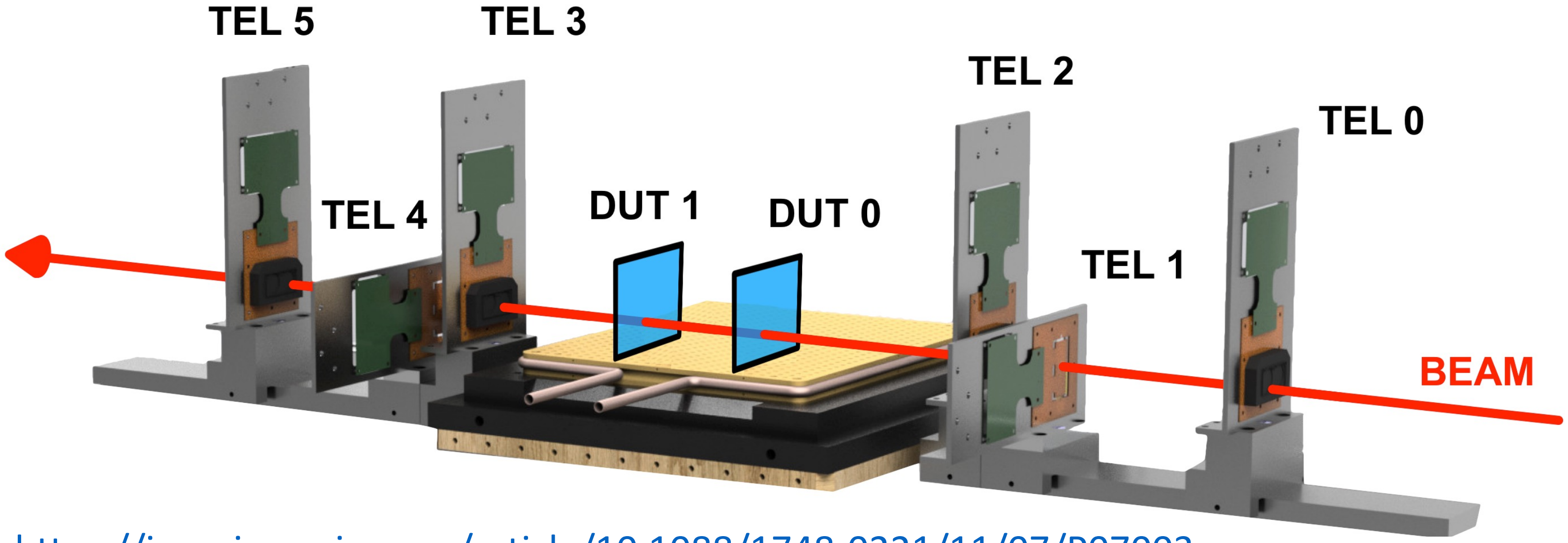
UNIGE FE-I4 Telescope for tracking:

- 6 planes, chip with rectangular pixels: 50 µm x 250 µm.
- Spatial resolution: σ_x=12 µm σ_y= 10 µm.

CERN SPS Test Beam with high intensity, 180 GeV/c pions.

Timing Resolution and **efficiency** measured as a function of:

- Sensor High Voltage
- Power consumption (pre-amplifier bias current)



Ref: https://iopscience.iop.org/article/10.1088/1748-0221/11/07/P07003

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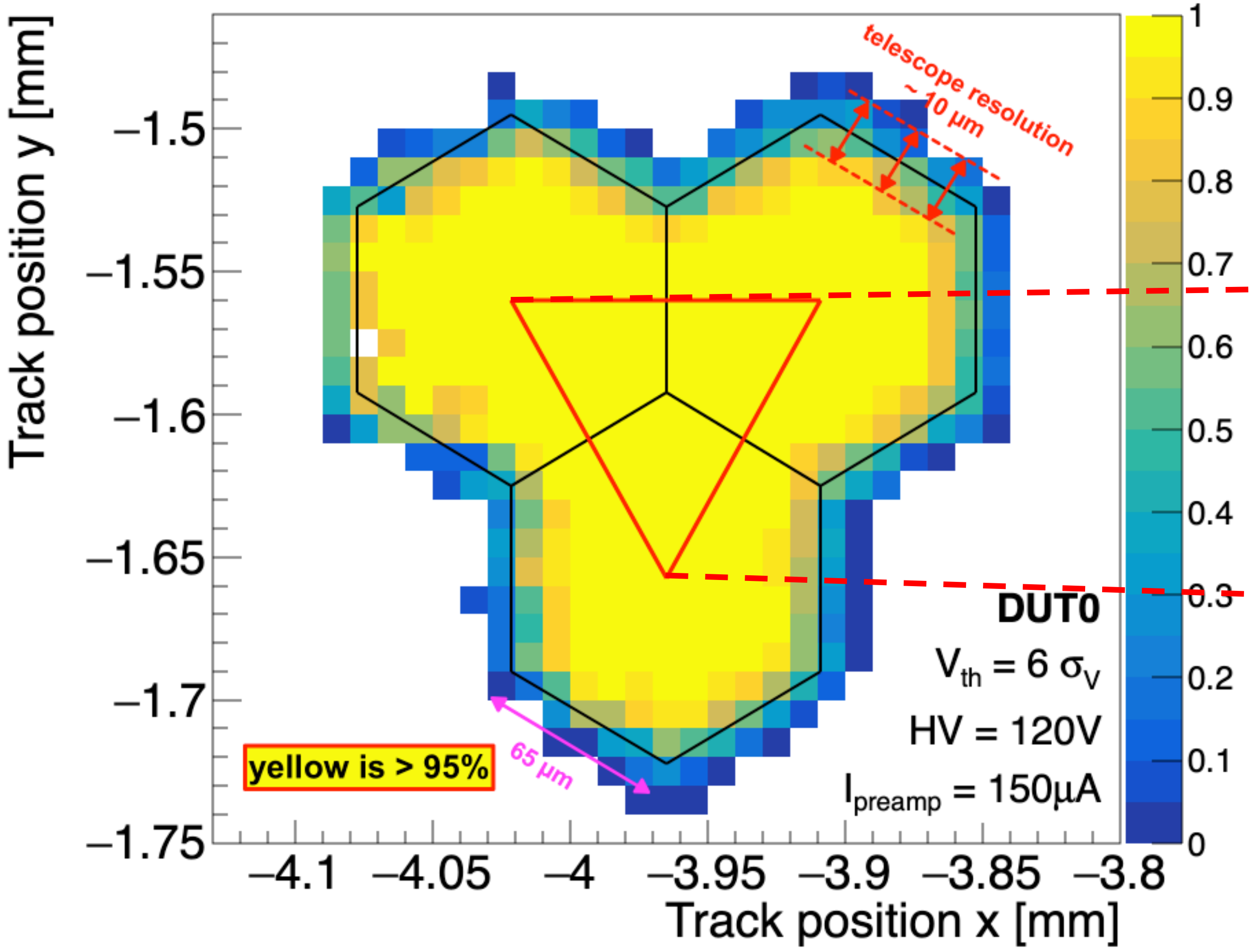
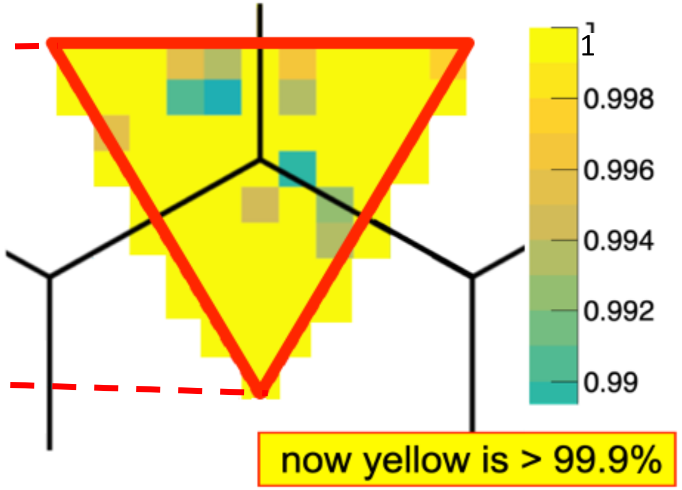
Efficiency map



Getting rid of border effect from FE-I4 telescope pointing resolution :

- Use bins inside area of **red triangle**, representing full pixel in right proportions.



Inside **red triangle** the efficiency is:

Efficiency = $99.91^{+0.03}_{-0.08}$ **%**

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Efficiency scan

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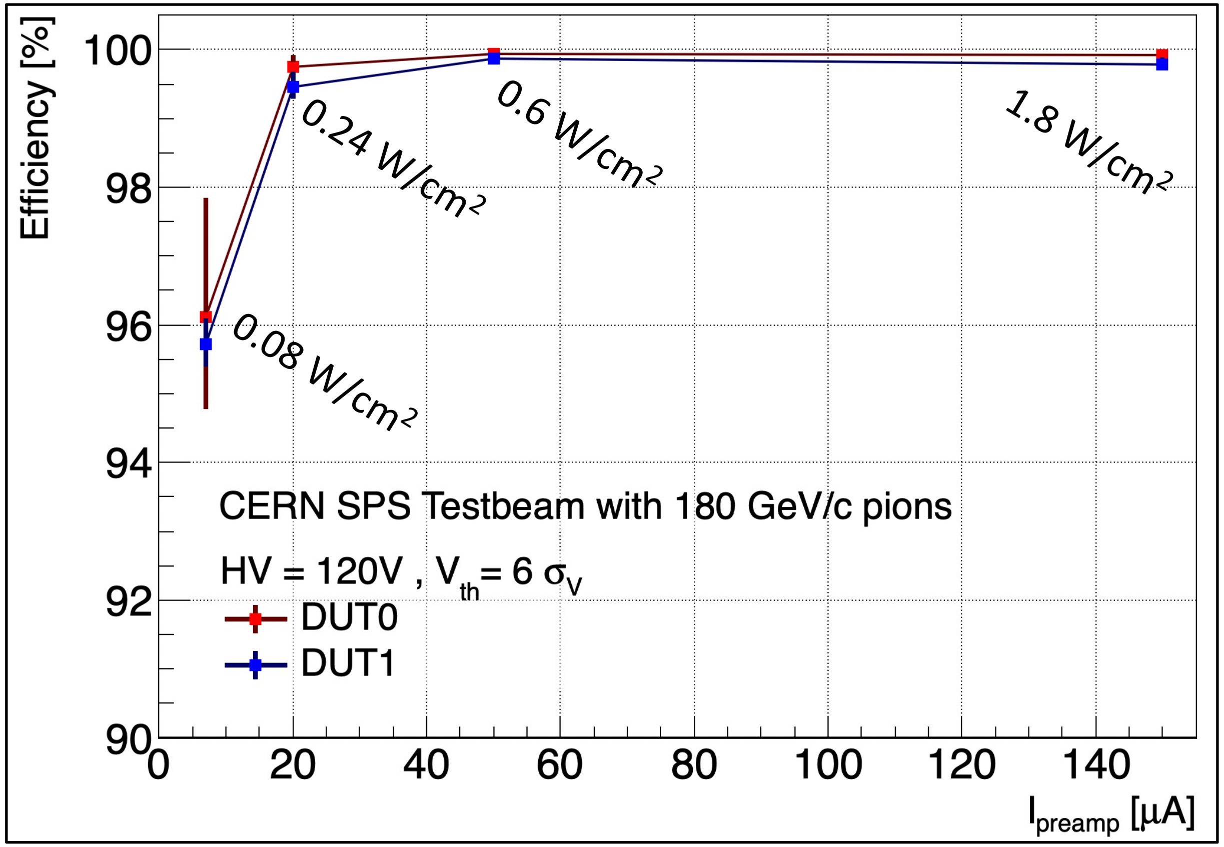

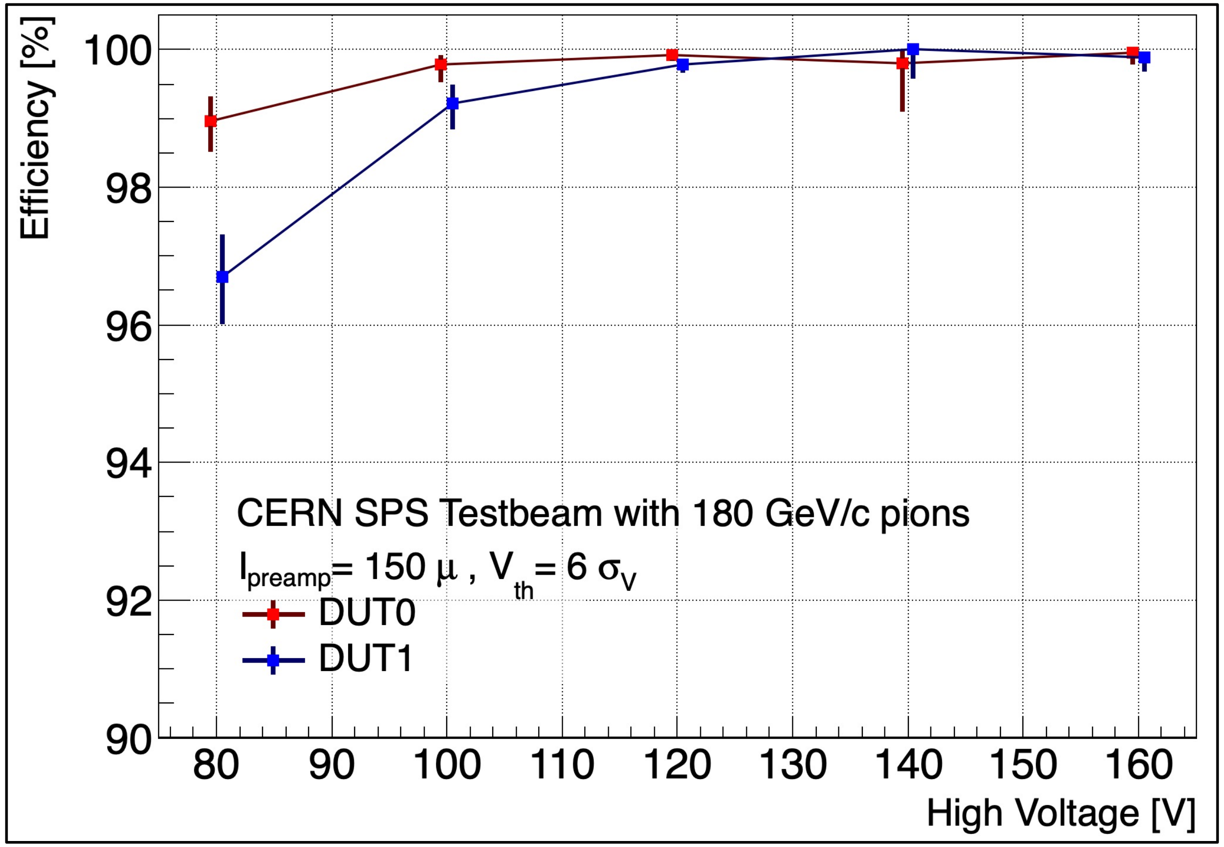

- From power consumption of 0.24 W/cm^2 on, efficiencies **well above 99%.**
- Efficiency "plateau" reached at 120 V.

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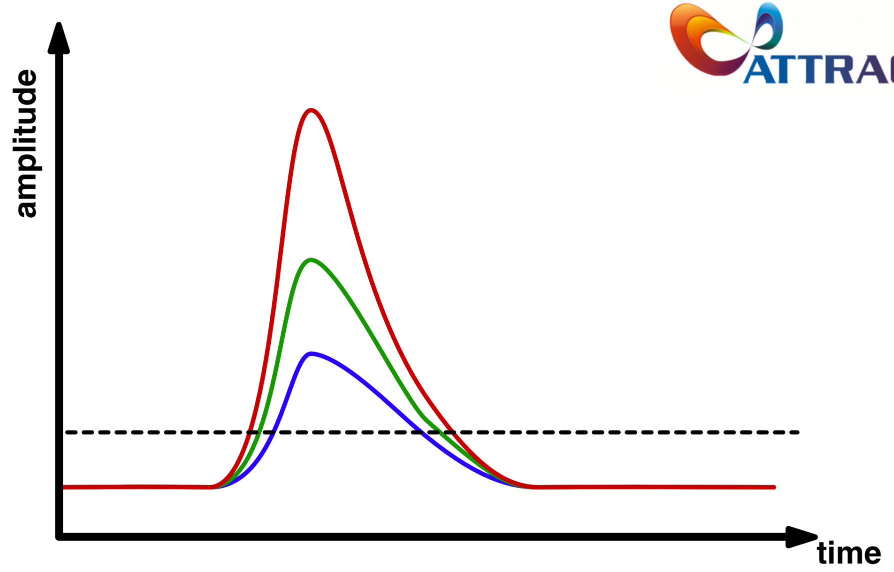
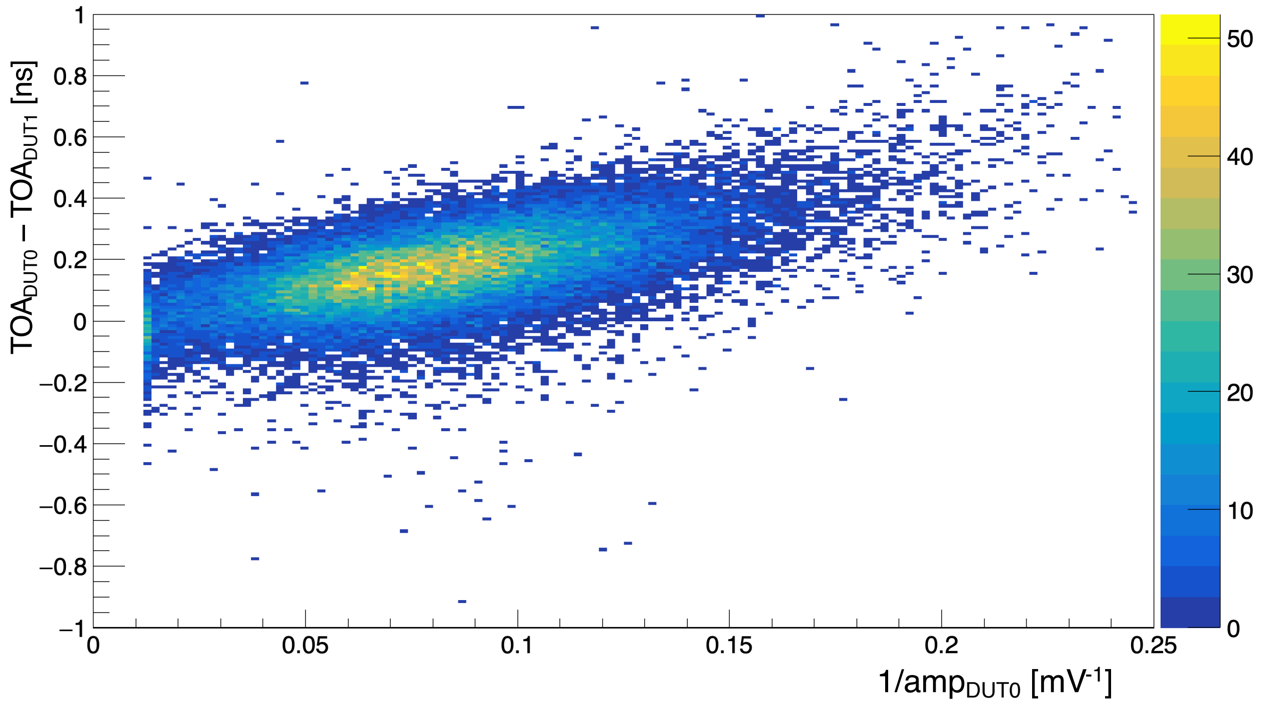
Correcting for time walk

Front-end electronics gives equivalent peaking time for all signals:

- Time Walk: Time Of Arrival (TOA) different from signal to signal.
- Can be corrected with respect to amplitude of signal.





- Timing resolution measured through standard deviation of distribution of difference of TOA.
- Both DUTs corrected for time walk with respect to their own amplitude.

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Correction procedure

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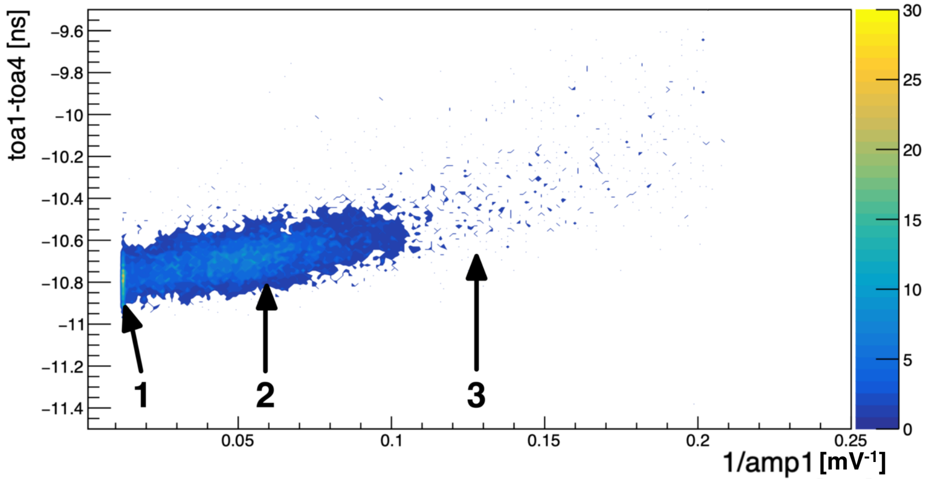

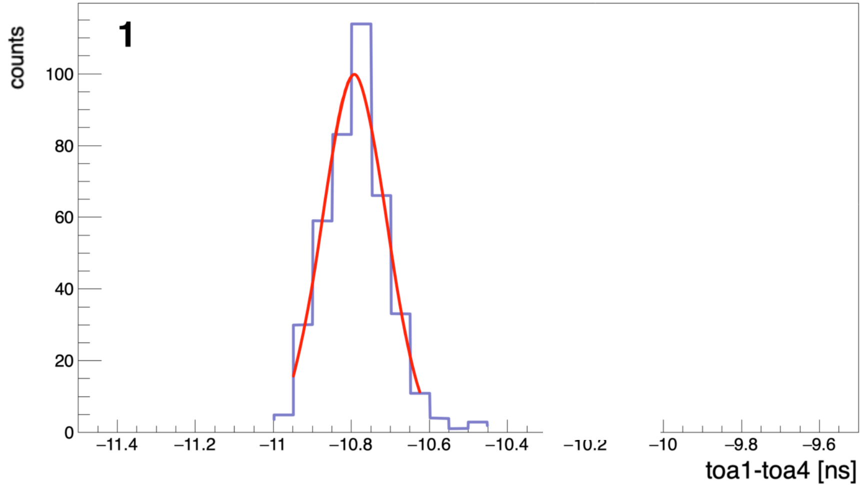

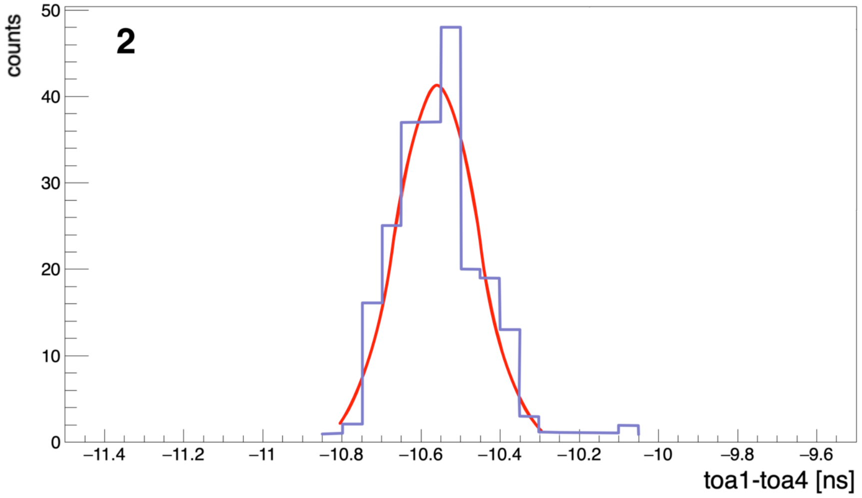

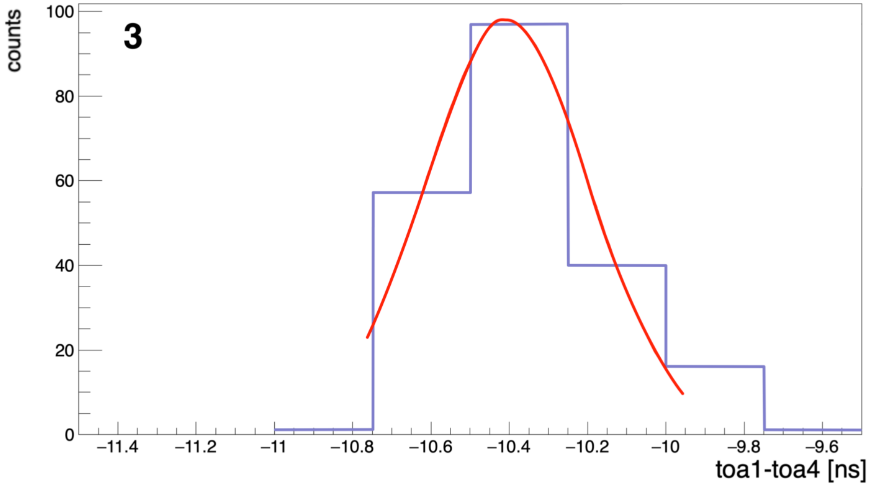

Data sampled for different values of amplitude.

Once enough events in every sample:

- Projection of the difference in TOA for the slice.
- Gaussian fit (since every subsample is a Gaussian) to extract the mean.
- Mean used to correct time walk

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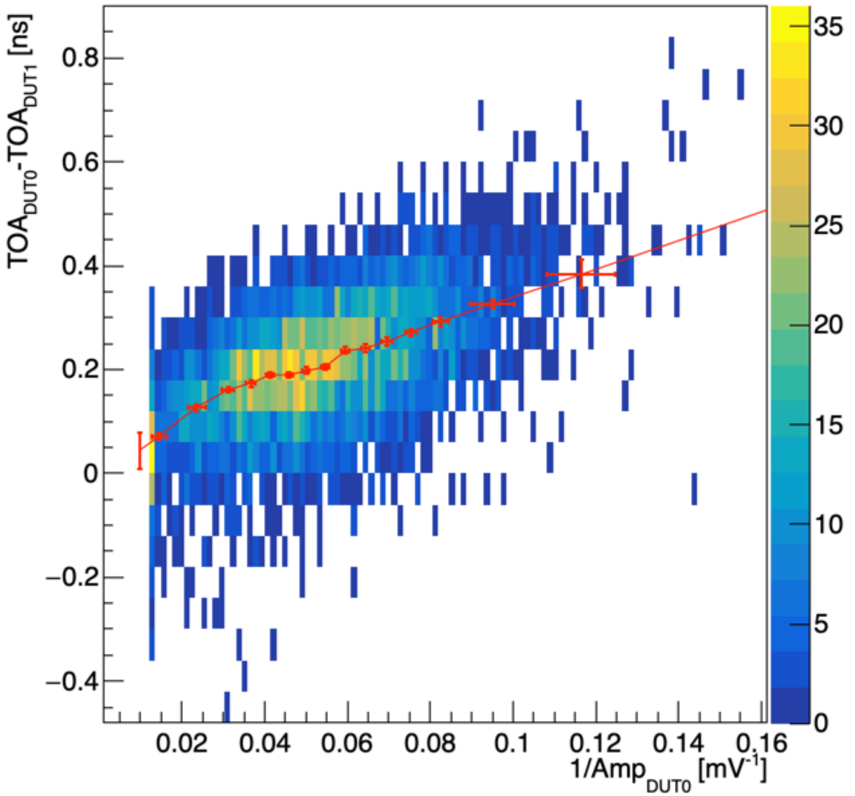
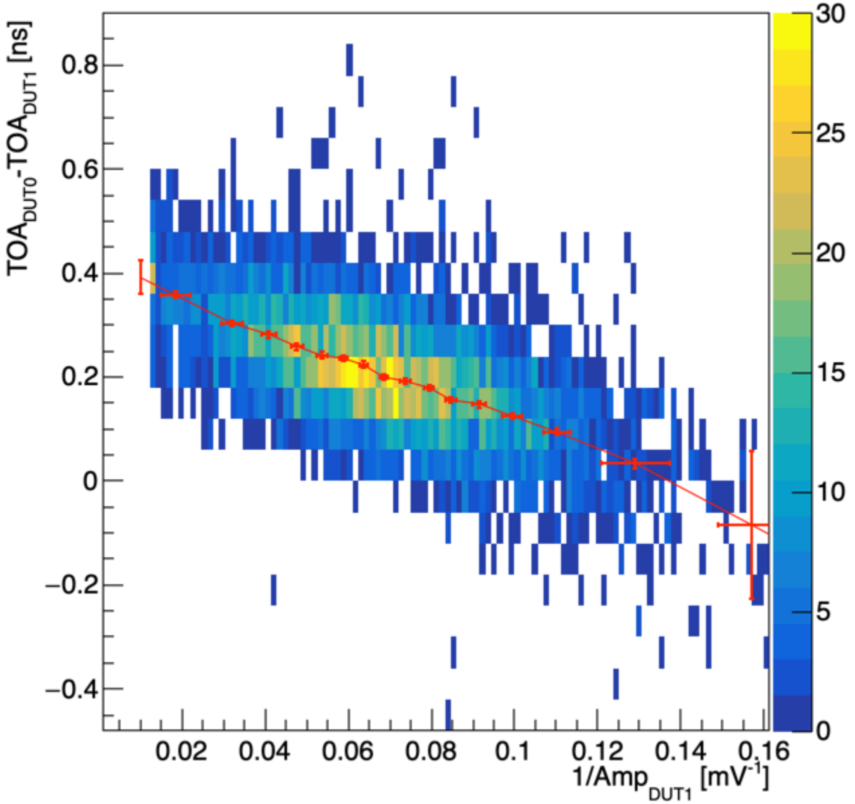
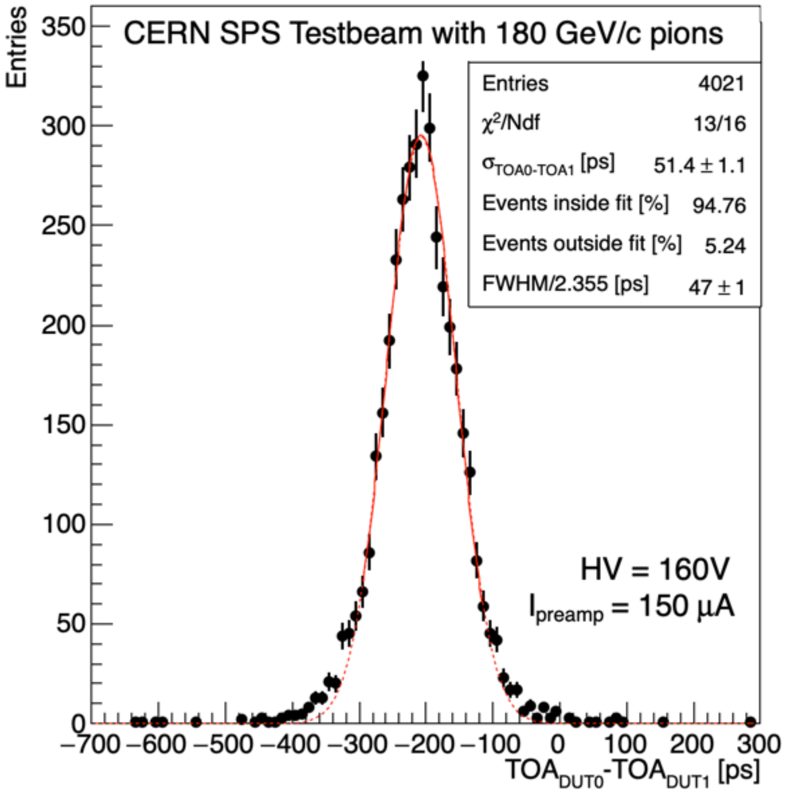
Corrected Time walk







- Correction performed with respect to inverse of signal amplitude for both DUTs.

$\sigma_t = 36.3 \pm 0.8$ ps

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Timing Resolution

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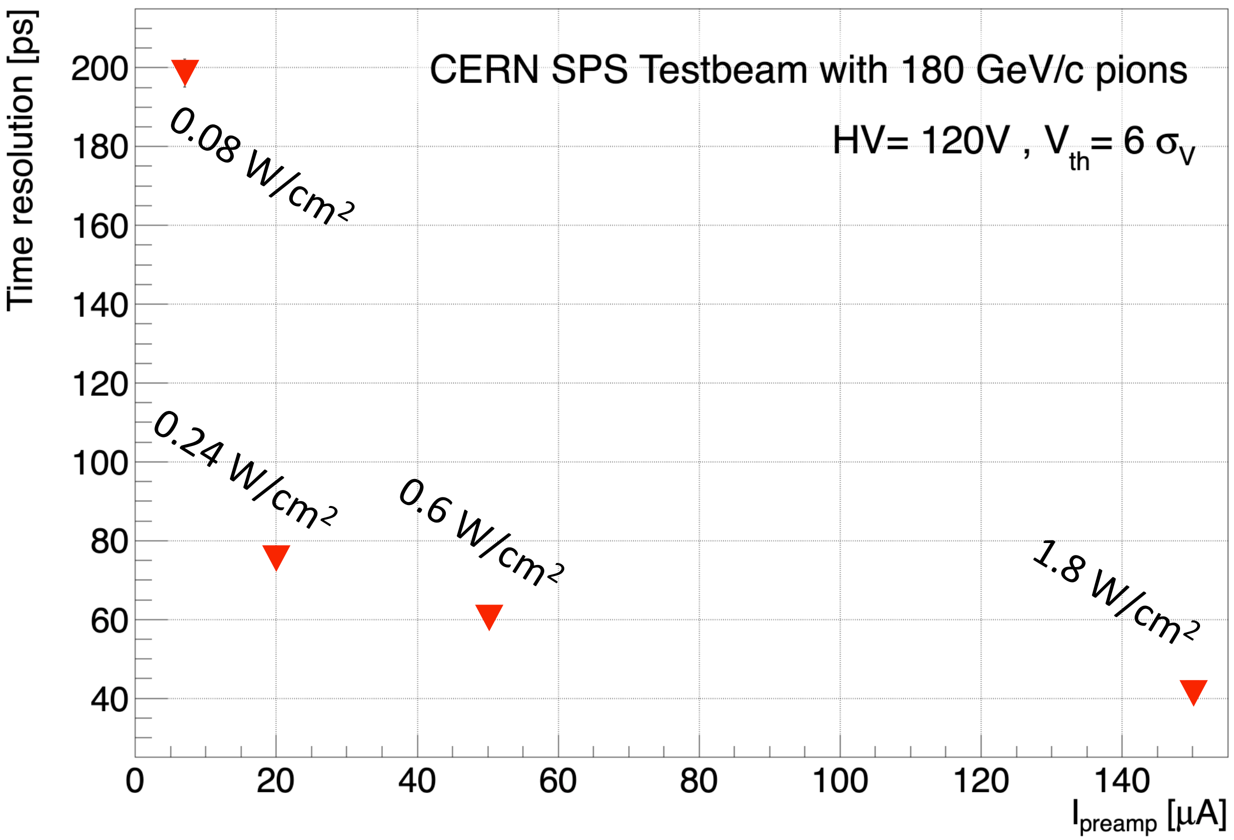

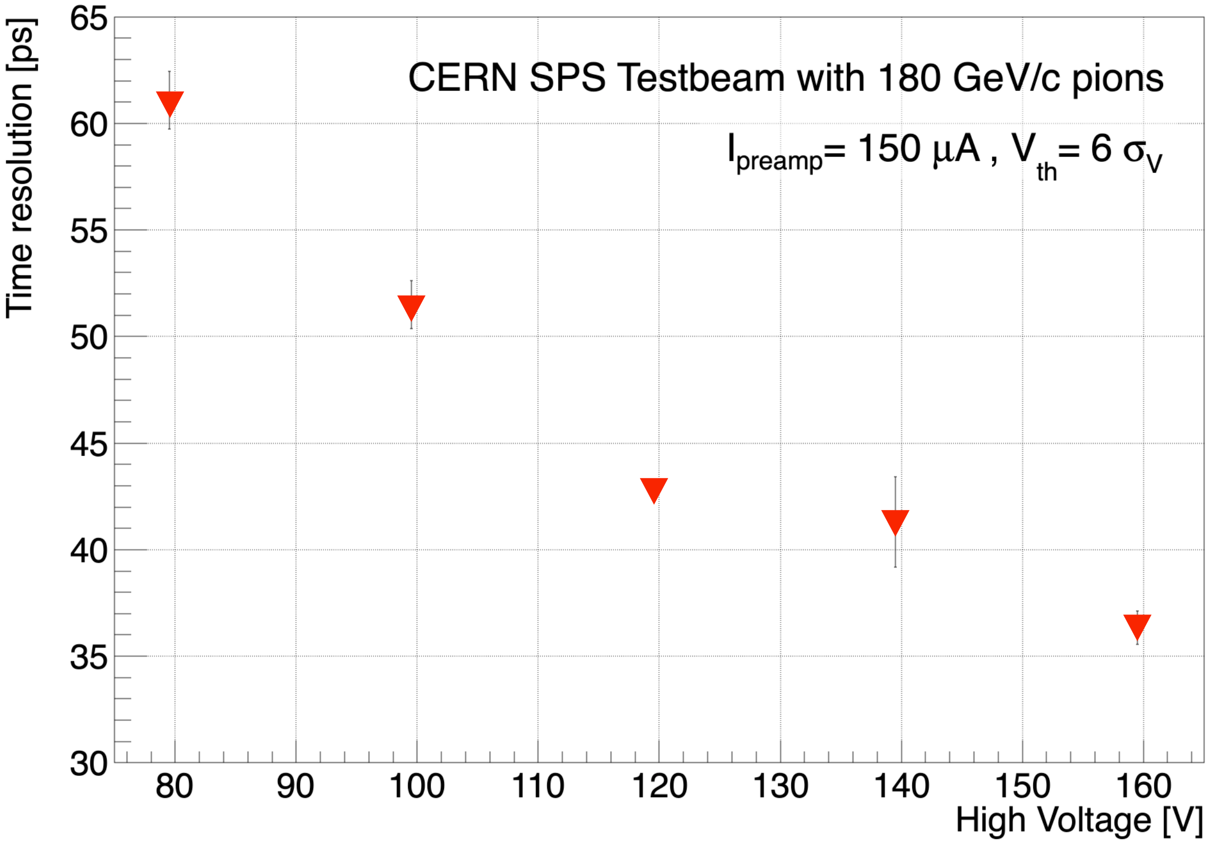

- Strong variation with power consumption as expect.
- Important degradation at 7 μA, still at the level of 200 ps.

- Time resolution varies between **60** and **36 ps** from 80V to 160V.
- Resolution at 160V is 20% better than at 120V.

Summary and Outlook

A monolithic silicon pixel sensor realized in SiGe BiCMOS 130nm process provides:

- Performance at **Power: 0.24 W/cm²** reaches 100 ps and 99.6% efficiency.
- Performance at **Power: 1.8 W/cm²** reaches 36 ps and 99.9% efficiency.

WITHOUT AVALANCHE GAIN LAYER

New sensor with integrated gain layer under study, results coming (very) soon !

Reference of paper: https://arxiv.org/abs/2112.08999

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Thanks for your attention

The MONOLITH Team:

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- project P.I.
- System design

Didier Ferrere
- System integration
- Laboratory test

Pierpaolo Valerio
- Lead chip design
- Digital electronics

Mateus Vicente
- System integration
- Laboratory test

Yana Gurimskaya
- Radiation tolerance
- Laboratory test

Stefano Zambito
- Laboratory test

Lorenzo Paolozzi
- Sensor design
- Analog electronics

Sergio Gonzalez-Sevilla
- System integration
- Laboratory test

Magdalena Munker
- Sensor design
- Laboratory test

Roberto Cardella
- Sensor design
- Analog electronics

Fulvio Martinelli
- Chip design

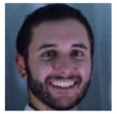
Yannick Favre
- Board design
- RO system

Stéphane Débieux
- Board design
- RO system

Théo Moretti
- Laboratory test

Antonio Picardi
- Chip design
- Laboratory Test

Chiara Magliocca
- Laboratory test



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Jihad Said
- Laboratory test

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Marzio Nessi
CERN & UNIGE

Ivan Peric
KIT

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Sensor design

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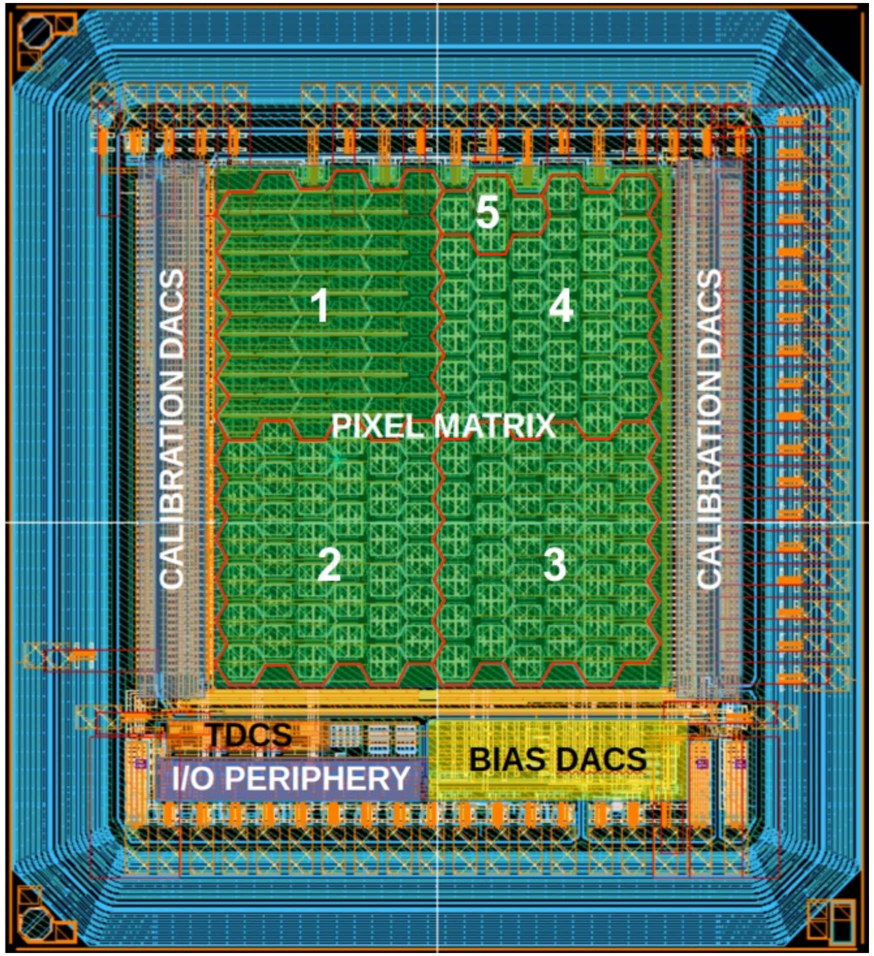

ASIC prototype with 12x12, 65µm side hexagonal pixels with 80fF capacitance come in different “flavors”:

1. Active pixel
   - Front end in pixel
   - HBT preamplifier + driver (in pixel) + CMOS discriminator (outside pixel)
2. PET-project version:
   - HBT preamplifier + CMOS discriminator
3. Limiting amplifier:
   - HBT preamplifier + HBT limiting amplifier
4. Double Threshold
   - HBT preamplifier + two CMOS discriminators

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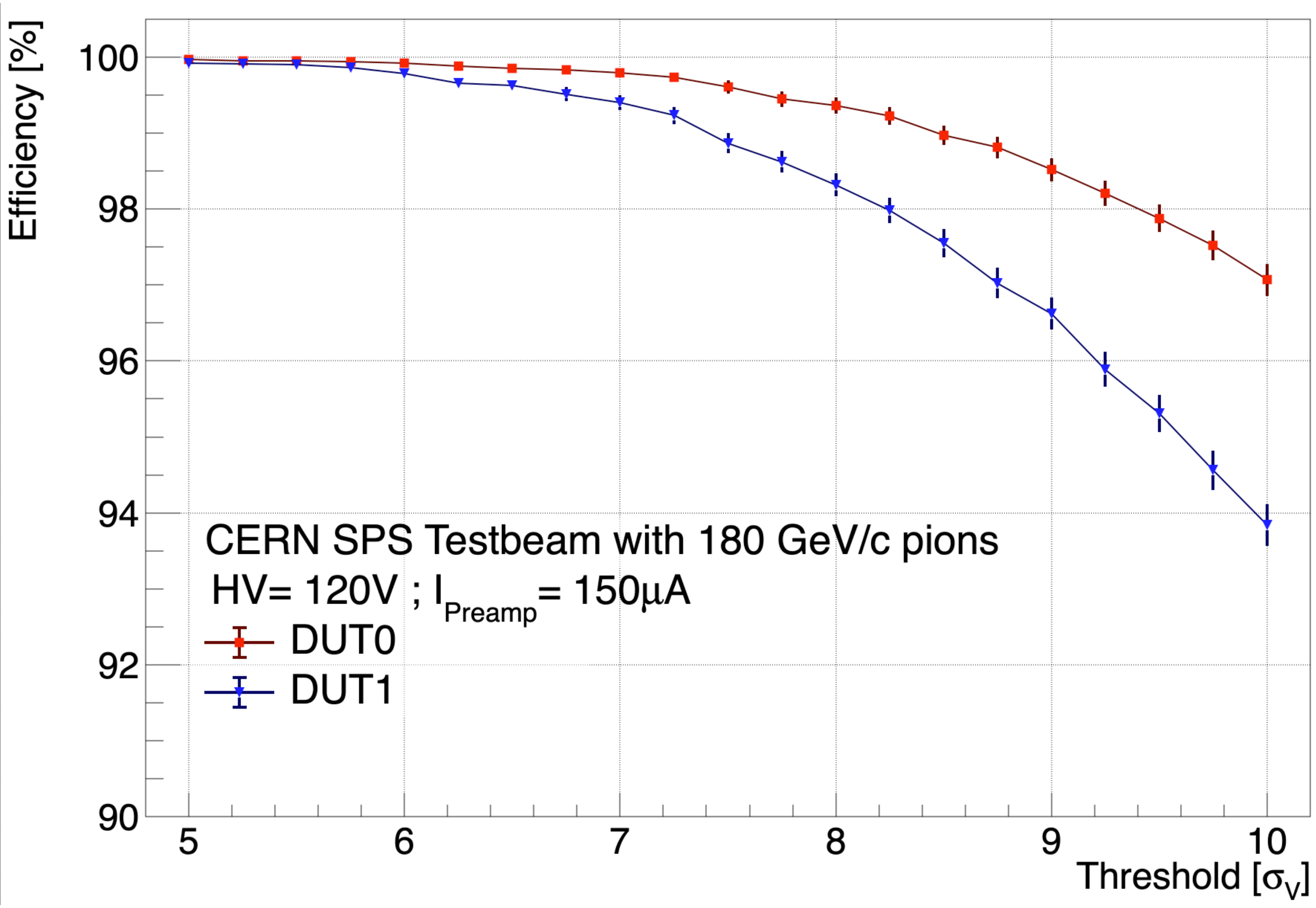
Efficiency Threshold scan



- Both DUT reach efficiency plateau at **6 standard deviation** from noise (σ_V), well above 99%.
- Clear difference in performance between the two sensors.
- Trend can be explained by the **difference in ENC**. (76 ± 1 electrons for DUT 0 and 82 ± 1 electrons for DUT 1)