Status of the Caribou DAQ System

Eric Buschmann

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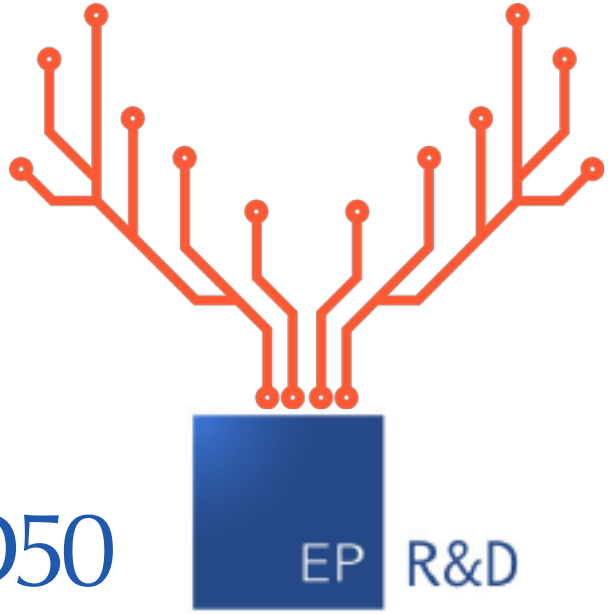
Motivation

- Motivation: Many different silicon detector technologies under investigation
  - Similar DAQ requirements: readout, control, powering for most silicon pixel detectors
  - Differences in voltage levels, number of channels (data/voltage) or protocols

- Goal: Provide a versatile DAQ system which
  - Offers re-usable hardware, firmware and software components
  - minimizes device integration effort
  - reduces time to get first data from a new detector

The Caribou Data Acquisition System

- Open source hardware, firmware and software for laboratory and high-rate beam tests
- Developed & maintained by collective effort



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DESY.

RD50

EP R&D

- Supported devices:
  - H35Demo/FEI4, ATLASPix/2/3
  - CLICTD, CLICpix2/C3PD
  - RD50-MPW1/MPW2
  - FASTPIX
  - DPTS, APTS

AIDA innova

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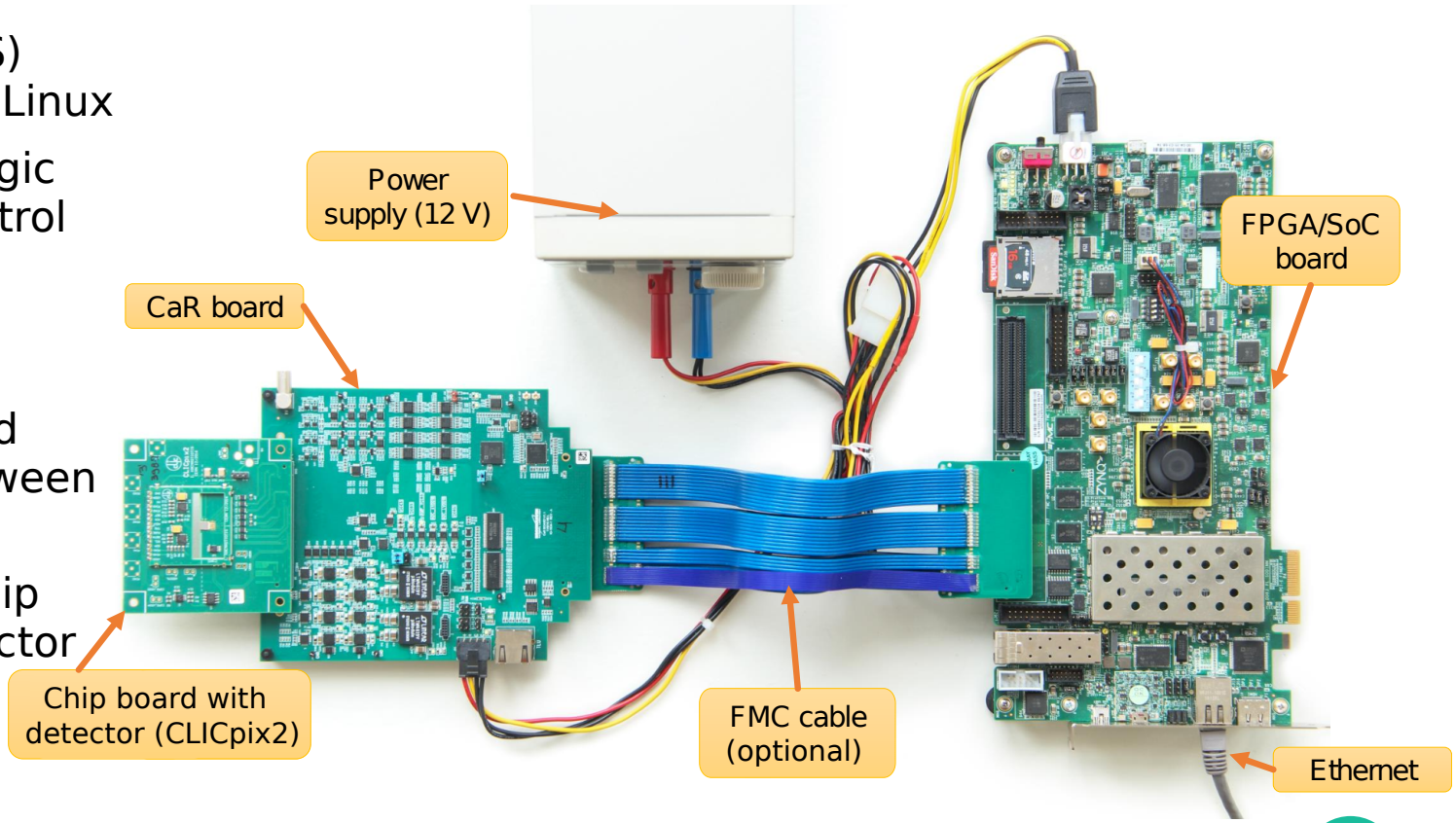
http://dx.doi.org/10.1088/1748-0221/12/01/P01008 http://dx.doi.org/10.22323/1.370.0100

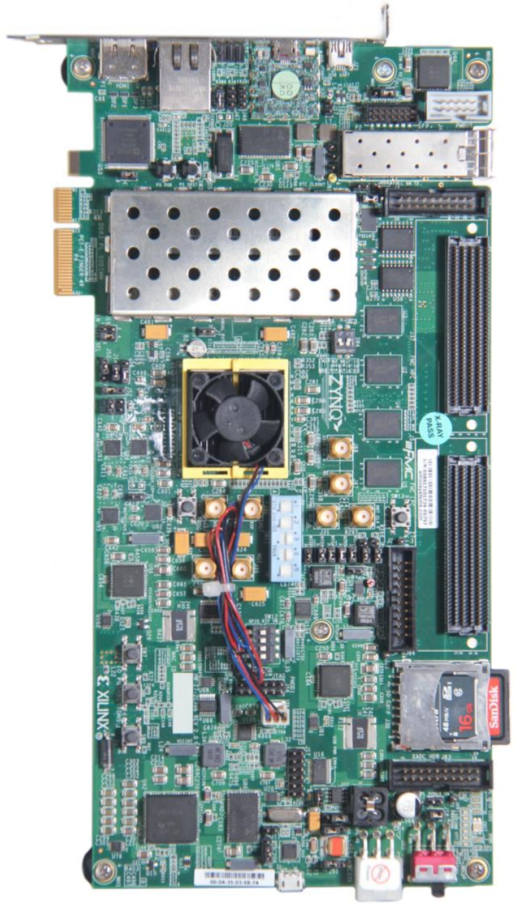
System Overview

- System on Chip (SoC) Processing System (PS) runs DAQ software on Linux
- SoC Programmable Logic (PL) runs detector control and data processing firmware
- Periphery CaR board provides resources and physical interface between SoC and detector
- Application-specific chip board containing detector



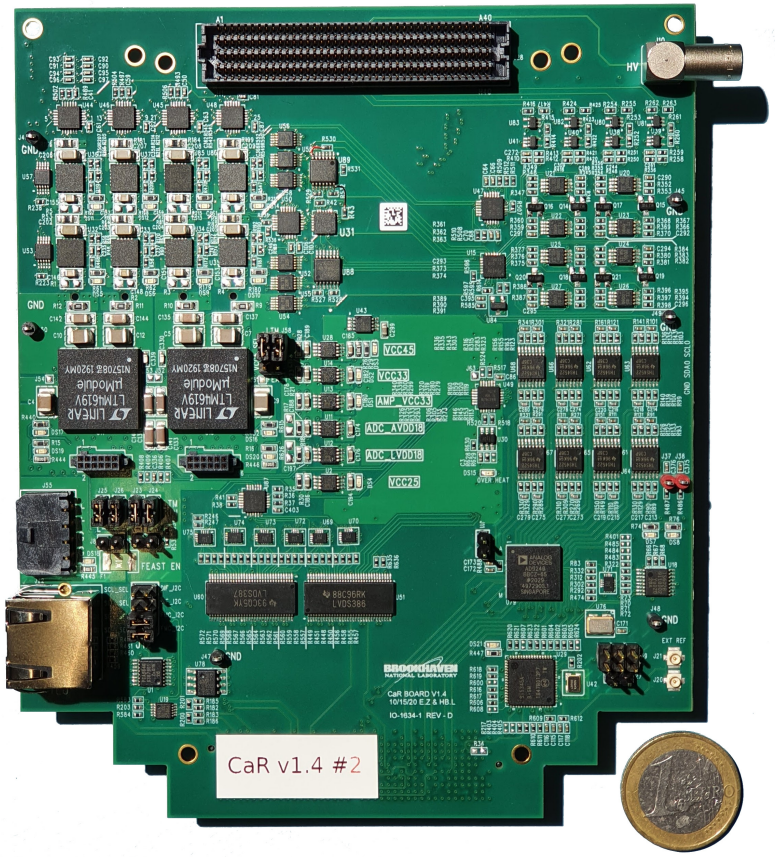
The Hardware: SoC Evaluation Board

- Based on Xilinx Zynq series, currently supported: ZC706
  - PS (embedded ARM CPU) runs full Linux operating system
  - Standalone machine, connect to via Ethernet (ssh)
  - Runs DAQ software (Peary)
  - Allows to run data analysis (quality monitoring) locally
  - Data stored locally (on SD card) or on network-mounted storage (NFS, …)
- PL runs custom firmware blocks for data processing, detector control
  - Interface between FPGA fabric and CPU available
  - Firmware for signalling & lower layers of communication protocols
  - Possibility to (pre)process data in hardware
  - DMA (direct memory access) for higher DAQ bandwidth

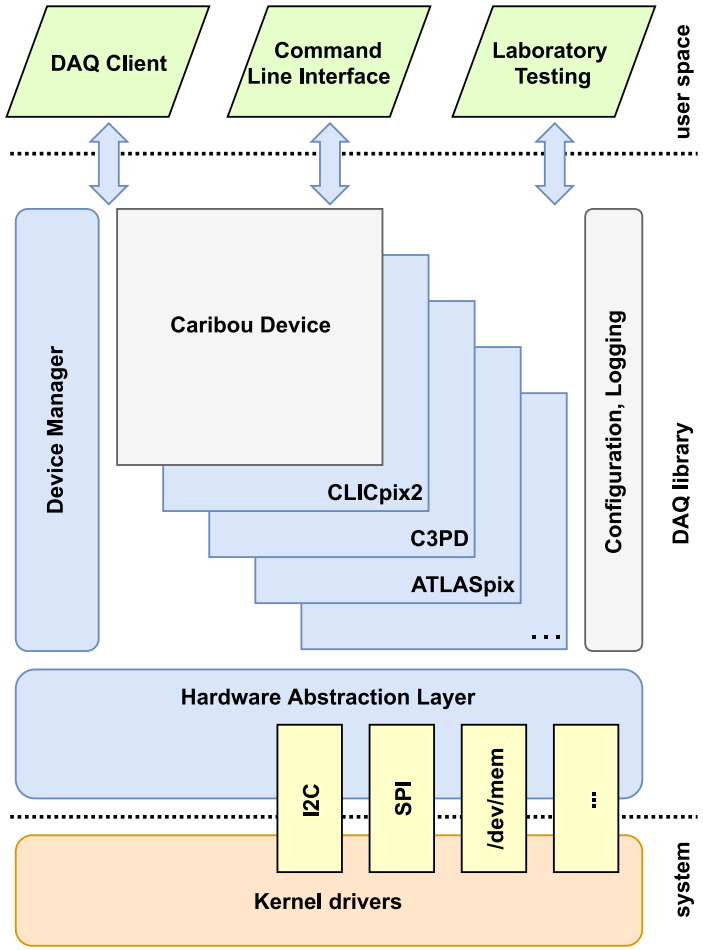


The Hardware: Control and Readout Board (CaR)

- Provides physical interface from the FPGA/SoC to the detector chip and hardware resources
  - 8 adjustable power supplies with monitoring (0.8 – 3.6 V, 3.
  - 32 adjustable voltage references (0 – 4 V)
  - 8 adjustable current references (0 – 1 mA)
  - 8 voltage inputs to slow (50 kSPS) 12-bit ADC (0 – 4 V)
  - 16 analog inputs to fast (65 MSPS) 14-bit ADC (0 – 1 V)
  - 4 programmable injection pulsers
  - 8 full-duplex high-speed GTx links (<12 Gb/s)
  - 17 LVDS links (bidirectional)
  - 10/14 output and input links, adjustable level (0.8 – 3.6 V)
  - Programmable clock generator, External inputs for high voltage, clock reference, trigger
  - Interfaces: FMC to FPGA, 320-pin SEARAY to detector



Firmware and Software

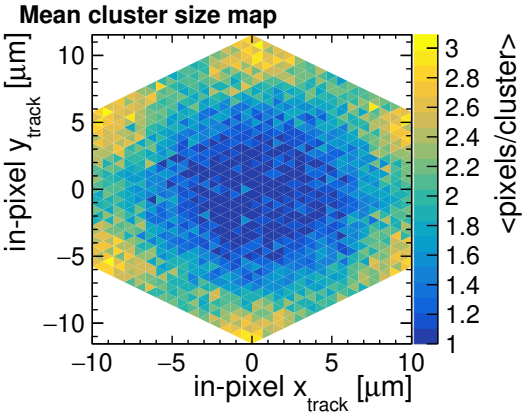


- **Firmware**: Based on combination of custom Caribou modules and commercial Xilinx IP cores
  - Provides an interface between CPU (SW) and a detector (HW)
  - Modules are connected to CPU through AXI bus
  - Registers are mapped to CPU memory space (/dev/mem)
- **Software Stack**: Custom **Yocto**-based Linux distribution (meta-caribou)
  - Common Linux tools and packages are pre-installed (ssh, python etc.)
  - Includes Caribou software (EUDAQ, Peary)
- **DAQ Software Framework**: **Peary**
  - Hardware Abstraction Layer (HAL) to handle peripherals as objects in C++
  - Functions to control CaR board, set/measure voltages, capture ADC, ...
  - Various user interfaces: command line, scripting, EUDAQ2 producer for test beam integration

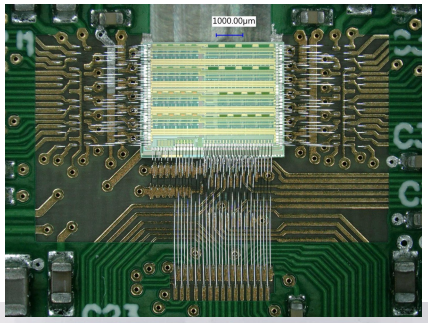
ATTRACT FASTPIX Integration

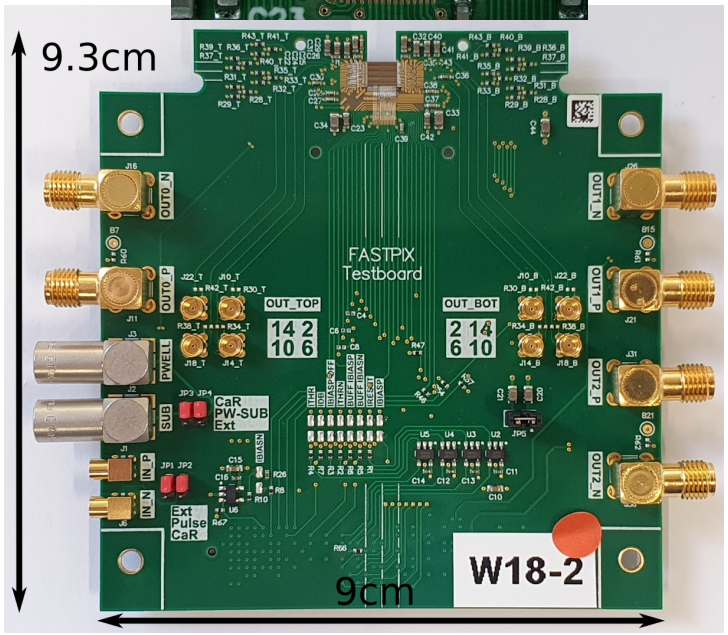
- Technology demonstrator for monolithic pixel detector with sub nanosecond timing in modified 180nm process
  - Hexagonal pixels with 8.66 .. 20µm pitch
- Optimised for fast charge collection and good time resolution
  - → Requires good timing reference: Microchannel Plate PMT (MCP-PMT)
- Time-based encoding of hit position and ToT on 3 digital channels
  - Readout of FASTPIX and MCP with oscilloscope integrated into Caribou
- Several campaigns with FASTPIX in CLICdp Timepix3 telescope at SPS in 2021/22

J. Braach
Wed. 12:40



Wafer 15, 20µm pitch, -6V bias

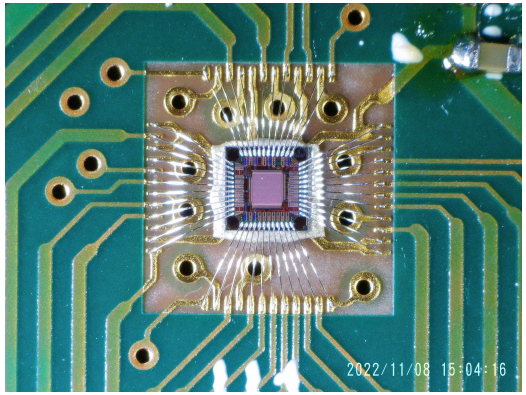


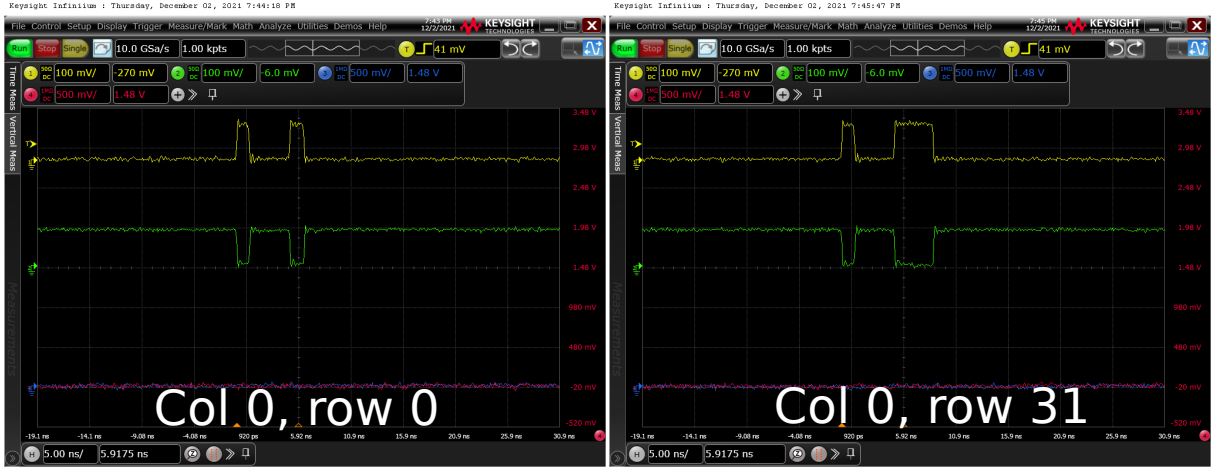


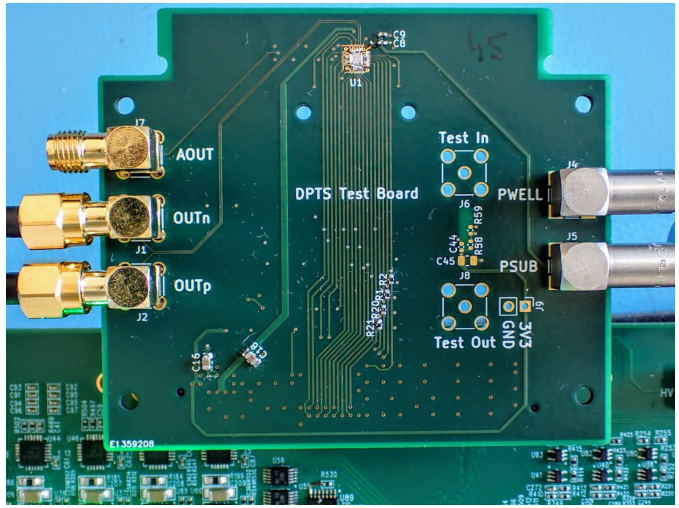
T. Kugathasan et al.: https://doi.org/10.1016/j.nima.2020.164461

Digital Pixel Test Structure (DPTS)

- Monolithic test chip in 65nm process with asynchronous readout scheme (similar to FASTPIX)
  - Developed within the CERN EP R&D programme
  - 32 x 32 matrix with 15 x 15µm² pixels
  - Powered and configured from Caribou
- Time-based encoding of hit position and ToT on single digital channel
  - Readout with oscilloscope via Caribou

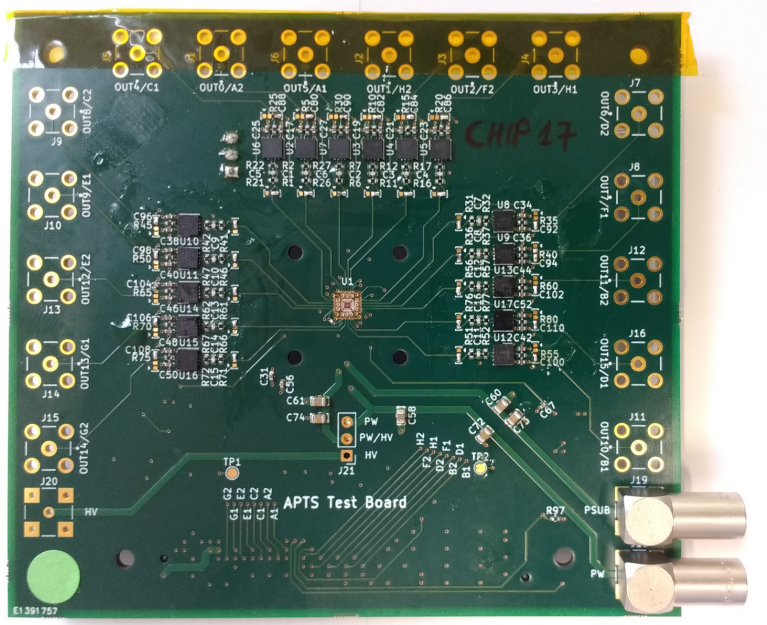


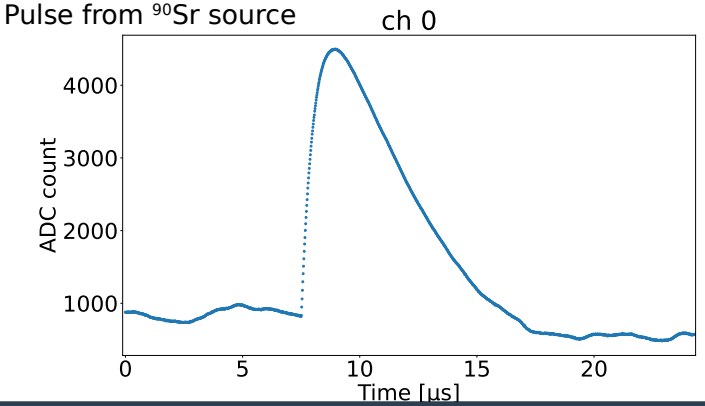


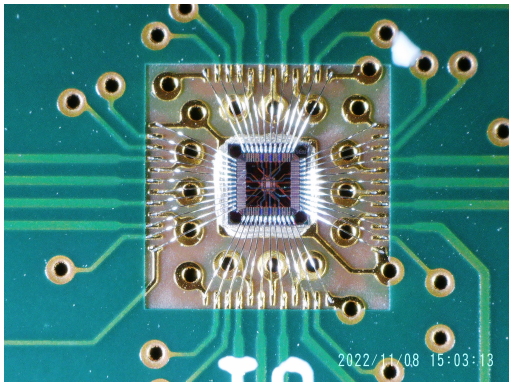


Analog Pixel Test Structure (APTS)

- Monolithic test chip in 65nm process aimed at sensor characterization
  - Developed within the CERN EP R&D programme
  - 4x4 matrix with 10..25µm pixel pitch
  - 16 buffered analog channels
- Amplification and shaping of signal on chip board
- Readout with 65 MSPS ADC on CaR board
  - Alternatively: individual channels on SMA connectors
  - Custom firmware block for ADC readout via DMA
  - Configurable trigger logic
    - Internal trigger with programmable thresholds, adjustable latency, dead time...
  - Supports AIDA Trigger Logic Unit (TLU) for readout in beam telescope

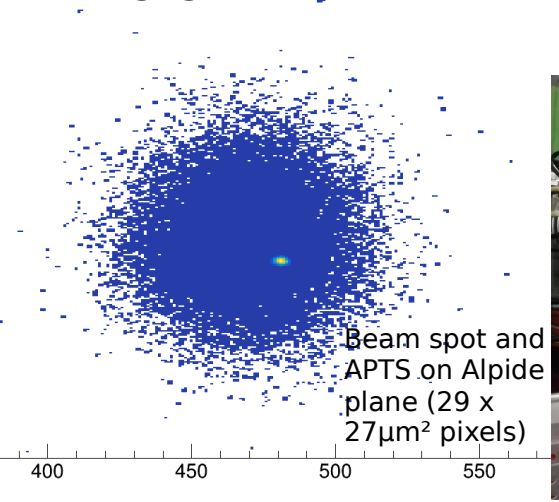




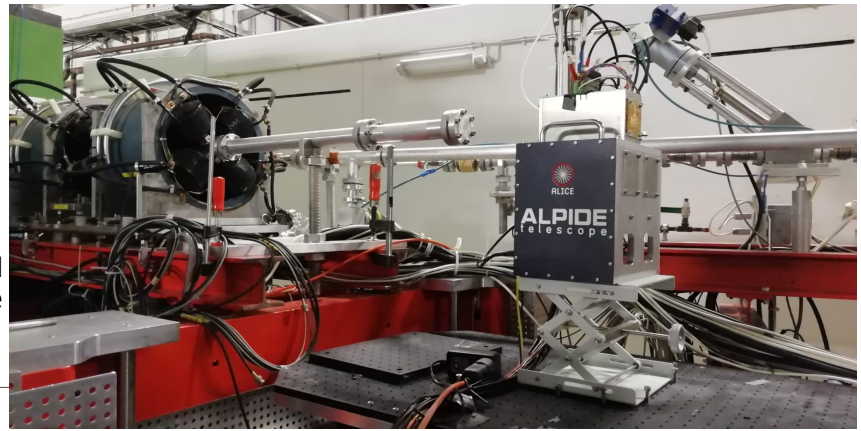


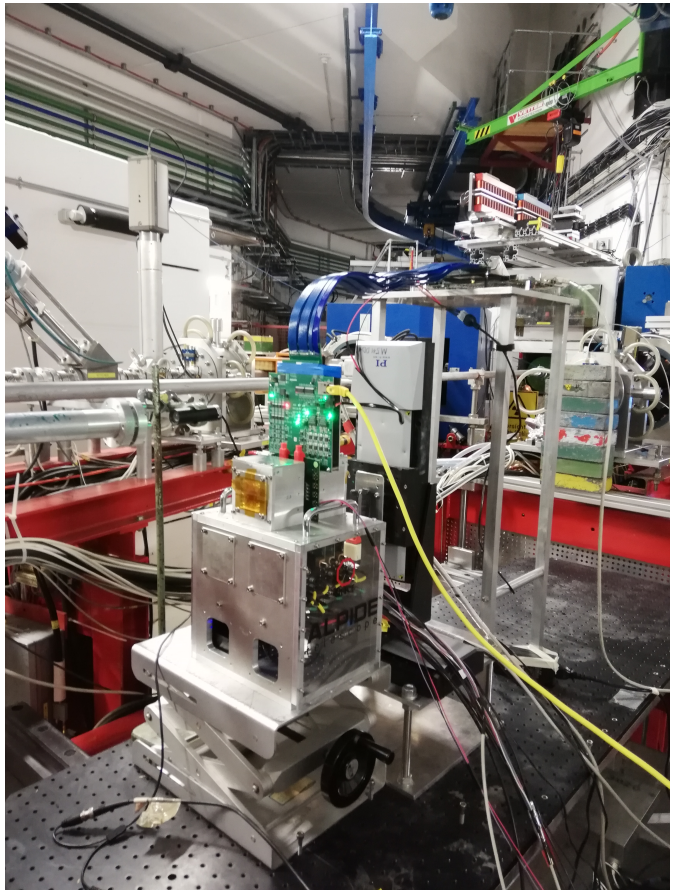
Analog Pixel Test Structure (APTS)

- Beam test with APTS at the MAinz MIcrotron (MAMI) in April 2022
  - 855 MeV electrons (up to 1.5 GeV)
  - O(1 mm²) beam spot
- Tracking with Alpide telescope
- Triggered on APTS or scintillators in anti-coincidence
- Discovered and fixed issues with ADC readout
- Analysis is ongoing, testing continues at DESY and planned for SPS



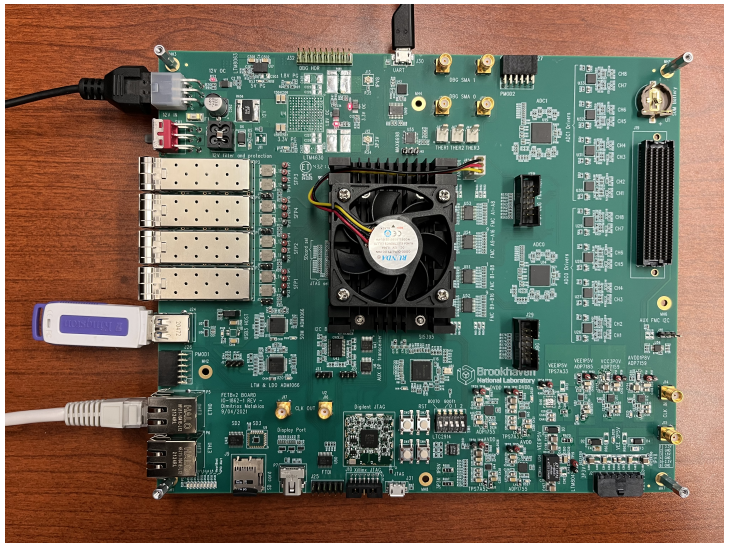
Beam spot and APTS on Alpide plane (29 x 27µm² pixels)





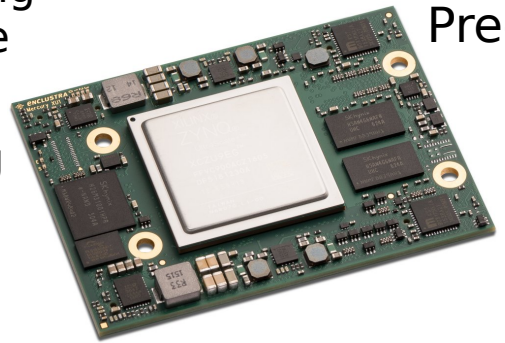
Conclusions and Outlook

- Caribou system supported and used by various collaborations
- Support for new devices added to Caribou
- Strong & continued collaboration on future Caribou system development and support



Pre-prototype for Caribou 2.0

- New hardware for Caribou 2.0 in progress
  - Reduce size and cost by integrating CaR board with system-on-module
  - Upgrade to UltraScale+ Zynq
  - 64 bit platform and increased CPU performance
  - Under development at BNL



Enclustra Mercury+ XU1 SOM

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