First test-beam result on MAPS prototypes in 65 nm process

Tangerine project at DESY

Gianpiero Vignola, on behalf of the Tangerine Collaboration BTTB10, Lecce, 22 Jun 2022





Tangerine Project overview

New Pixel Detector for Beam Telescopes

- **Goal**: Design a monolithic pixel detector in 65nm CMOS imaging technology
 - Main application: beam telescope
 - **Potential applications**: e⁺ e⁻ colliders, etc.
- Requirements:
 - Position resolution: ~ 3µm
 - Rate capabilities: 1 MHz particle rate
 - Time resolution: ~ 1-10 ns
 - Energy measurement via ToT
 - Low material budget: $< 0.05\% X/X_0$
- Founded By InnoPool & DESY
- Tangerine project start in Sep. 2020



MIMOSA Beam Telescope, DESY II Test Beam Facility



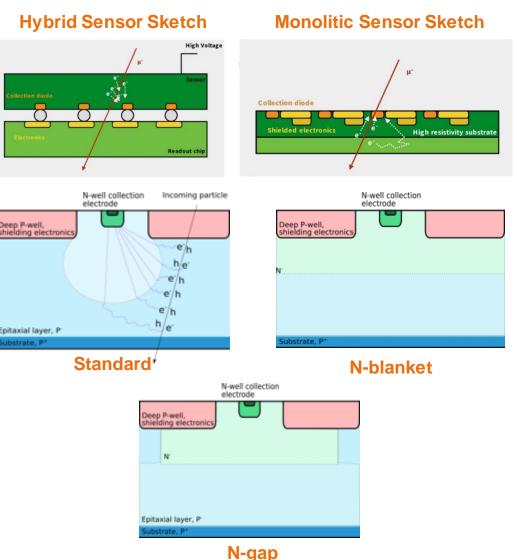


TowArds Next GEneRation SilicoN DEtectors

Tangerine Project overview

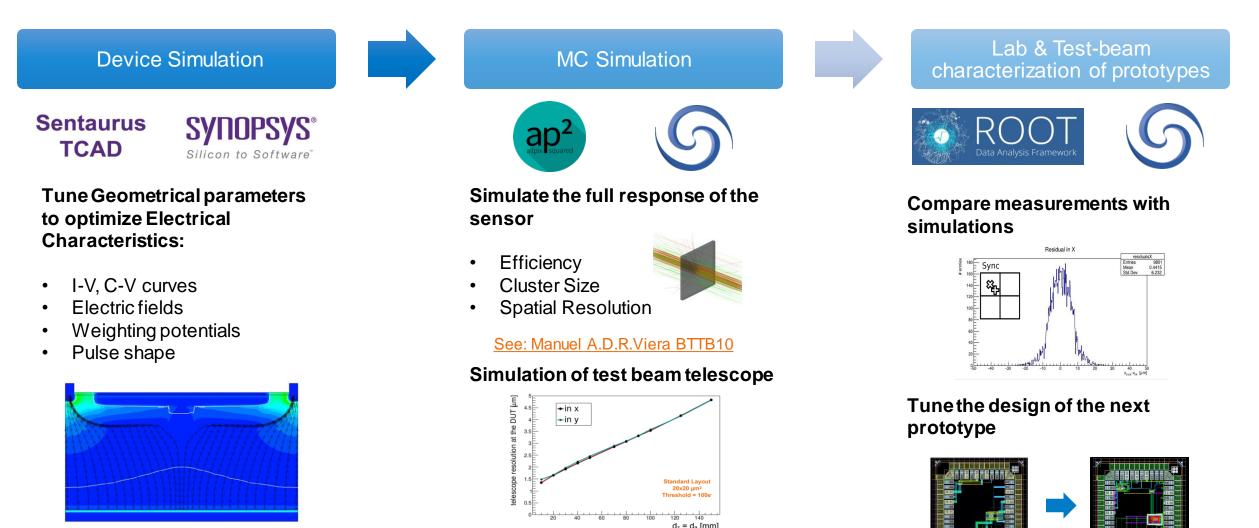
Why Monolitic Active Pixel Sensor in 65 nm CMOS imaging process?

- Reduce: Material budget, Production cost & Complexity
- Recent improvements thanks to ALICE ITS & MALTA:
 - 180 nm CMOS imaging process
 - Small collection electrode (reduce noise and power consumption order ~40 mW cm⁻²)
 - Spatial resolution ~ 5 μ m
- Three layouts under study for the **sensitive volume design**: Standard, N-blanket, N-gap
- 65 nm process allows:
 - Higher logic density -> small pixel pitch and/or increase in-pixel functionality (fast CSA, in-pixel ToT)
 - Further decrease in power consumption



Tangerine Project overview

Workflow: from simulations to test-beam



See: Sara Ruiz Daza BTTB10

See: Adriana Simancas BTTB10

Tangerine MLR1 Chip Details

2020

Dec-2020

2 Test structures

DESY MLR1 timetable

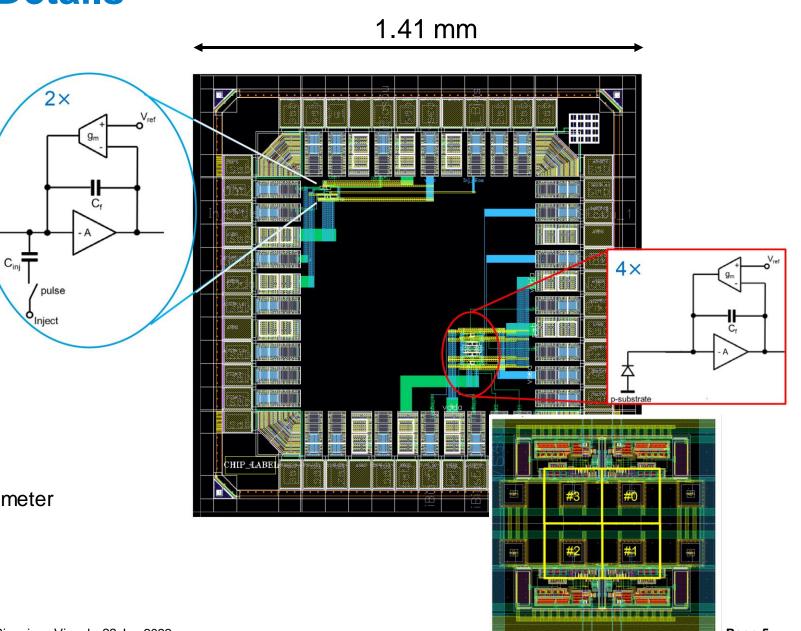
- Chip design
- Submitted to foundry
- prototype in Hamburg October 2021

2 CSAs with different gains

- a) feedback cap $1.5 \text{fF} \rightarrow 107 \mu \text{V/e}$
- b) feedback cap 2.0fF \rightarrow 80 μ V/e-
- Use Charge injection as stimulus
- No Pixel diode
- Aim: Evaluation of CSA performance

Block of 2x2 pixel with CSA

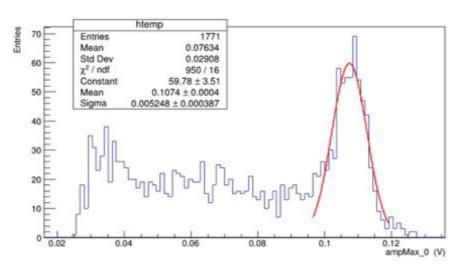
- **Gain**: 80 µV/e- , Cf = 2fF (typ)
- Sensing node: nwell hexagon 1.2µm diameter
- **Pitch**: 16 µm
- outputs: 4 analog read-out
- Aim: Pixel characterization

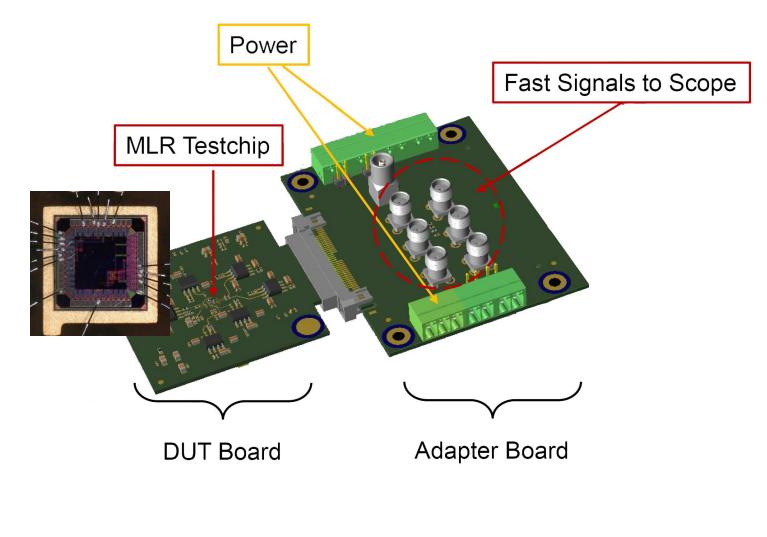


Tangerine MLR1 Chip at DESY

October 2021

- MLR1 Chip arrived at DESY in early October 2021
- Chip glued and bonded on **DUT board**
- First **tests on CSAs** comparing them with simulations. Evaluation of: Gain, Delay, Rise Time, Falling edge
- First waveforms obtained with Fe⁵⁵ source





DESY Test Beam

18 Oct - 01 Nov 2021

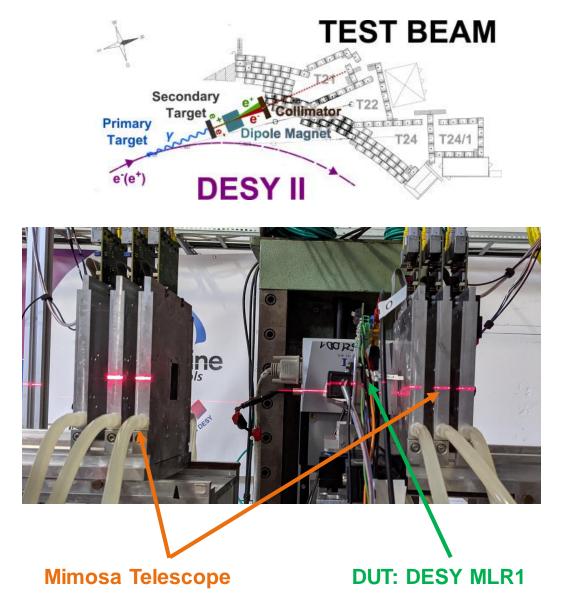
Setup

- Electron beam, 2-5 GeV
- Oscilloscope based Read-out of 4 pixels
 Full waveforms stored (4GHz 10 Gs/s)
- Mimosa telescope used for track reconstruction
- Self-Trigger of MLR1 (OR of Scope Channels)

Results

- Event rate: 1 event every 5-15 minutes
- MIP response: order of 50 mV
- Rise time: 5-10 ns
- Slew rate: on the order of mV/ns

Rate too low at DESY Facility, gained confidence with the Chip & preliminary results



CERN Test Beam

SPS, 10 - 15 Nov 2021

Setup

- Pion beam, 120 GeV, 1e6 per spill
- Oscilloscope based Read-out of 4 pixels
 Full waveforms stored (4GHz 10 Gs/s)
- Timepix3 telescope used as reference
- Self-Trigger of MLR1 (OR of Scope Channels)

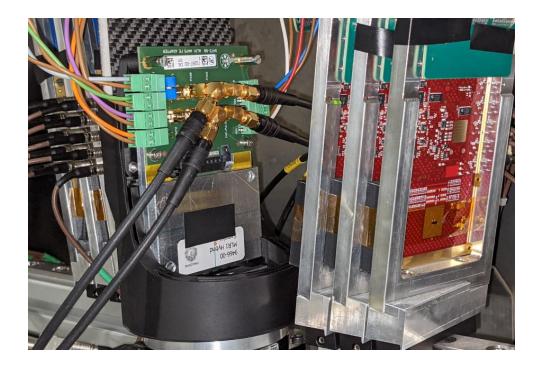
Results

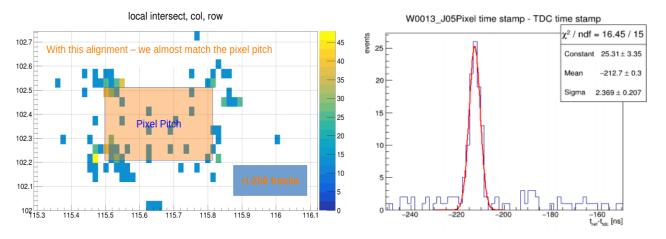
- Scope trigger correlate nicely in time -> time resolution ~ few ns
- After tracks reconstruction **pixel structure** is recognizable
- event rate extremely lower than expected!

Discovered a sensor layout issue in DESY MLR1 Chip that affect the efficiency of device

Thanks to the SPS testbeam support team





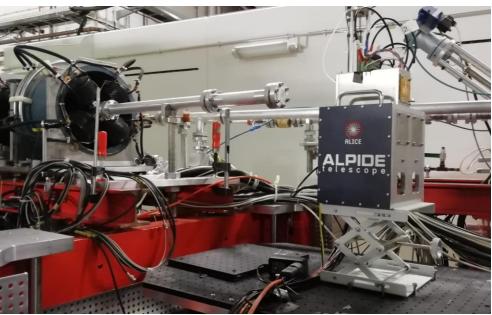


Mainz Test Beam

MAMI Microtron, 02 – 06 Dec 2021

Setup

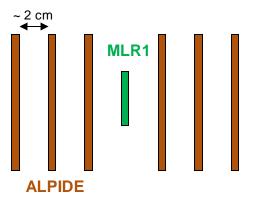
- Electron beam, 855 MeV
- Beam Imax: ~ 100 μA
- Beam size: ~ 1mm²
- ALICE ALPIDE Telescope used as reference
- **Self-Trigge**r of MLR1 (OR of Scope Channels)

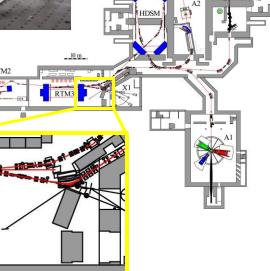


Results

- Recorded events: > 500k (few µm² of active area)
- Bias & Current scans on Pixel & CSA
- Detailed Waveform analysis

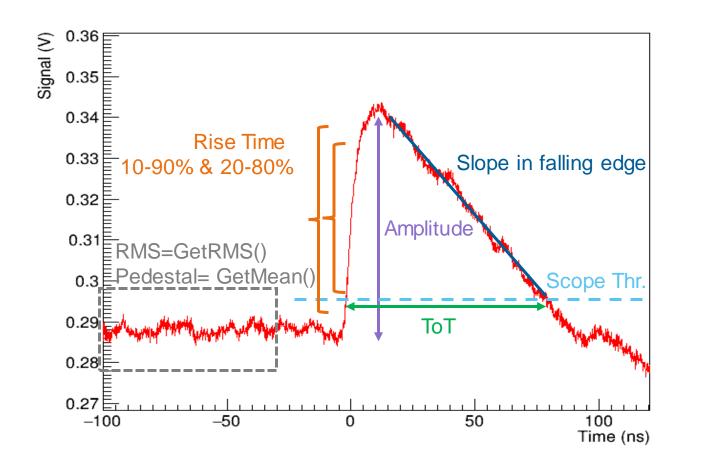
Thanks to the MAMI testbeam support team

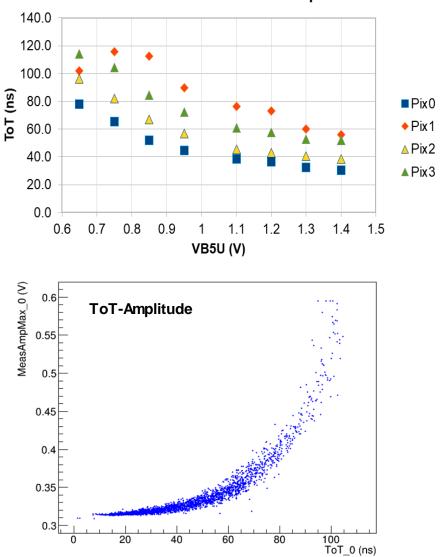




Mainz Test Beam: Results

Waveform Analysis with ROOT

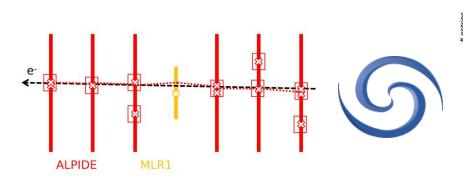




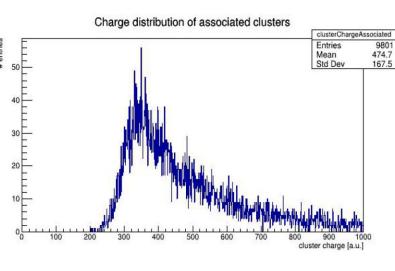
Mean Time over Threshold Sample #7

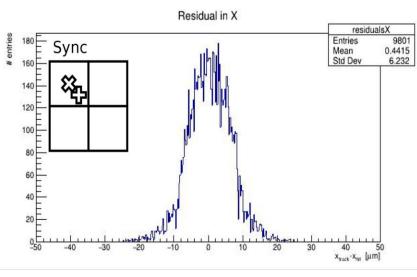
Mainz Test Beam: Results

Corryvreckan Analysis

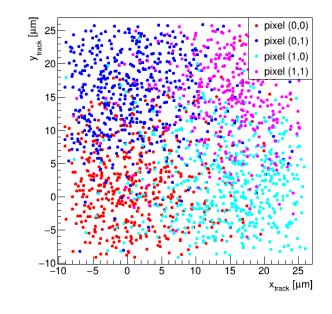


- Corryvreckan uses hit ⁽²⁾ (pixels above threshold) and Clusters □ (groups of adjacent hits) to recontruct particles trajectories ····
- Residuals (Difference between positions from track interpolation and DUT meas) ~ 6µm is dominated by ALPIDE resolution and low beam momentum





1-pixel cluster map



55

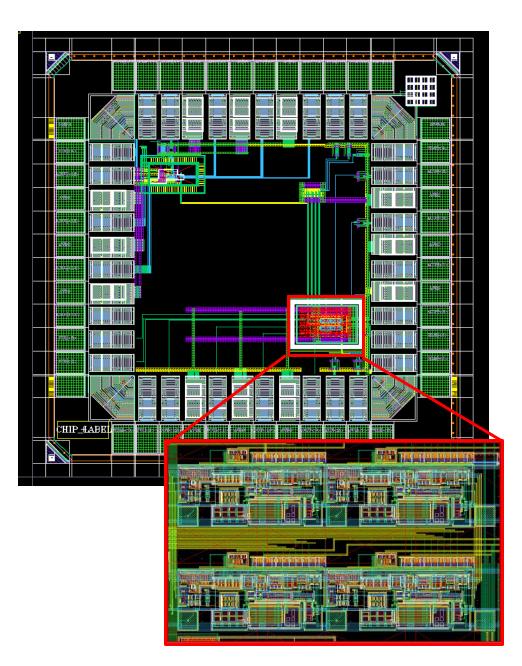
-45

Work in progress & next

not only MLR1

Design of the **next TANGERINE prototype** submitted (ER1 Submission):

- 4x4 pixel (35x25 µm²) matrix with all in pixel functionality
- External access to CSA and discriminator output
- N-blanket with gap layout with 2.5 µm and 4 µm gap
- Single Front-End with Injection
- Expected in Hamburg in early 2023

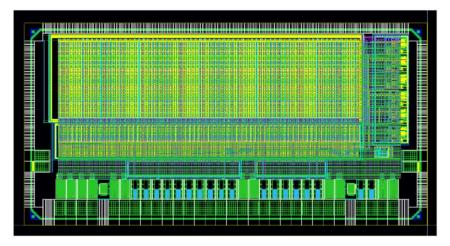


Work in progress & next

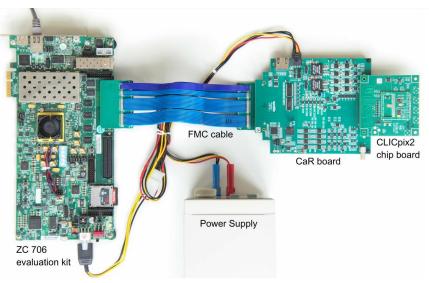
not only MLR1

H2M (Hybrid-To-Monolithic):

- Collaboration of DESY, CERN and IFAE
- $3 \times 1.5 \text{ mm}^2$, 64 x 16 square pixel, 35 µm pitch
- 8-bit counter per pixel
- 4 acquisition modes:
 - Time of Arrival (ToA)
 - Time over Threshold (ToT)
 - \circ Photon counting
 - Triggered binary readout
- Expected in Hamburg in early 2023 (ER1 Submission)



H2M ASIC design



http://dx.doi.org/10.22323/1.370.0100

Conclusions

Results from the tangerine MLR1 Chip

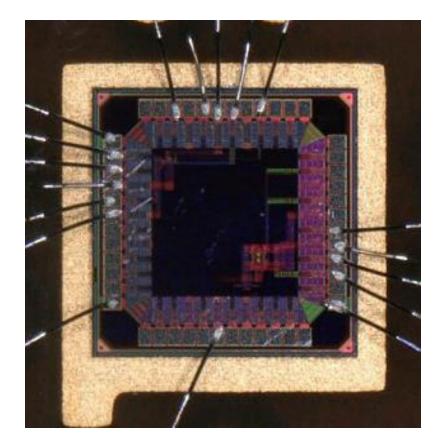
- A 65 nm CMOS pixel detector was for the first time developed & investigated at DESY
- DESY MLR1 Chip allowed the **first tests on designed CSAs** with the direct study of the waveforms
- Results of the studies on MLR1 allowed improvements in the **next prototype**
- The Tangerine group is now focused on TCAD studies, Allpix² simulations & test on other MAPS prototype in preparation of **next submissions**
- Results of Tangerine MLR1 Chip confirm the MAPS technology as good candidate for the next generation of pixel detector for beam telescopes
- Thanks for the great support from CERN EP R&D in MLR1 submission







TowArds Next GEneRation SilicoN DEtectors



Thank you

Contact

Deutsches Elektronen-Synchrotron DESY Gianoiero Vignola ATLAS gianpiero.vignola@desy.de

www.desy.de

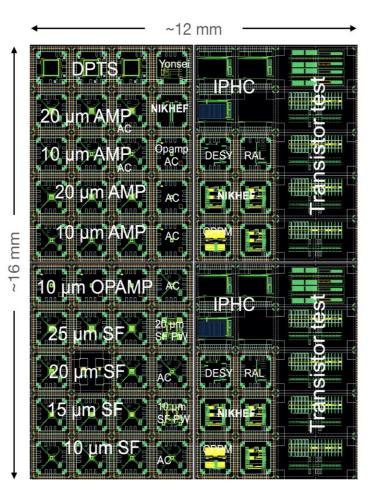
Backup

MLR1 production

Multi Layer Reticle 1

- Wafer divided up into "sites" of 1410x1410 µm for different test chips shared between DESY, CERN, RAL, Nikhef, etc.
- TJ 65nm ISC Process limitations in MLR1:
 - Only 3+1 metal layer
 - \circ 10µm epitaxial layer
- MLR1 timetable:
 - Design submitted
 - MLR1 at CERN
 - DESY MLR1 in Hamburg

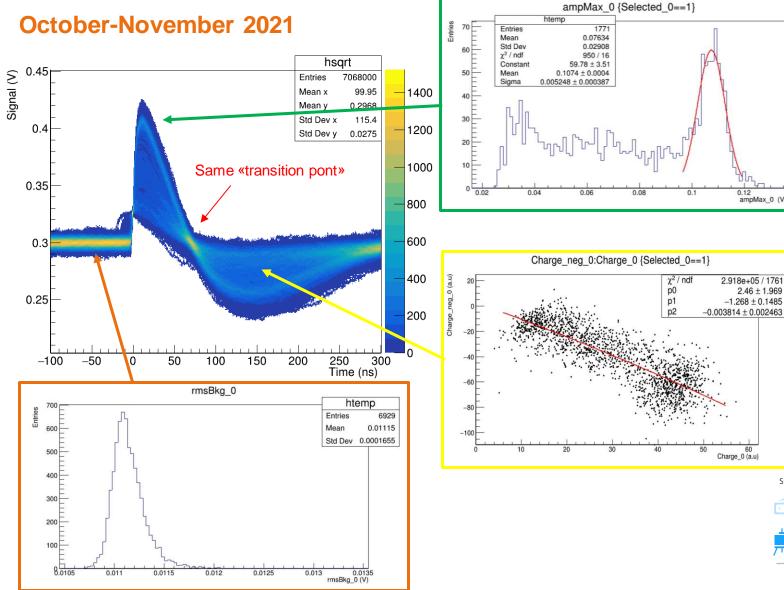
Dec-2020 June 2021 October 2021



expect O(500) dies per wafer



Fe⁵⁵ source studies



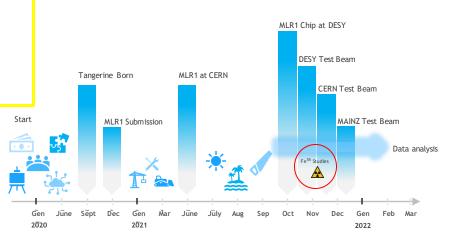
Example reported:

- Sample ID: 4 pixel 0
- Exposure time: ~ 1 night
- # Trigger: 6929 (all 4 channels)
- Thresholds: 20 mV over noise

Signal amplitude Expected:

(@ Christian Reckleben)

- K_{α} : 5.8 keV \rightarrow ~ 1590 e-
- @ Cf = 2fF $\pm 10\% \rightarrow \sim 127 \text{ mV}$
- Gain $1.33 \rightarrow \sim 168 \text{ mV} \pm 10\%$

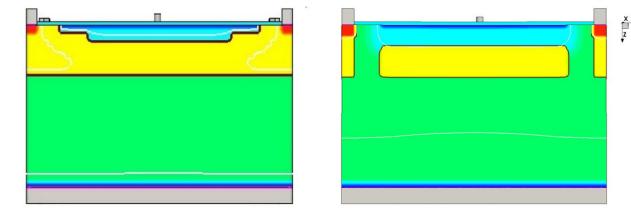


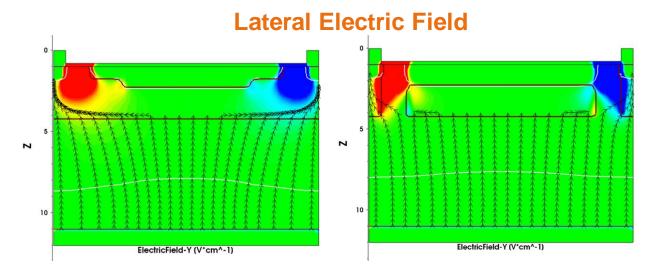
MLR1 Real Chip

Doping Concentration

Explanation for the low efficiency of the chip

- The very low rate at DESY and CERN prompted an in-depth analysis of the MLR1 chip
- After Interactions with CERN people involved in MLR1 production, a sensor layout issue in DESY MLR1 Chip was found
- TCAD simulations confirmed that the chip cannot perform as expected
- The expected efficiency is now ~ 0.5%





Expected MLR1 Pixel

Real MLR1 Pixel

@ A. Simancas

Mainz Test Beam: Results

Waveform Analysis with ROOT, sample #7

- IB5U scan (amps bias current) 4-14 µA (VB5U 0.65 1.4 V)
- VSUB scan (pwell sub voltage, sensor cathode) 1.25 2.2 V

