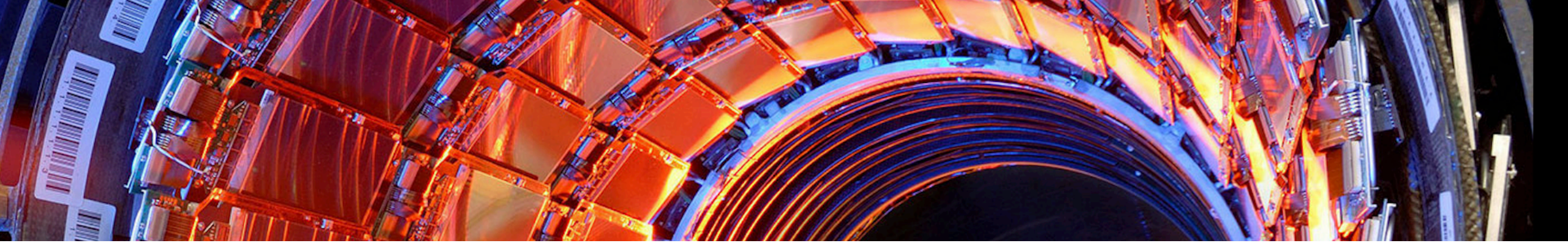


Younes Otarid

On behalf of the CMS collaboration

Silicon Pixel-Strip module characterisation for the CMS Outer Tracker Phase II Upgrade

BEAM TELESCOPES AND TEST BEAMS WORKSHOP
24.06.2022

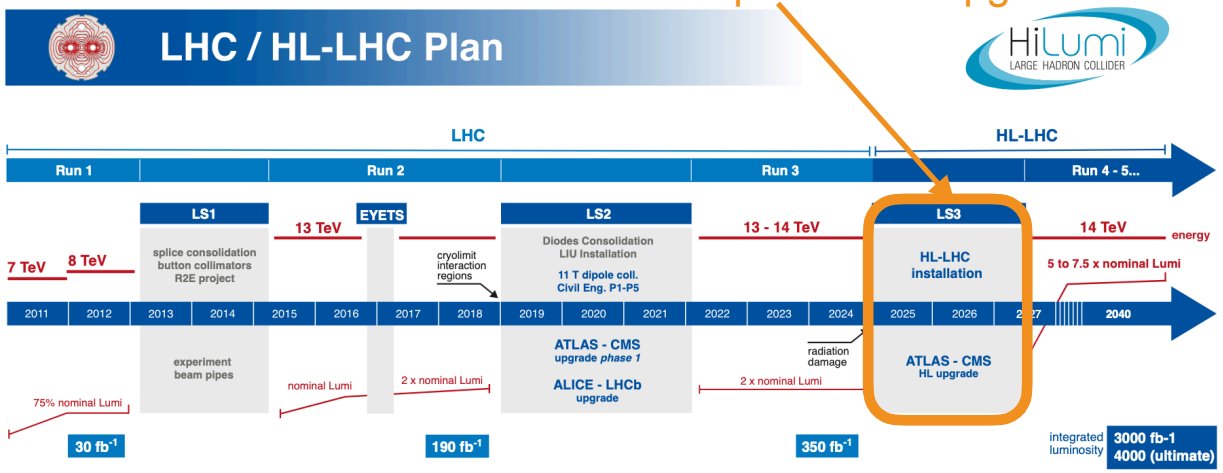
HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

CMS Compact Muon Solenoid

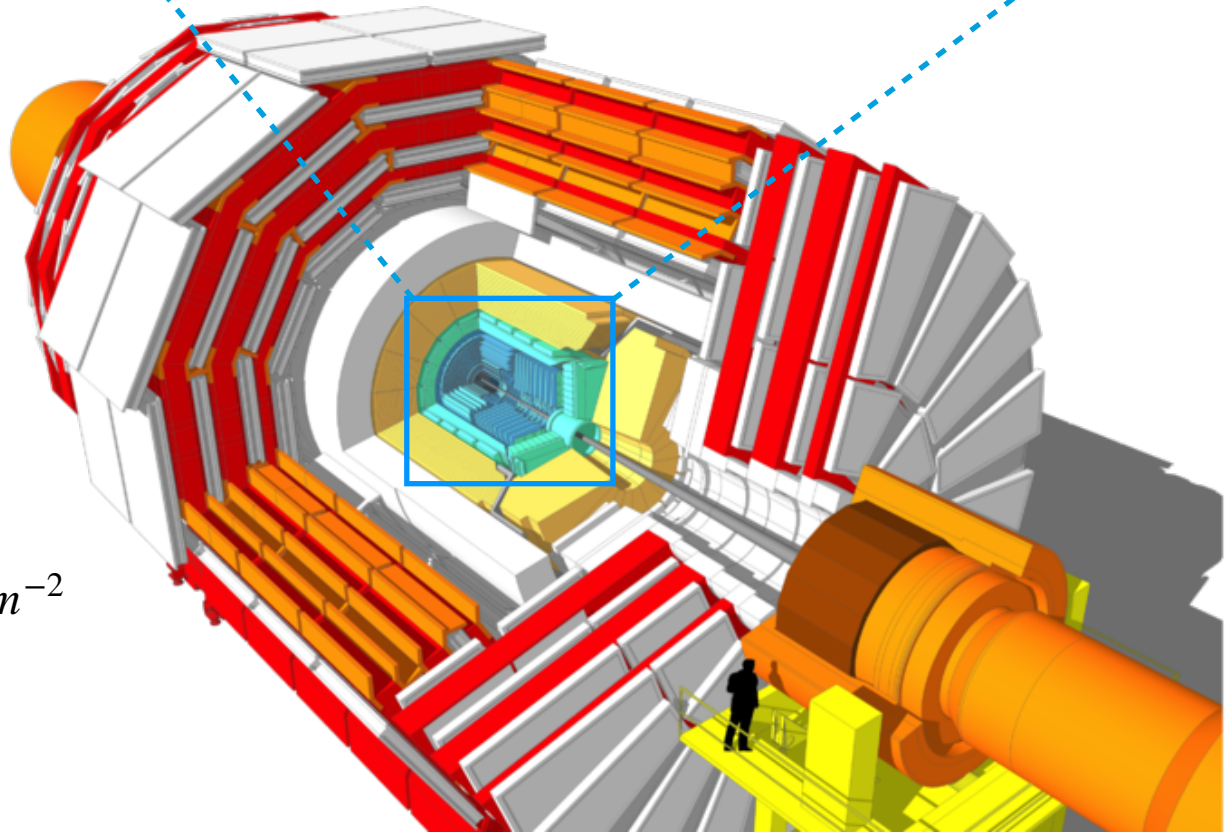
DESY.

High Luminosity LHC

Phase II Experiments Upgrade



New Tracker
- Radiation tolerant - granularity - less material
- Tracks in hardware trigger (L1)
- Coverage up to



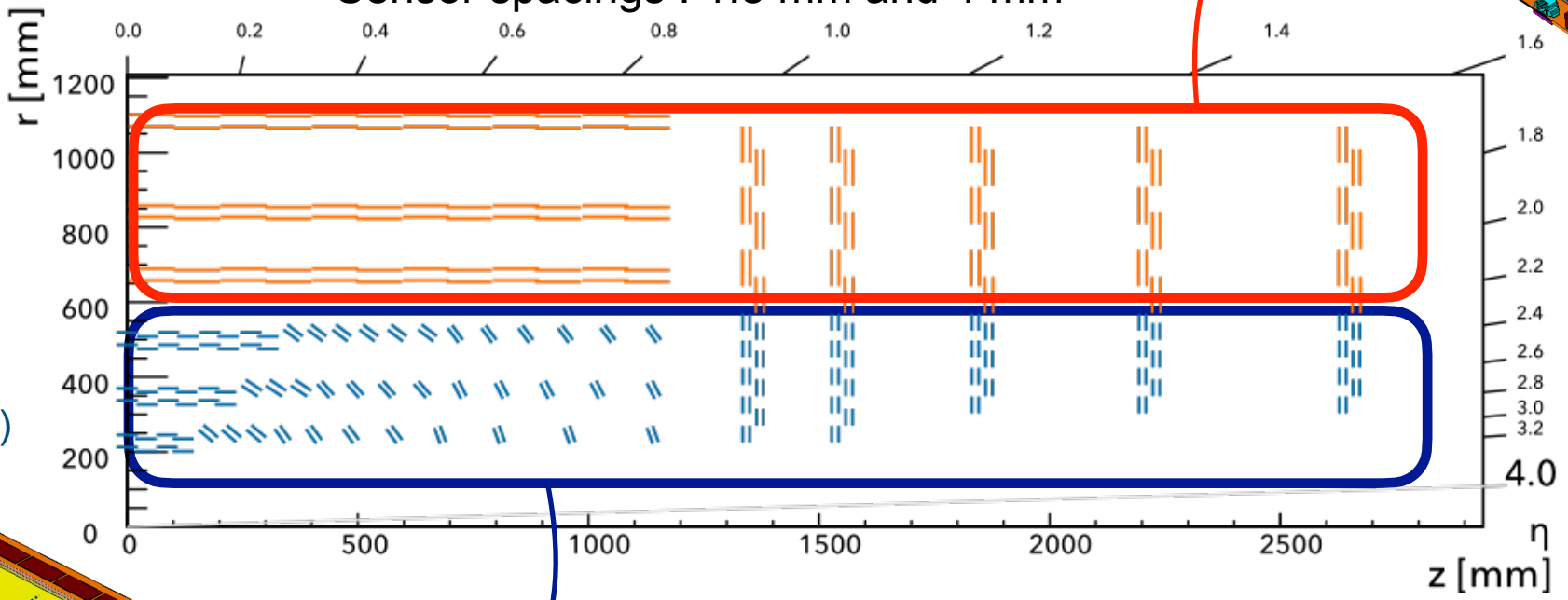
Accelerator performance :
- Peak instantaneous luminosity $5 - 7.5 \times 10^{34} cm^{-2} s^{-1}$
- $300\ fb^{-1}$/ year and up to $3000\ fb^{-1}$ over 10 years

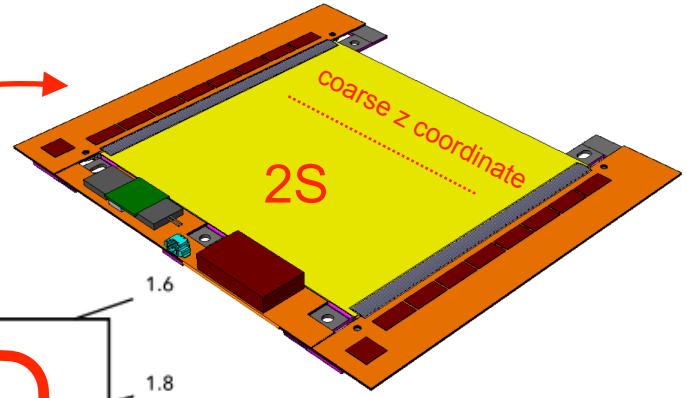
CMS environment :
- Unprecedented radiation levels up to $1.1 \times 10^{15}\ n_{eq} \times cm^{-2}$
- 10 times higher pile-up
- Higher data rates

CMS Outer Tracker upgrade

Layout with 6 barrel layers and 5 end cap double disks

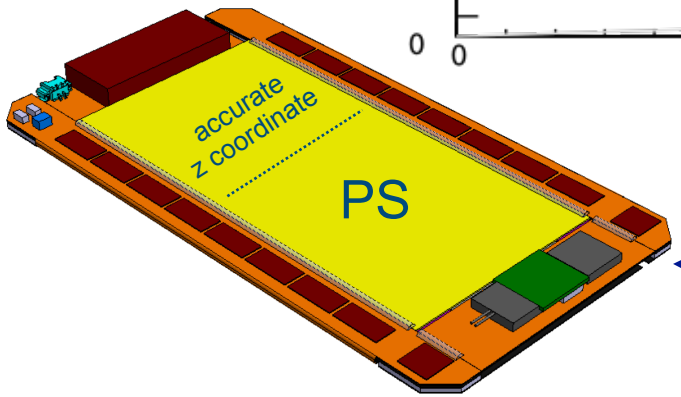
- Stack of two strip sensors at r > 60 cm (2S)
- Sensor spacings : 1.8 mm and 4 mm





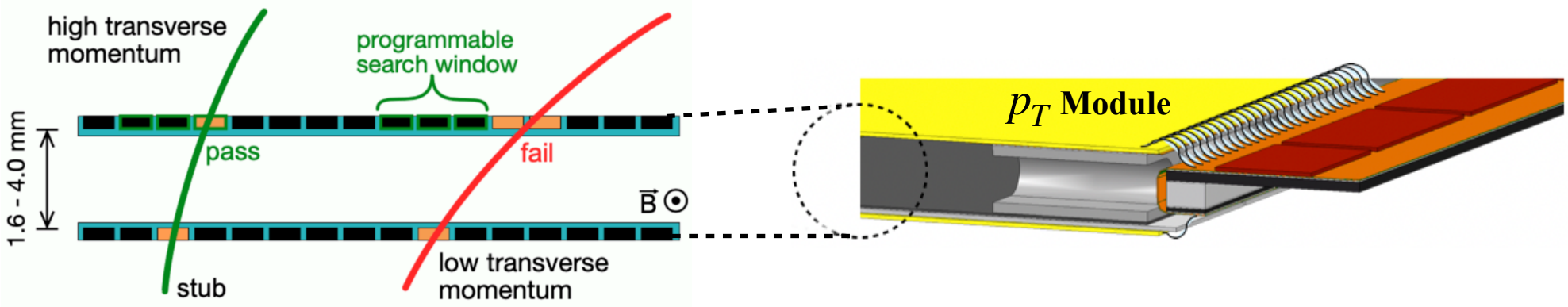
Strip-Strip (2S) Modules

Pixel-Strip (PS) Modules



- Stack of pixel and strip sensor at r < 60 cm (PS)
- Sensor spacings : 1.6 mm, 2.6 mm and 4 mm

Momentum discriminating module concept

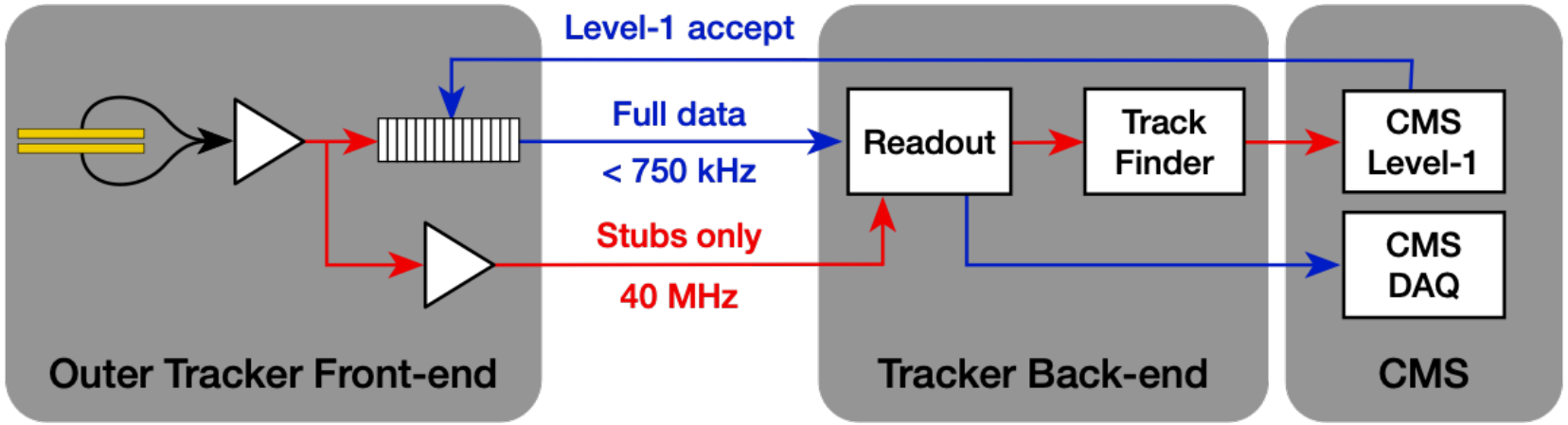


Modules with on-board p_T discrimination

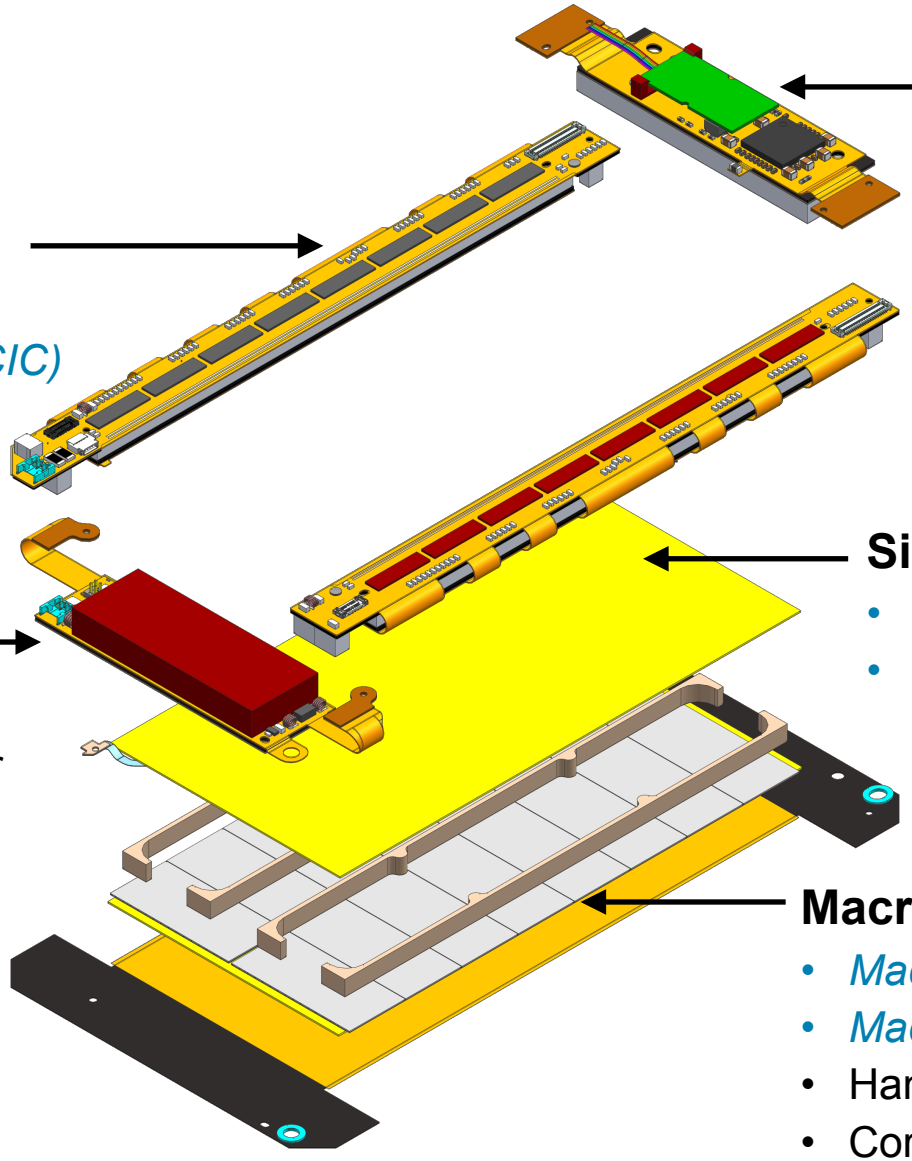
- Correlation of signals from two closely spaced sensors
- Strong magnetic field exploited for local p_T measurement
- Local rejection of low-p_T tracks to reduce data volume

Modules provide both Level-1 and readout data

- Trigger data ("stubs") sent every bunch crossing (40MHz)
- Readout data up to 750KHz
- "stubs" are used to form Level-1 tracks



Pixel-Strip silicon module design



Front-End Hybrid
- *Single-Strip ASIC (SSA)*
- *Concentrator Integrated Circuit (CIC)*
- Handles signal from strip sensor
- Transfers data to pixel chip

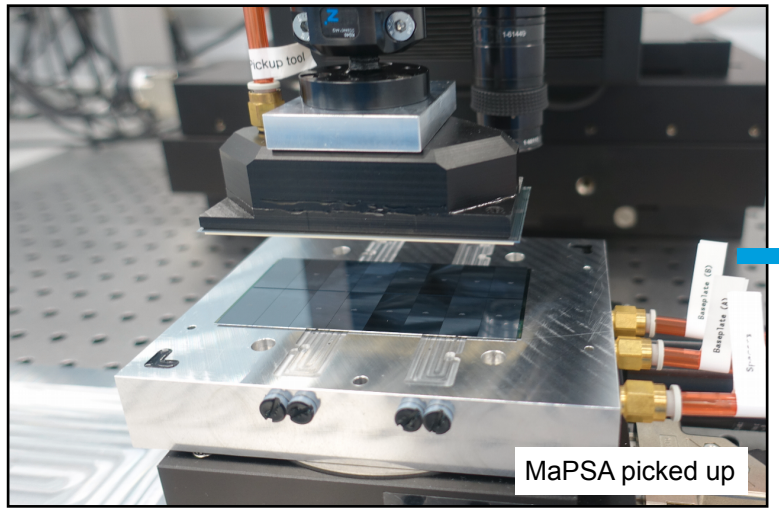
Power Hybrid
- DC-DC converter
- Used for module power

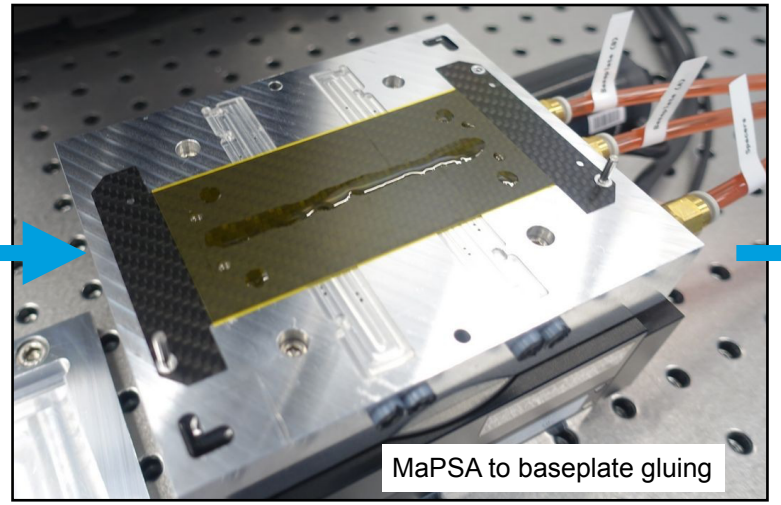
Read-Out Hybrid
- *Low-power Gigabit Transceiver chip*
- *VTRx+* optical module
- Transmits data over optical fibre

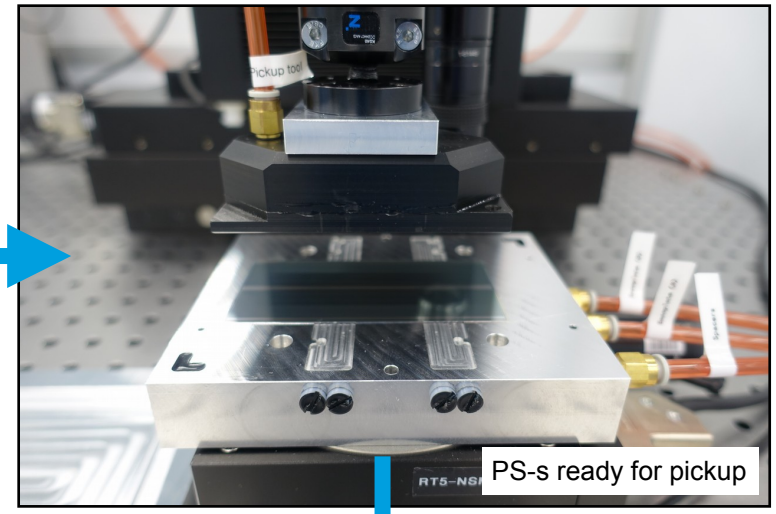
Silicon Strip Sensor
- *10 x 5 cm Silicon Strip Sensor*
- *2.5 cm long strips, 100 um pitch*

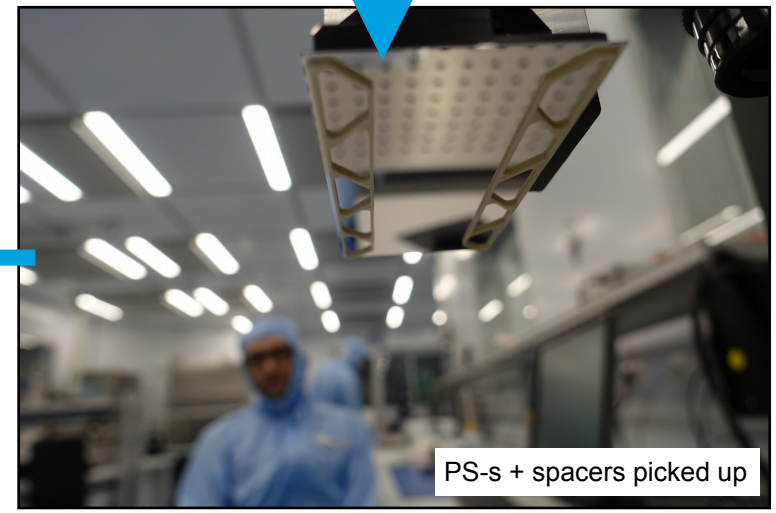
Macro Pixel Sub Assembly (MaPSA)
- *Macro Pixel ASIC*
- *Macro Pixel Silicon sensor 1400 x 100 um*
- Handles signal from pixel sensor
- Correlates signal from both sensors

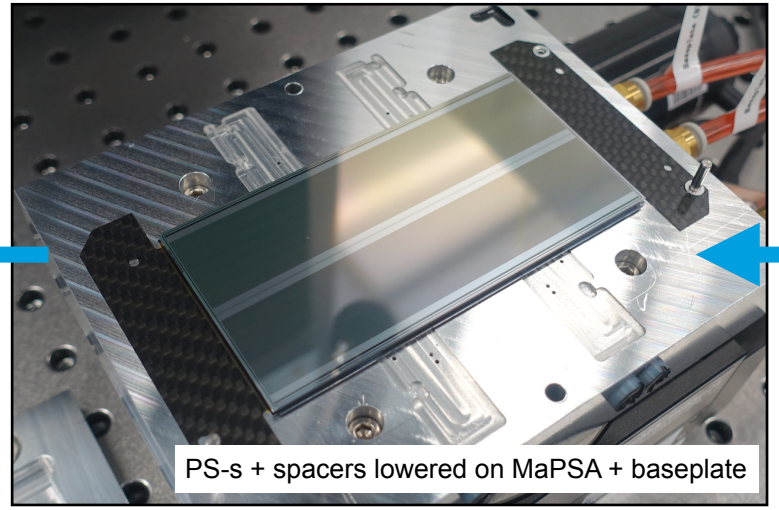
Pixel-Strip silicon module assembly

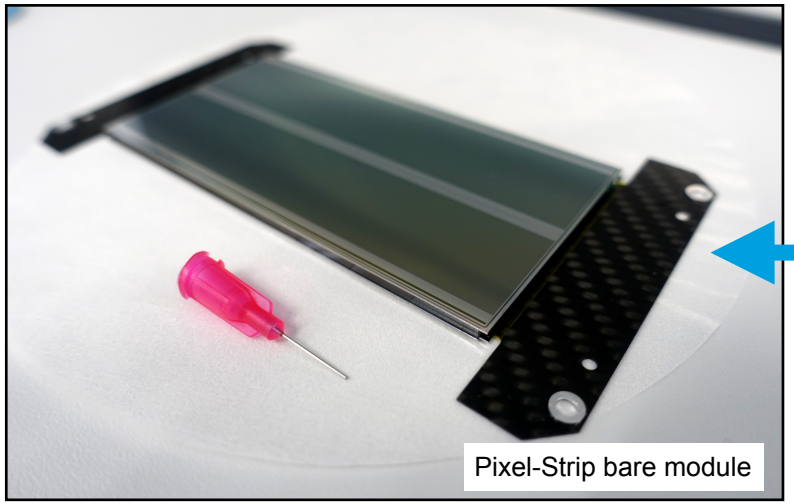

MaPSA picked up


MaPSA to baseplate gluing

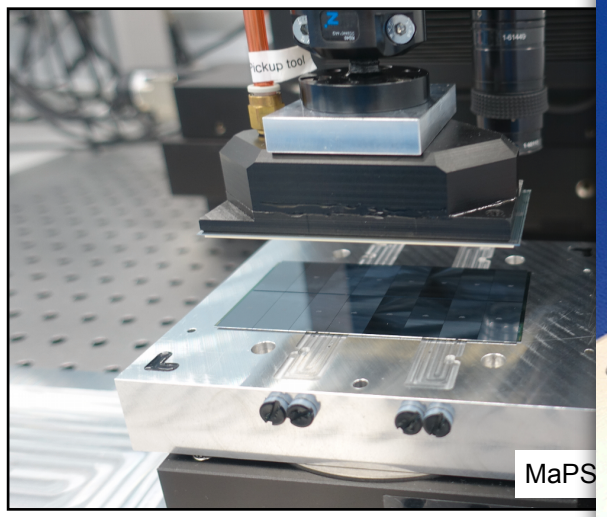

PS-s ready for pickup

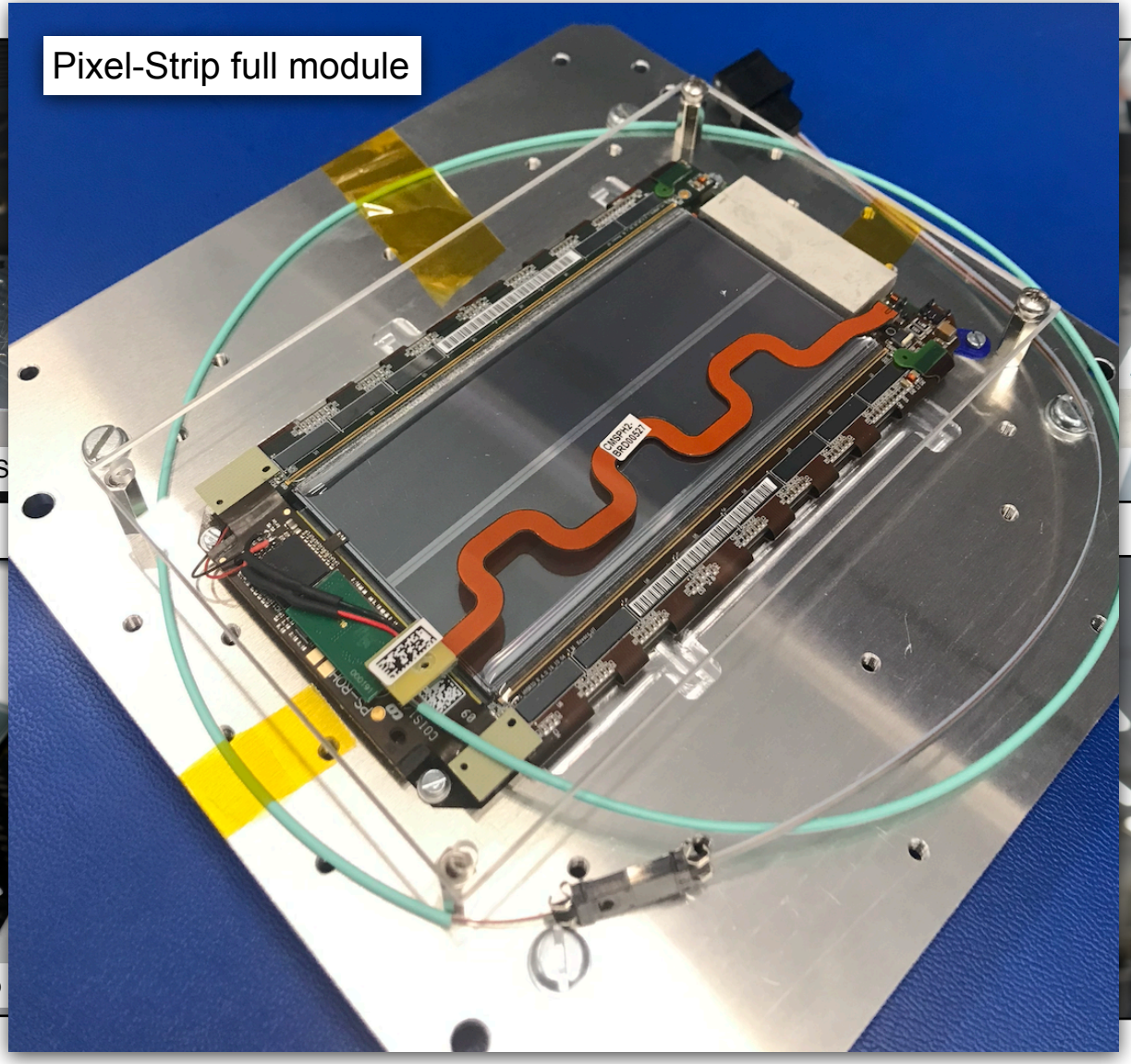

PS-s + spacers picked up

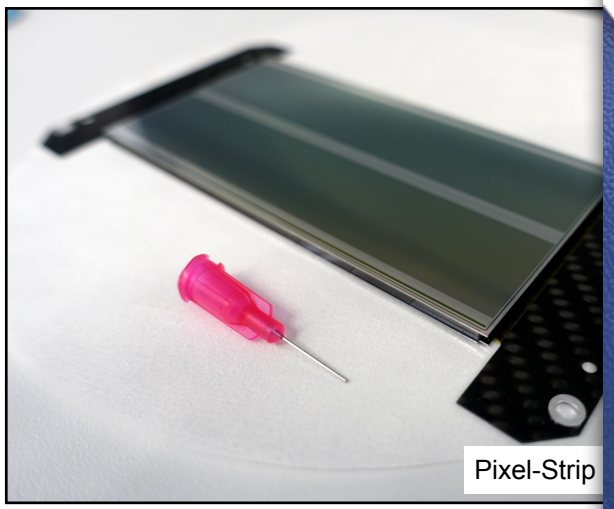

PS-s + spacers lowered on MaPSA + baseplate


Pixel-Strip bare module

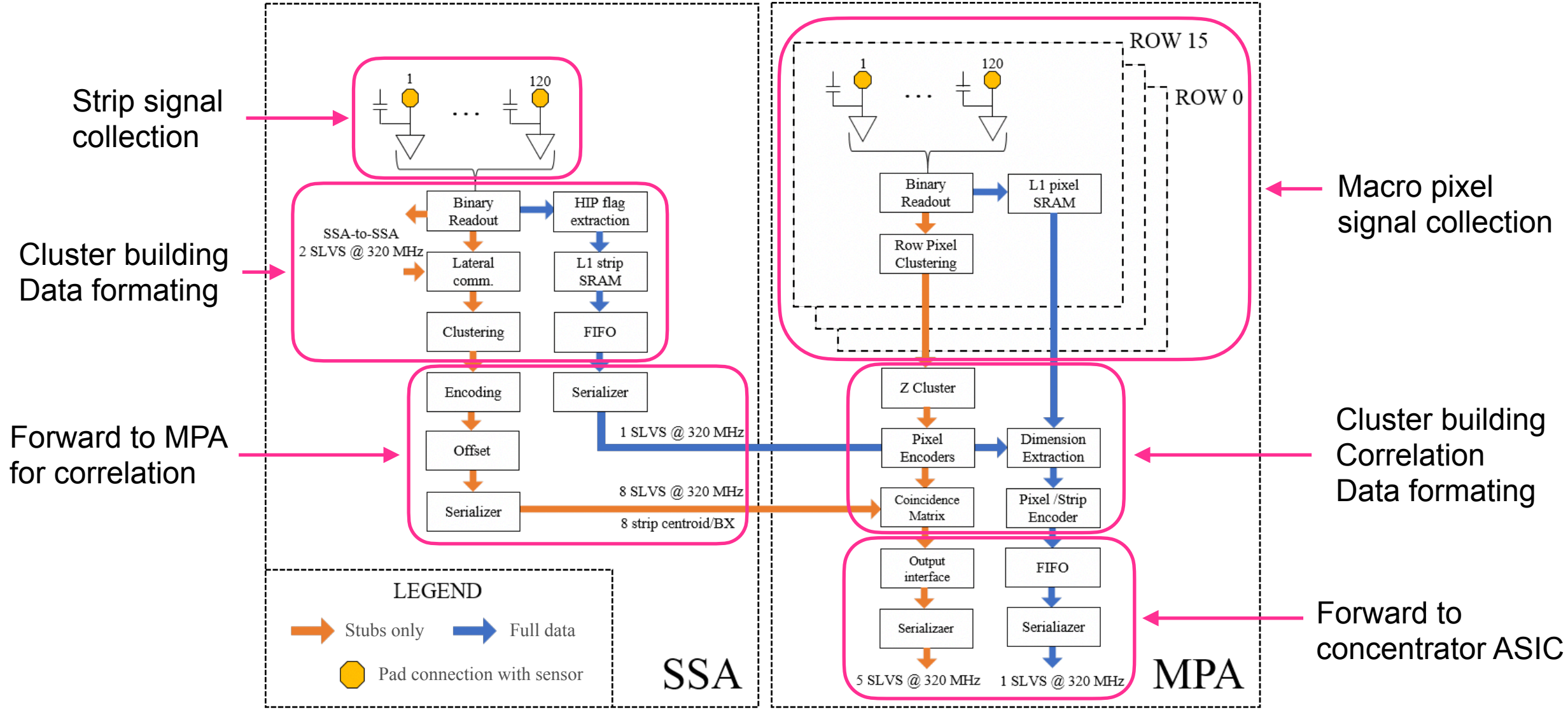
Pixel-Strip silicon module assembly







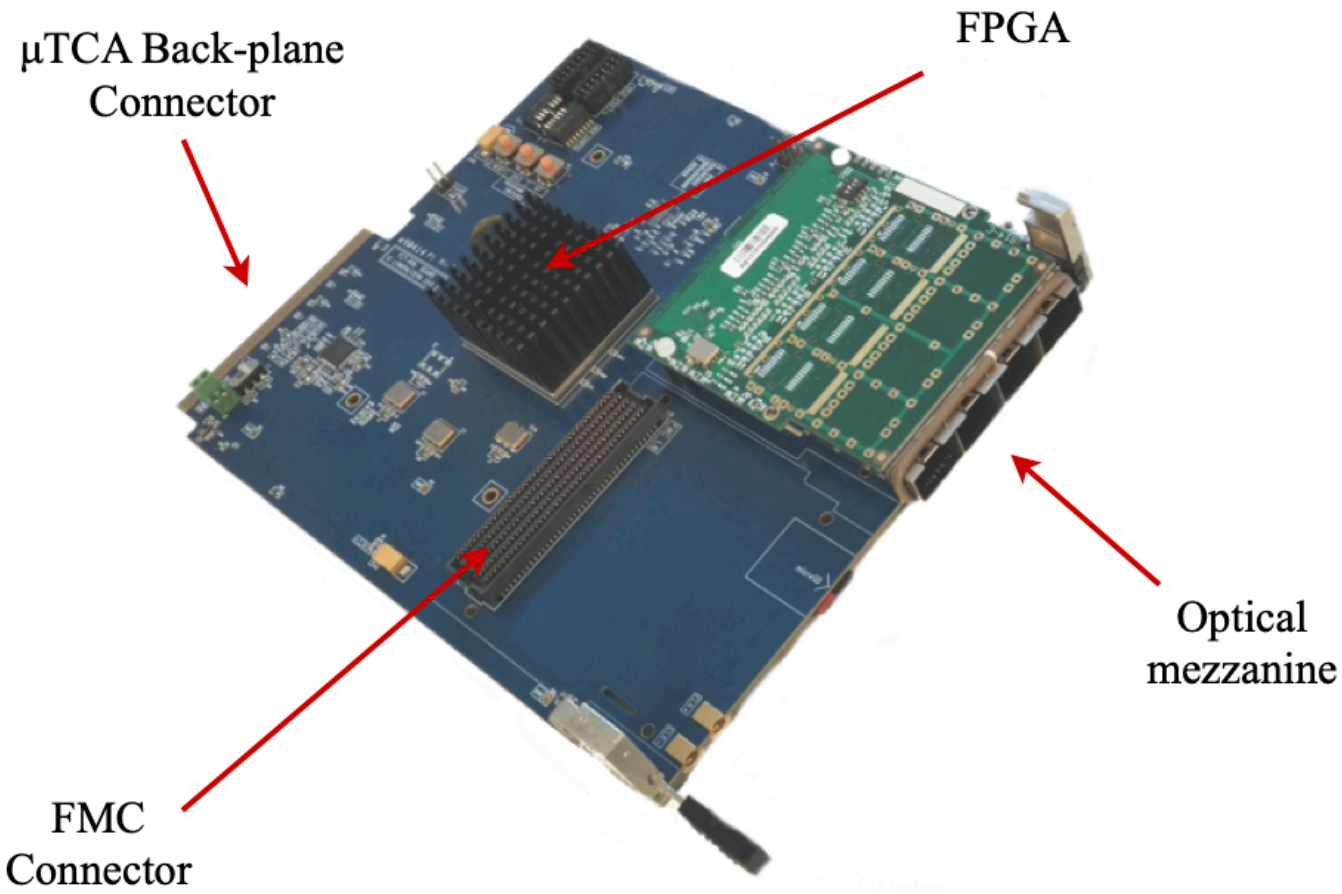
Pixel Strip ASIC read-out architecture



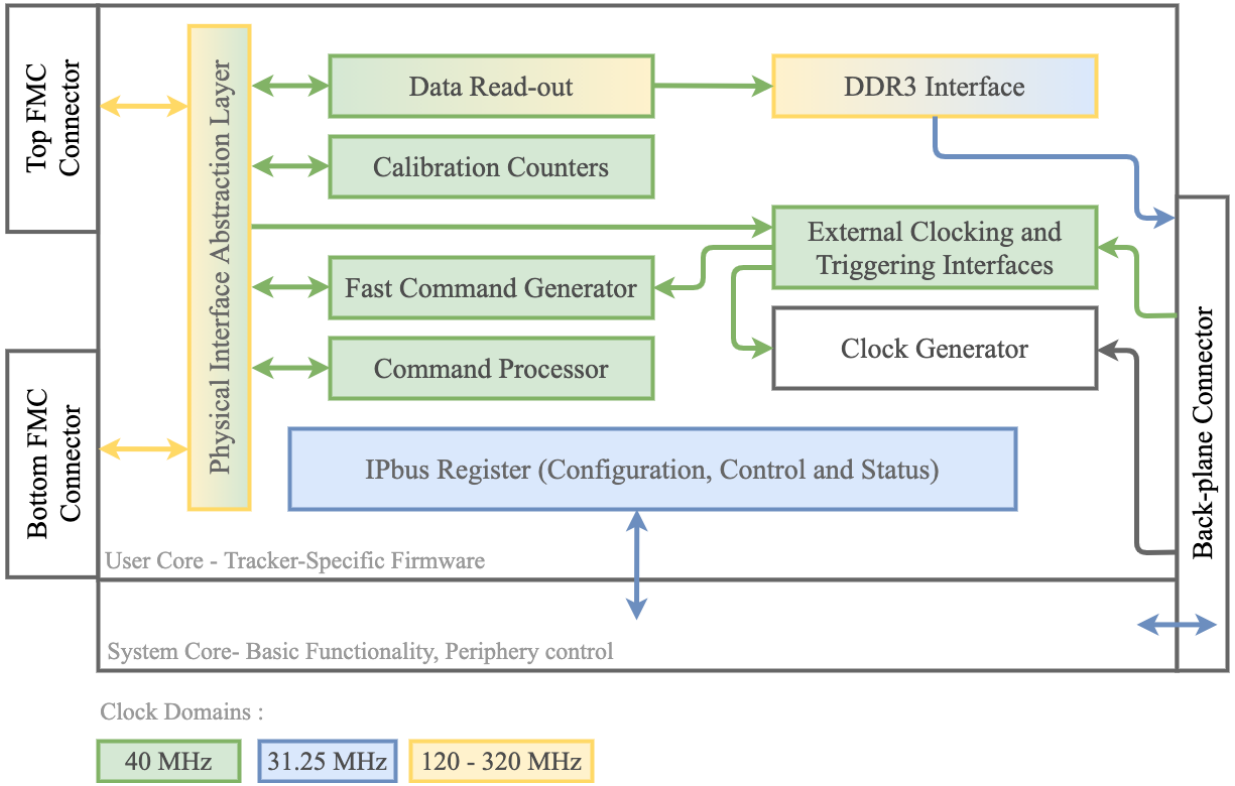
DAQ test system

- Exploits ***FC7*** uTCA-compatible board for generic data acquisition and control applications
  - Kintex-7 FPGA
  - 2 FMC Connectors
  - Advanced clock distribution system
  - External DDR3 memory
  - uTCA integration

- Several custom interface are supported by the system in case of needed synchronous operation
  - Trigger Logic Unit (TLU)
  - DIO5 (5 LEMO I/O)
  - AMC13 (interface to the TCDS)



uDTC firmware



Firmware development specifically dedicated to the prototyping and production phases of the CMS Tracker Phase II Upgrade

IPbus registers :
- Configuration, control or status monitoring

Clock Generator :
- 40MHz to 640MHz clock generation and distribution

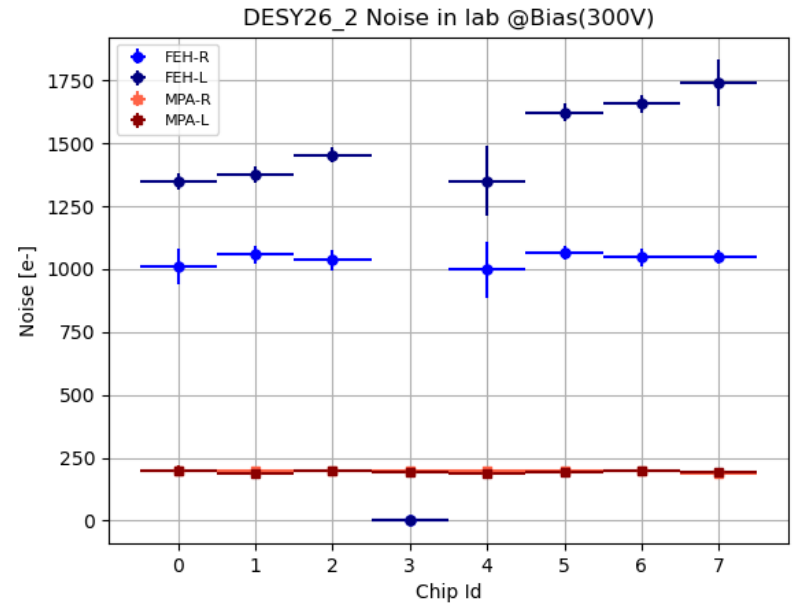
Fast Command Generator :
- Interface for synchronisation, calibration and trigger fast signals

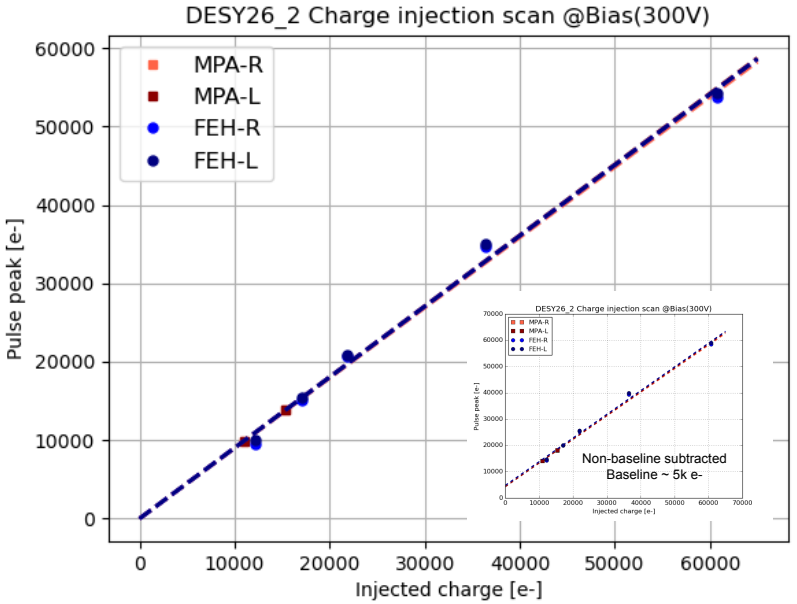
Command Processor :
- Slow control, configuration and calibration

Physical Interface Abstraction Layer :
- Abstract interface for optical or electrical control/ readout

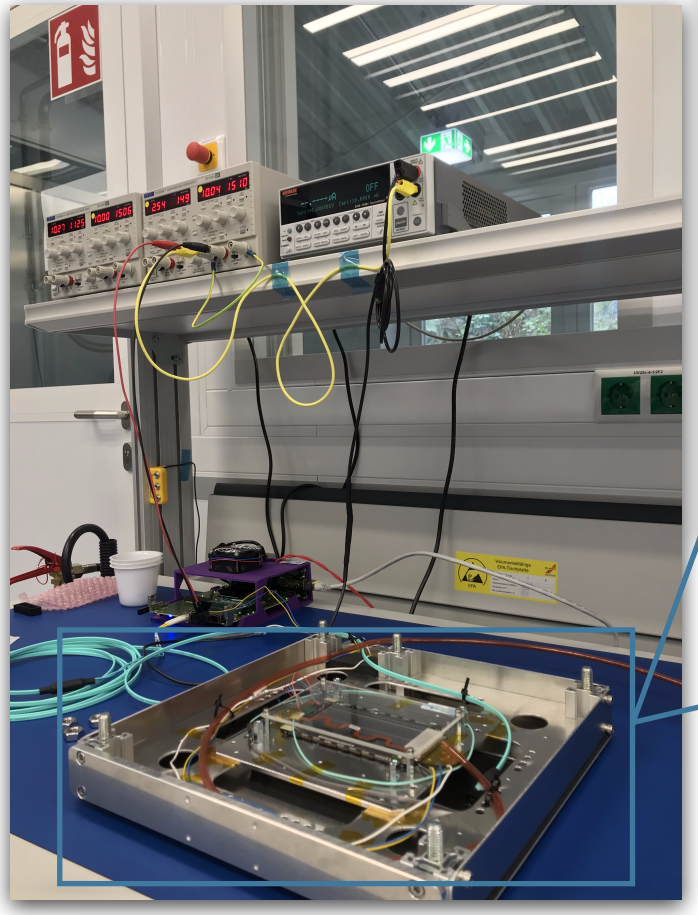
Data Readout :
- Processing and aggregation of data from all connected front-end modules/components

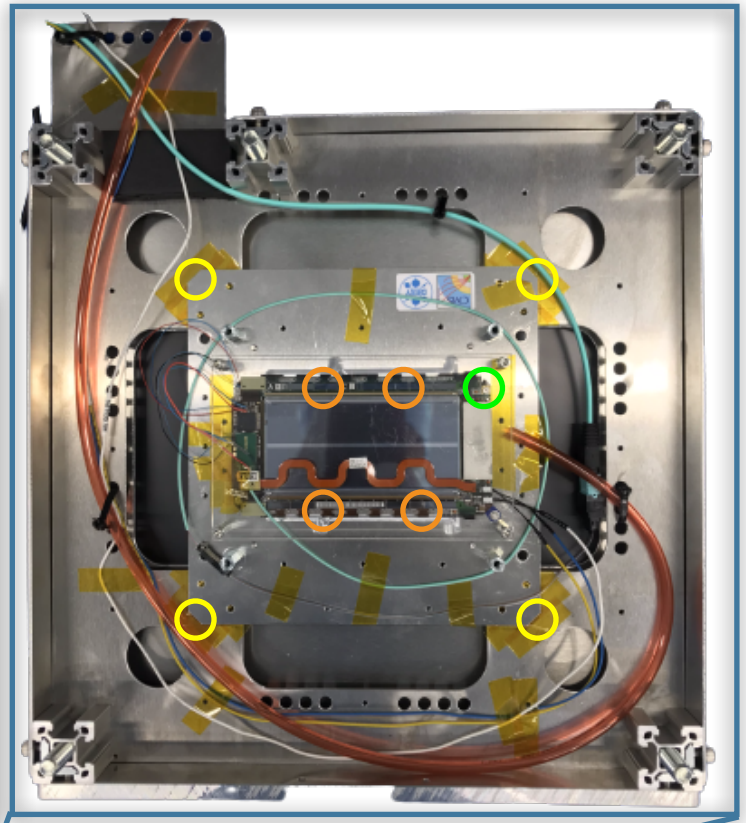
Preliminary lab commissioning



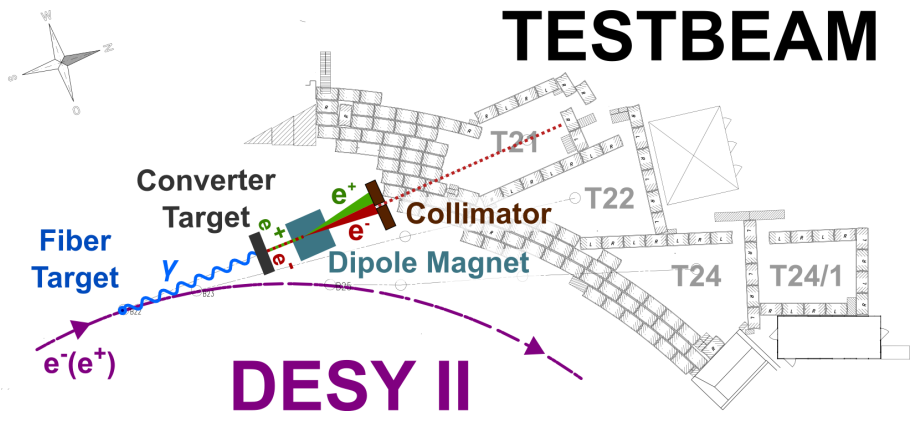


- POH ground hole
- FEH spring finger contacts
- Kapton tape isolation



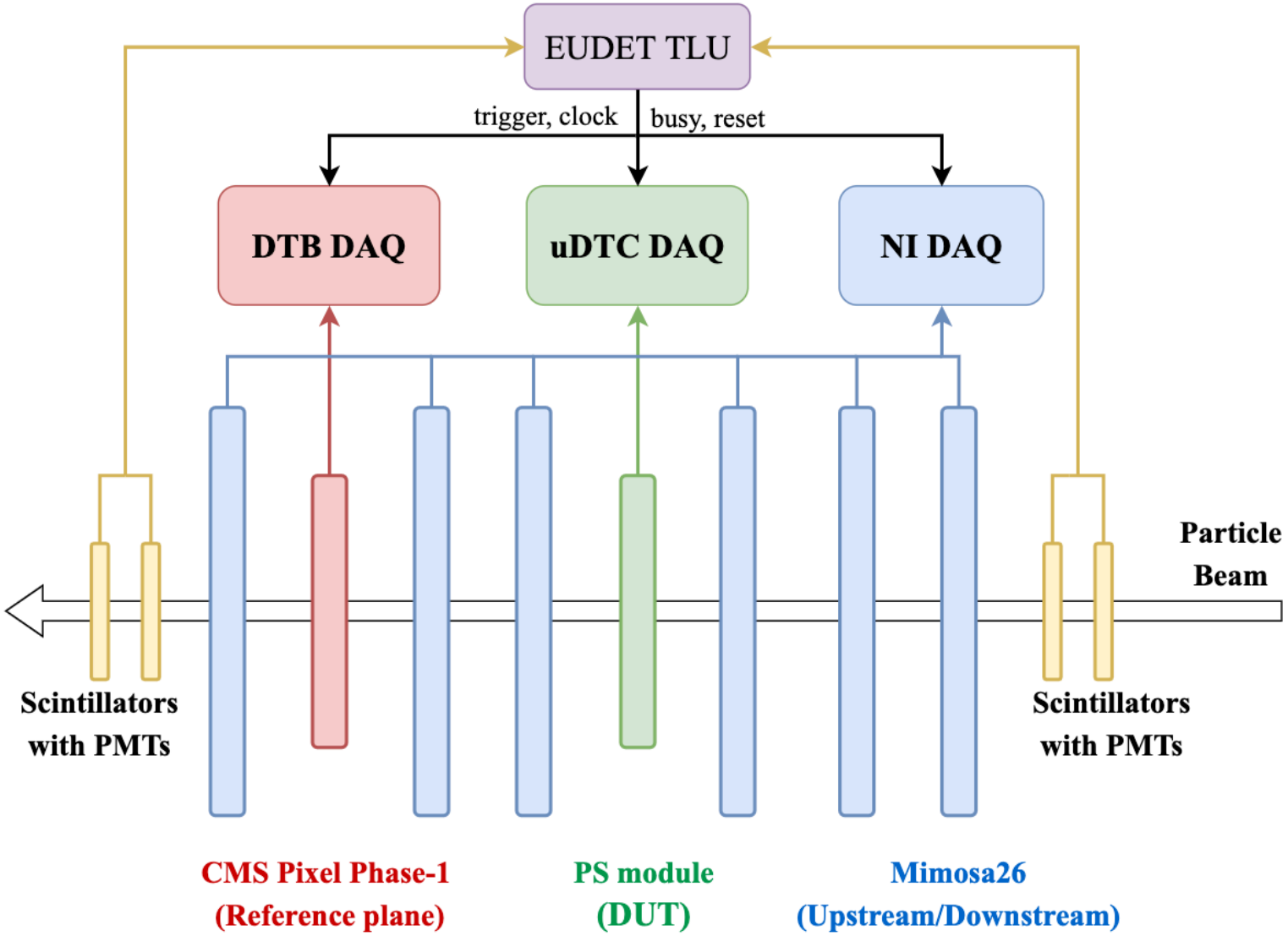


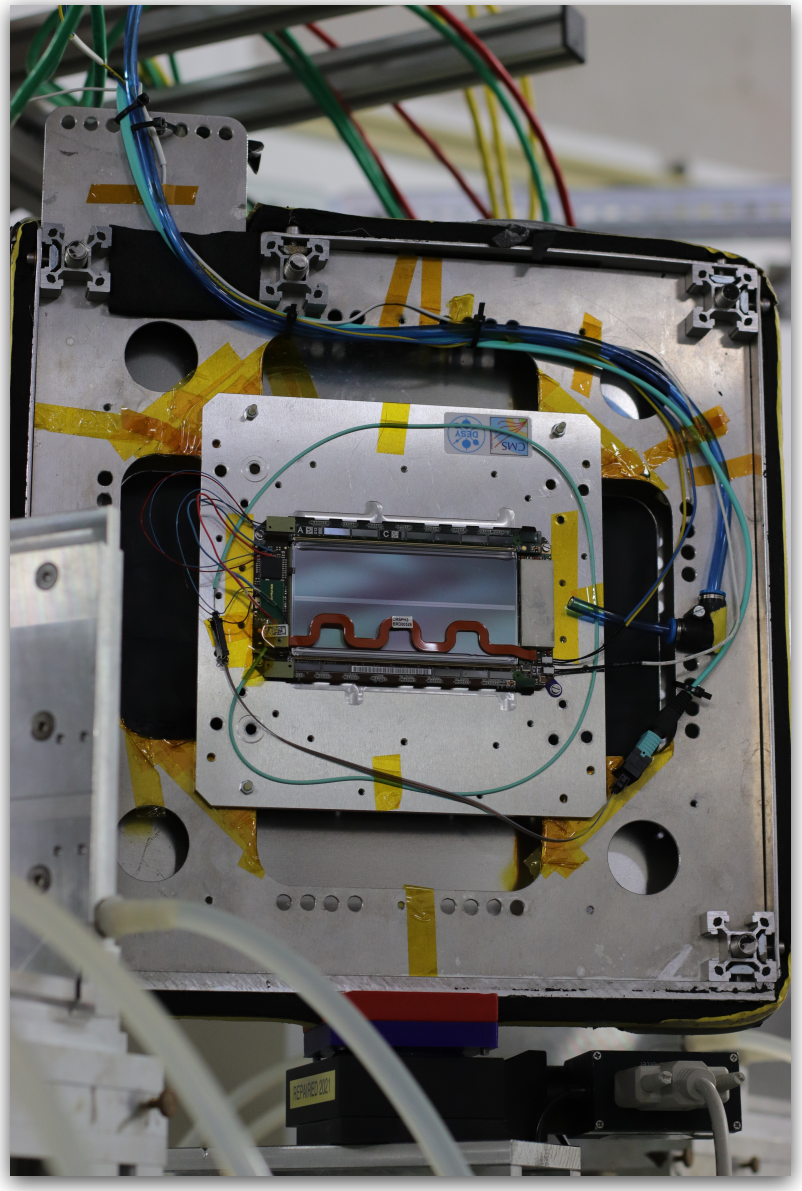
DESY Test-Beam infrastructure



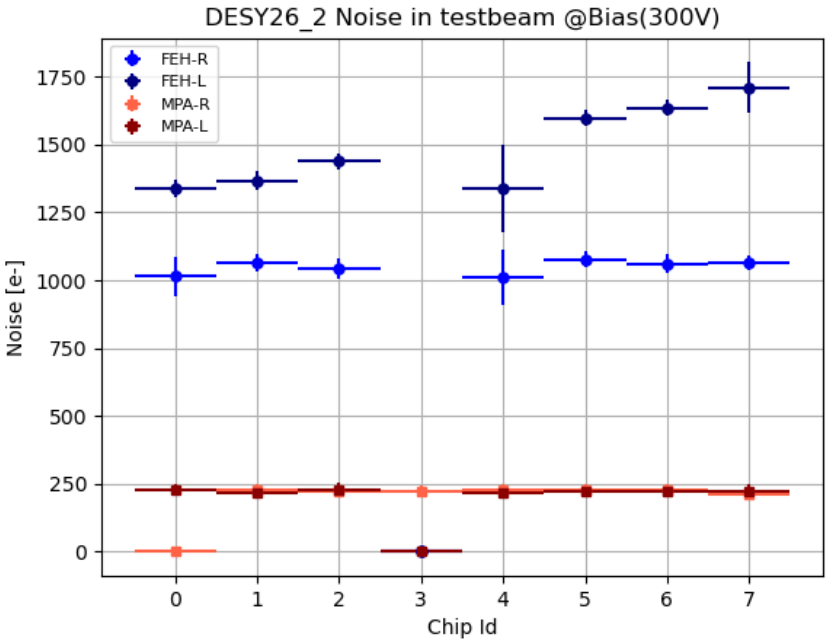
- 1-6 GeV/c electron beam @kHz rate
- DATURA Beam Telescope
- CMS Pixel Phase-1 reference plane
- Triggering crossed scintillators
- EUDET TLU
- EUDAQ data taking framework

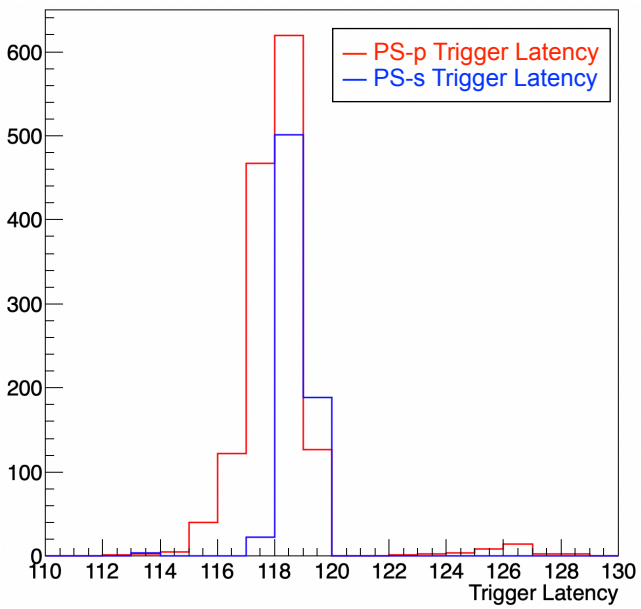
Experimental setup and readout scheme

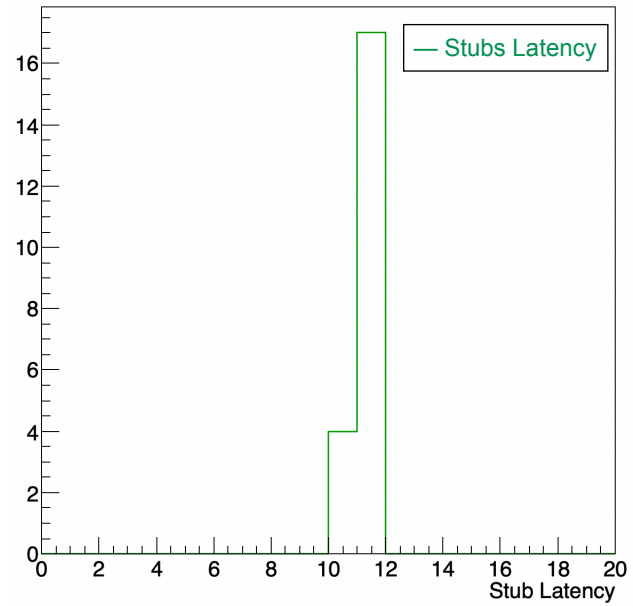




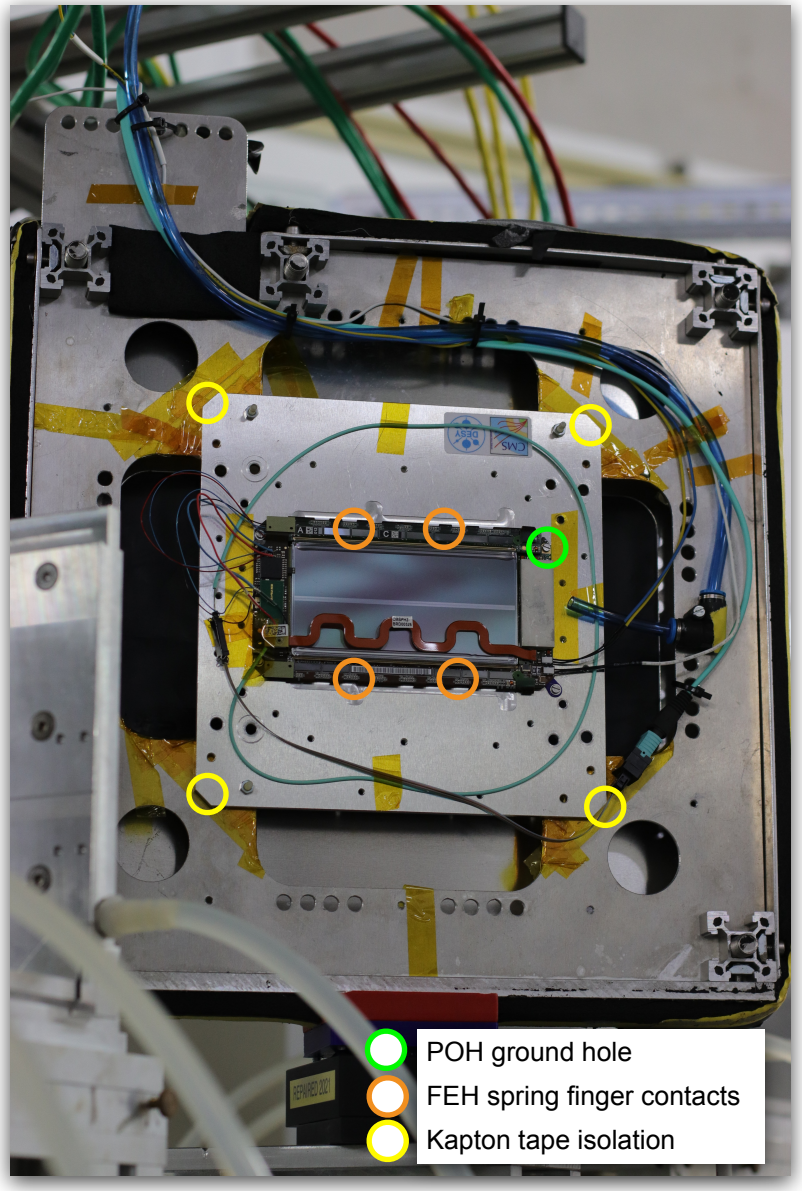
Module test-beam commissioning



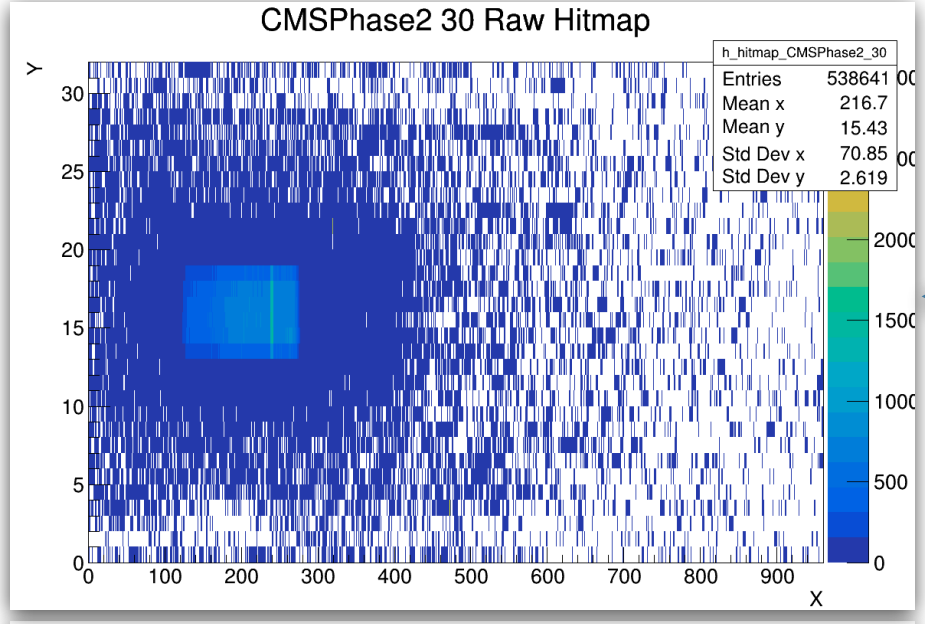




- Comparison of lab and test beam noise measurements
- Search for optimal trigger & stub latencies to maximise hit & stub occupancies

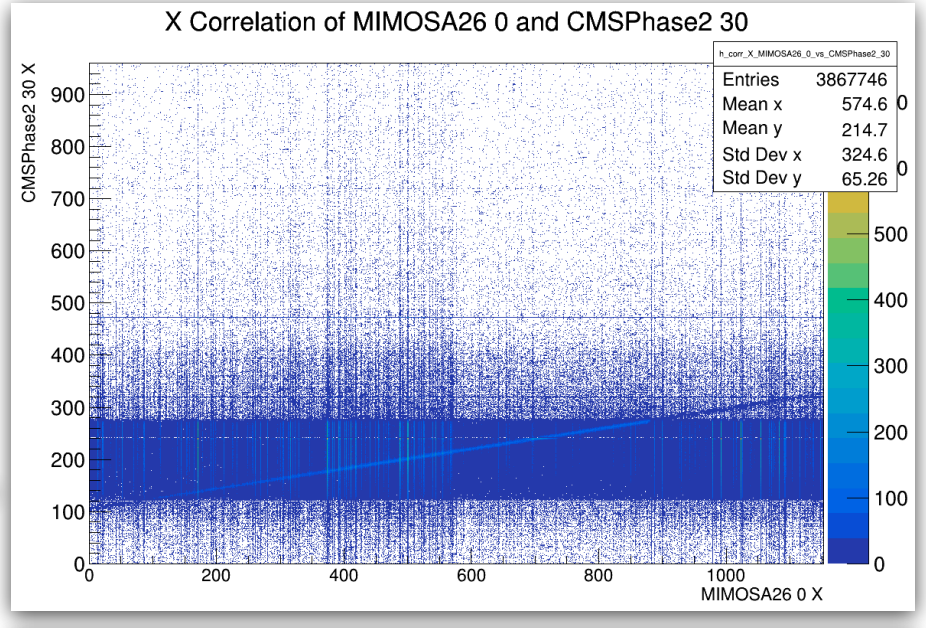


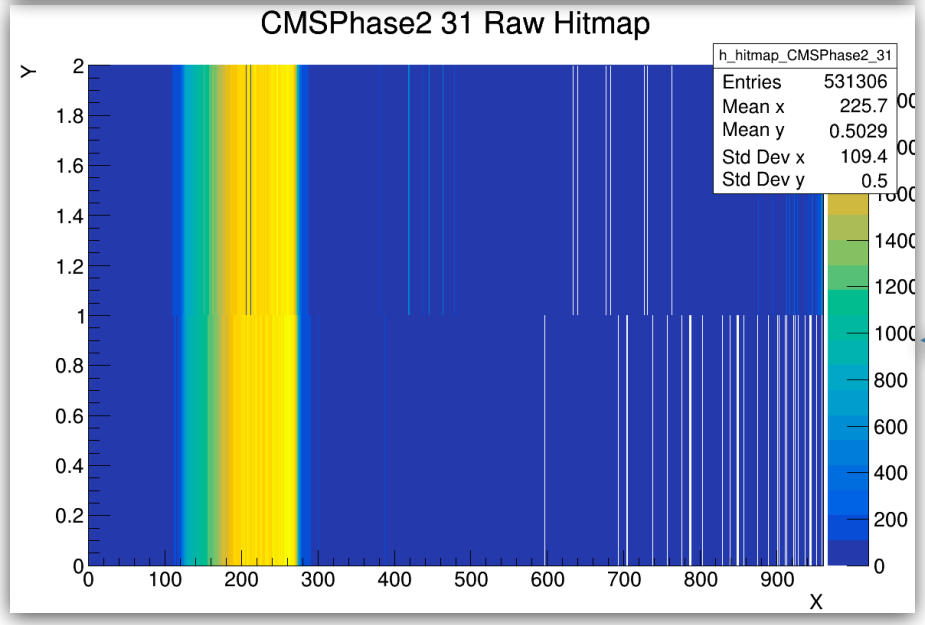
Synchronous readout



PS-p hit map

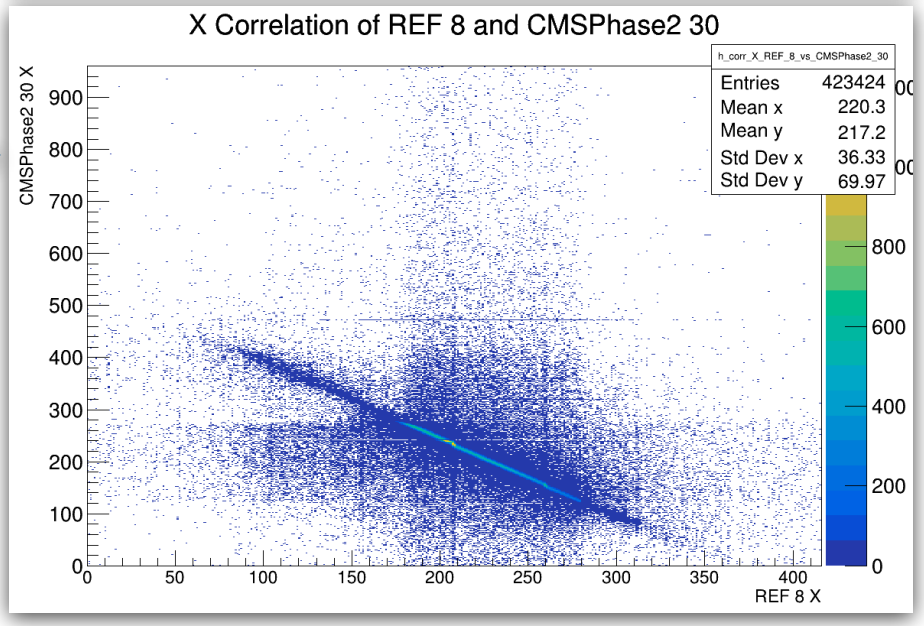
PS-Telescope correlation



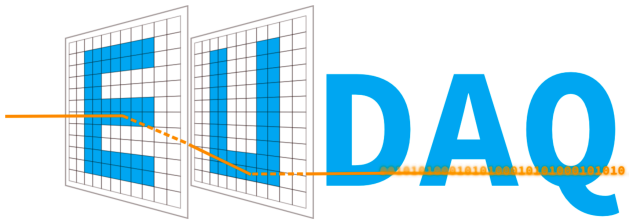


PS-Reference plane correlation

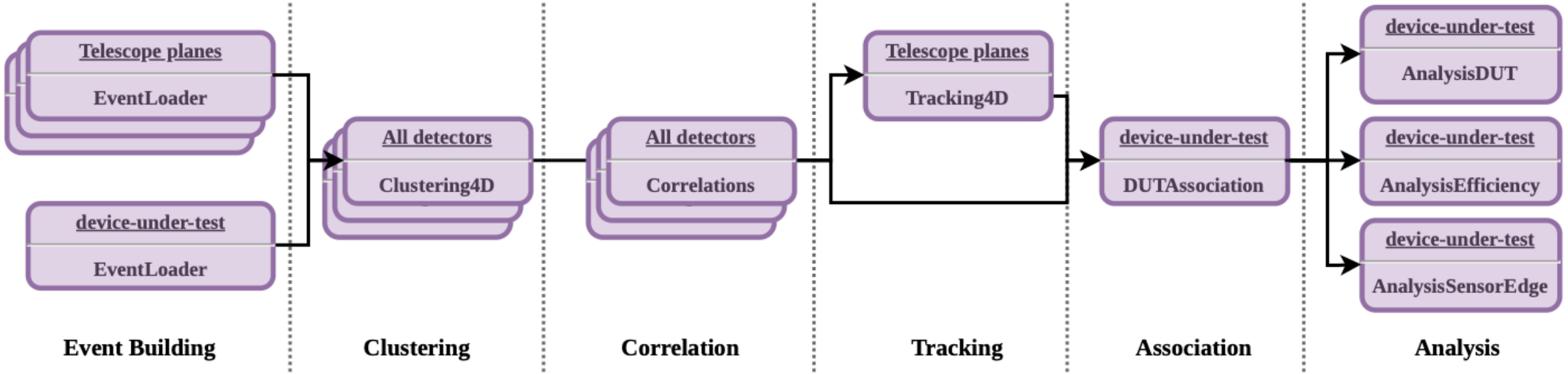
PS-s hit map



Analysis flow

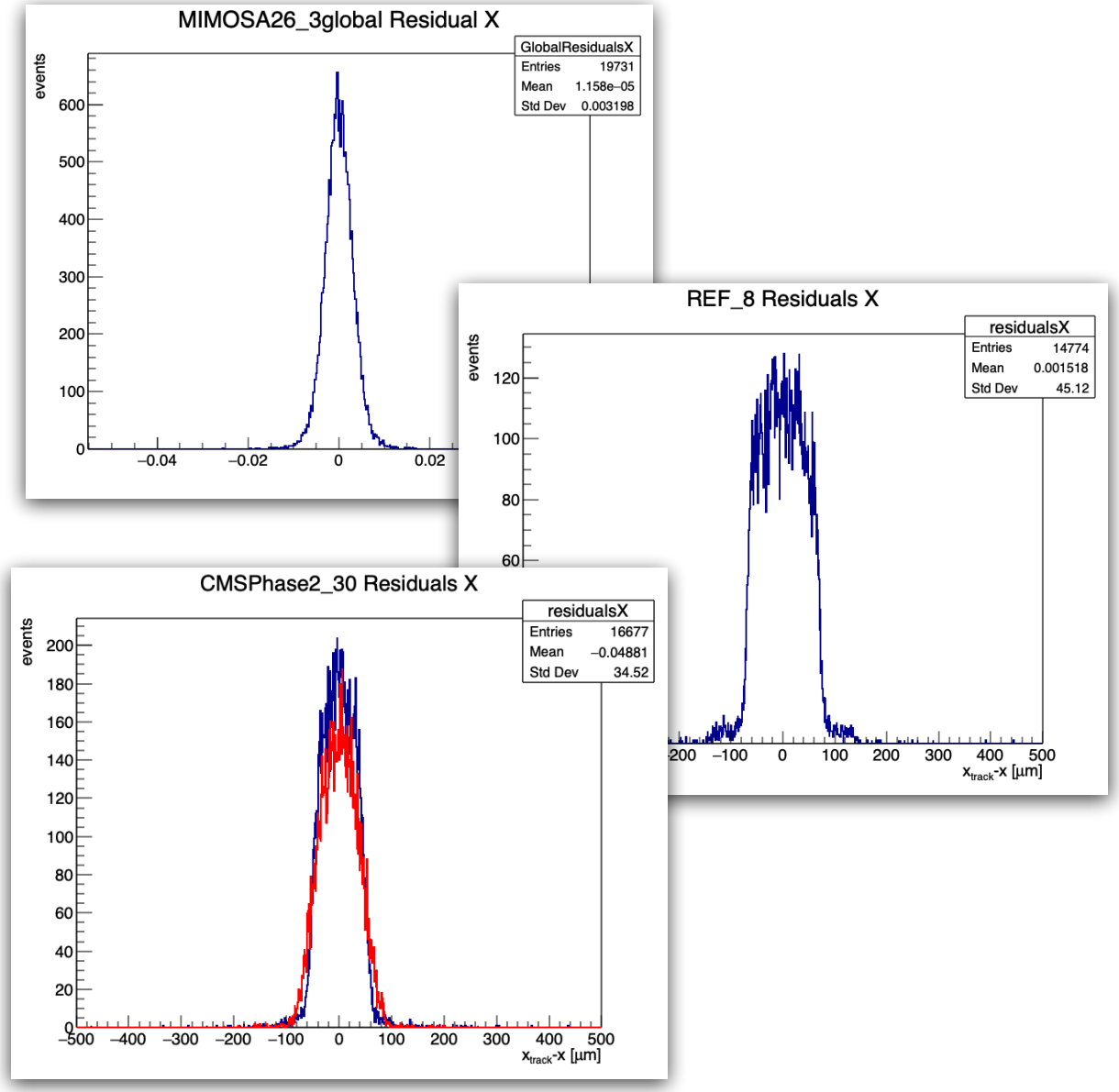


- AnalysisEfficiency & AnalysisDUT module applied to PS-p and PS-s sensors
- Custom AnalysisStubEfficiency module for Stub analysis
- New Tag-based event filtering feature to allow for TDC selection



Alignment strategy

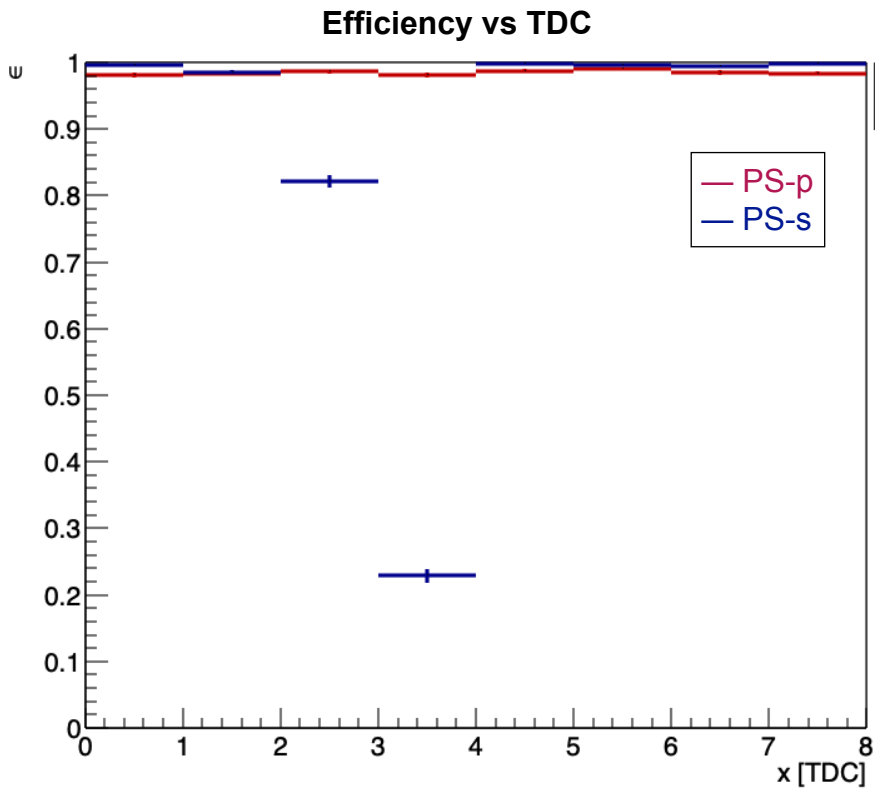
1. **Telescope alignment :**
   - Pre-alignment : 5 iter using maximum method
   - Alignment : 5 iter using GBL method with both rotation and position alignments
2. **Reference plane alignment :**
   - Pre-alignment : 5 iter using maximum method
   - Alignment : 5 iter using GBL method with both rotation and position alignments
3. **PS module alignment :**
   - Pre-alignment : 5 iter using maximum method
   - Alignment : 5 iter using GBL method with position and only z-rotation alignments



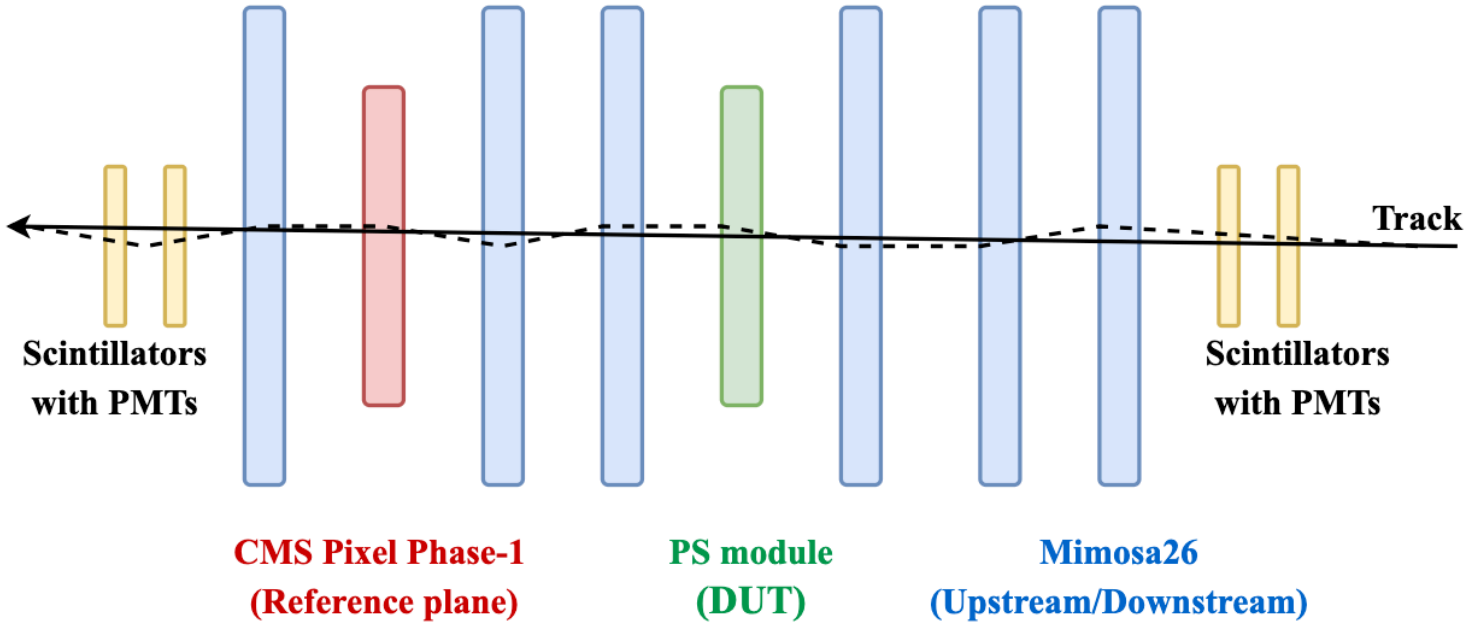
Efficiency measurement strategy

Efficiency measurement :

- Exclusive use of tracks with associated hit in reference plane
- Random triggers —> TDC dependency —> Selection of high efficiency TDC bins with Corry tag-based filtering



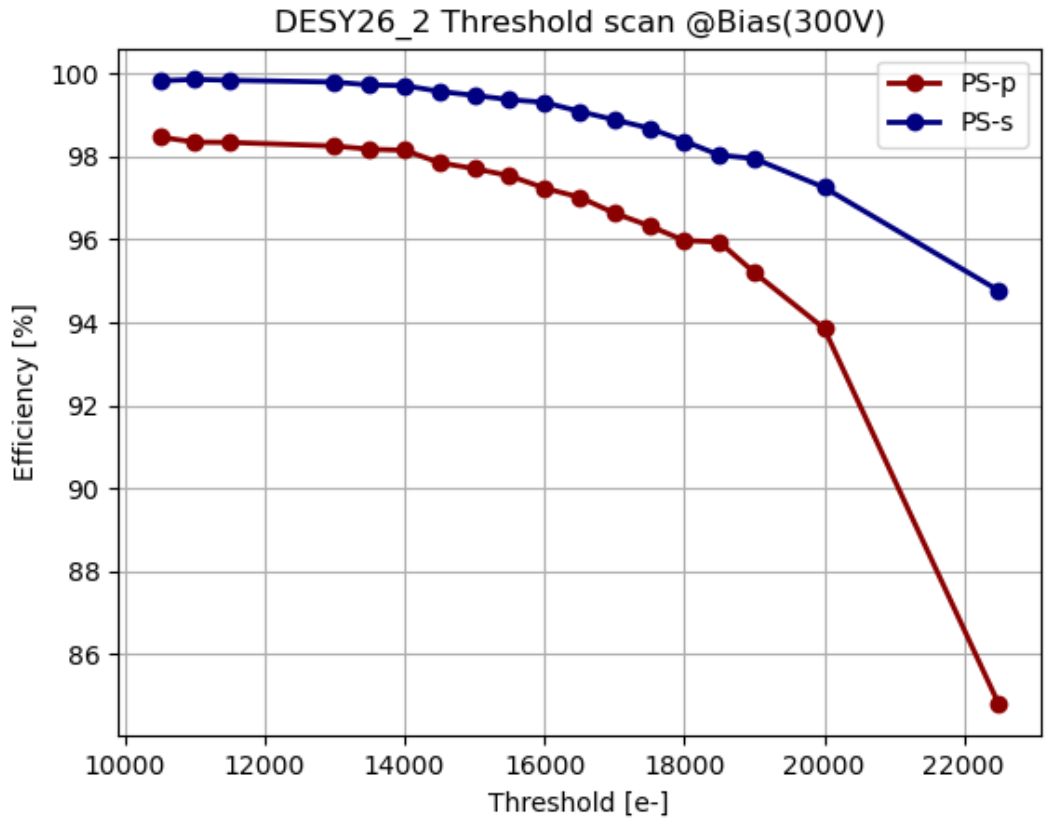
$$\text{Efficiency} = \frac{\#\ \text{DUT Hits linked to isolated telescope tracks associated to reference plane}}{\#\ \text{Isolated telescope tracks associated to reference plane}}$$

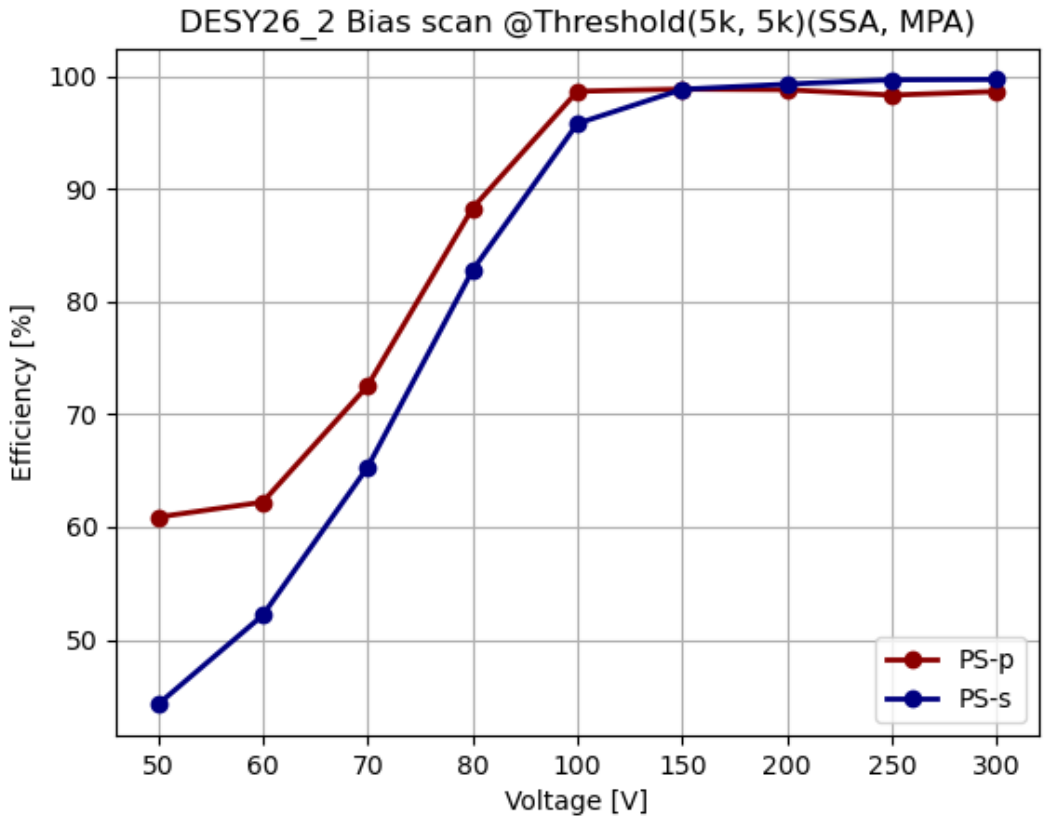


Hit efficiencies - Threshold & Bias scans

$$\text{Efficiency} = \frac{\#\ \text{DUT Hits linked to isolated telescope tracks associated to reference plane}}{\#\ \text{Isolated telescope tracks associated to reference plane}}$$

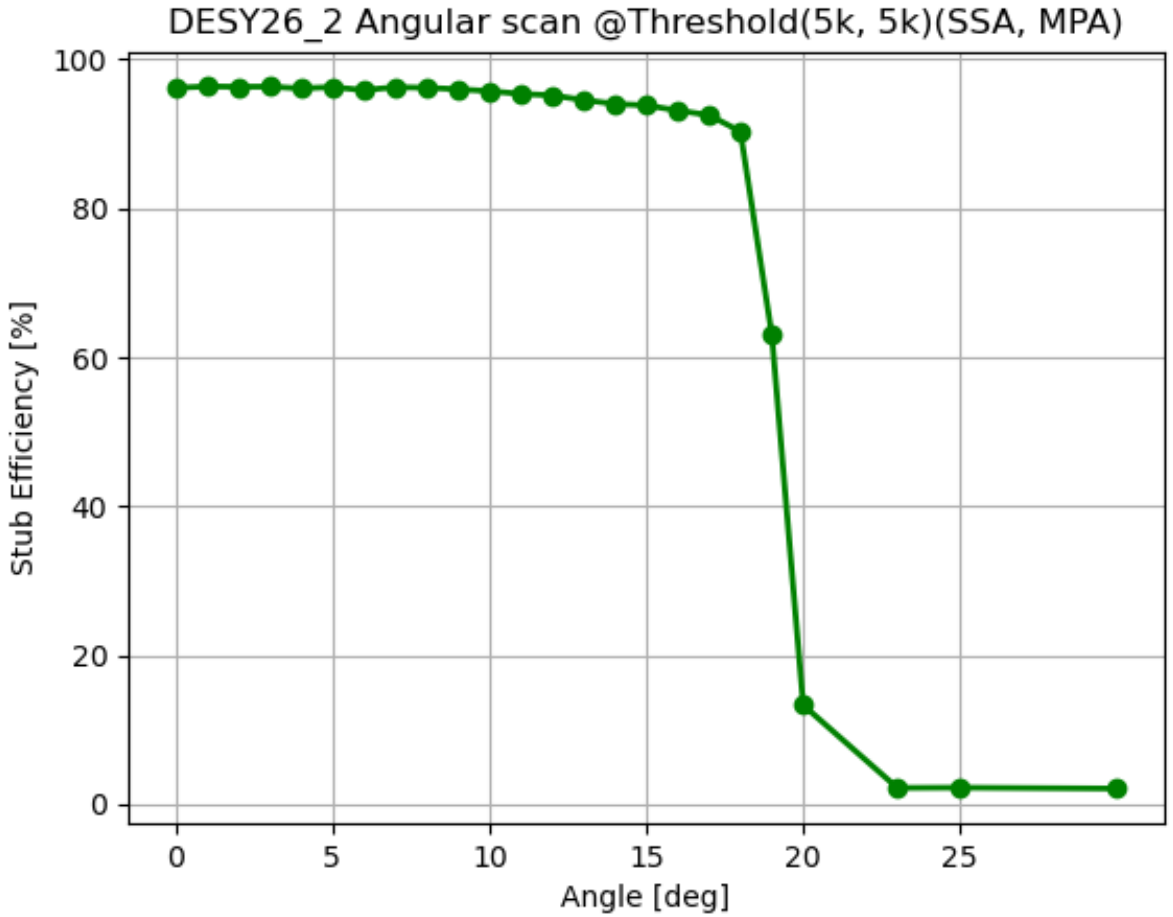
- ~99.6% strip efficiency, ~98.6% pixel efficiency :
  - Pixel inefficiency caused by PS-p bias structure





Stub efficiency - Angular scan

$$\text{Efficiency} = \frac{\#\ \text{DUT stub linked to isolated telescope tracks associated to reference plane, pixel and strip planes}}{\#\ \text{Isolated telescope tracks associated to reference plane, pixel and strip planes}}$$



- Angular scan to emulate bending of particles
- Correlation window 16 <=> efficiency drop @~18 degrees
  - Stub logic working as expected
- ~96% stub efficiency
  - Still relatively low, to be further investigated
- 2% residual stubs beyond the correlation window

Summary - Prospects

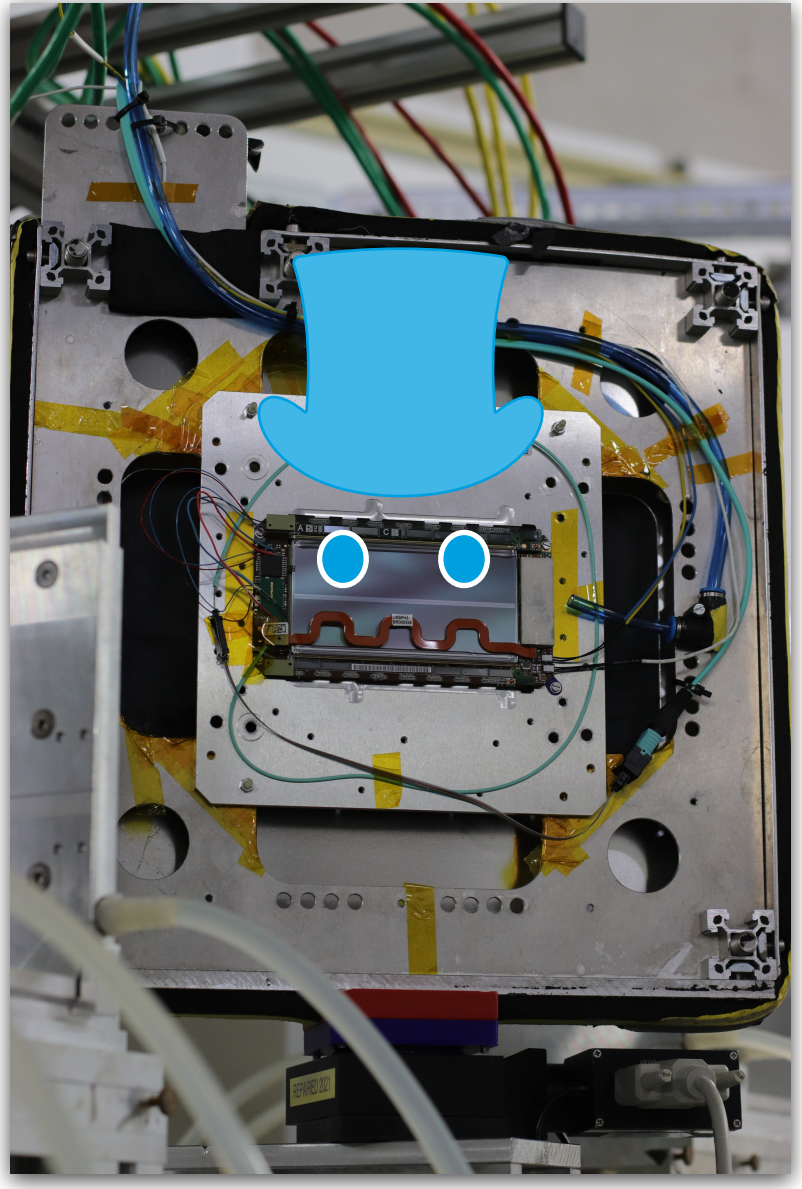
Summary

- First Pixel-Strip Module test beam results (preliminary)
- Strip noise higher than expected
- 99.6% strip efficiency, 98.6% pixel efficiency, 96% stub efficiency

"The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)".

Prospects

- Understand source of high strip noise
- Investigate hit and stub inefficiencies
- Carry on with hit and stub resolution studies, cluster size, … etc
- Test multiple modules synchronously
- Perform comparative studies with an irradiated module



THANK YOU.

Contact

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www.desy.de

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