Device simulations of a MAPS in 65 nm CMOS Imaging Technology dedicated for test beam measurements

Adriana Simancas on behalf of the Tangerine Collaboration

10th Beam Telescopes and Test Beams Workshop
Lecce, June 21th 2022

HELMHOLTZ RESEARCH FOR GRAND CHALLENGES
UNIVERSITÄT BONN
DESY.

Outline

- Introduction to TCAD Simulations
- Applications & Motivation
- Tangerine Project
- TCAD Simulations for the Tangerine Project
- Results for:
    - Standard Layout
    - N-blanket Layout
    - N-gap Layout
- Conclusion

Introduction to TCAD Simulations

Technology Computer Aided Design

- Model semiconductor devices
- Physical models to represent the wafer fabrication steps and device operation

Input

Structural characteristics:
- Physical: geometry, materials, …
- Electrical: doping profiles…

SYNOPSYS® Silicon to Software™

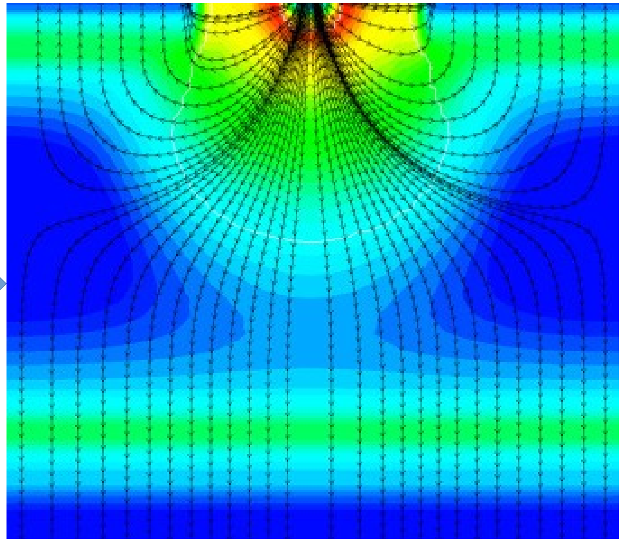
Sentaurus TCAD

Solves Poisson's equation and carrier continuity equations

Output

Electrical properties:
- I-V, C-V curves
- Electric fields
- Weighting potentials
- Pulse shape

Electric field of MAPS near collection implant

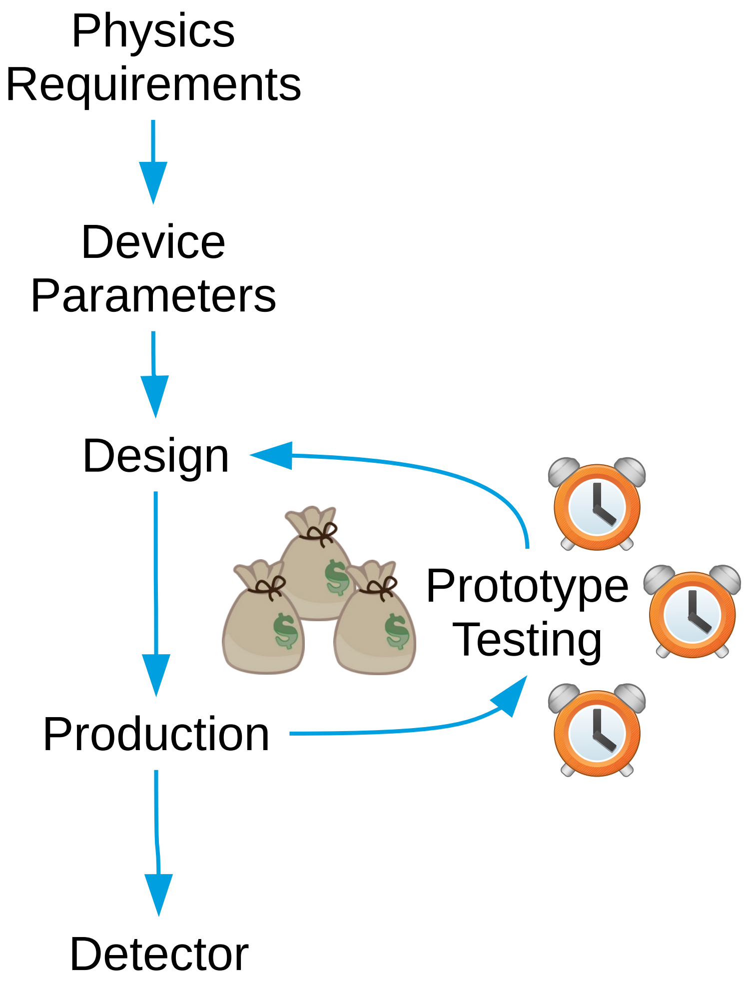


S. Spannagel et al. https://doi.org/10.1016/j.nima.2020.163784

Applications & Motivation

- Semiconductor Devices:
  - CMOS, FinFET
  - Memory (DRAM, NVM)
  - Power Devices (Si, SiC, GaN)
  - RF Devices (GaAs, InP, GaN)
  - Optoelectronics (CIS, Solar Cells, Photodetectors)
  - **Particle Detectors (since 2000's)**
    - Tangerine
    - CLICTD
    - ATTRACT FASTpix (talk by J. Braach)
    - MALTA (talk by M. Van Rijnbach)
    - ELAD
    - AGIPD
    - MSSD
    - MIMOSA
    - ...

- Development of Semiconductor Particle Detectors:



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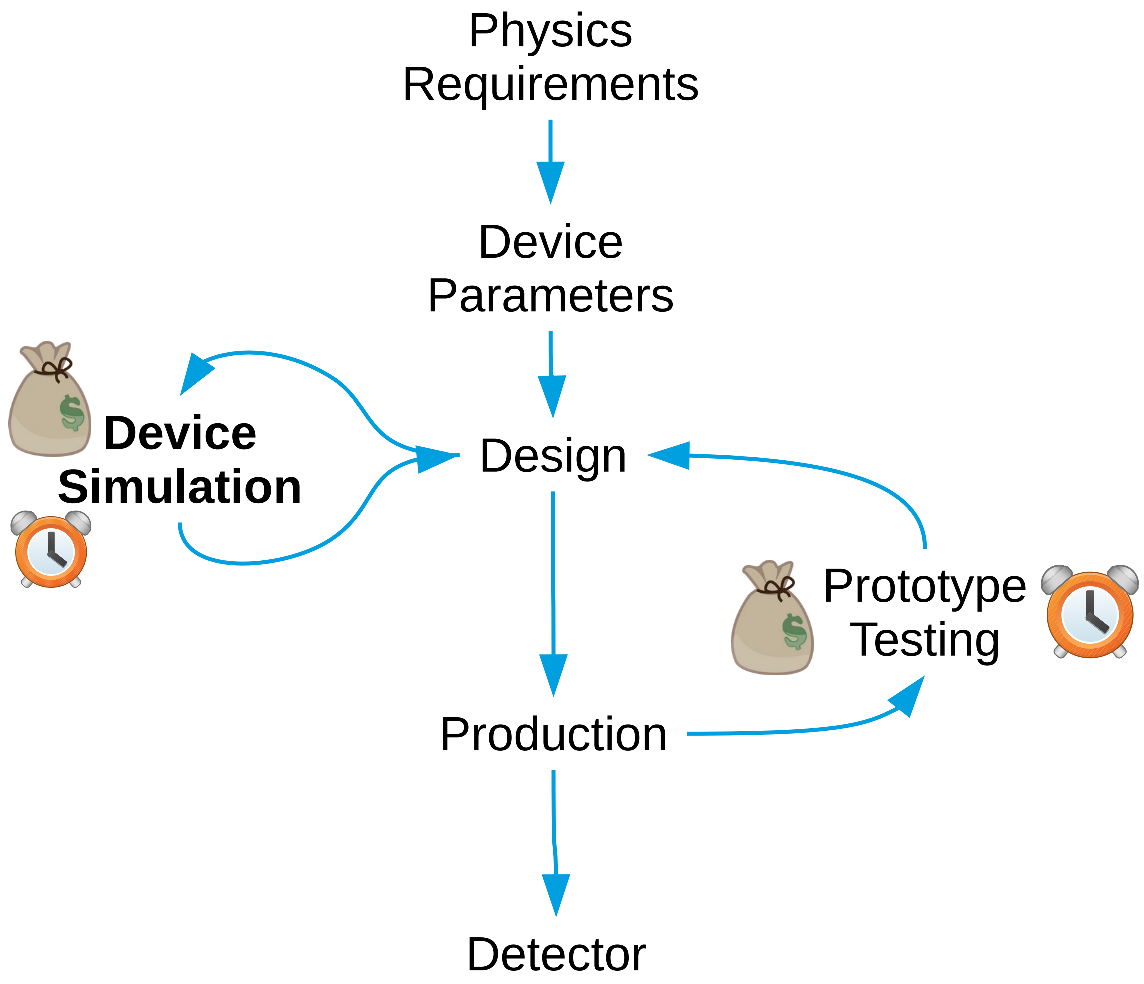
- Development of Semiconductor Particle Detectors:



Development of MAPS in 65 nm CMOS Imaging Technology

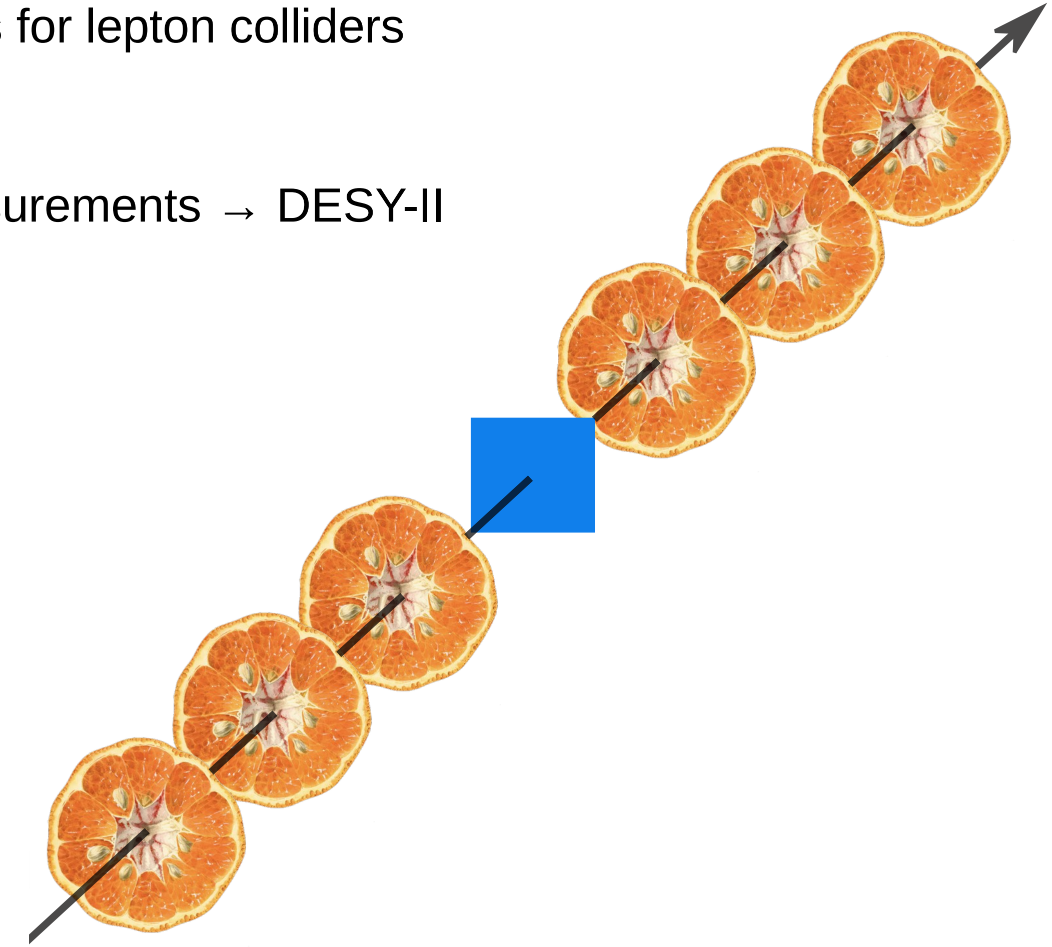
The Tangerine Project - Towards Next Generation Silicon Detectors

Goal: develop the next generation of silicon pixel sensors for lepton colliders

First application: reference detectors in test beam measurements → DESY-II (talk by A. Herkert)

Performance targets:

- Position resolution ≤ 3 µm
- Time resolution ~ 1 – 10 ns
- Material budget ~ 50 µm Si



Development of MAPS in 65 nm CMOS Imaging Technology

The Tangerine Project - Towards Next Generation Silicon Detectors

Challenges of small collection electrode MAPS:

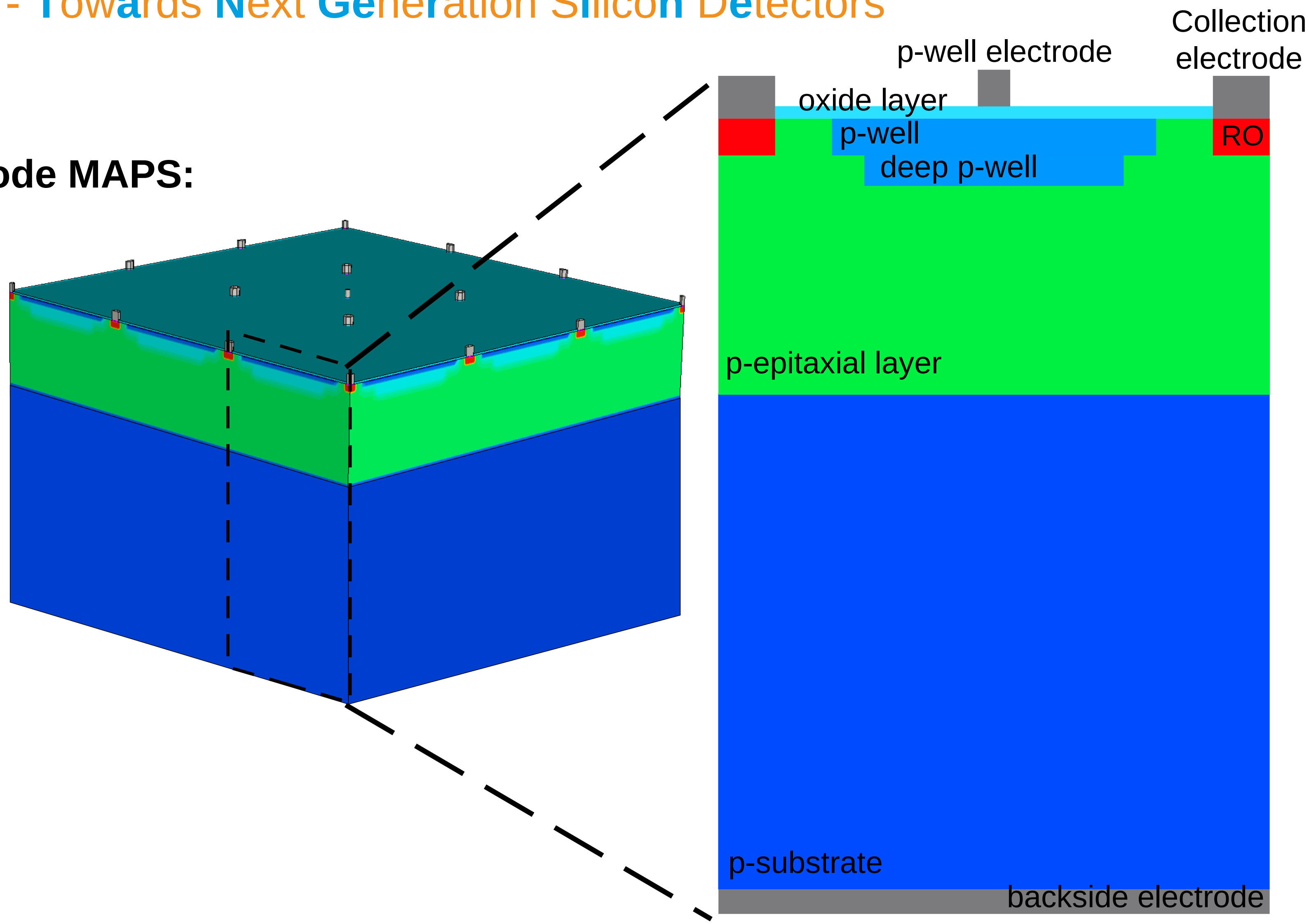
- Small signal → ASIC design
- Slow charge collection (diffusion)

⇩

Electric Field Optimization

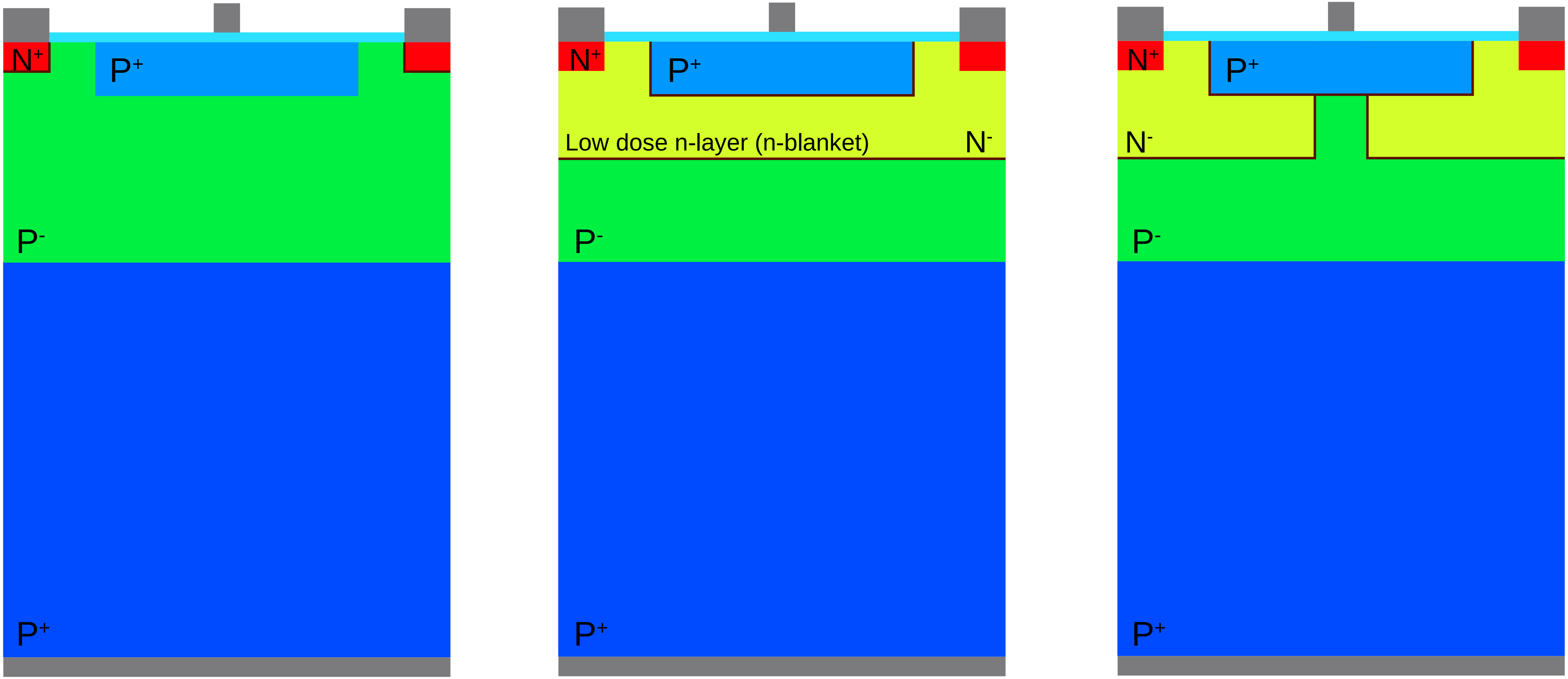
⇩

Sensor Design



Sensor Modifications

Standard Layout | N-blanket Layout | N-gap Layout

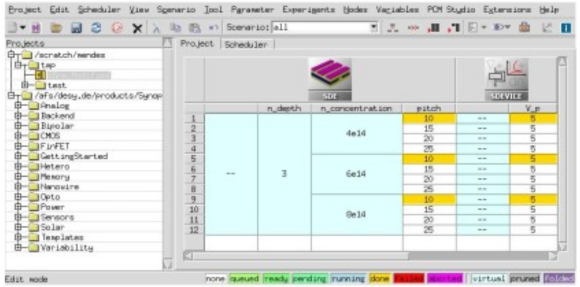


TCAD Simulations for the Tangerine Project

Goal: optimization of electric field → **Device simulations with TCAD** + MC simulations with Allpix^2

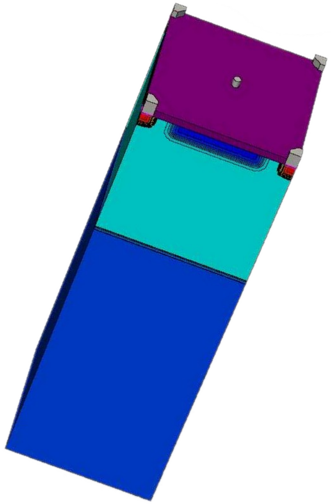
Manage simulations

Sentaurus Workbench (SWB)



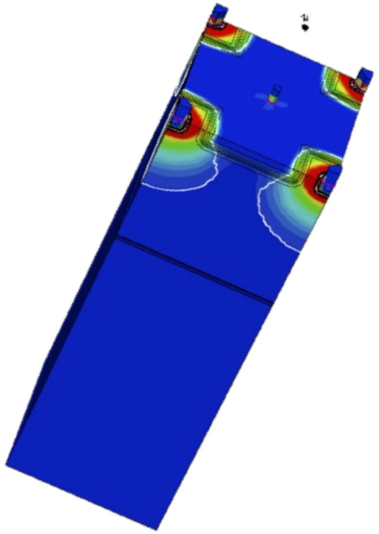
Create detector geometry

Sentaurus Structure Editor (SDE)



Obtain electrical properties

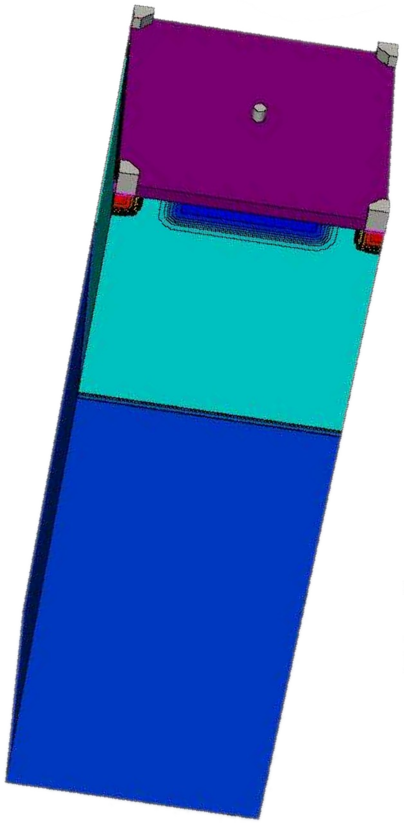
Sentaurus Device (SDEVICE)



Visualize results

Sentaurus Visual (SVISUAL)

TCAD Simulations: Needs and Strategy



What we need:

- Geometrical parameters ✗
- Doping profiles ✗

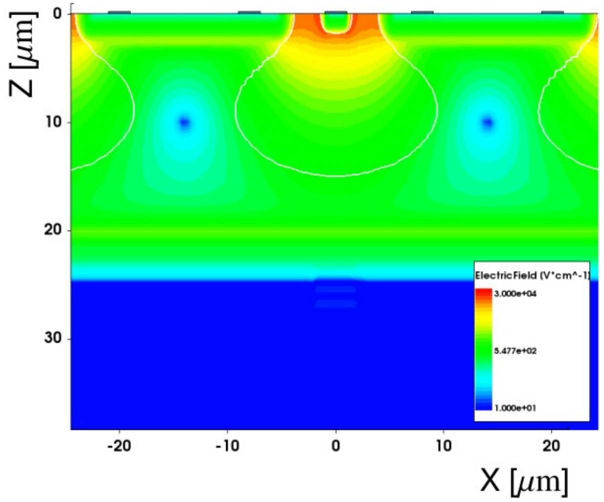
→ No access to real doping profiles

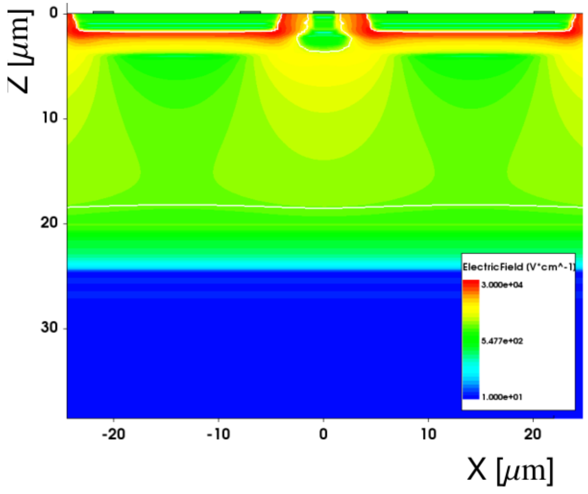
Strategy:

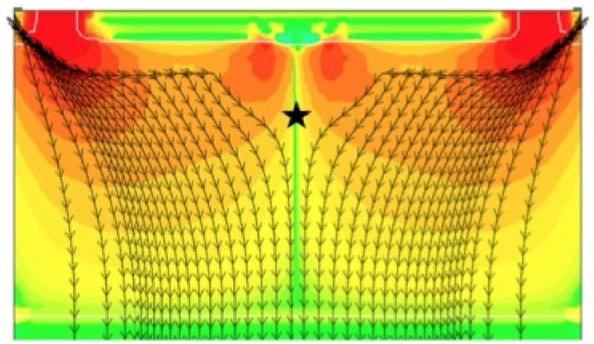
Use generic doping profiles and scan over different parameters.

Scans:

Select parameter to study, vary it within range of values while fixing all the other parameters and observe behavior of electric, lateral field and depleted volume.



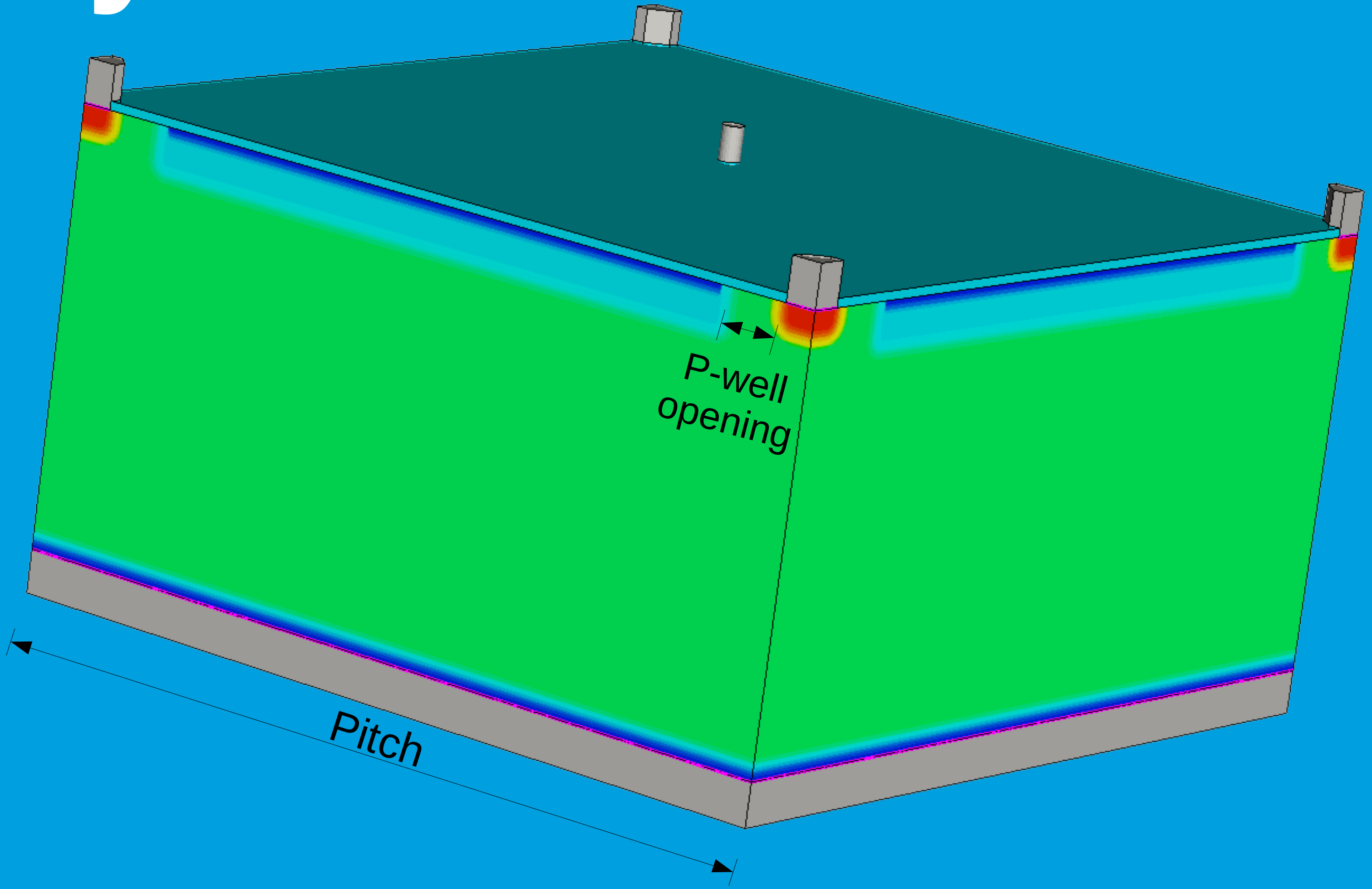




Münker, M. 2018, "Test beam and simulation studies on High Resistivity CMOS pixel sensors", PhD Thesis, Universität Bonn, Bonn.

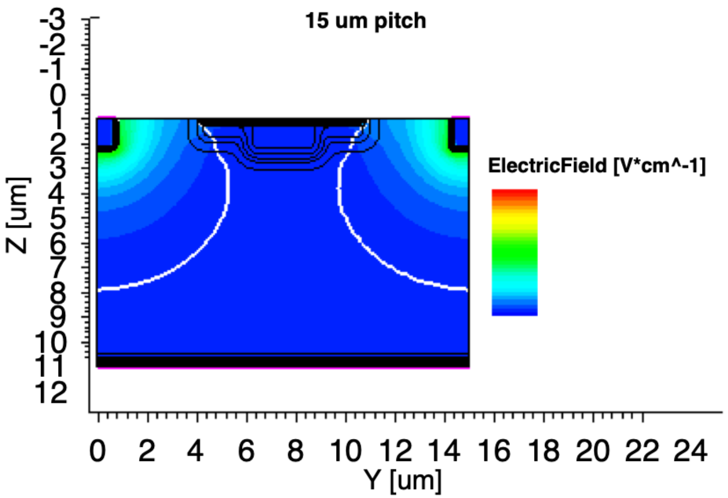
Results for Standard Layout

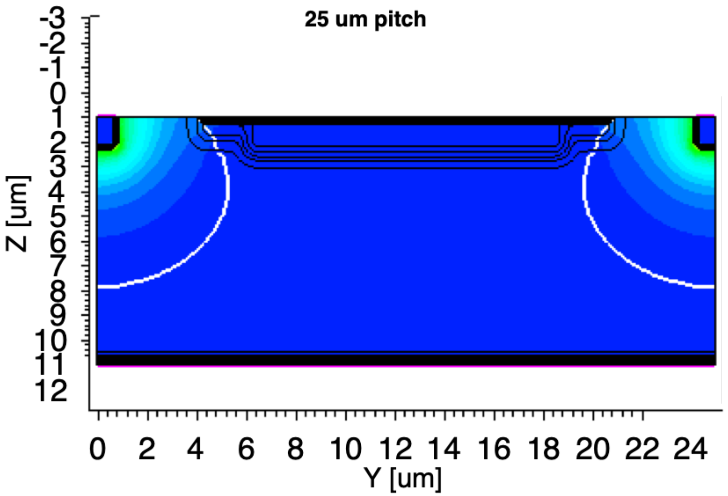
- Pitch
- P-well opening
- Transient simulation



Results for Standard Layout

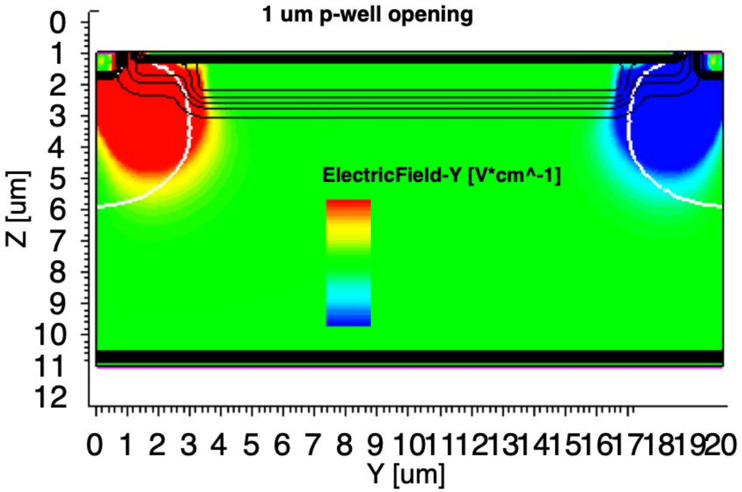
- **Pitch:** Decreasing improves depleted volume fraction within the sensor.

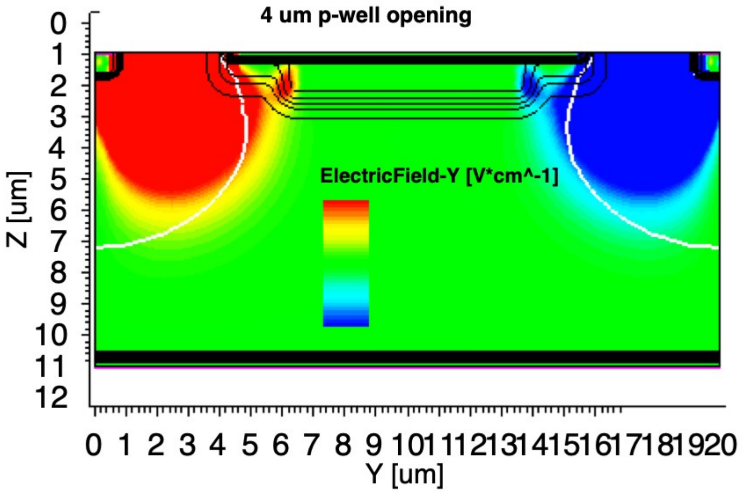




- More charge collected
- Less space for electronics

- **p-well opening:** Increasing improves lateral field.





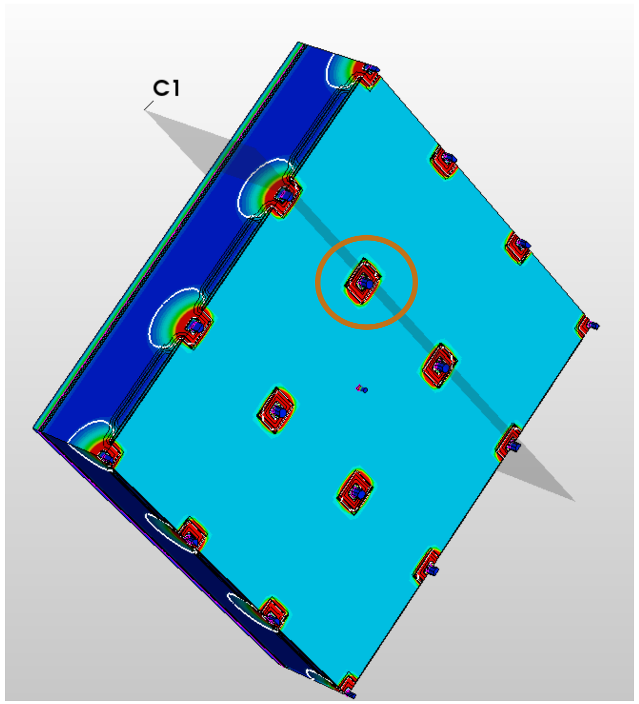
- More charge collected
- Faster collection
- Less space for electronics

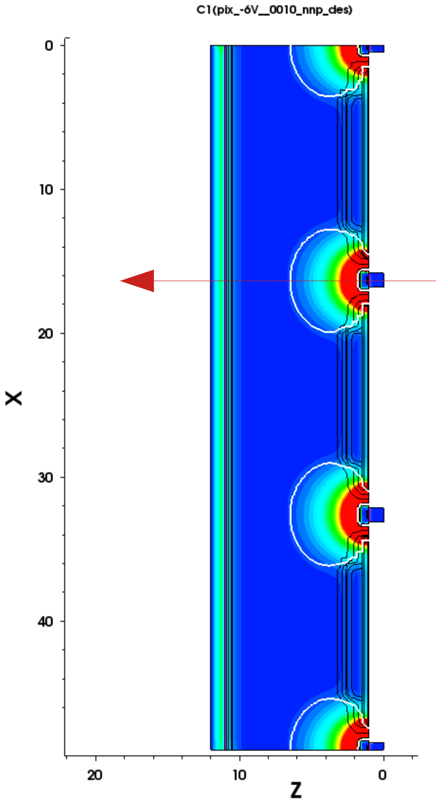
By A. Velyka

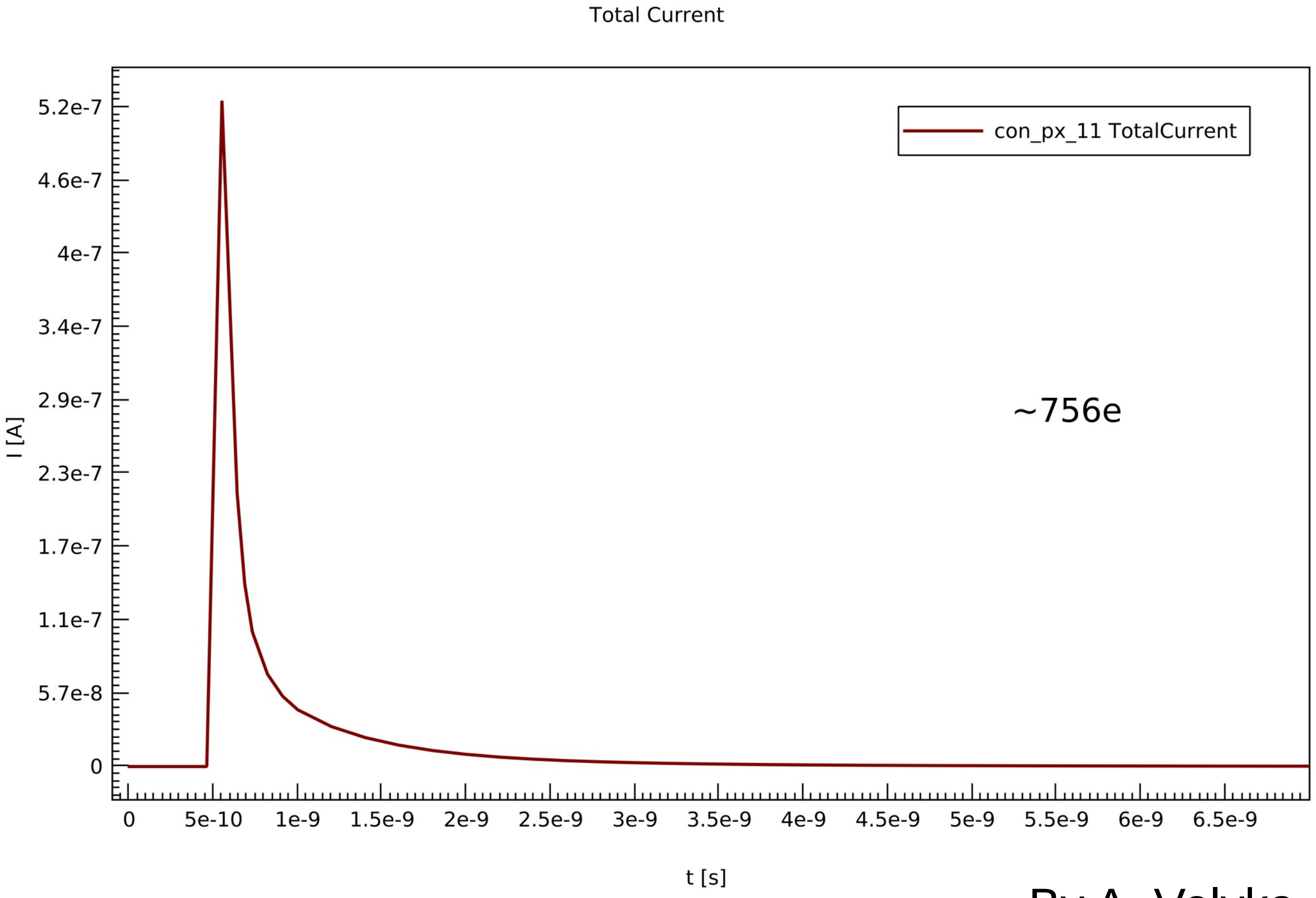
Results for Standard Layout

- **Transient Simulation:** Best case scenario (particle traversing center of pixel)

  - Estimate signal characteristics → useful input for ASIC designers and MC simulations



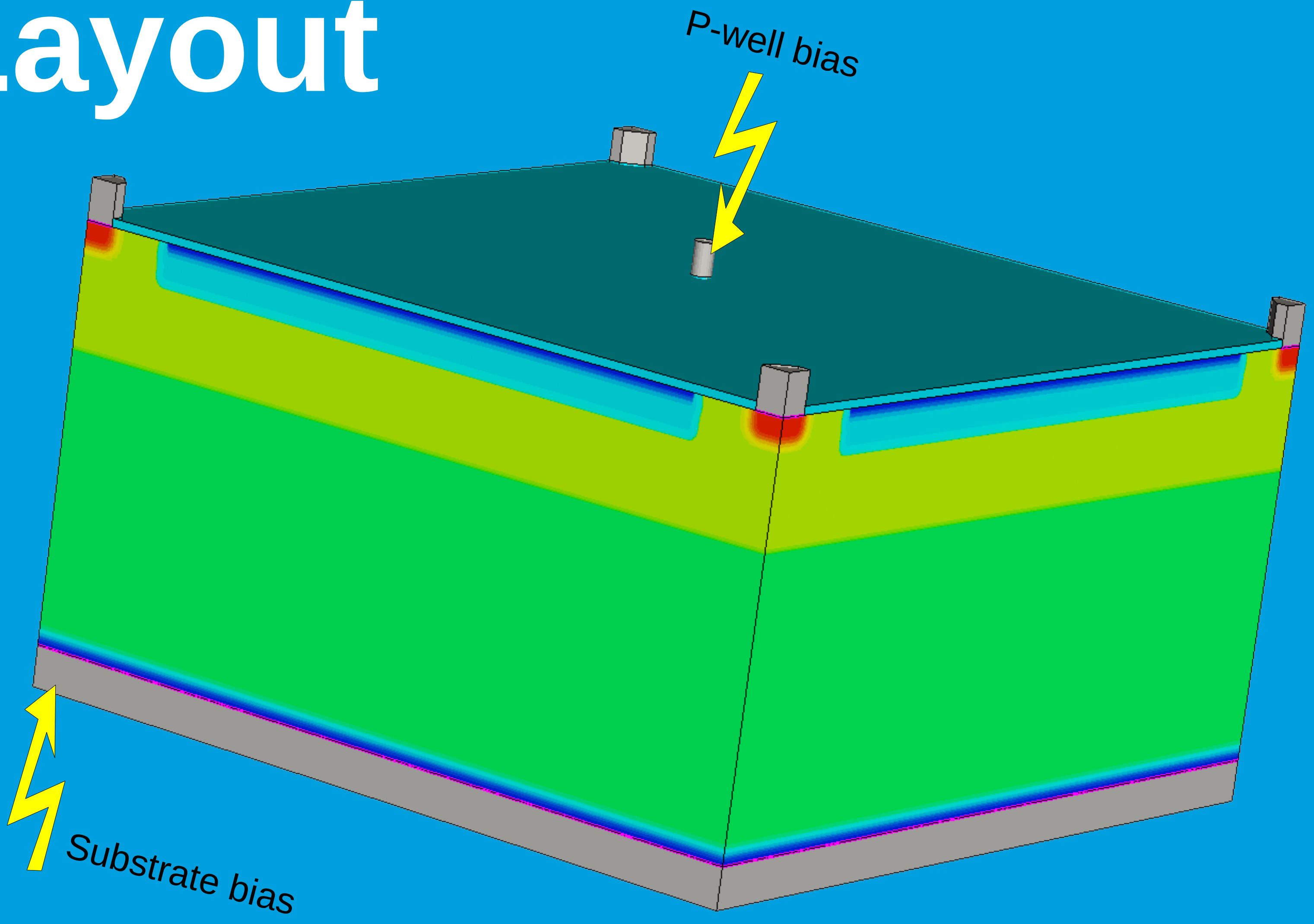




By A. Velyka

Results for N-blanket Layout

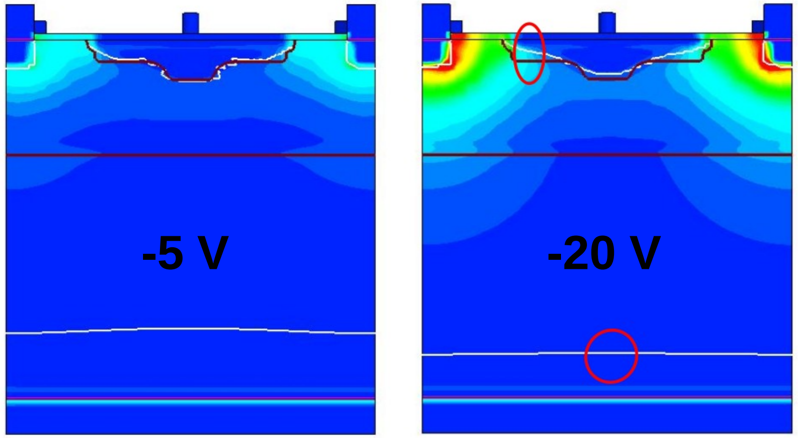
- Substrate and p-well bias



Results for N-blanket Layout

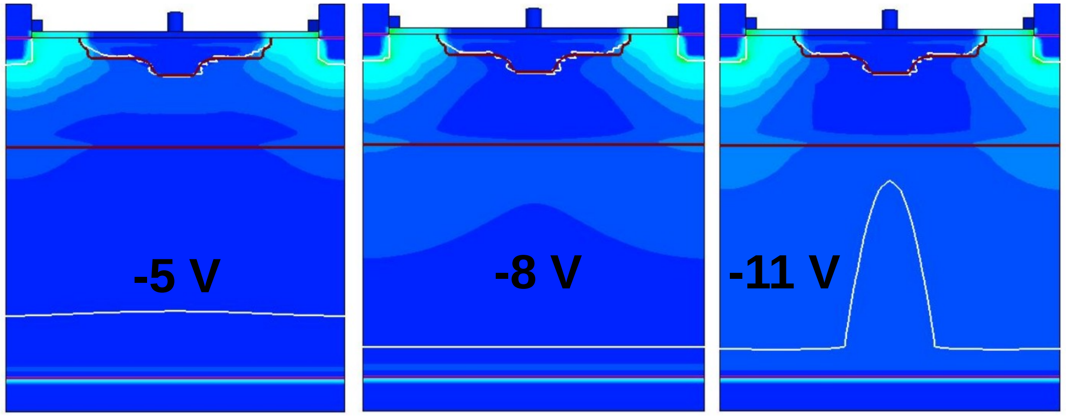
- Bias scan over p-well and substrate simultaneously
- Bias scan over substrate only, p-well fixed at -5 V

Electric Field

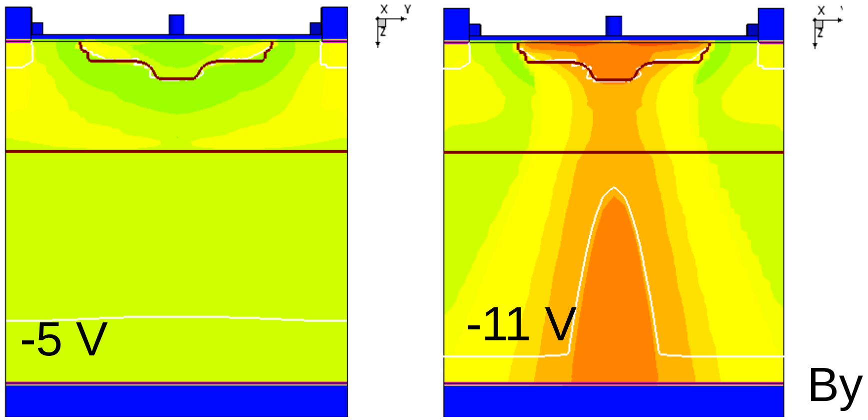


- Increase depleted volume
- High electric field inside p-well
→ damage to readout electronics

Electric Field



Total Current Density

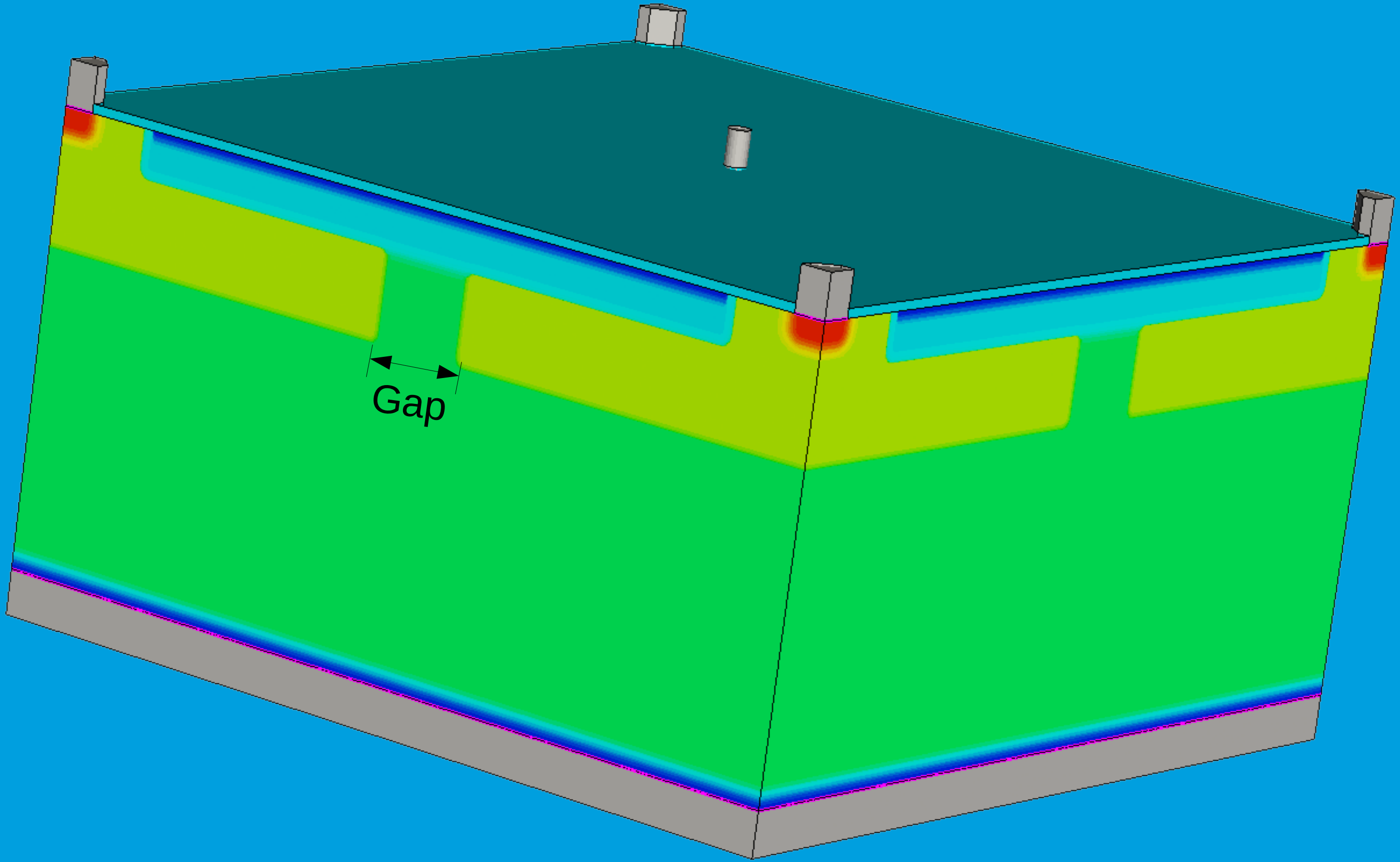


- Increase depleted volume
- P-well integrity conserved
- Breakdown at -11 V

By L. Mendes

Results for N-gap Layout

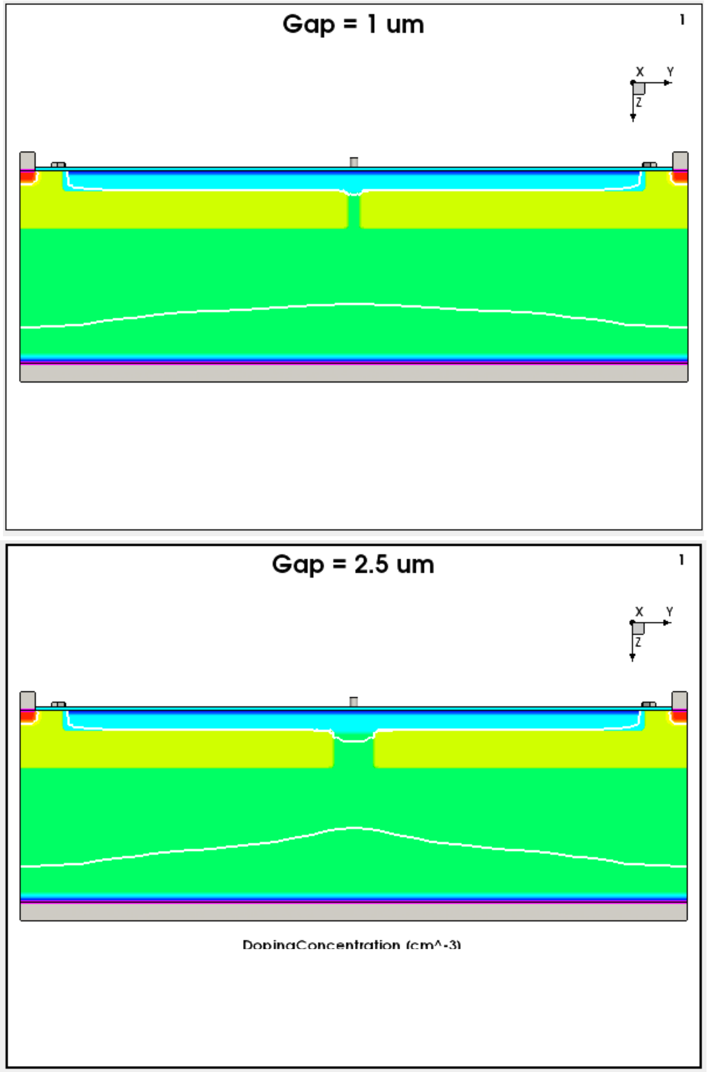
- Gap size



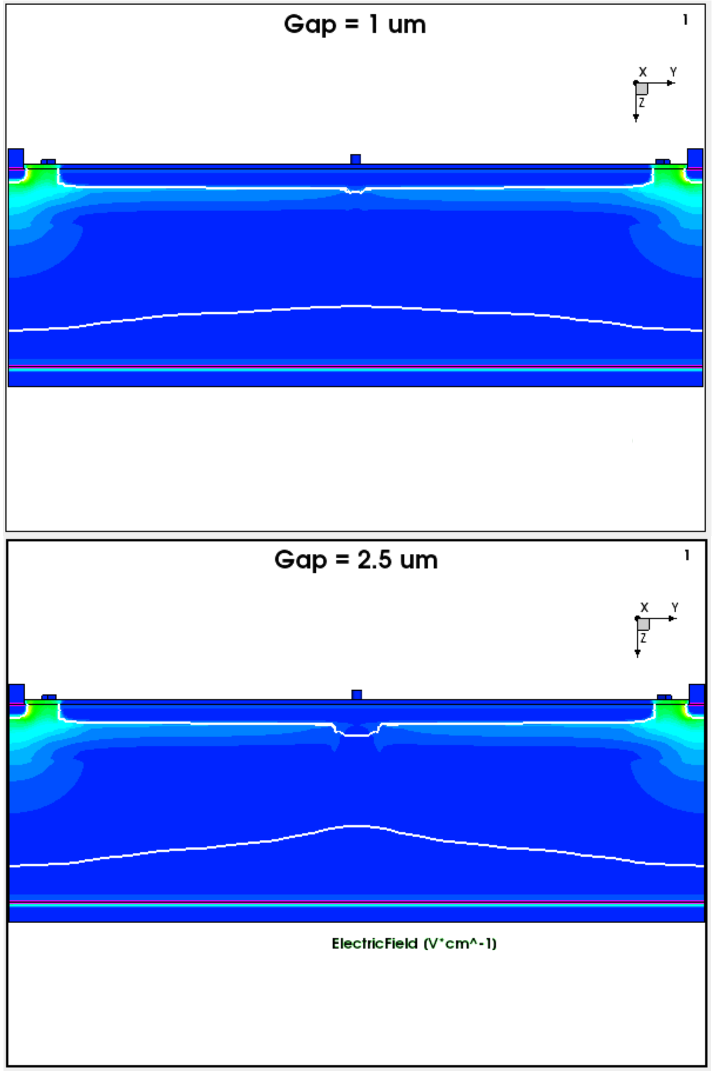
Results for N-gap Layout

- **n-gap size**: Increasing improves lateral field in corner of pixels. → - Faster charge collection
  - Less charge sharing

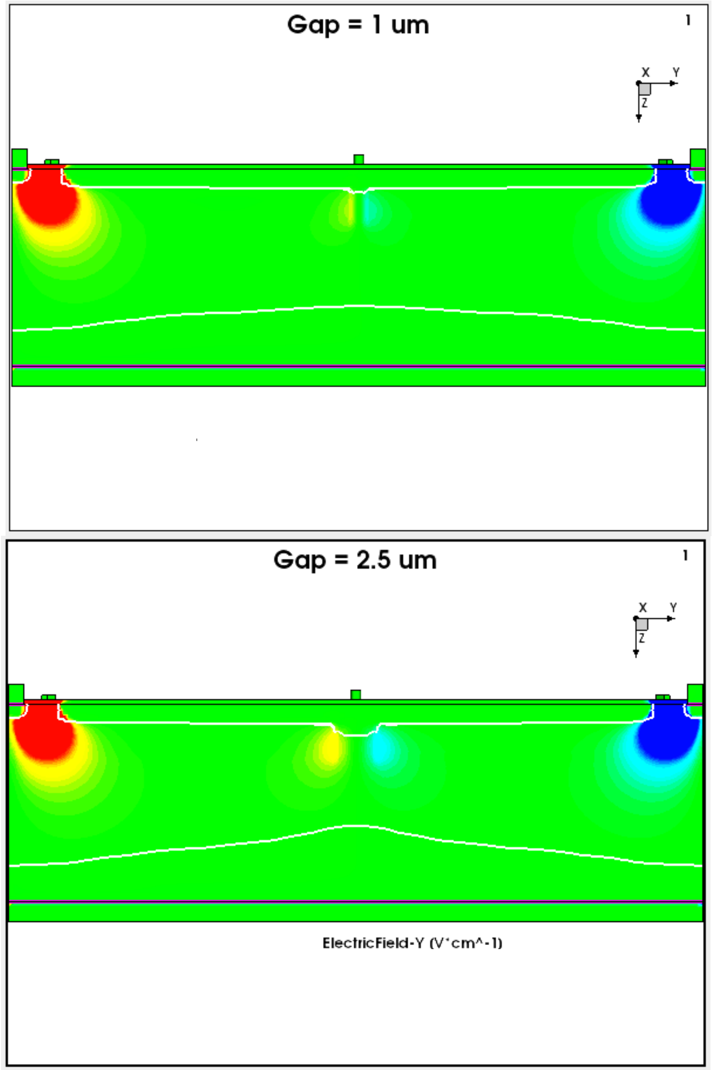
Doping Concentration



Electric Field



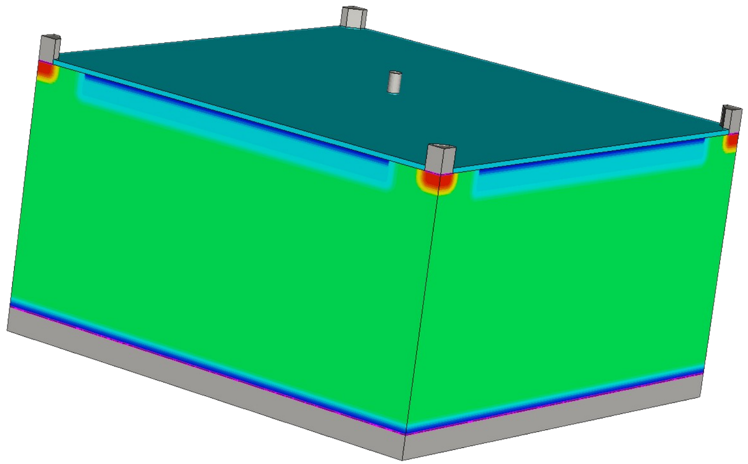
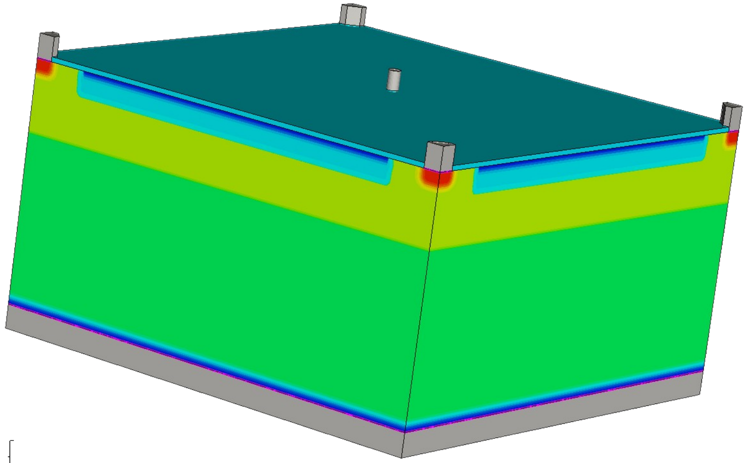
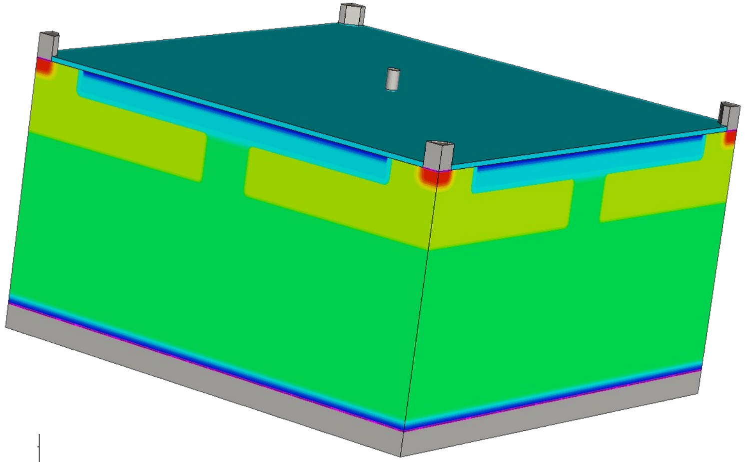
Lateral Field



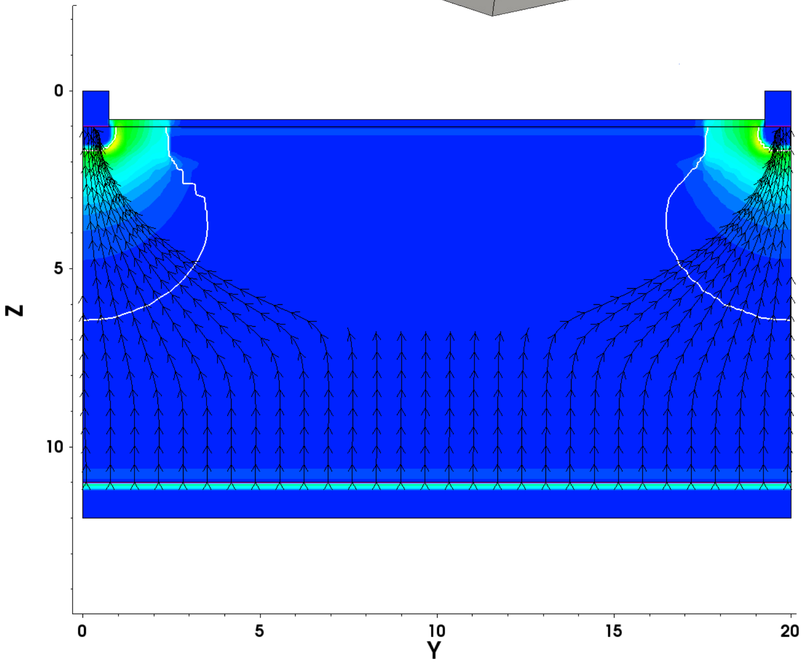
All Layouts After Tuning Parameters

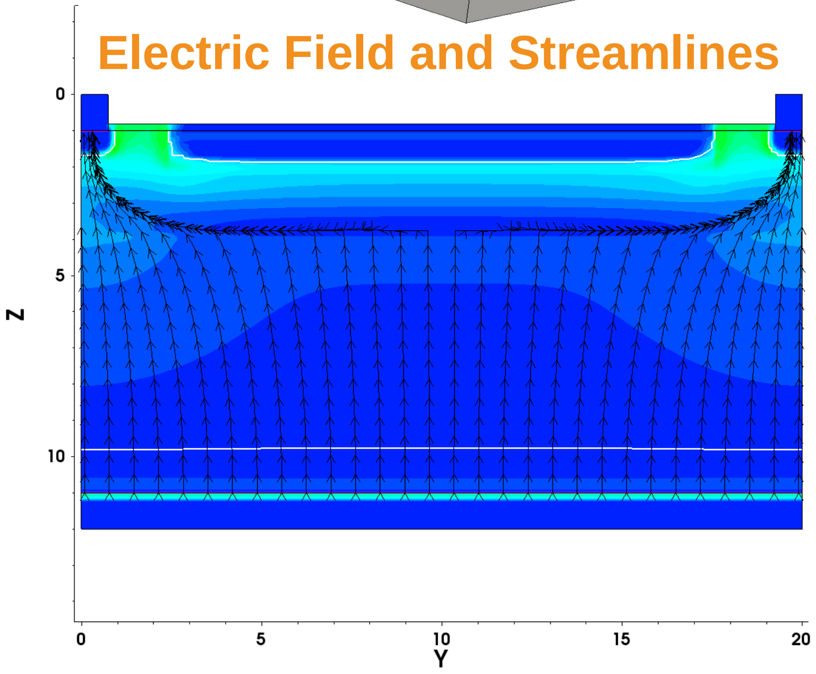
Standard Layout | **N-blanket Layout** | **N-gap Layout**

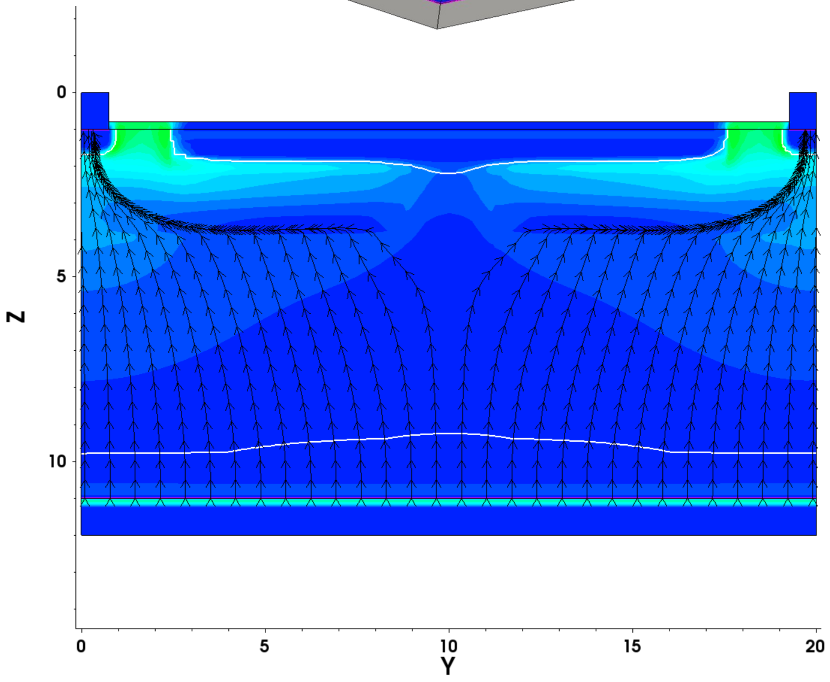
Doping Concentration

Electric Field and Streamlines

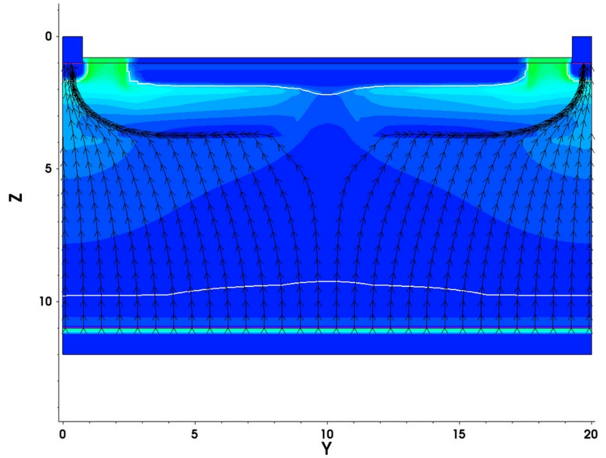






Conclusions

- TCAD simulations using generic doping profiles have provided very useful insights for sensor optimization.
- Sensor layouts: standard, n-blanket and n-gap.
- Scans: pitch, p-well opening, substrate and p-well bias, n-gap size…
- Transient studies.
- Understood effect of parameters on electric field and depleted volume.
- Established sensible values for some parameters.
- Complemented with Monte Carlo Simulations using Allpix^2 (see talks from M. Del Rio Viera and S. Ruiz Daza).
- Experimental results of first test structures (see talk from G. Vignola).



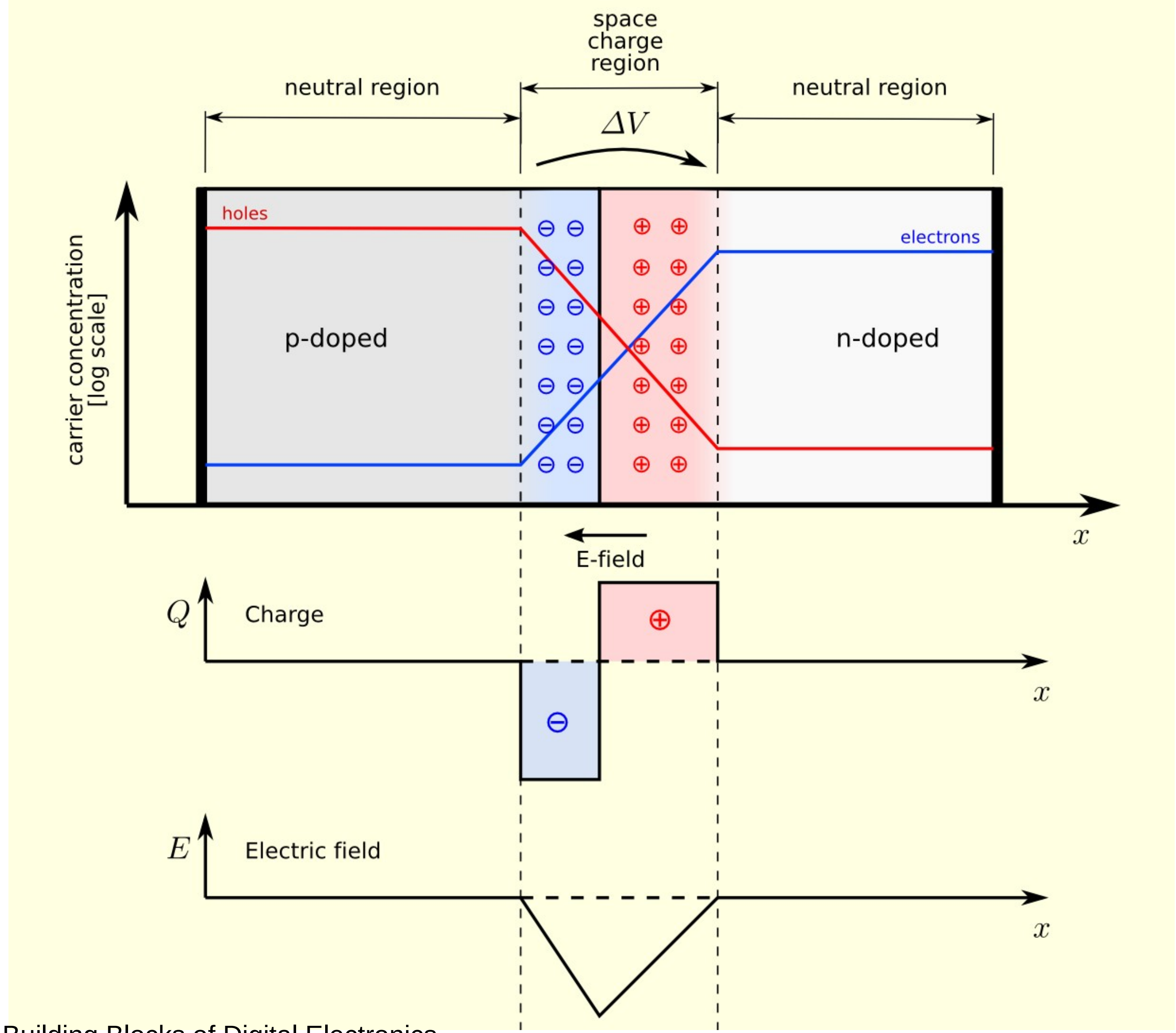
Prospective Work

- Continue transient studies.
- Capacitance studies.
- Weighting potentials.
- Hexagonal grid.

Thank you!

Backup

PN Junction



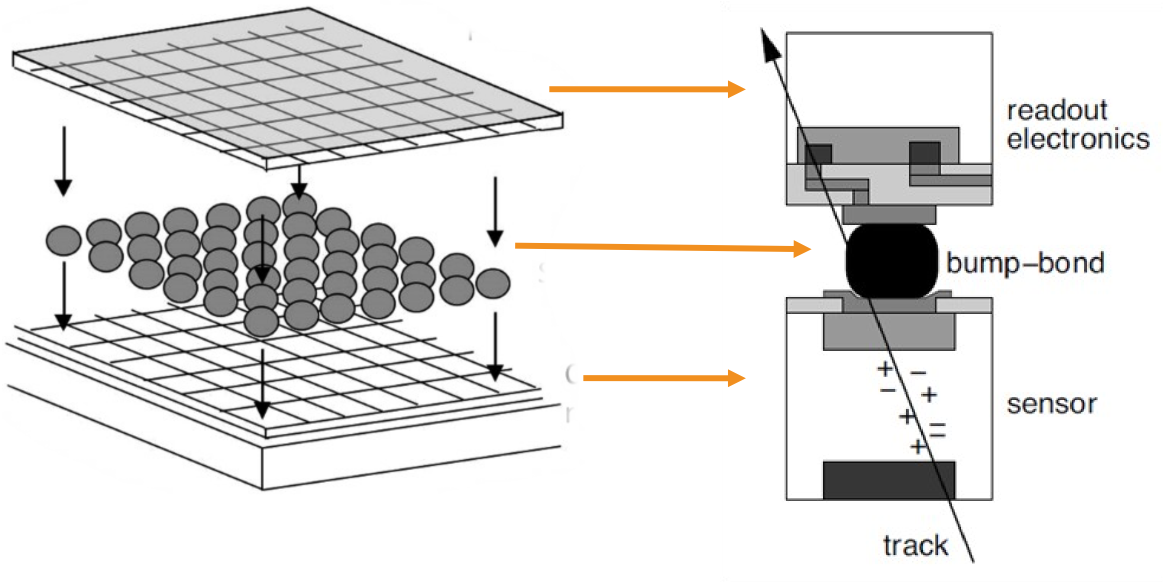
Fairfield, J. (2022). P-N Junctions: Building Blocks of Digital Electronics.

From https://letstalkaboutscience.wordpress.com/2012/06/28/p-n-junctions-building-blocks-of-digital-electronics/

State-of-the-art Silicon Pixel Sensors

DEVELOPMENT

Hybrid

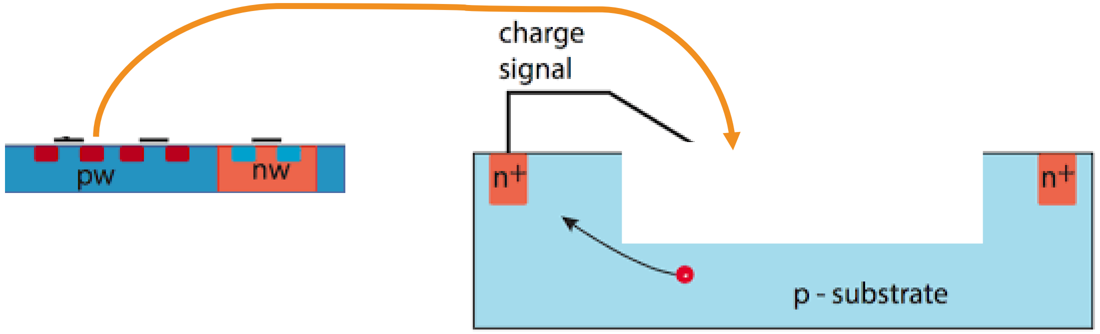


Adapted from D. Pennicard and N. Wermes

Monolithic

Readout Electronics

Sensor



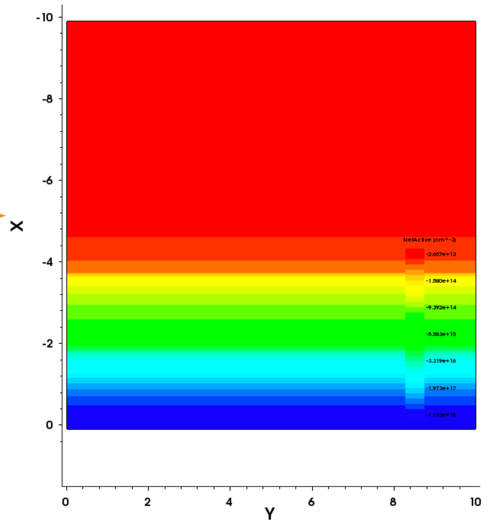
Adapted from H. Kolanoski and N. Wermes

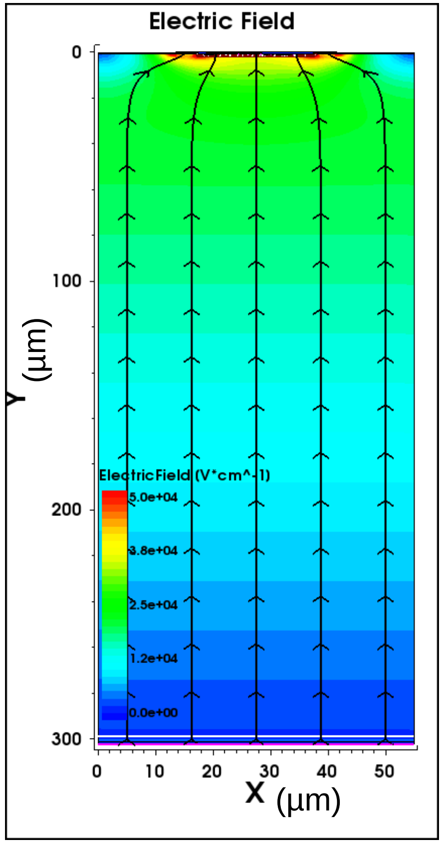
- Material
- Production effort
- Cost

→ **Reduced**

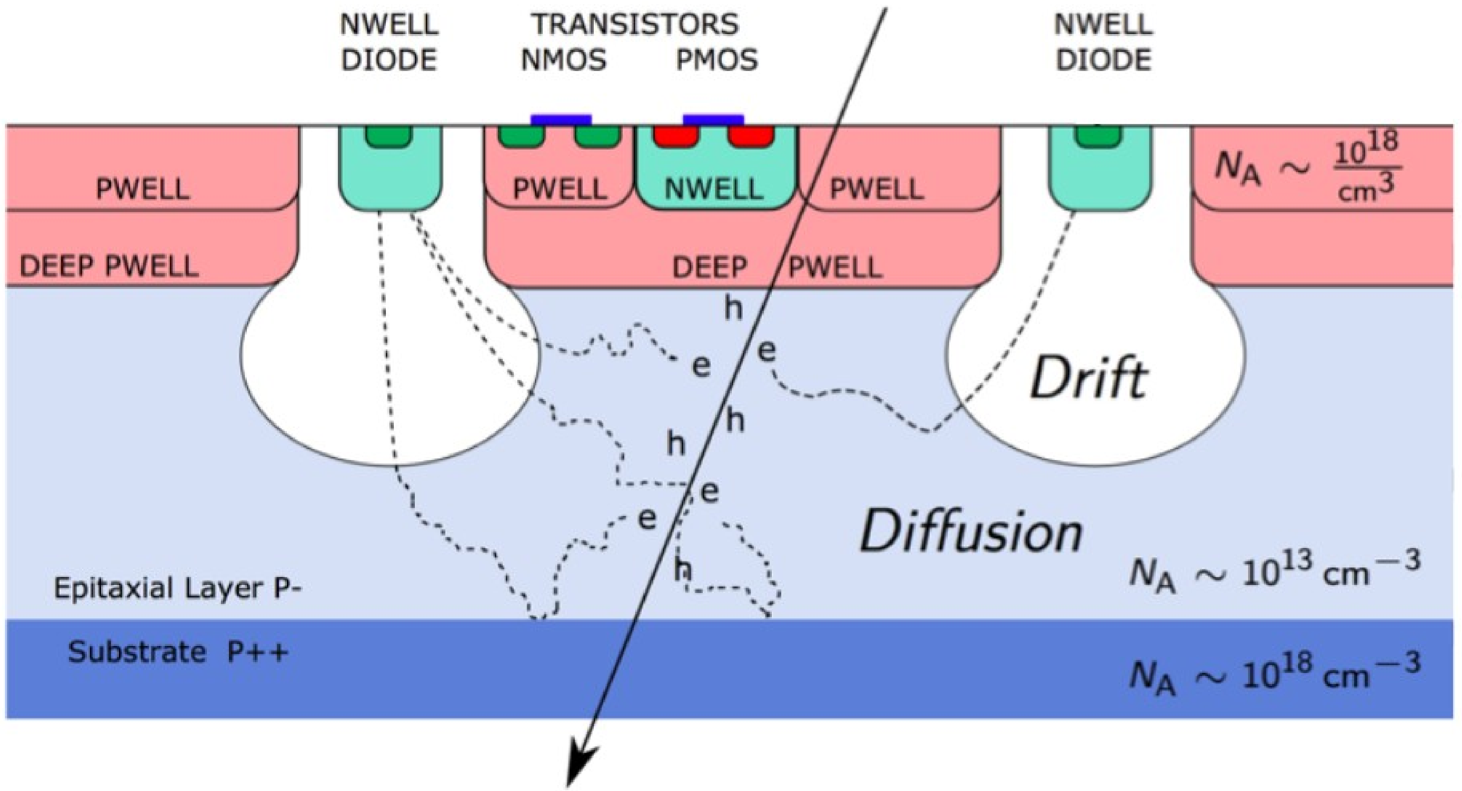
TCAD Tools

- **Process Simulations:** fabrication steps in silicon process technologies in 2D and 3D.
- **Structure Editing:** build and edit device structures in 2D and 3D using geometric operations.
- **Device Simulations:** electrical, thermal, and optical characteristics of silicon and compound semiconductor devices in 2D and 3D.
- **Interconnect Simulations:** physical phenomena concerned with back-end-of-line reliability.
- **Frameworks:**
  - Workbench: graphical environment for creating, managing, executing, and analyzing TCAD simulations.
  - Visual: interactive 1D, 2D, and 3D visualization and data exploration environment.
  - Process Compact Model Studio: encapsulate relationships between process variations and device performance to identify manufacturing problems.





Charge movement within sensor



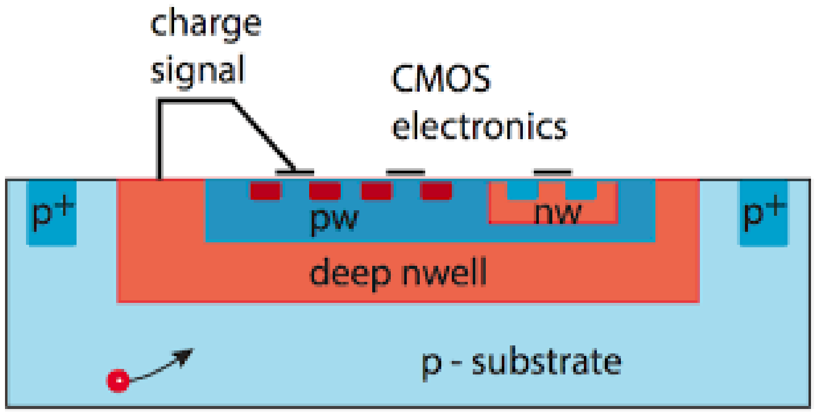
(c)

Figure 1. Top view of a sub-matrix (a) and of a pixel (b). (c) Cross-section of the TJ180 standard process for p-type epi silicon and substrate and n-type collection diode.

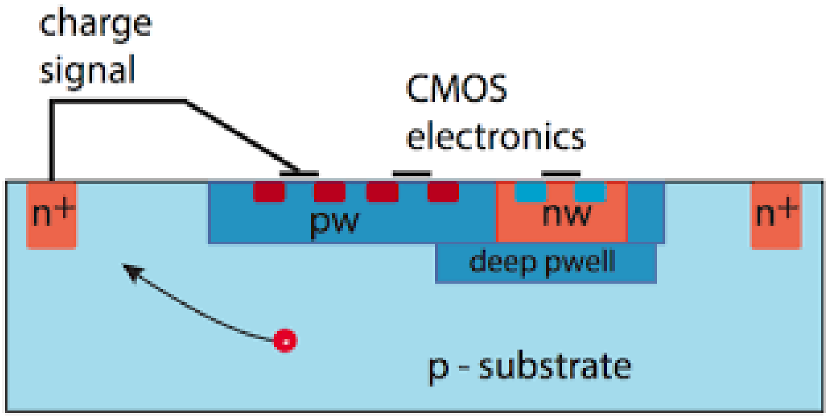
H. Pernegger et al. 2017, “First tests of a novel radiation hard CMOS sensor process for Depleted Monolithic Active Pixel Sensors”, JINST 12 P06008.

Monolithic Active Pixel Sensors - MAPS

Large collection electrode



Small collection electrode



From H. Kolanoski and N. Wermes

- High electric field
- Good timing
- Short drift paths
- Radiation hard

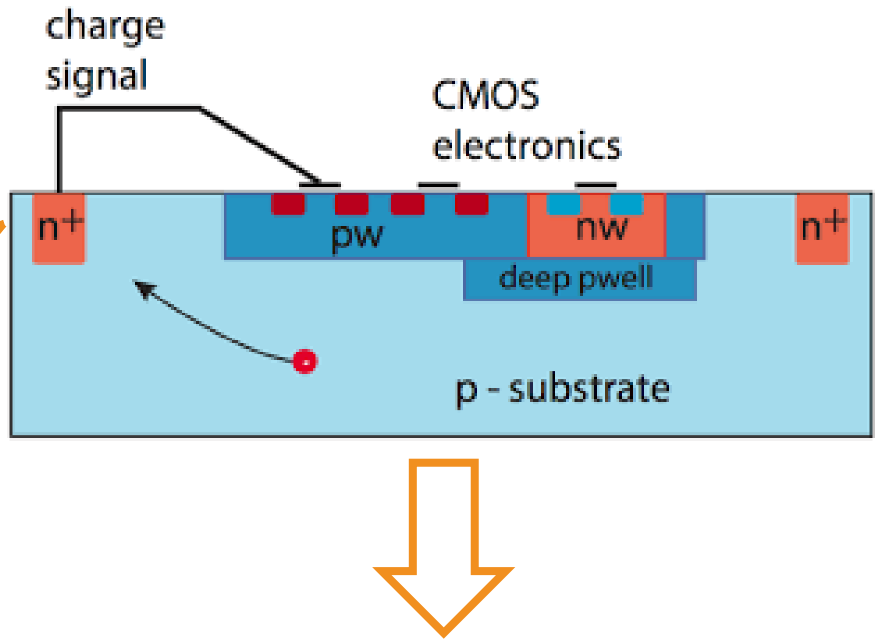
- Small capacitance (~fF)
- High signal/noise
- Low power consumption (~V)
- Slow charge collection (diffusion, ~100 ns)

Why Monolithic Active Pixel Sensors (MAPS)?

Pixel detectors in HEP used as track and vertex detectors.

General requirements for pixel sensors:

- Spatial resolution
- Time resolution
- **High S/N**
- Radiation hardness
- **Low material budget**
- **Low power consuption**
- Low pasive materials (mechanic, cooling, …)
- **Costs and production effort reduction**

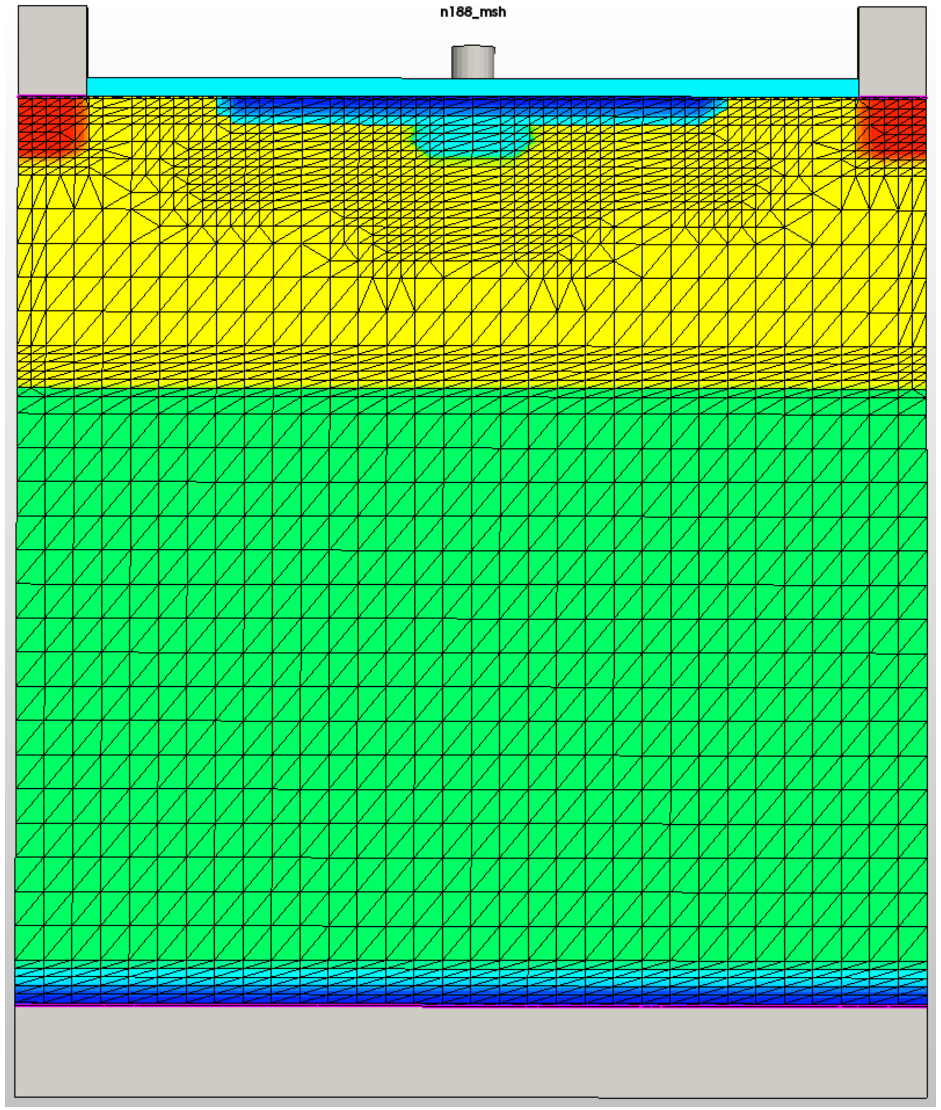


Small capacitance

Mesh Example

Dependent on Doping Concentration

- Finite-element mesh
- In 2D: triangles, in 3D: tetrahedra.
- Calculation of the quasistationary simulation performed in the vertices of these shapes

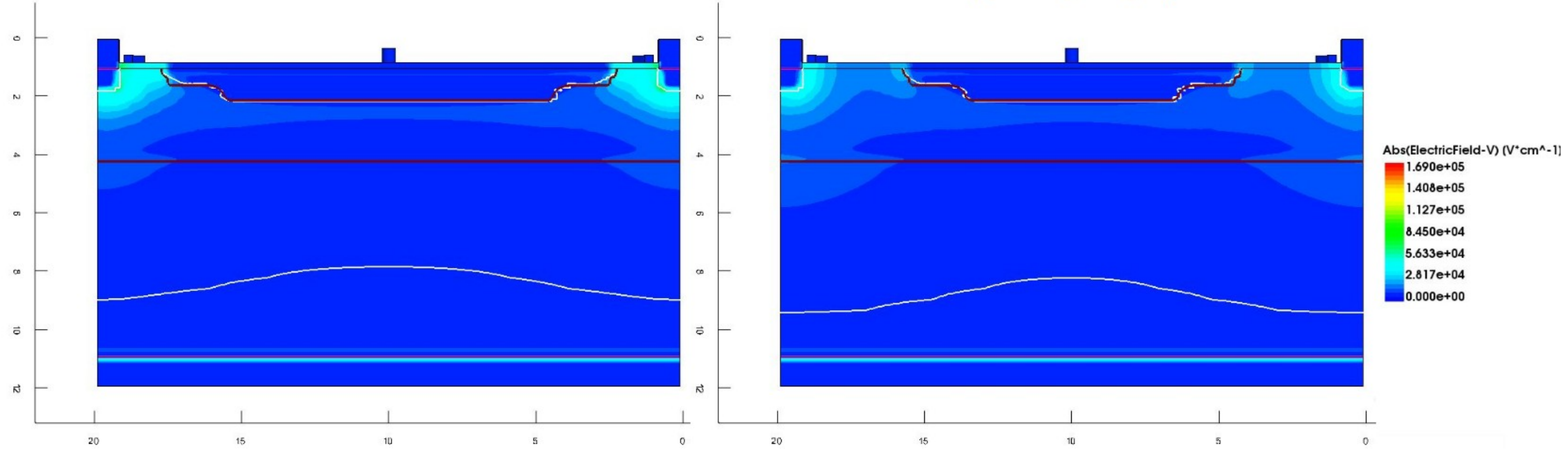


N-blanket Layout | p-well opening Scan

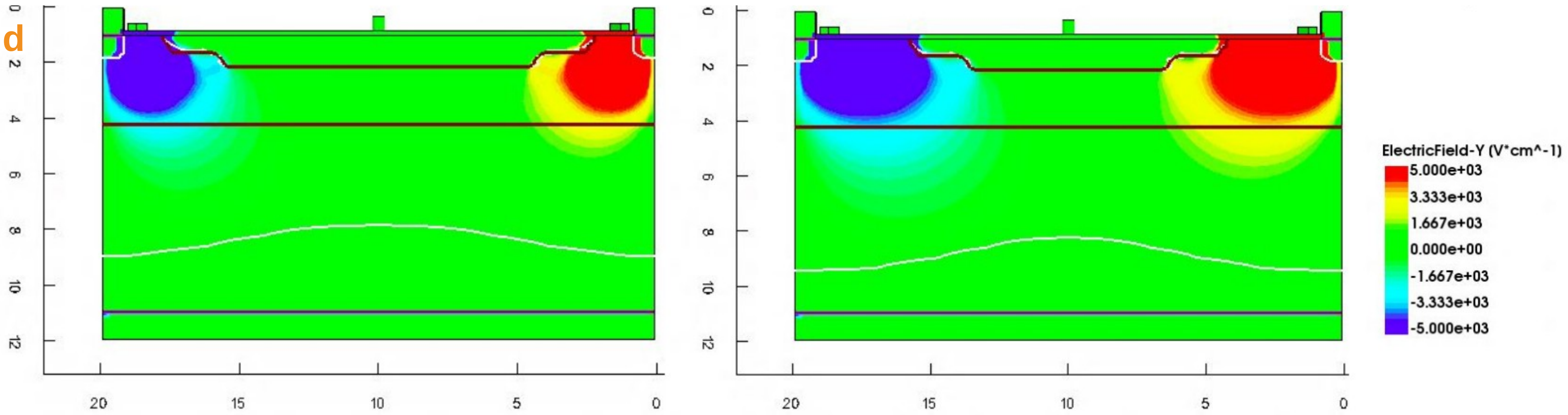
Electric Field

p-well opening 2 µm
deep p-well opening 2 µm

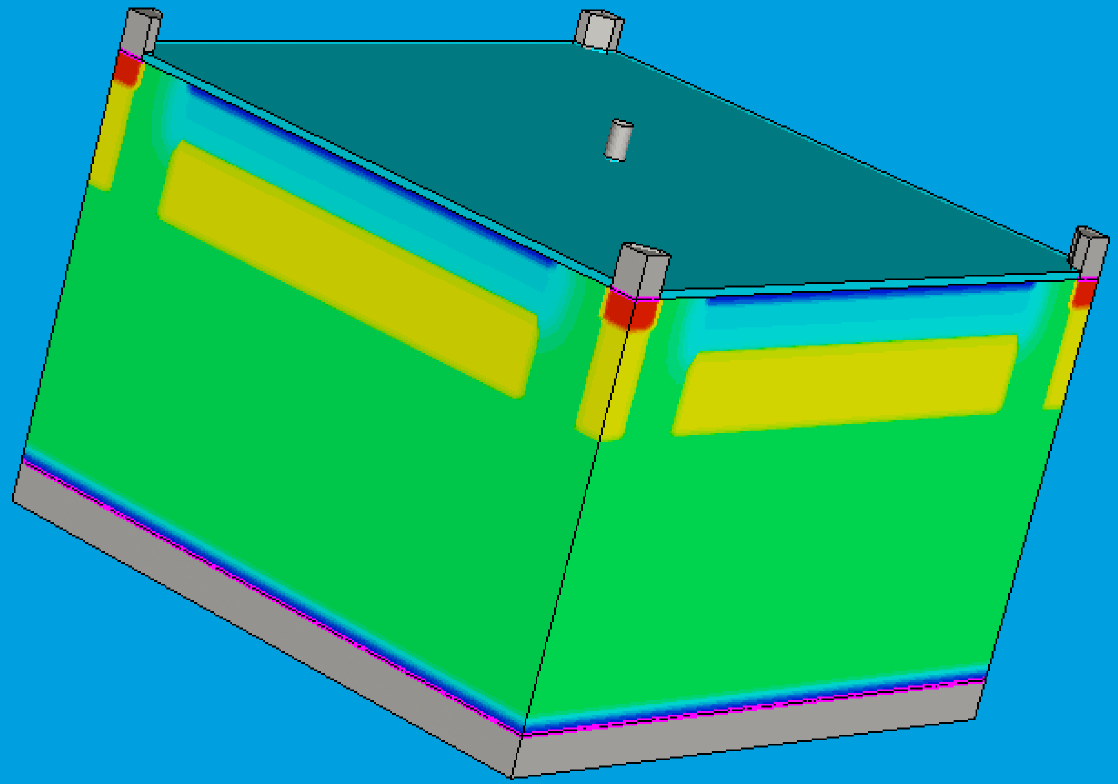
p-well opening 4 µm
deep p-well opening 2 µm



Lateral Electric Field



MLR1

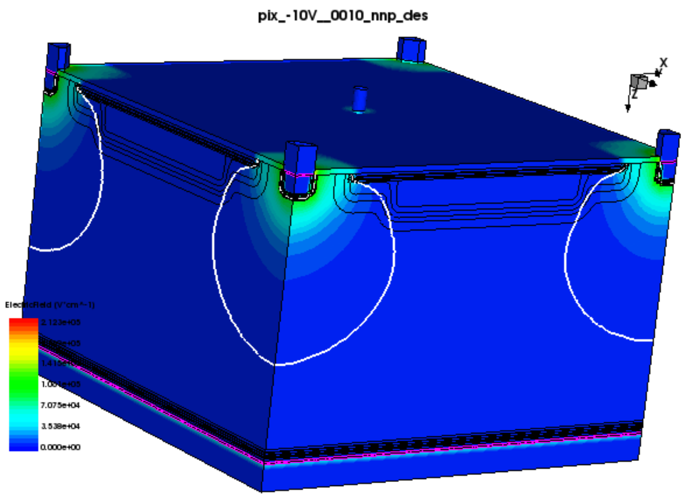


Simulations of MLR1 Test Structure

Simulation Parameters

Known:

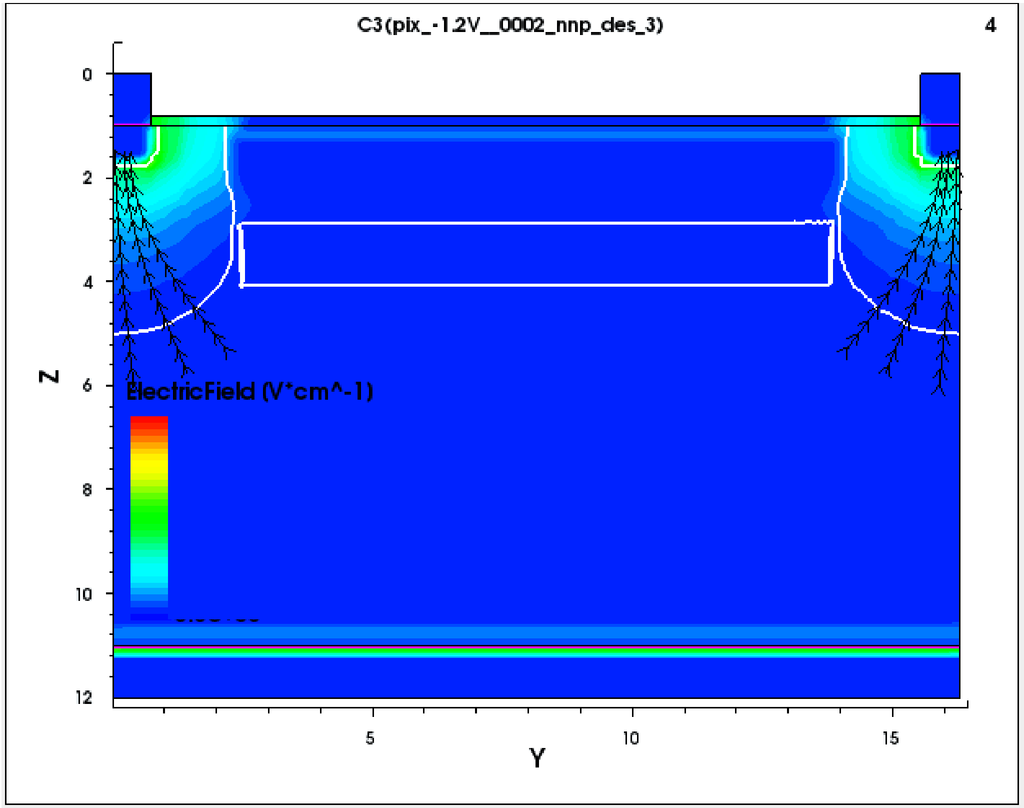
- Pitch: 16.3 µm
- RO implants shape: octagon
- RO implants diameter: 1.1 µm (used 1 µm)
- p-well opening shape: square
- p-well opening: 2 µm



MLR1

Pitch (µm)	Scans/Studies	Conclusions
16.3	Standard Layout	Streamlines show charge collection from just a small fraction of the epi layer
	N-blanket Layout	

Standard Layout



N-blanket Layout