Digital Pixel Test Structure characterization with the ALPIDE telescope

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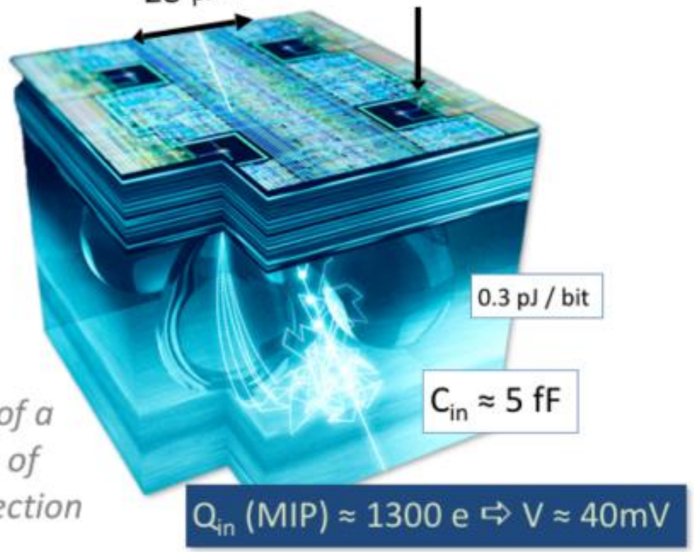
Motivation

- Development and characterization of sensors for the ALICE Inner Tracking System (ITS) upgrade
  - ➢ Monolithic CMOS pixel sensors (MAPS) with small collection electrode
  - ➢ Low noise, low power consumption, reduced material budget
  - ➢ ALPIDE (ALice Pixel DEtector) chip (180 nm CMOS MAPS) is the base of the current tracker
  - ➢ It is the starting point for the ITS3 development



Artistic view of a SEM picture of ALPIDE cross section
Not to scale

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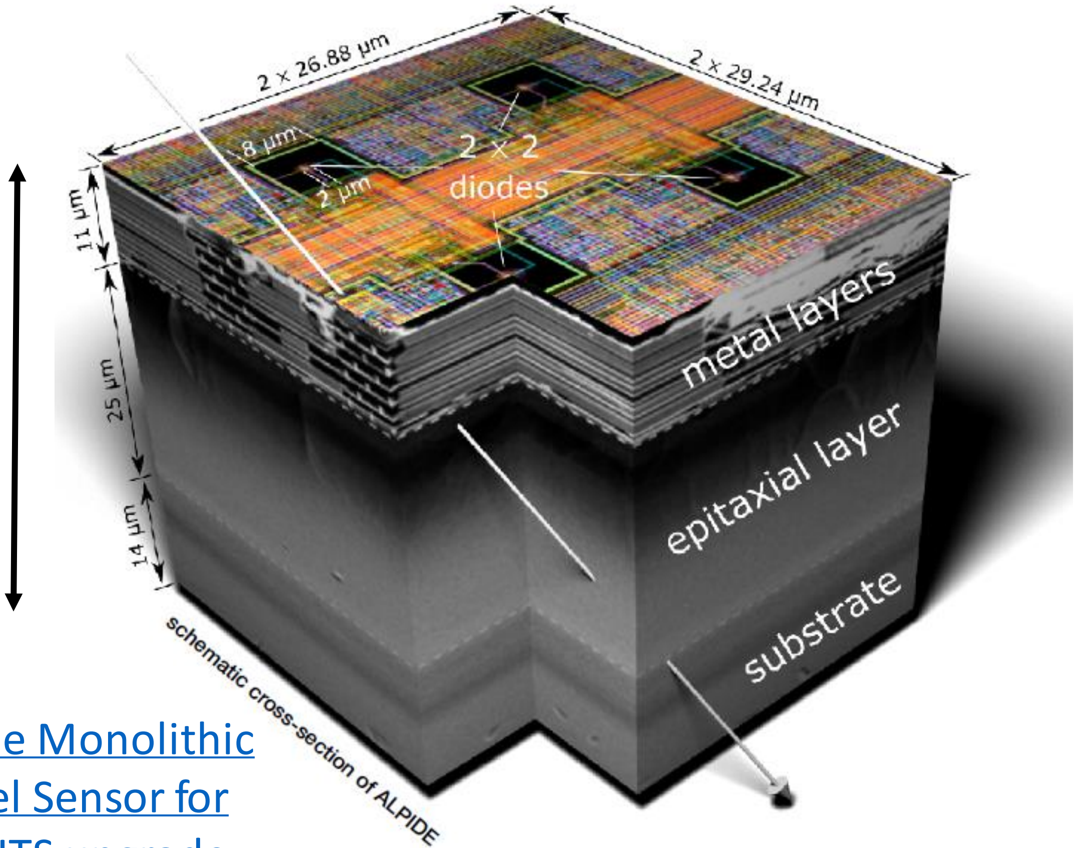
- Target technology for ITS3 is 65 nm CMOS process (12 inch wafers)
  - Several test structures available for testing
    - APTS, **DPTS**, CE65, …
  - Intensive laboratory and testbeam characterization effort
  - Flexible and advanced tools required

The ALPIDE telescope

- Based on the ALPIDE chip
  - 1024 × 512 pixels, 29 µm × 27 µm pixel size
  - Reduced material budget (50 µm of silicon per plane)
  - 5 µm spatial resolution
  - Detection efficiency above 99.99%

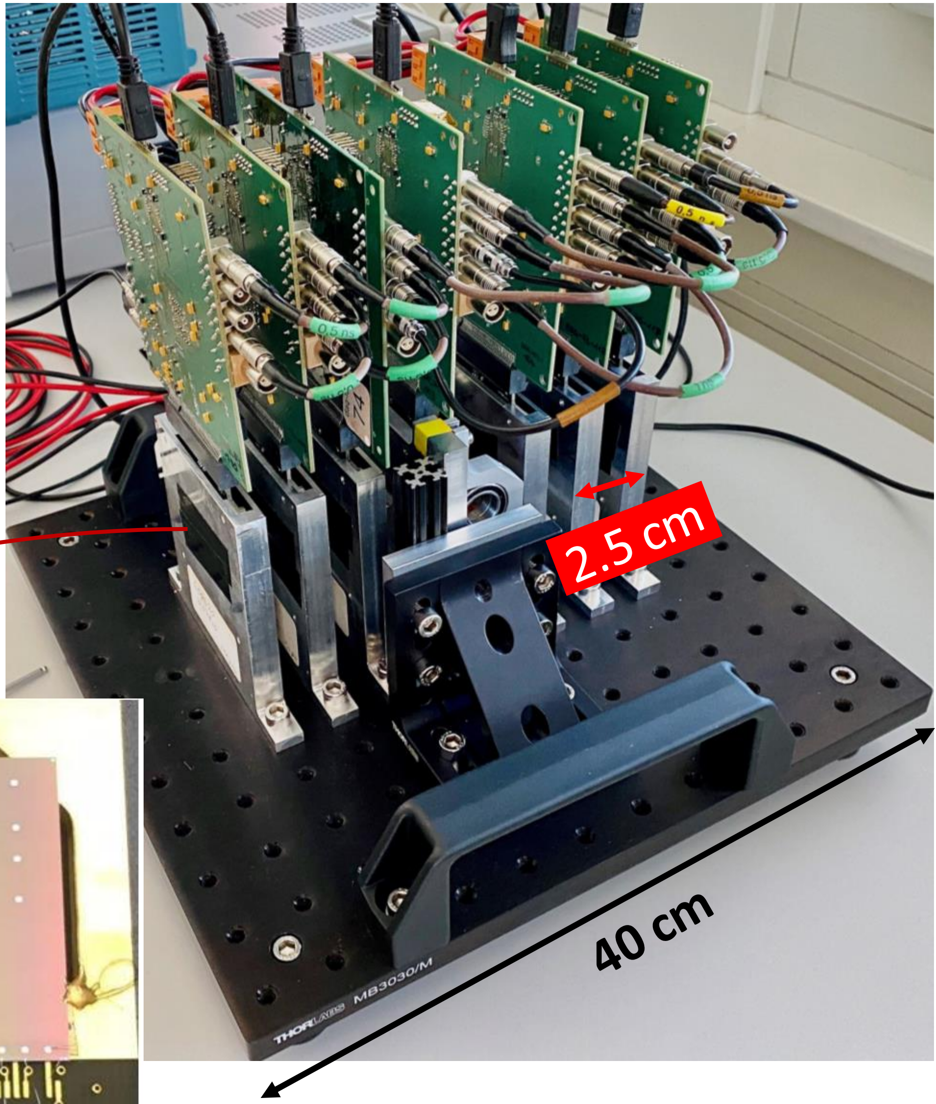
50 µm

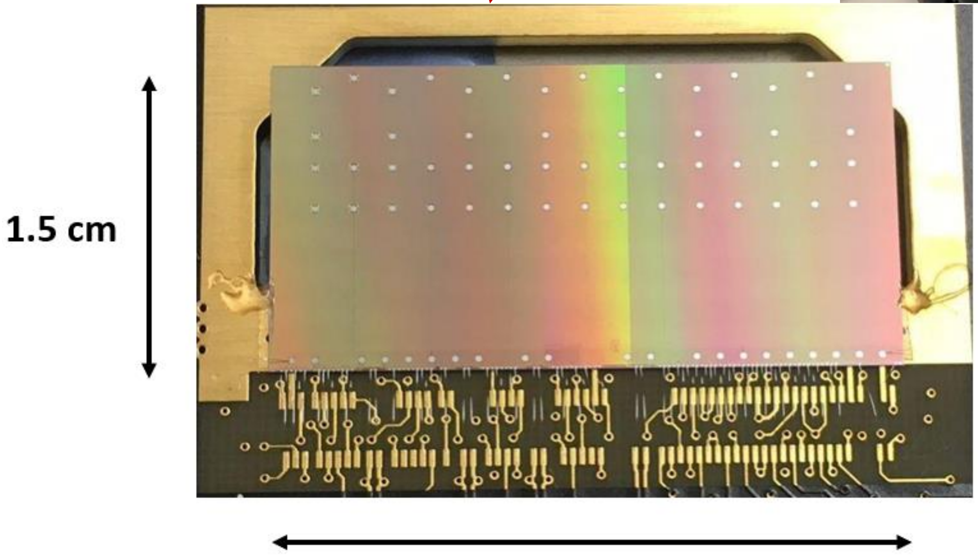


[ALPIDE, the Monolithic Active Pixel Sensor for the ALICE ITS upgrade]

The ALPIDE telescope

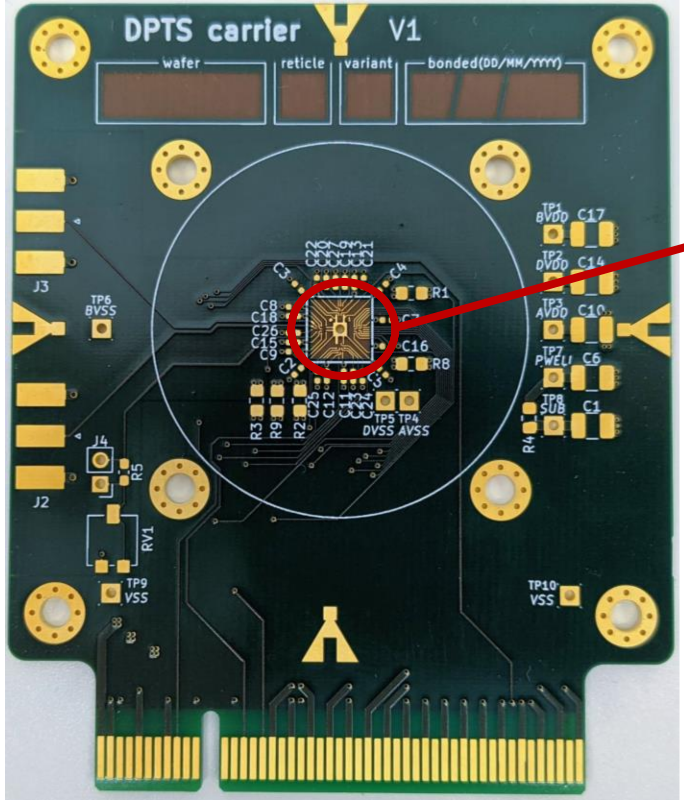
- Based on the ALPIDE chip
  - 1024 × 512 pixels, 29 µm × 27 µm pixel size
  - Reduced material budget (50 µm of silicon per plane)
  - 5 µm spatial resolution
  - Detection efficiency above 99.99%
- 6 ALPIDE tracking planes as standard configuration
  - 3 planes before the Device(s) Under Test (DUT)
  - 3 planes after the DUT(s)
  - 2.5 cm distance between planes
  - 3 µm tracking resolution on the DUT plane
- Designed for high flexibility and portability

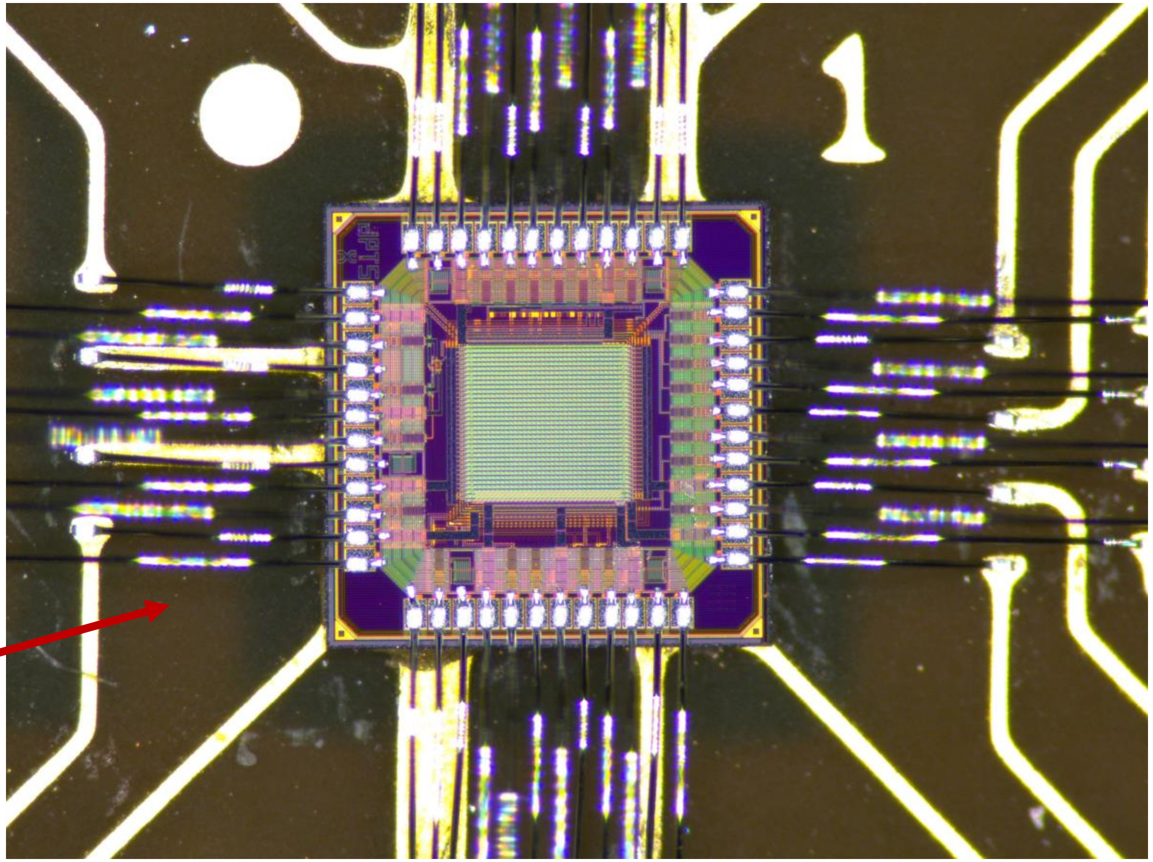




Digital Pixel Test Structure (DPTS)

- Test structure of the first chips submission in TPSCo (Tower Partners Semiconductor Co) 65 nm CMOS imaging process
- 32 × 32 pixels, 15 µm pixel pitch
- 50 µm silicon thickness
- Asynchronous digital readout with Time over Threshold (ToT) information
- Time-based encoding of the hit position



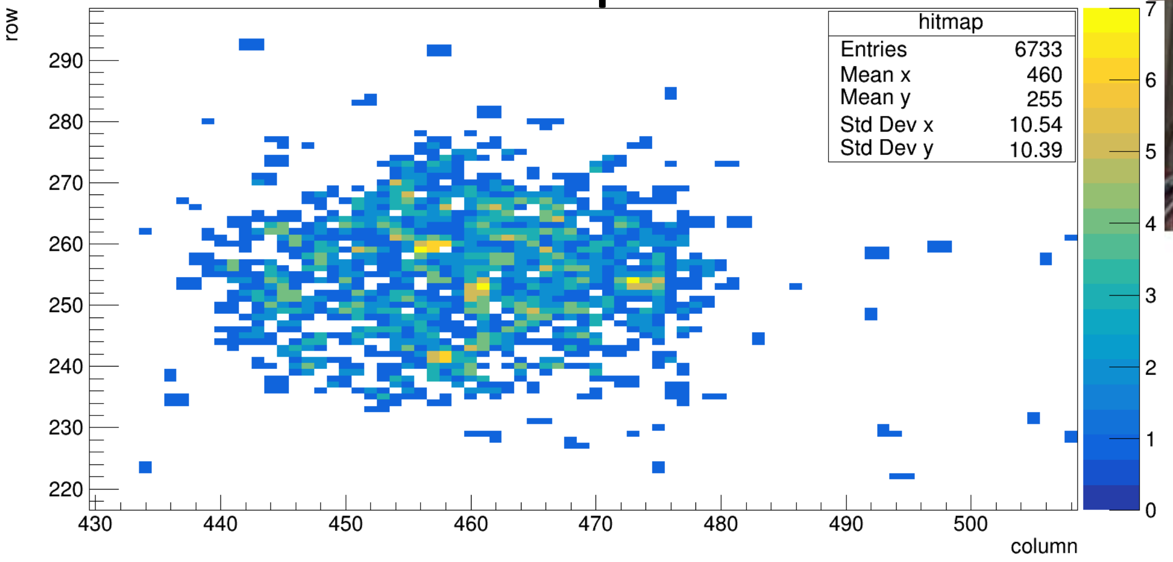


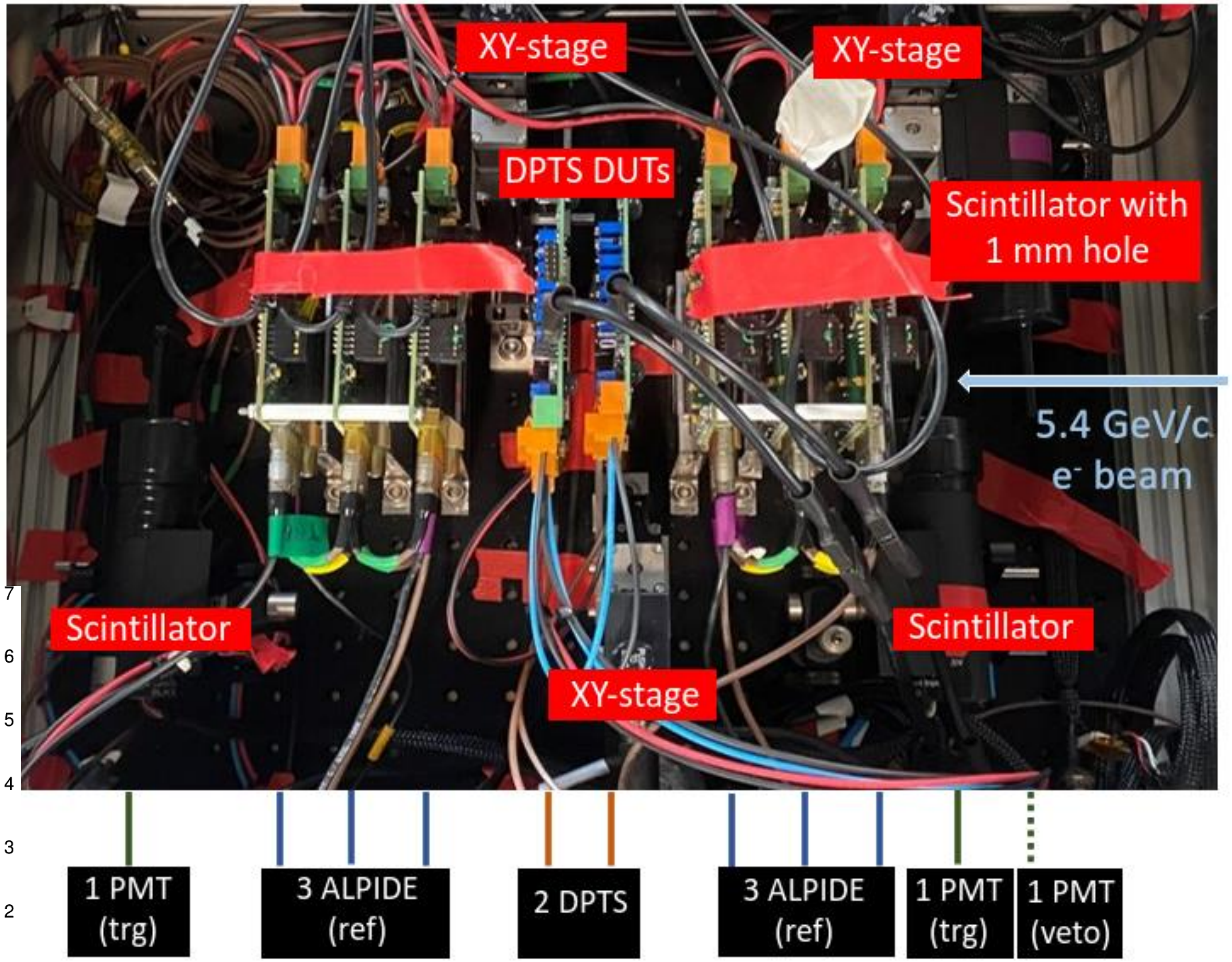
1.5 mm
(active 0.48 mm)

Testbeam setup – DESY September 2021

- 2 DPTS as DUTs
  - ➢ New devices (not irradiated) at standard operation conditions (-1.2 V back bias)
- Scintillator with 1 mm hole (veto) to trigger on a narrower beam spot
- Moving stages to align hole scintillator and DUTs

Scintillator hole as seen by the closest upstream ALPIDE plane

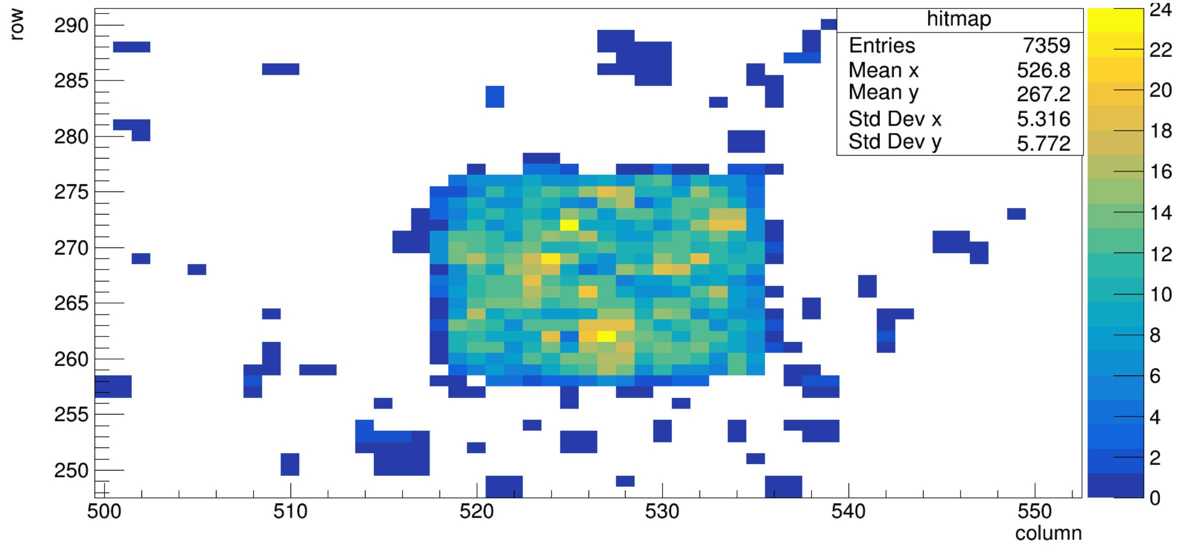


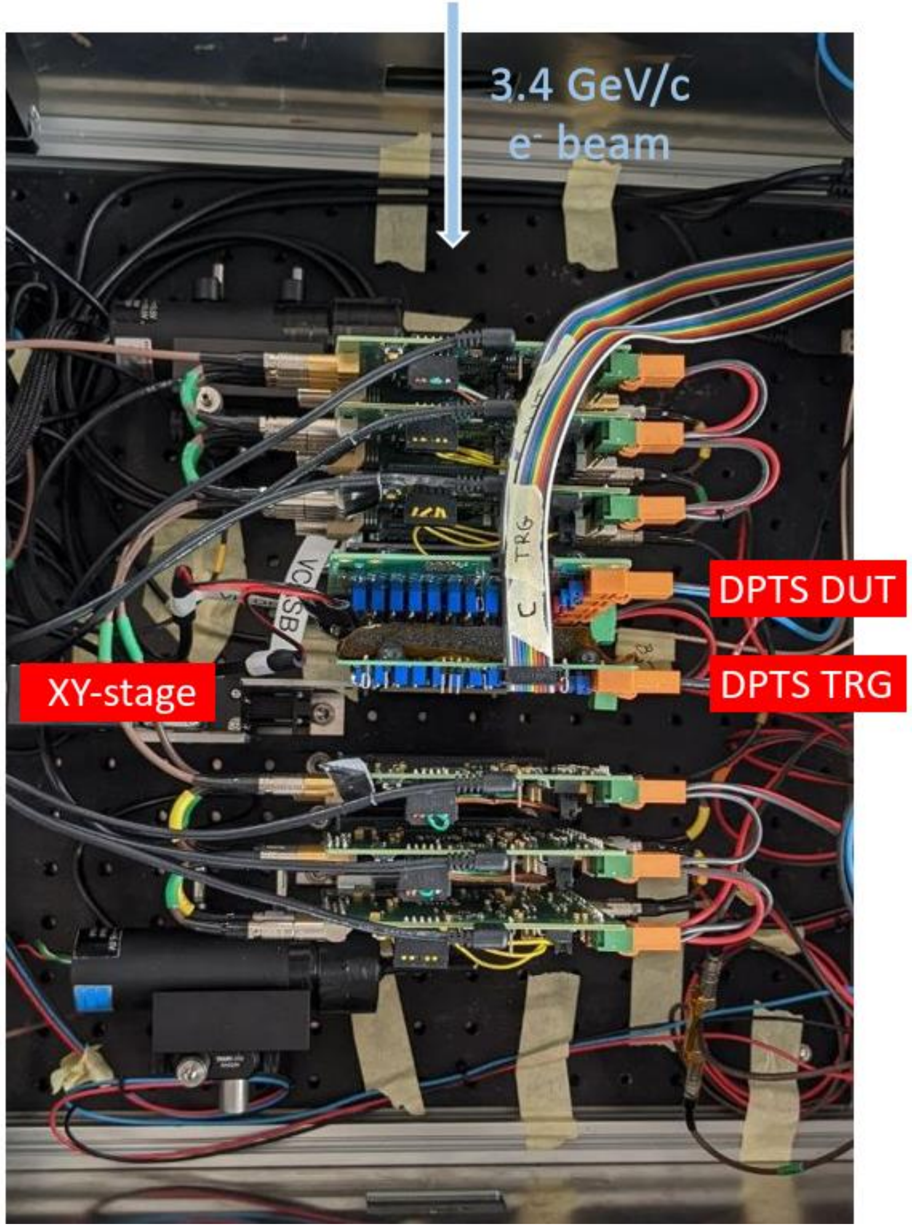


Testbeam setup – DESY March 2022

- DPTS DUT
  - ➢ Different levels of irradiations at varying operation parameters
- One DPTS as trigger
- Moving stage to align DPTS trigger

DPTS trigger as seen by the closest upstream ALPIDE plane





Data acquisition and analysis

- DPTSs digital outputs are read out with a PC oscilloscope (picoscope)
- ALPIDE planes and picoscope are controlled and data acquired by using EUDAQ2

https://github.com/eudaq/eudaq

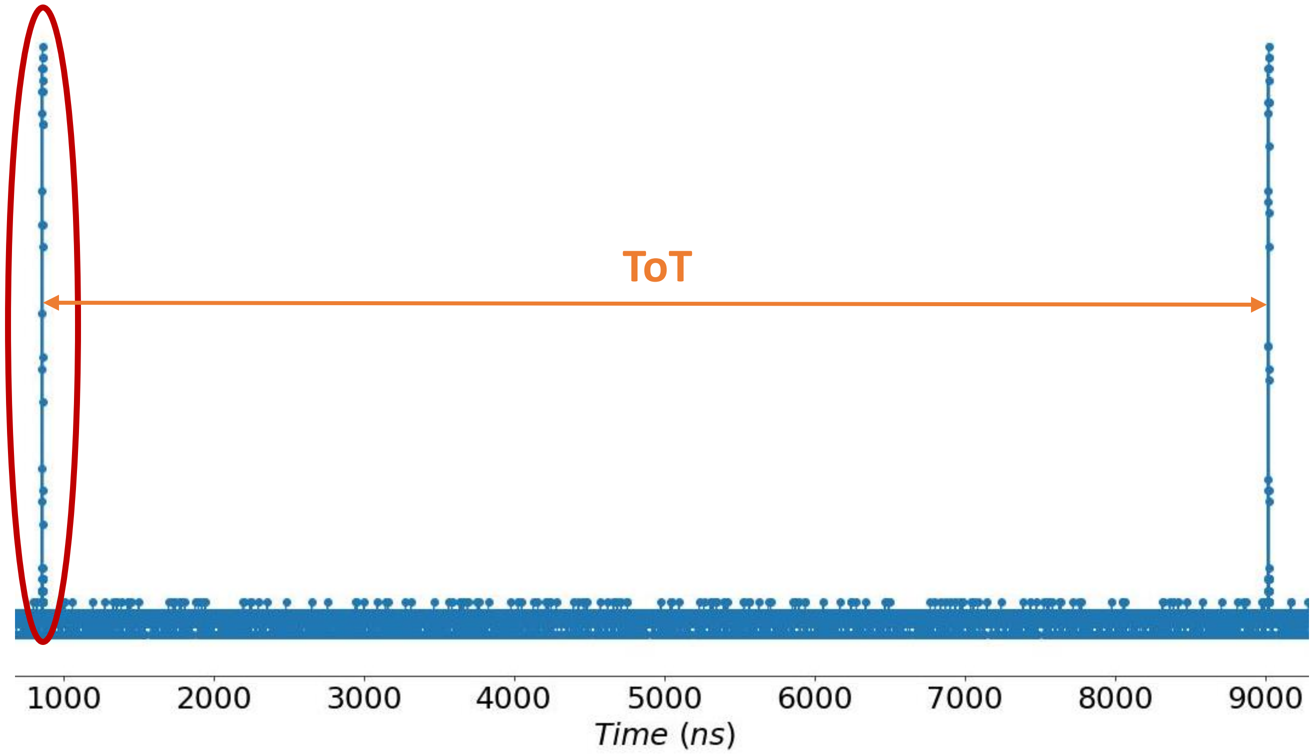
- Analysis is conducted with Corryvreckan

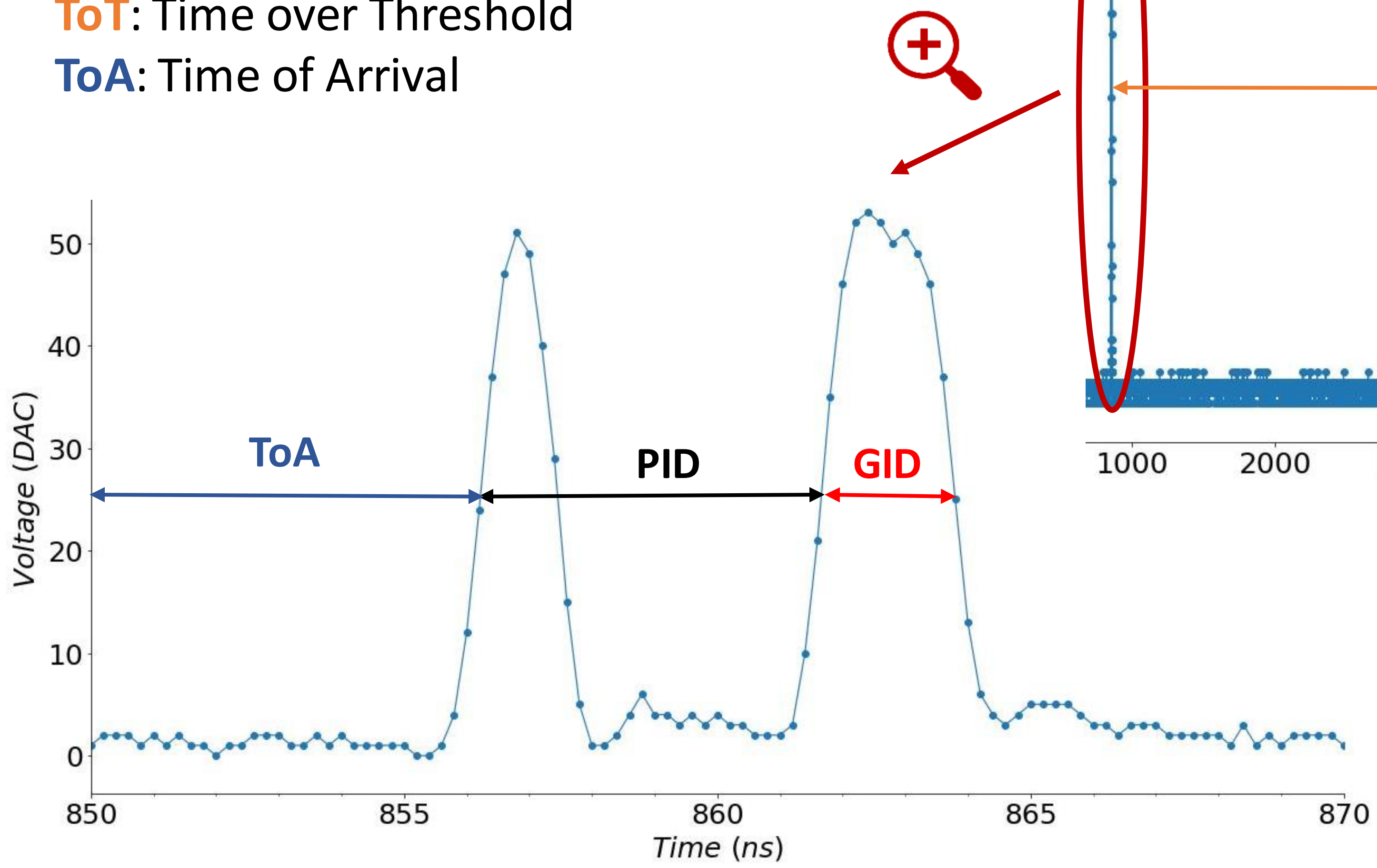
https://gitlab.cern.ch/corryvreckan/corryvreckan

DPTS Readout features

- The hits from all the pixels are digitized and conveyed by the readout into a single digital output

GID: Group ID – pixel column
PID: Pixel ID – pixel row
ToT: Time over Threshold
ToA: Time of Arrival

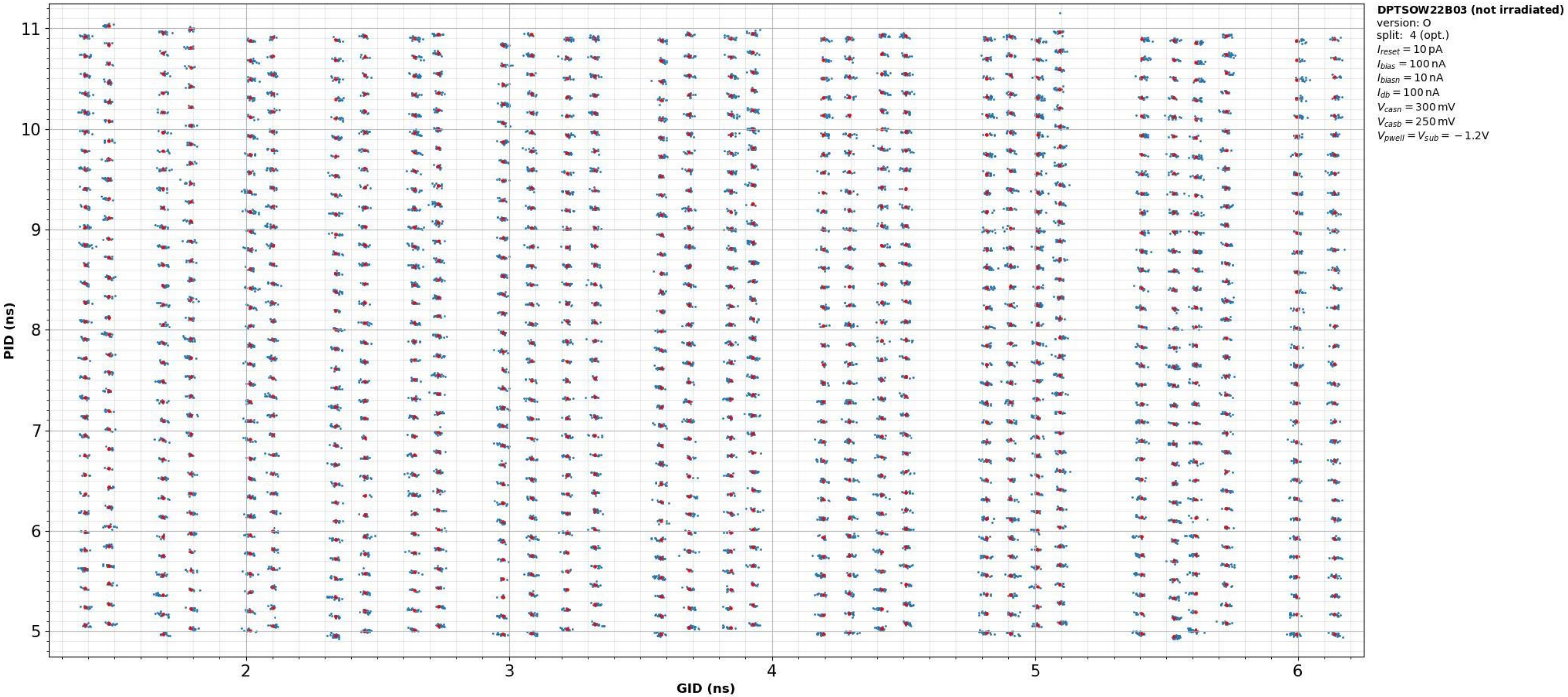




Pixel hit position encoded by PID and GID values

Time to position decoding map

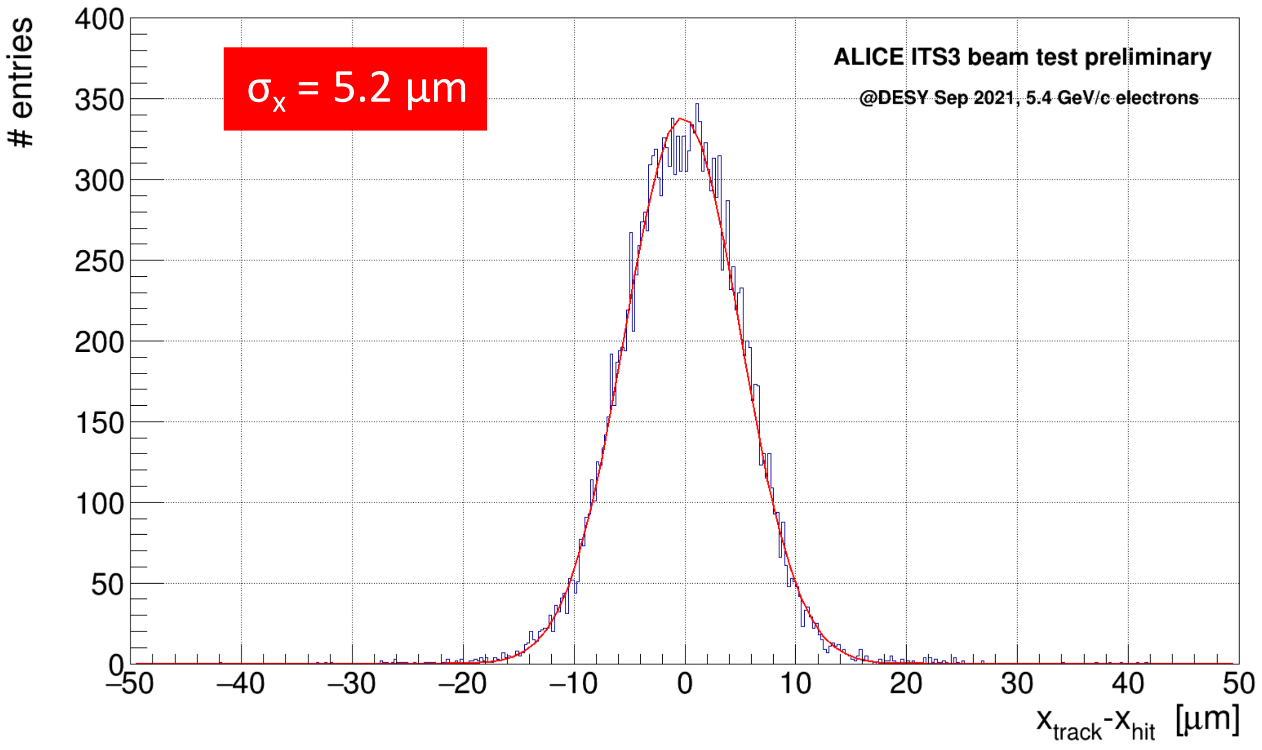
- Additional calibration file passed to Corryvreckan to address DPTS pulses decoding
- For each pulse, GID and PID are measured and hit is assigned to a pixel according to nearest neighbor logic

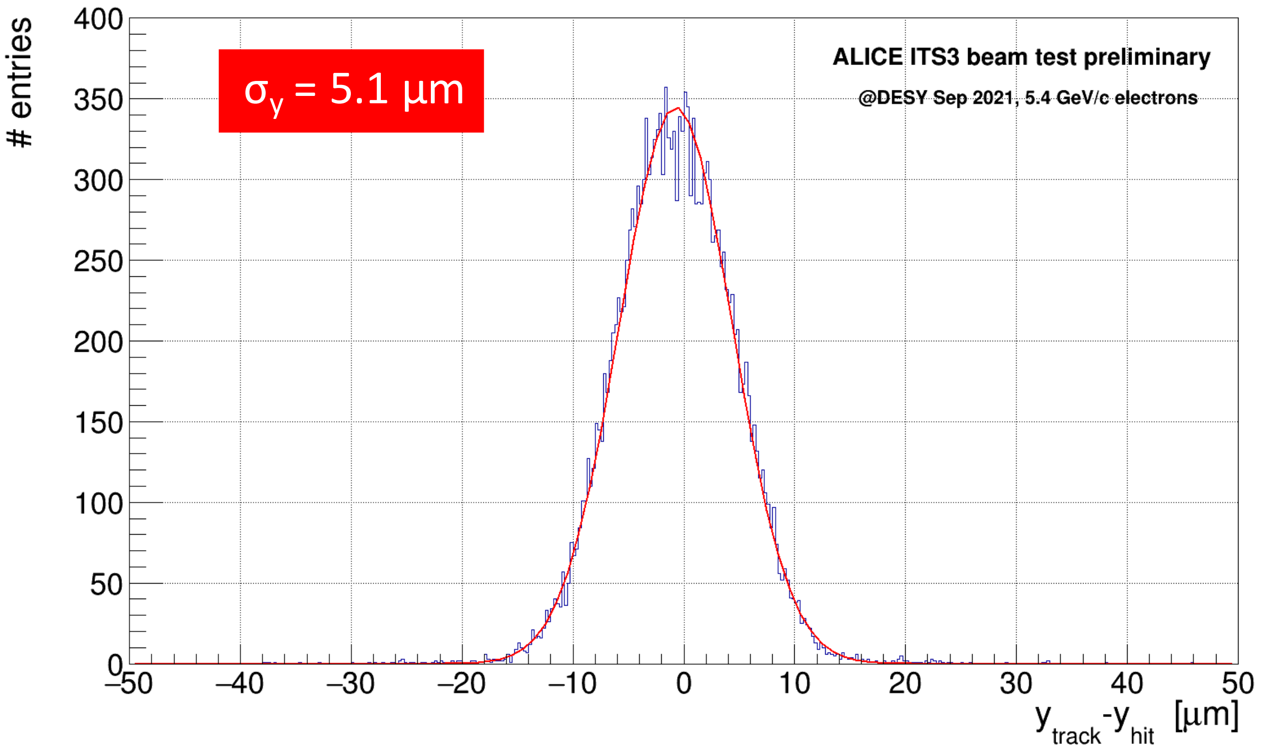


Spatial residuals

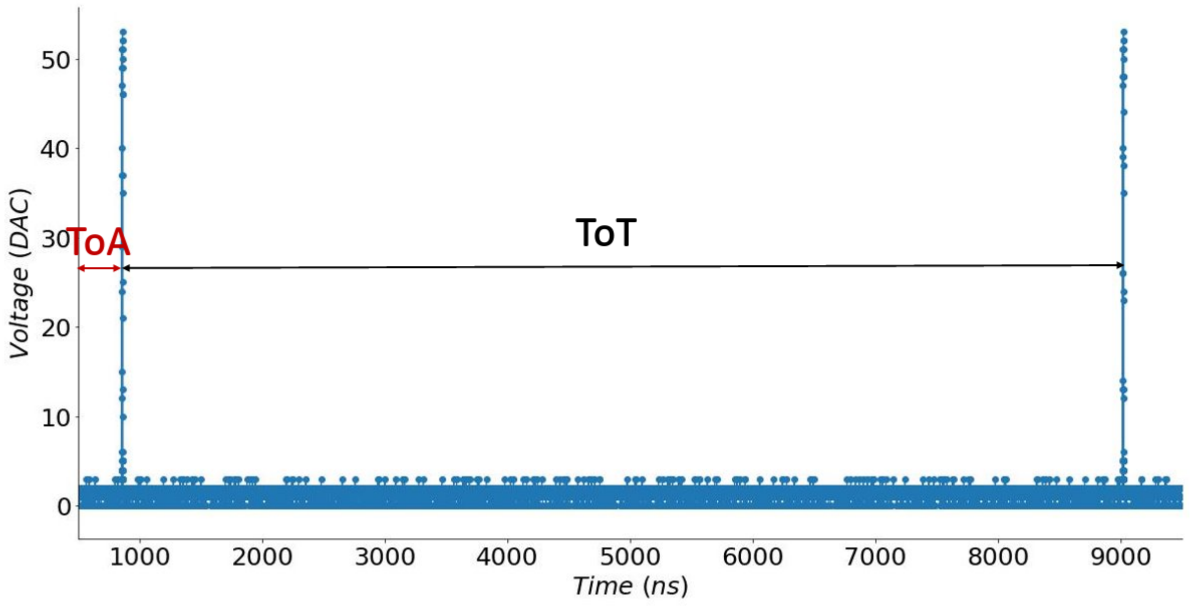
- DESY September 2021 data: DPTSXW22B1, standard operation conditions
- Track selection: $\chi^2/n_{dof} < 5$
- Spatial resolution *O(4.3 μm)*

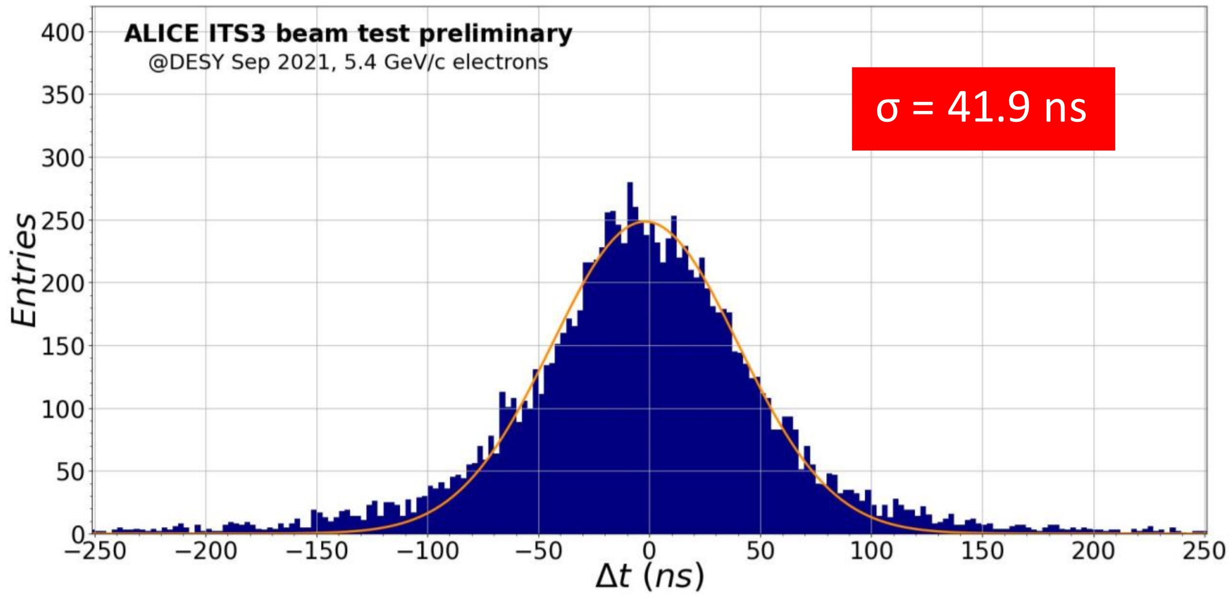
DPTSXW22B1 (not irradiated)
version: X
split: 4 (opt.)
$I_{reset} = 10$ pA
$I_{bias} = 100$ nA
$I_{biasn} = 10$ nA
$I_{db} = 100$ nA
$V_{casn} = 300$ mV
$V_{casb} = 280$ mV
$V_{pwell} = V_{sub} = -1.2$V
$thr = 110e^-$





Timing resolution - analysis



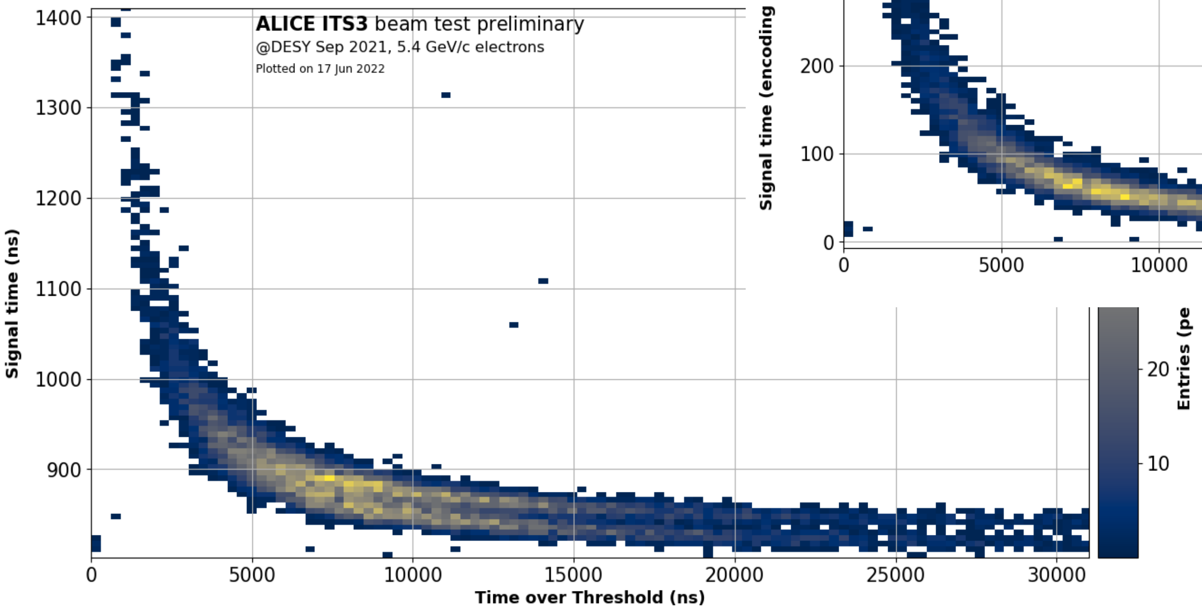


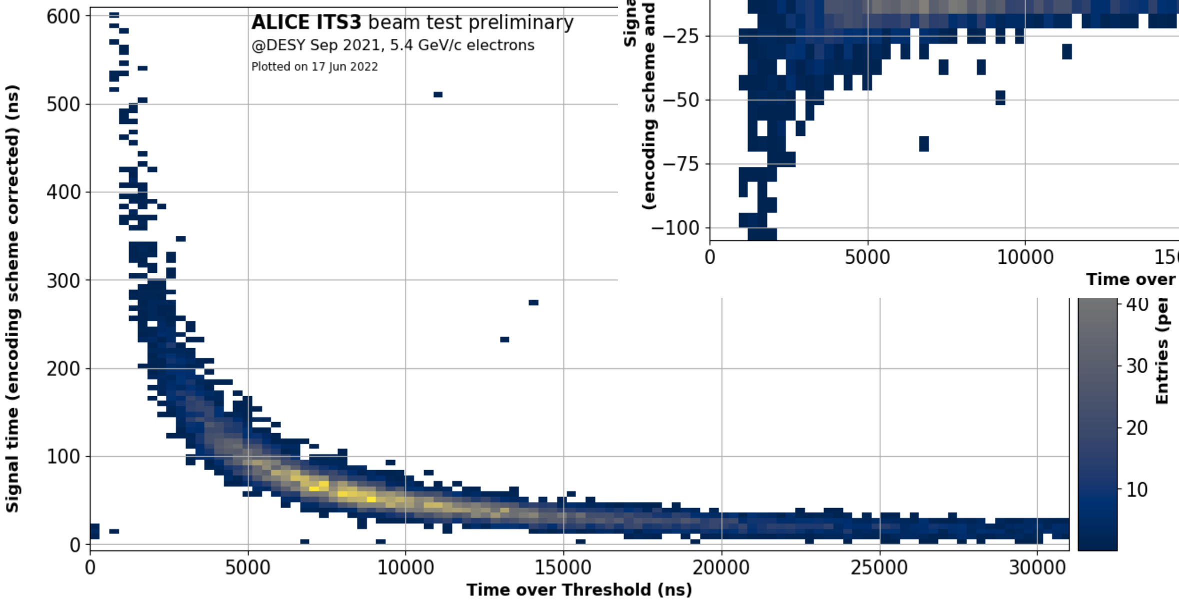
- DESY September 2021 data
- No timing layer in the ALPIDE telescope
- Only tracks associated to both DUT are considered
- Track selection: $\chi^2/n_{dof} < 5$
- The timestamp is given by the Time of Arrival (ToA) of the pixel signal with respect to the trigger
- 2 timestamps per track
- **Time residuals distribution = ToA DPTS1 – ToA DPTS2**
- Corrections to be performed
  - Pixel encoding scheme
  - Timewalk correction

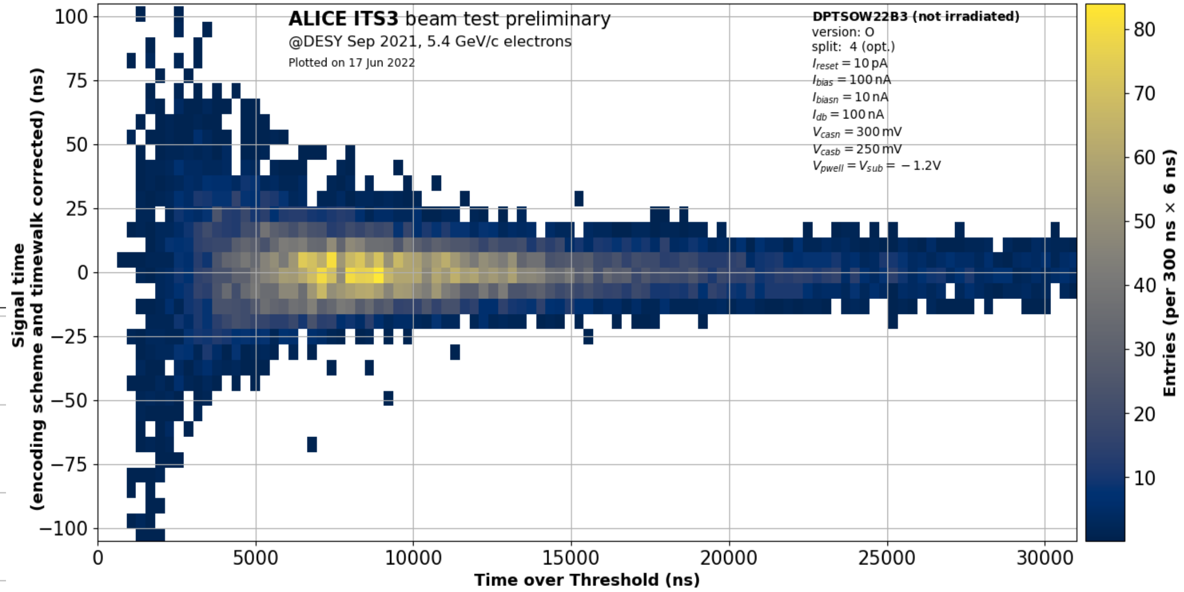
Timing resolution - corrections

- Corrections applied separately to both devices

Encoding scheme correction







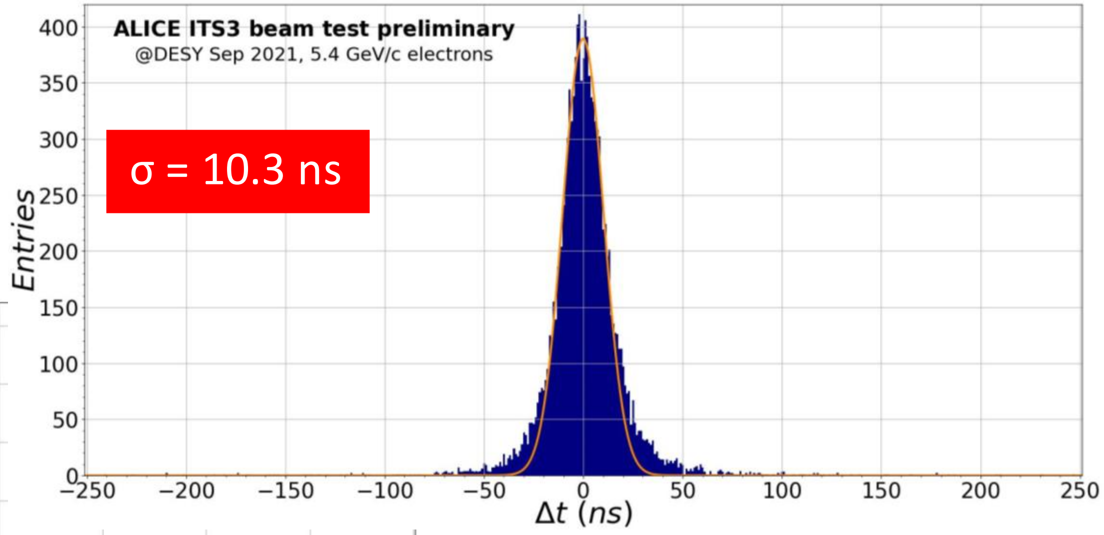
Timewalk correction

$$ToA = \frac{a}{ToT - t_0} + b$$

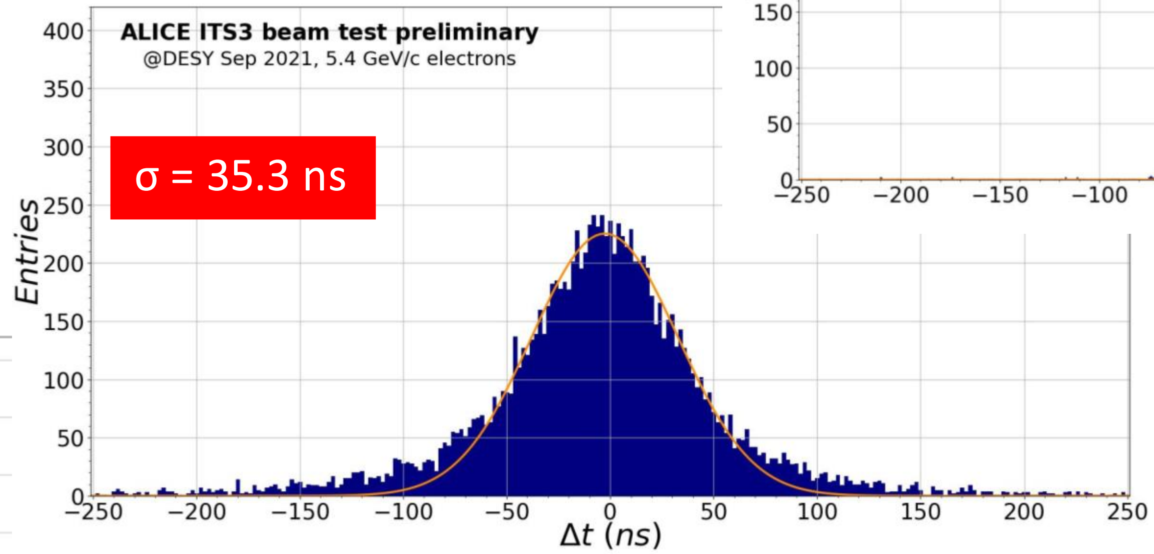
Timing resolution - results

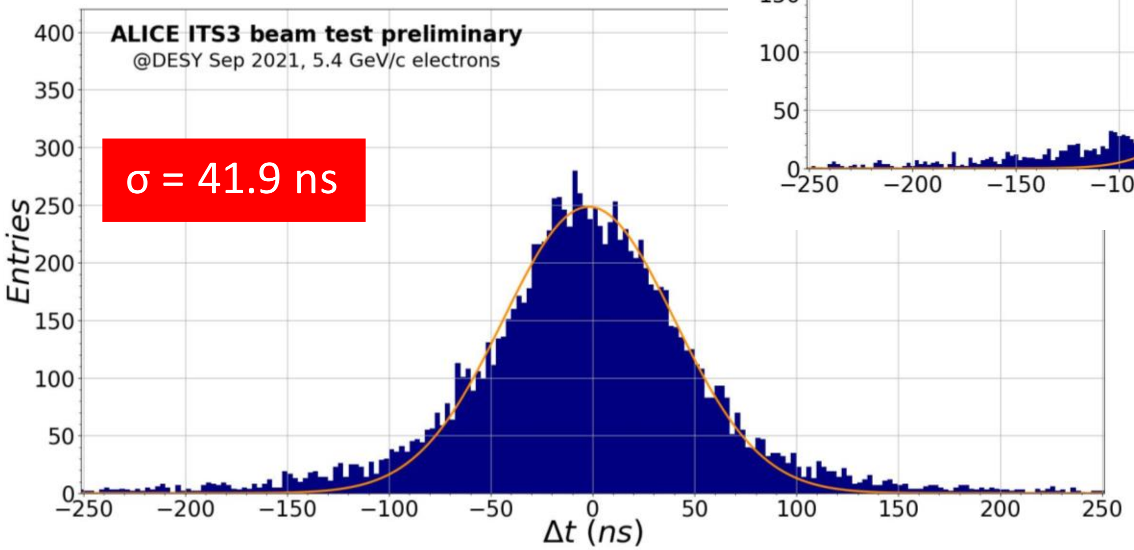
- Estimated sensor time resolution

$$\frac{10.3\ ns}{\sqrt{2}} = 7.3\ ns$$



Encoding scheme correction





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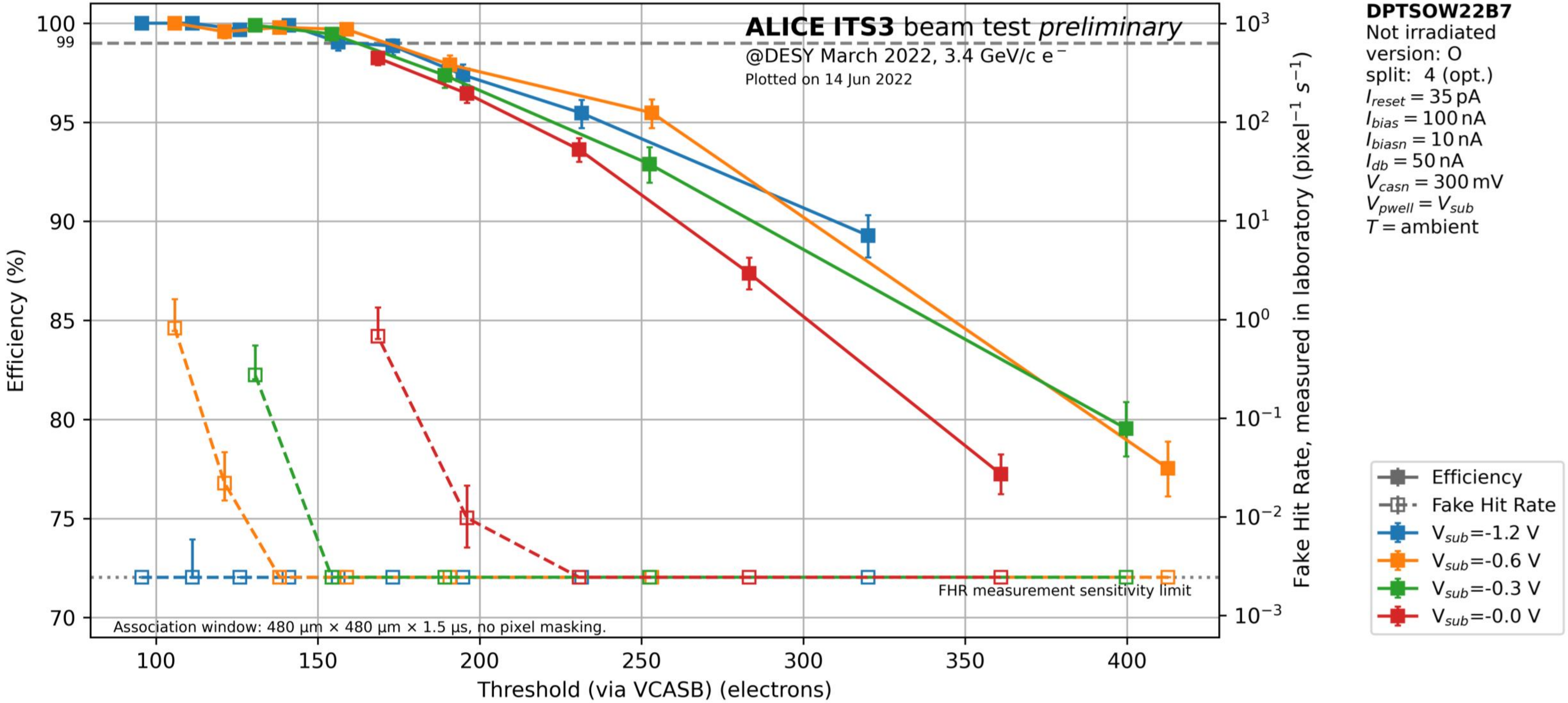
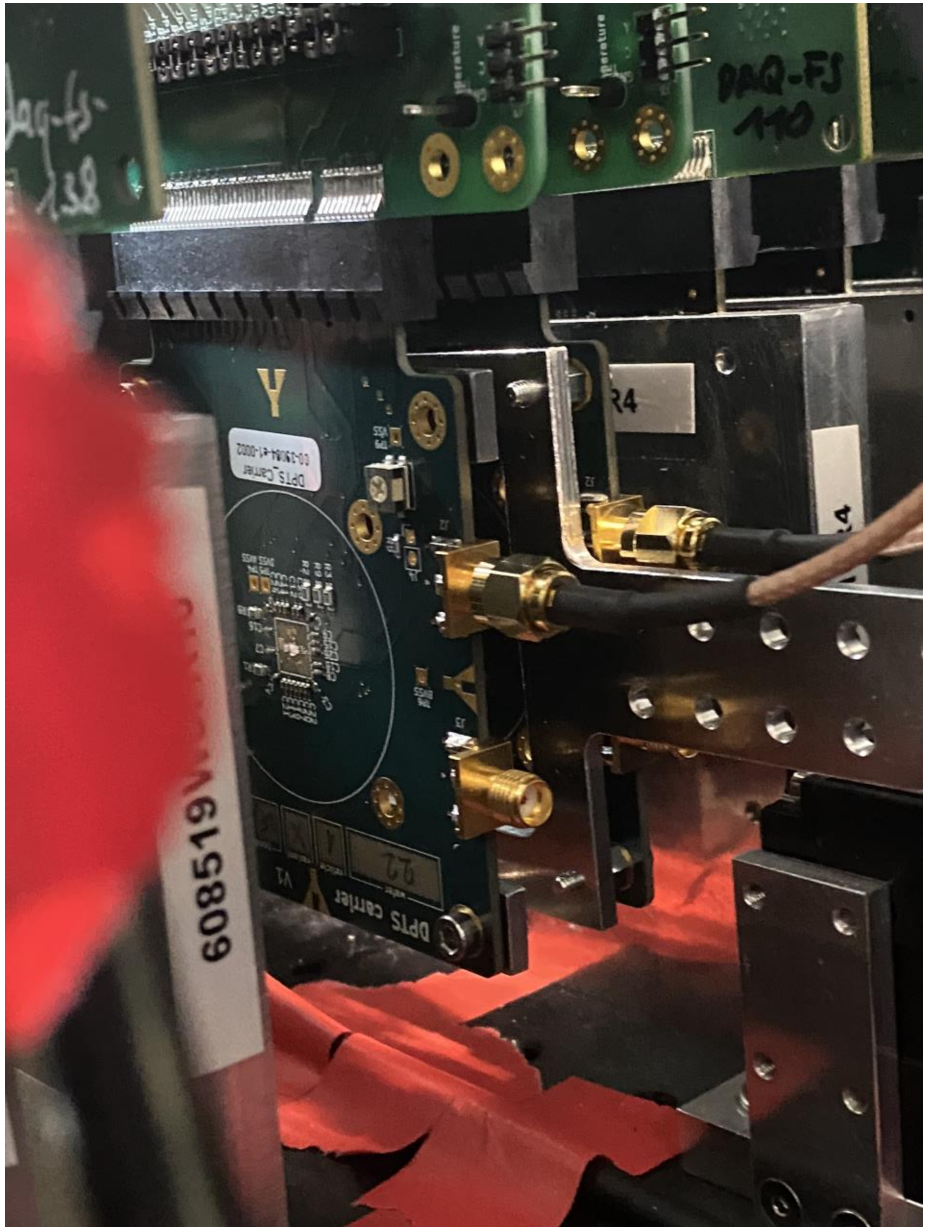
Detection efficiency

- DESY March 2022 data: DPTSOW22B7, operation condition scan at room temperature
- Efficiency above 99.7% below 150 e⁻ threshold at -1.2 V back bias



Summary

- DPTS is a MAPS fabricated in 65 nm CMOS imaging sensor technology
- Chip thoroughly tested during several testbeam campaigns
- Non-irradiated device under standard operation conditions:
  - Spatial residuals *O(5 μm)*
  - Time residuals *O(10 ns)*
  - Detection efficiency above 99.7%
- Performance figures of first prototype are very promising for the ITS3 requirements



Outlook

- Irradiated devices analysis ongoing (NIEL irradiation levels from 10^{13} to 10^{15} 1 MeV n_{eq} cm^{-2})
- In-pixel efficiency studies
- Another testbeam (at CERN PS) data taking has just concluded:
  - Studied chip behavior under controlled temperature
  - Studied new operation conditions (larger back-bias range, up to –3 V)
  - Analysis ongoing

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Big thank you to the DESY testbeam support team!

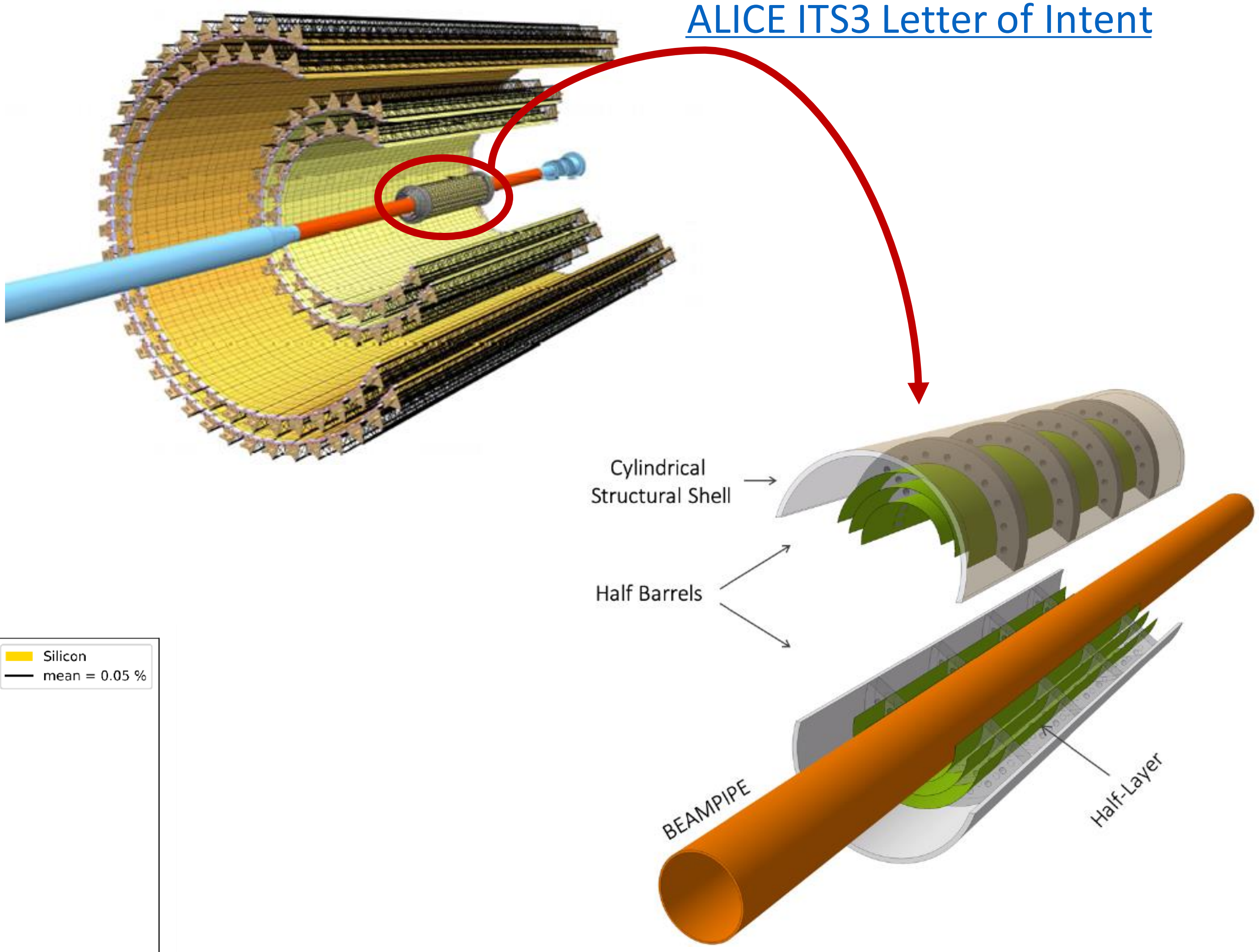
The measurements leading to the shown results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a Member of the Helmholtz Association (HGF)

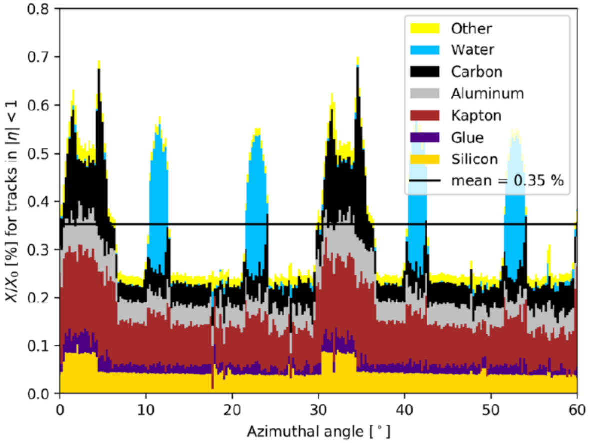
Additional slides

ALICE Inner Tracking System 3 (ITS3)

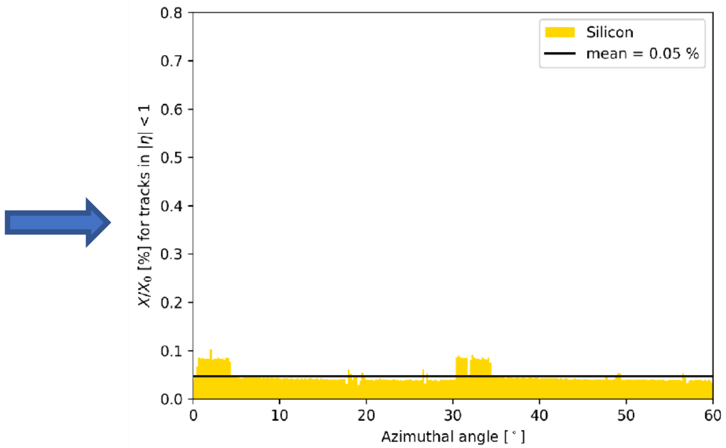
- Improve vertexing at high rate and low transverse momentum
- Replace the 3 layers of the ITS Inner Barrel
  - Fully cylindrical layers with radii of 18/24/30 mm around the beam pipe
- Design based on wafer-scale bent MAPS thinned down to 20-40 µm
- Target technology: 65 nm CMOS sensors
- “Moderate” radiation hardness requirements
  - NIEL: 10^{14} 1 MeV n_{eq}/cm^2
  - TID: 10 MRad

ALICE ITS3 Letter of Intent



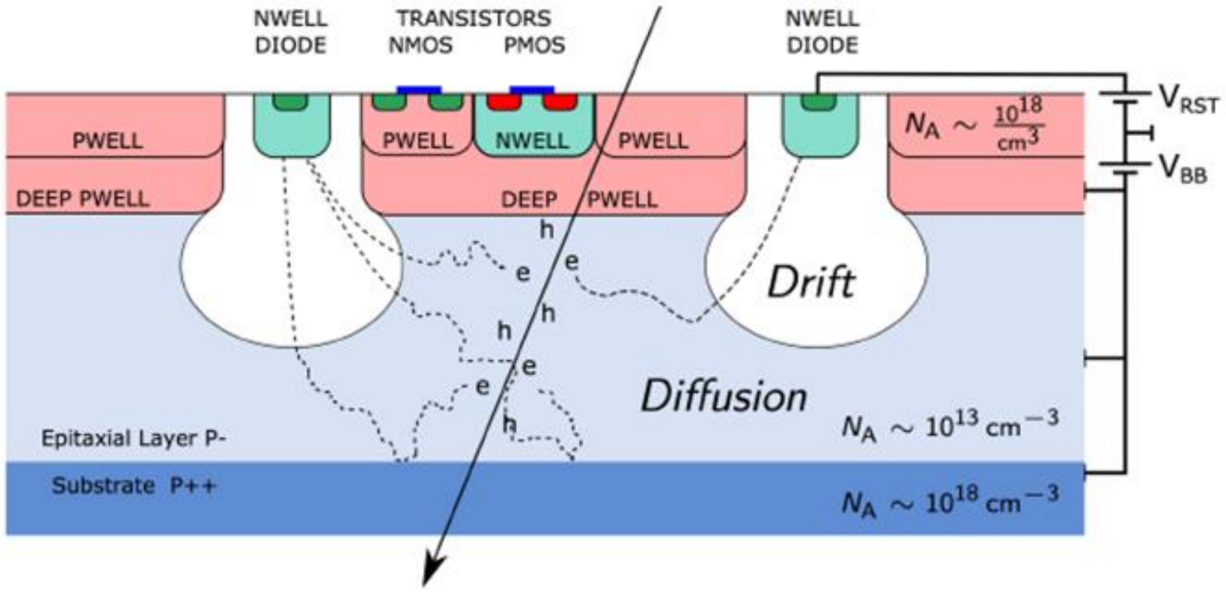


ITS2 Layer 0: X/X_0 = 0.35



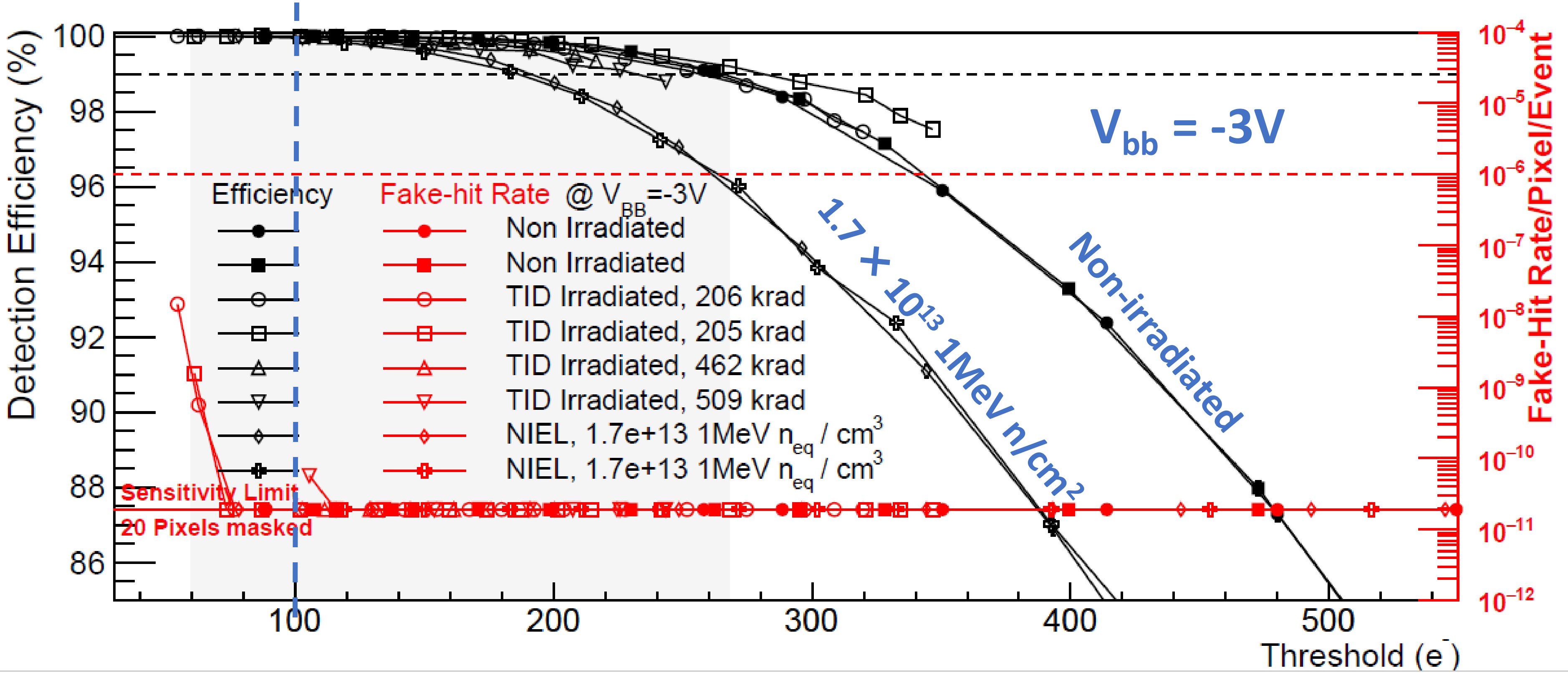
ITS3 Layer 0: X/X_0 = 0.05

ALPIDE, the ALICE PIxel DEtector



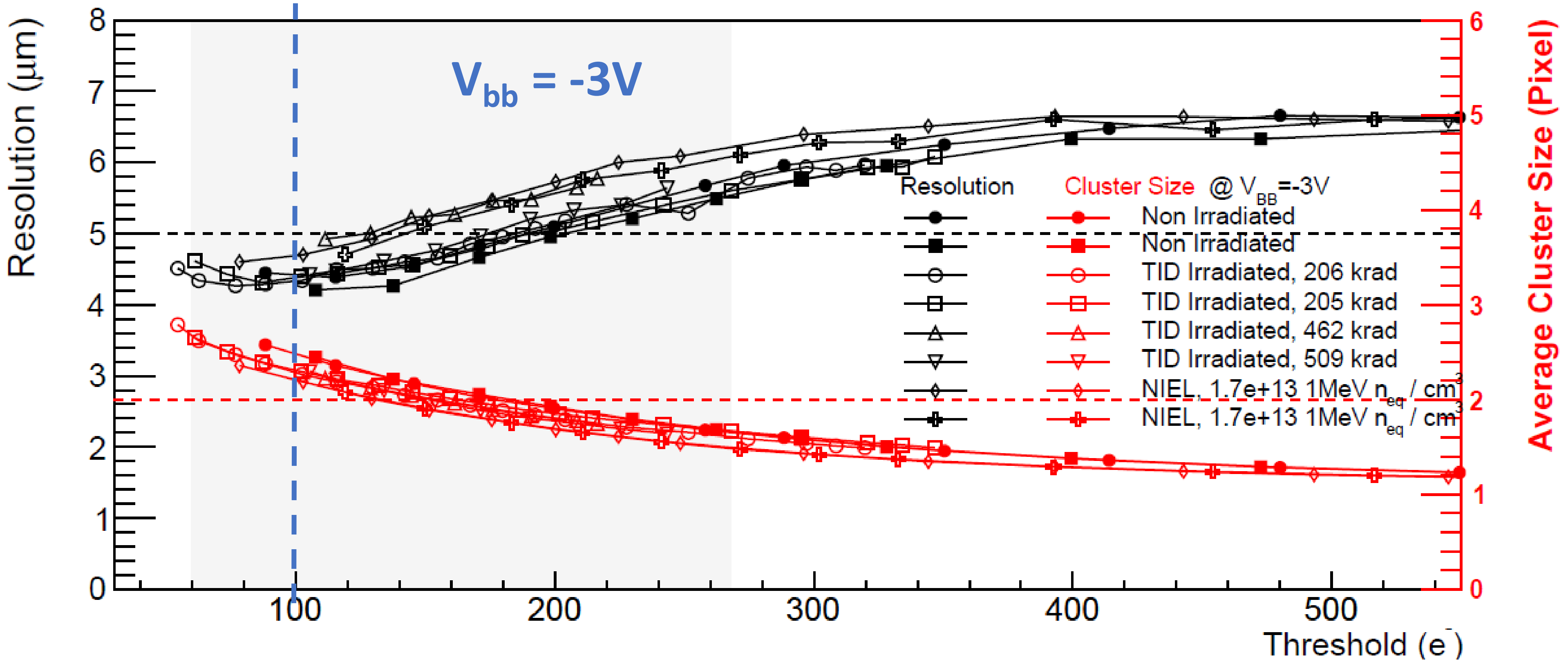
- TowerJazz 180 nm CMOS Standard Imaging Process pixel sensor:
  - High-resistivity (> 1 kΩ·cm) p-type epitaxial layer (25 µm) on p-type substrate
  - 2 µm diameter n-well electrode, ~ 5 pF input capacitance
  - **50 µm overall sensor thickness**
- Monolithic design:
  - In pixel amplification, discrimination, 3 hit storage registers
- Ultra-low power consumption:
  - **40 nW/pixel**
  - **20 mW/cm²**
- High hit rate transmission:
  - **~6 MHz/cm² hit rate chip output data transfer**

ALPIDE performance figures



- Measured with 6 GeV/c pion beam
- At 100 e^- of operation threshold and V_{bb} = -3 V:
  - ➢ Detection efficiency above 99.99%
  - ➢ Fake hit rate < 2 × 10^{-11} pixel hits/event
  - ➢ Irradiated chips performance is comparable with not-irradiated chips

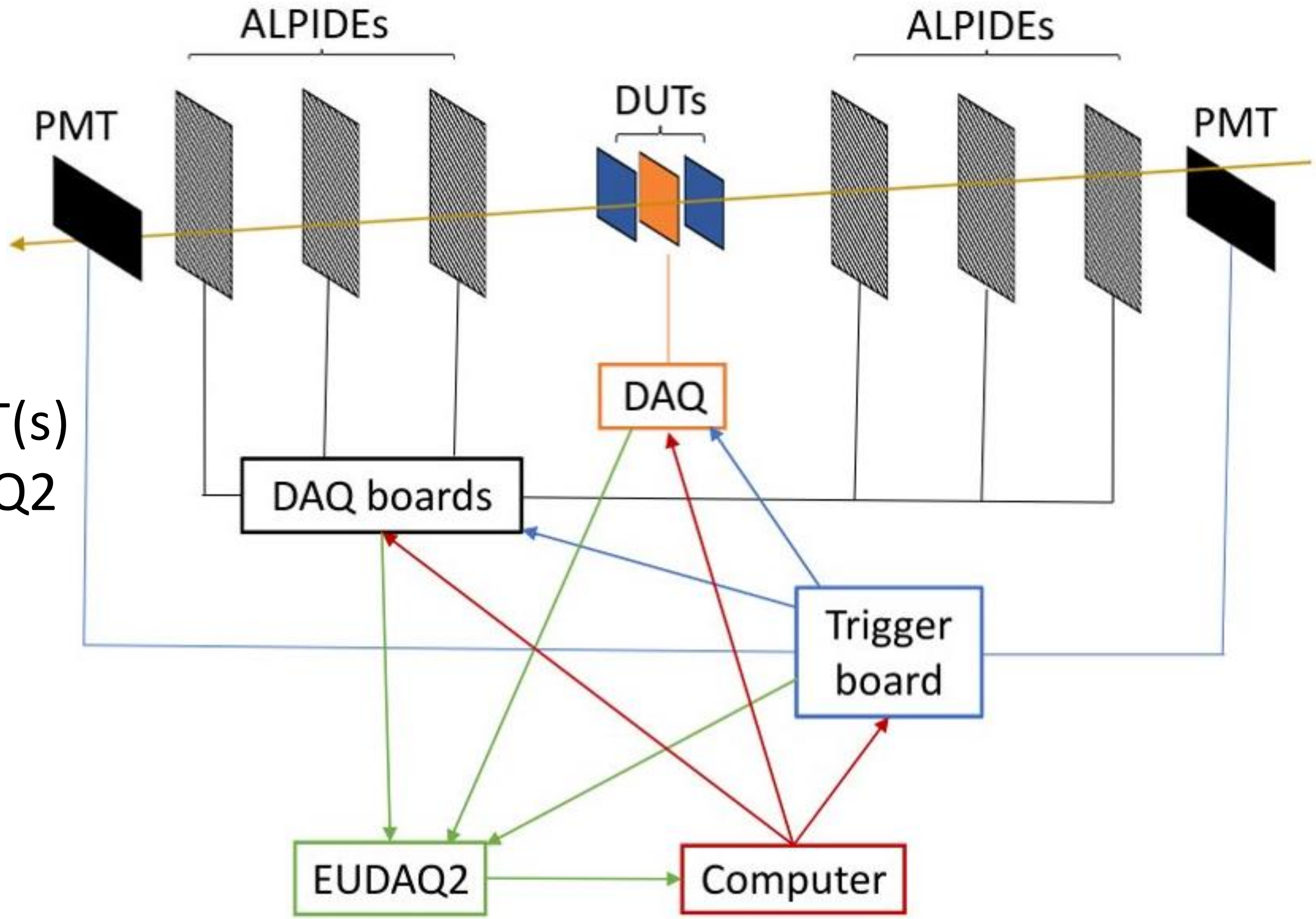
ALPIDE performance figures



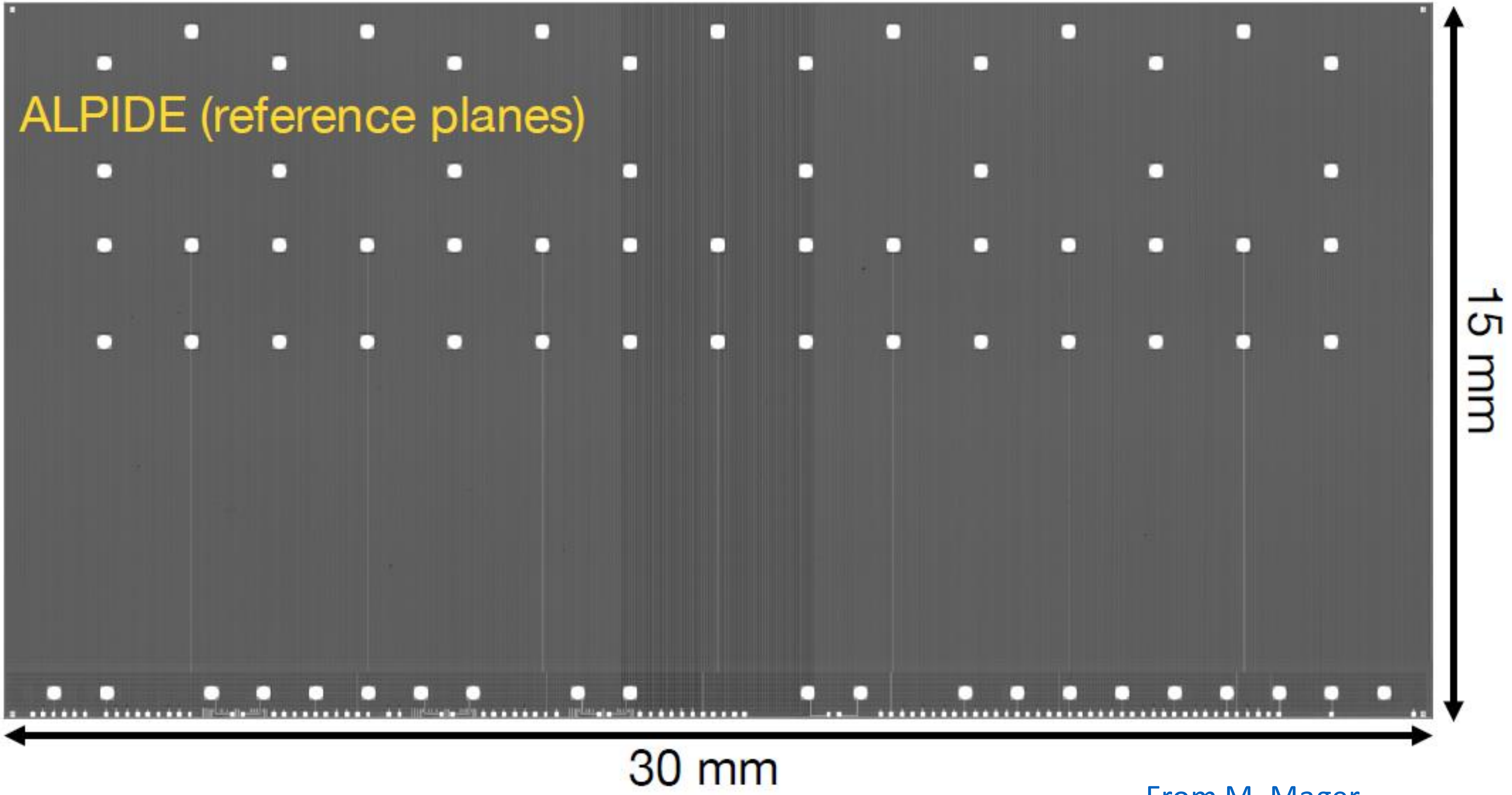
- Measured with 6 GeV/c pion beam
- At 100 e^- of operation threshold and V_{bb} = -3 V:
  - Spatial resolution below 5 µm
- Not irradiated and TID/NIEL chips show similar performance

The ALPIDE telescope

- High flexibility and portability
- 6 ALPIDE tracking planes as standard configuration
- ALPIDE DAQ board based on FPGA
- Custom trigger board
- Movable XY stages for DUT(s) and PMT(s)
- Data acquisition integrated into EUDAQ2

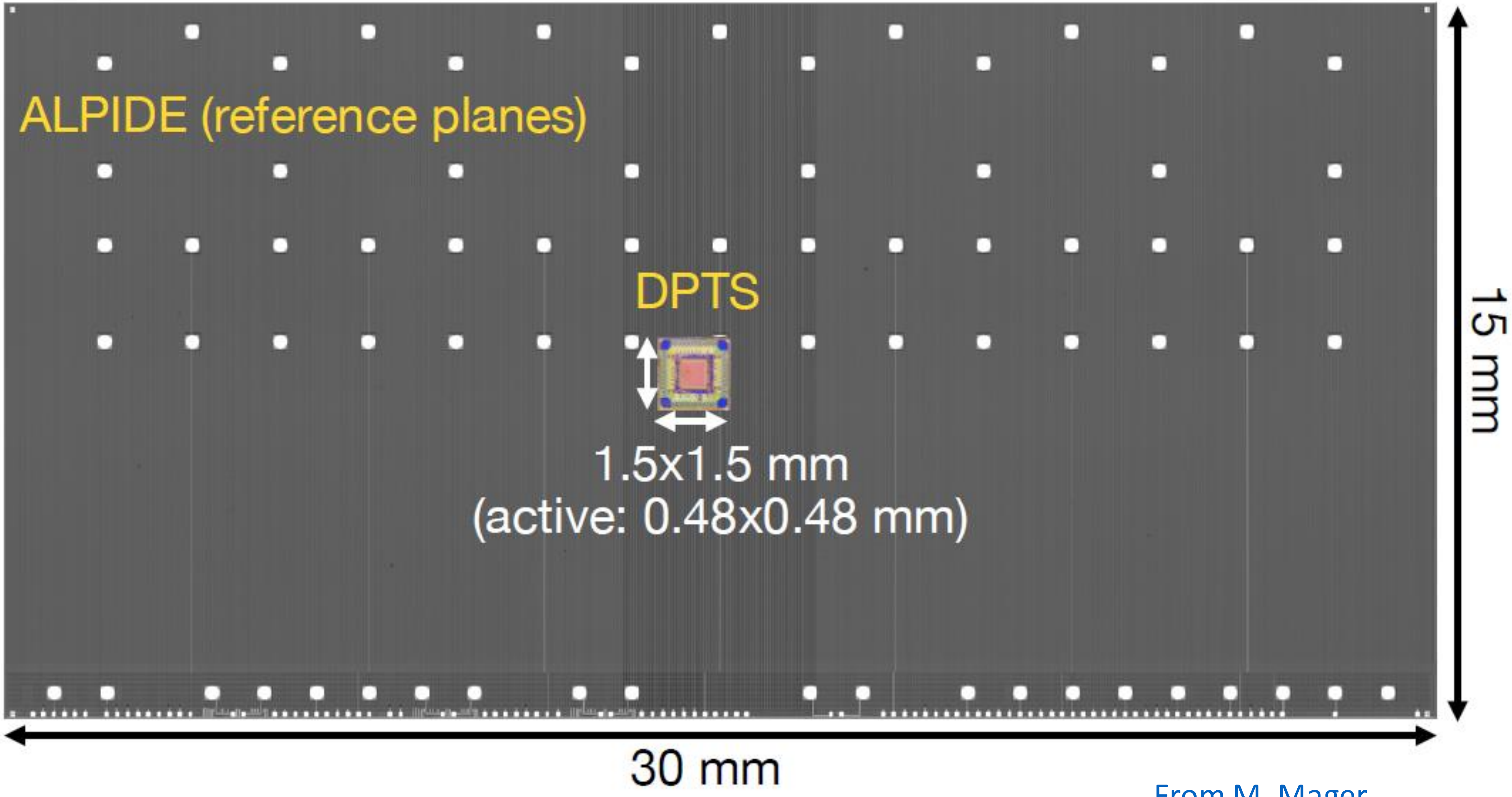


Trigger on veto scintillator



From M. Mager

Trigger on veto scintillator



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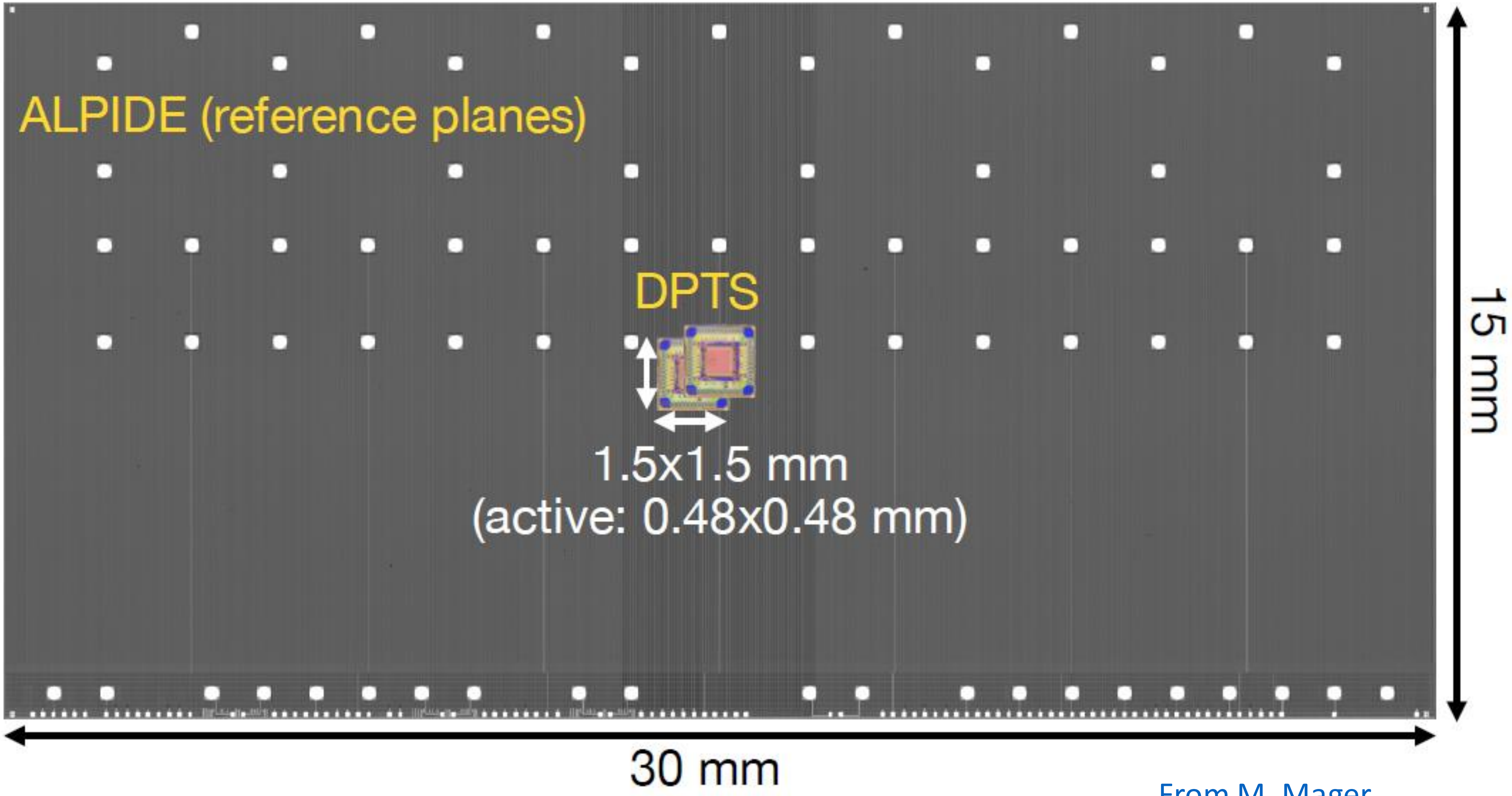

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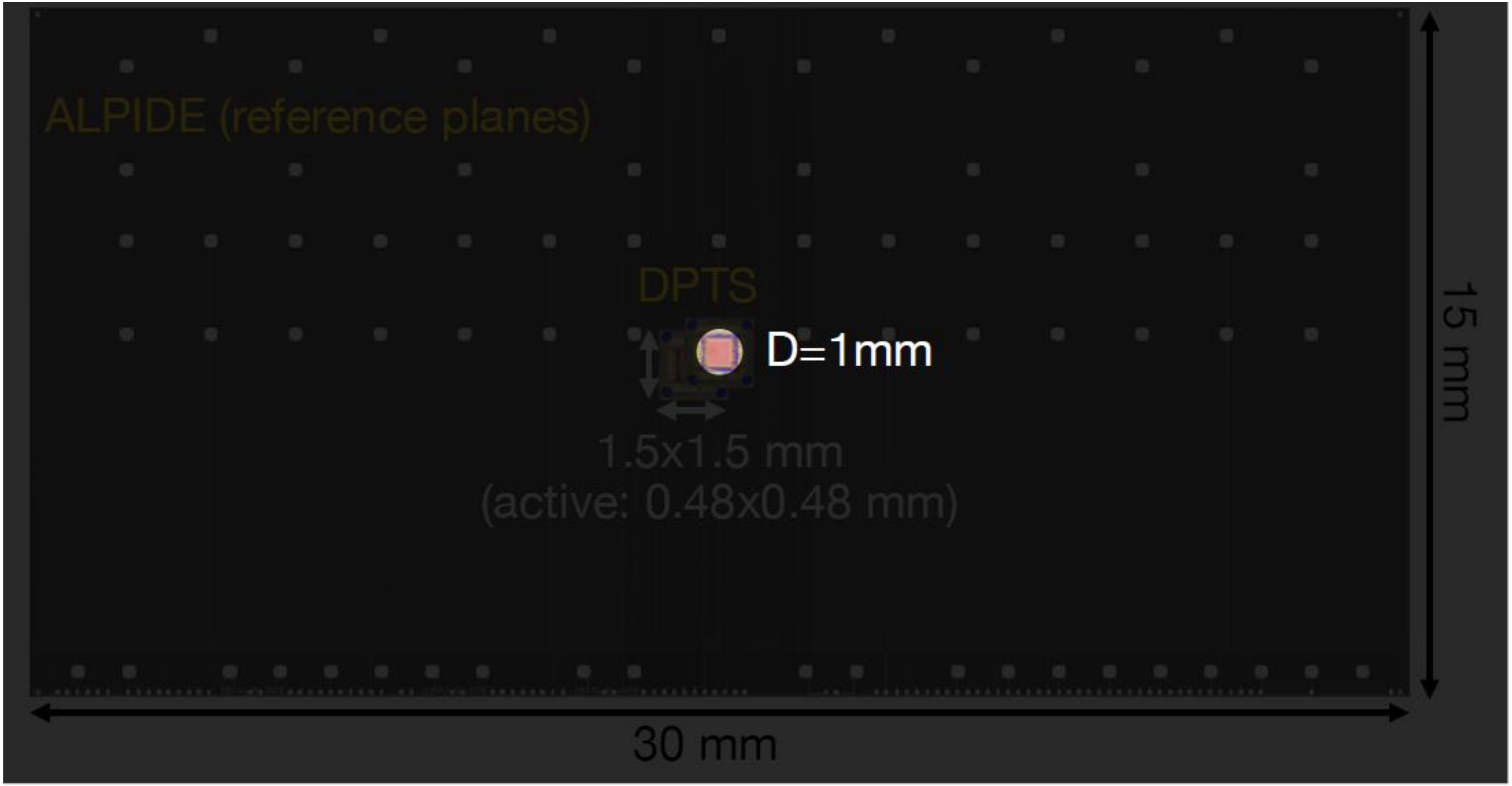

From M. Mager

Encoding scheme time correction