UNIVERSITÉ DE GENÈVE
FACULTÉ DES SCIENCES
Département de physique nucléaire et corpusculaire

FASER

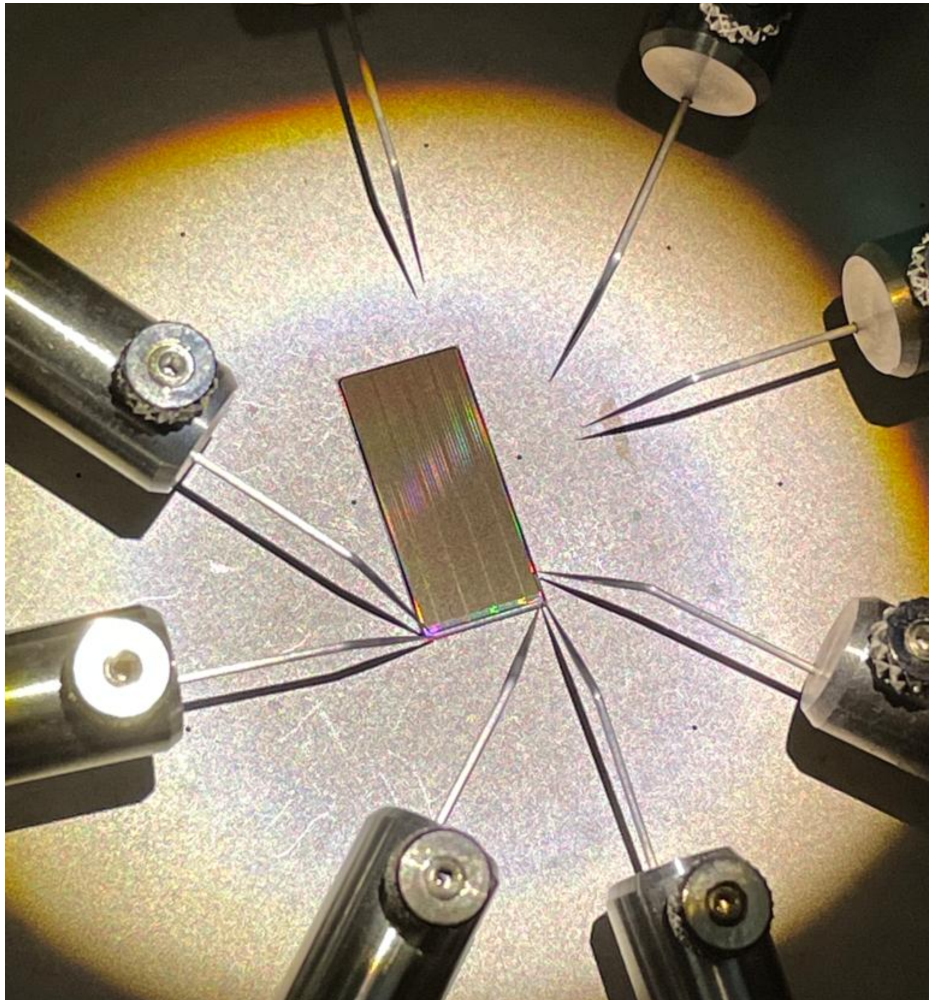
The Monolithic ASIC for the High Precision Preshower Detector of the FASER Experiment at the LHC

CHIARA MAGLIOCCA
on behalf of the FASER Preshower Upgrade team

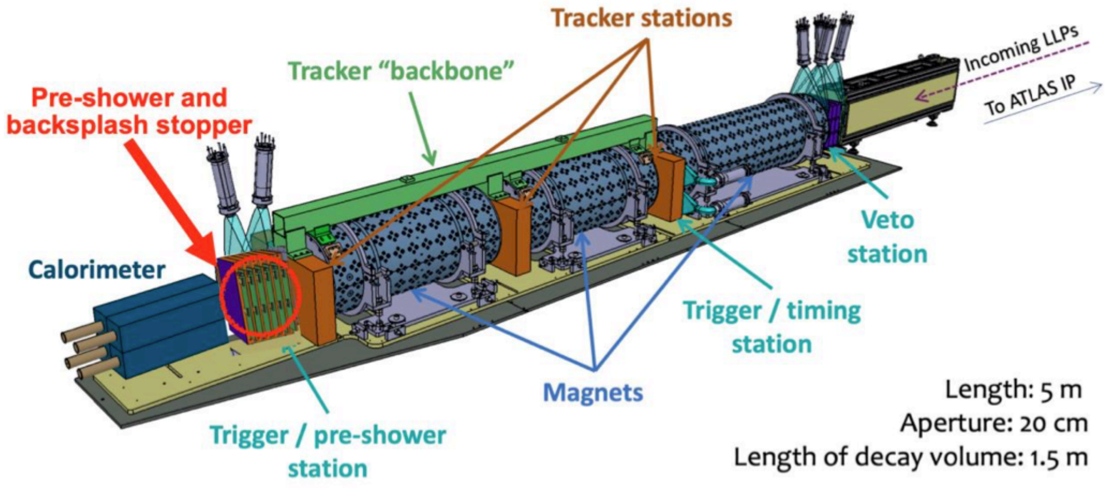
10th Beam Telescopes and Test Beams Workshop, Lecce

Talk Outline

1. Introduction: FASER Experiment
2. Preshower Upgrade: Small-size ASIC Prototype
3. Preshower Upgrade: Pre-production ASIC
4. Summary & Outlook



The FASER Experiment at LHC



- **F**orw**A**rd **S**earch **E**xpe**R**iment
- Designed to search for **light and weakly-interacting particles** + study the **interactions of high-energy neutrinos** (FaserNu)

- Fluxes of high-energy SM particles are supressed
- Muons and neutrinos only exception

Zero degrees angle → huge LLPs flux

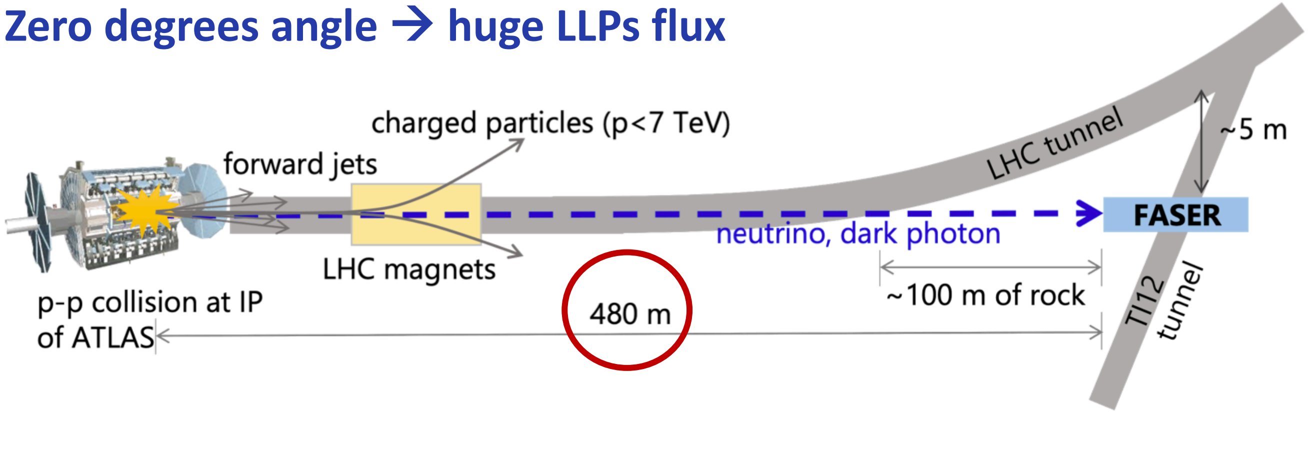
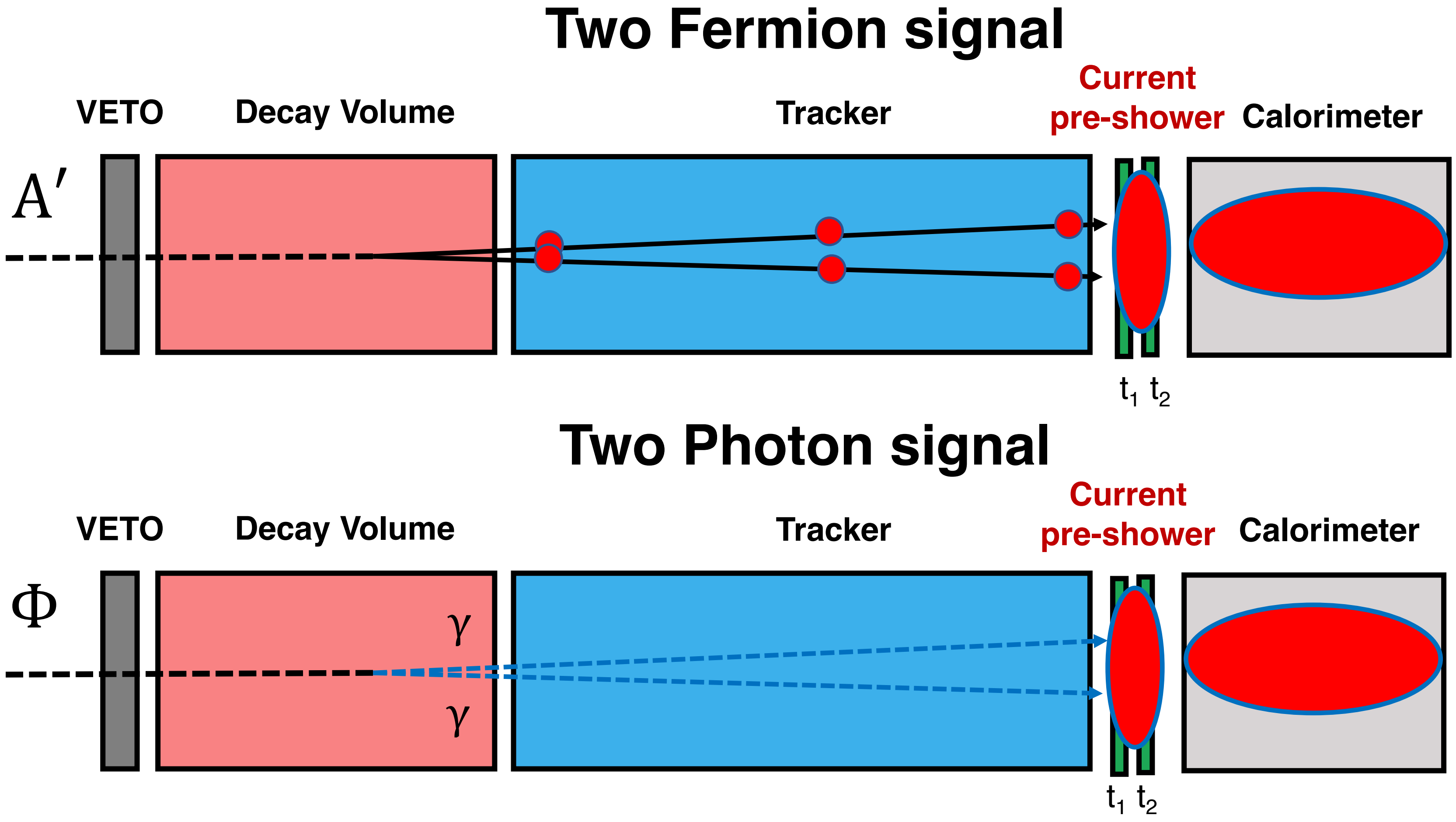
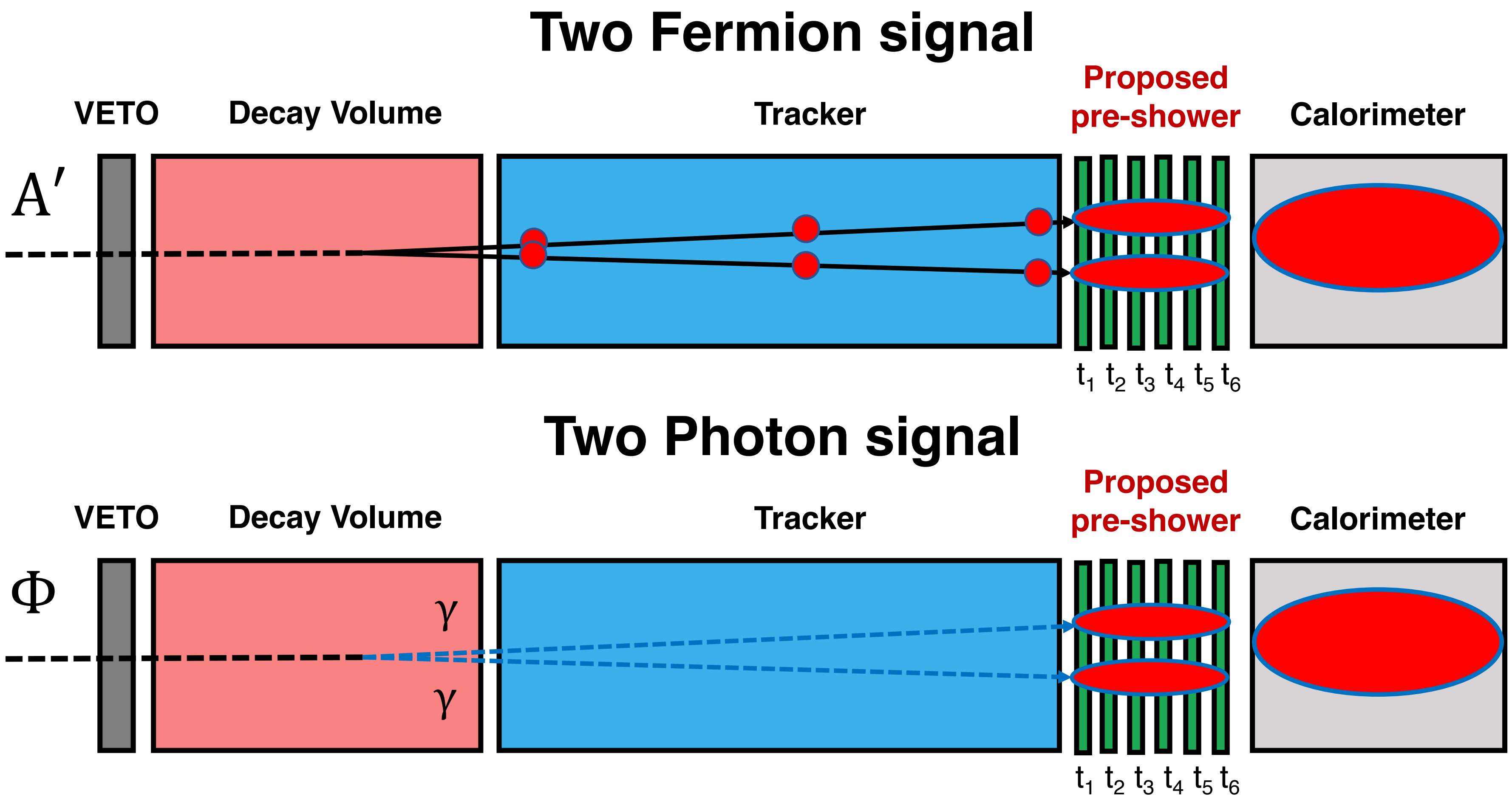


Figure: Location of FASER in the tunnel - schema is not in scale.

What Are We Able to Detect Well: Two Fermion Signal

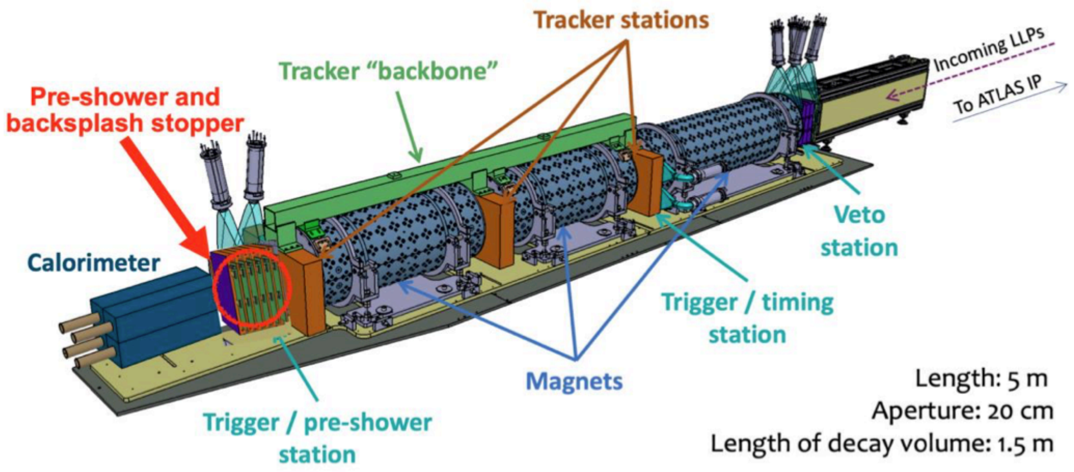


What Are We Willing to Detect: Two Photon Signal



The FASER Pre-shower Detector Upgrade

- MAIN CHALLENGE: ***Resolve separate photon signatures*** before coarser calorimeter ⇨ preshower needed



- <u>**Current preshower**</u>:

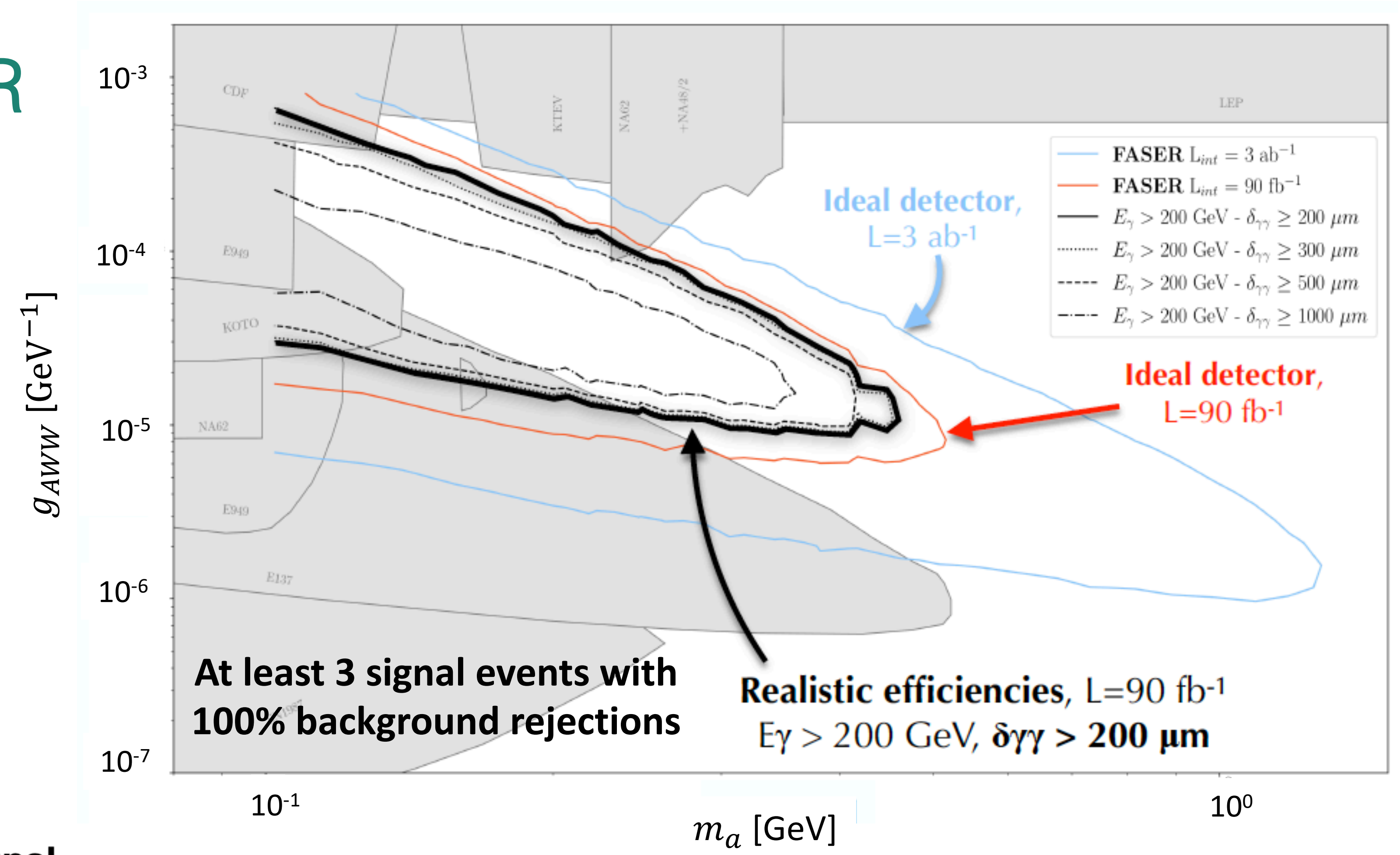
  2 layers of tungsten (1X0) + scintillating detectors
  ⇨ no XY granularity

- Main goal of the upgraded preshower detector:
  - **High granularity/high dynamic range** for charge measurements
  - Pre-shower based on monolithic silicon pixel sensors
  - Discriminate **TeV scale electromagnetic showers**
  - Targeting data-taking in 2024/2025, during LHC Run3 and during HL-LHC

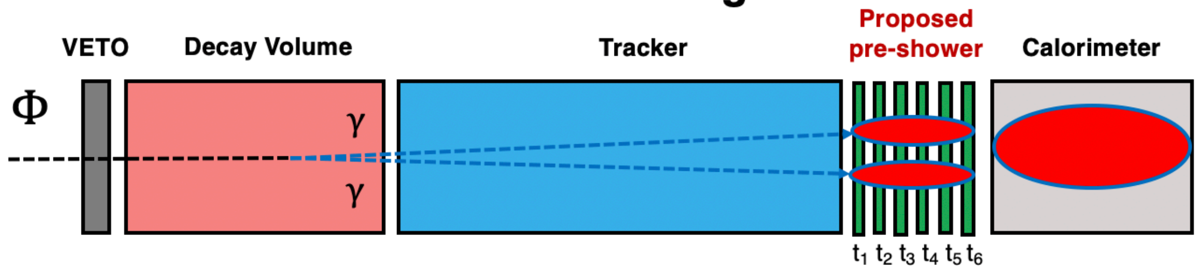
Independent measurement of two very collimated photons

Physics with FASER

- FASER can probe **Axion-Like-Particles** (ALPs) model
- ALPs produced via the aWW coupling
- ALPs **decay into a photon-pair** within FASER volume



Two Photon signal

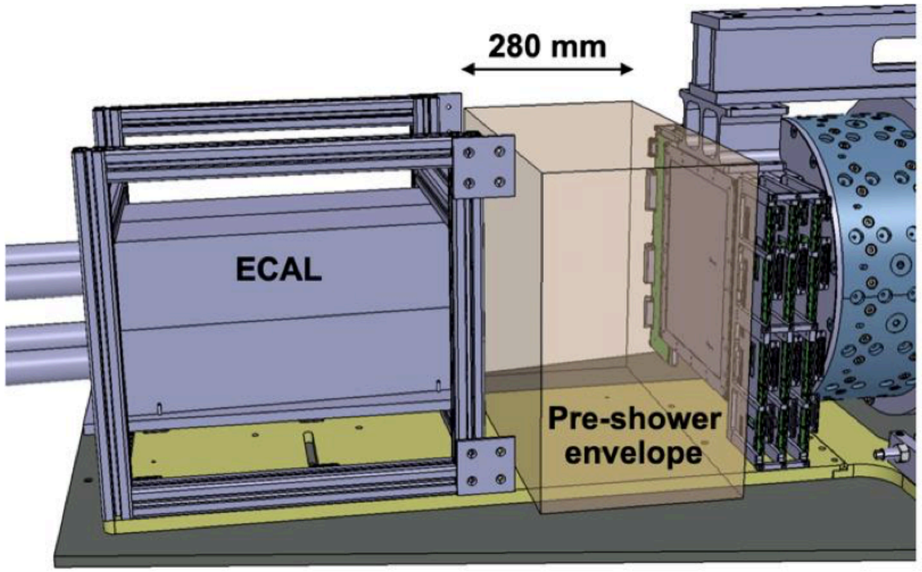


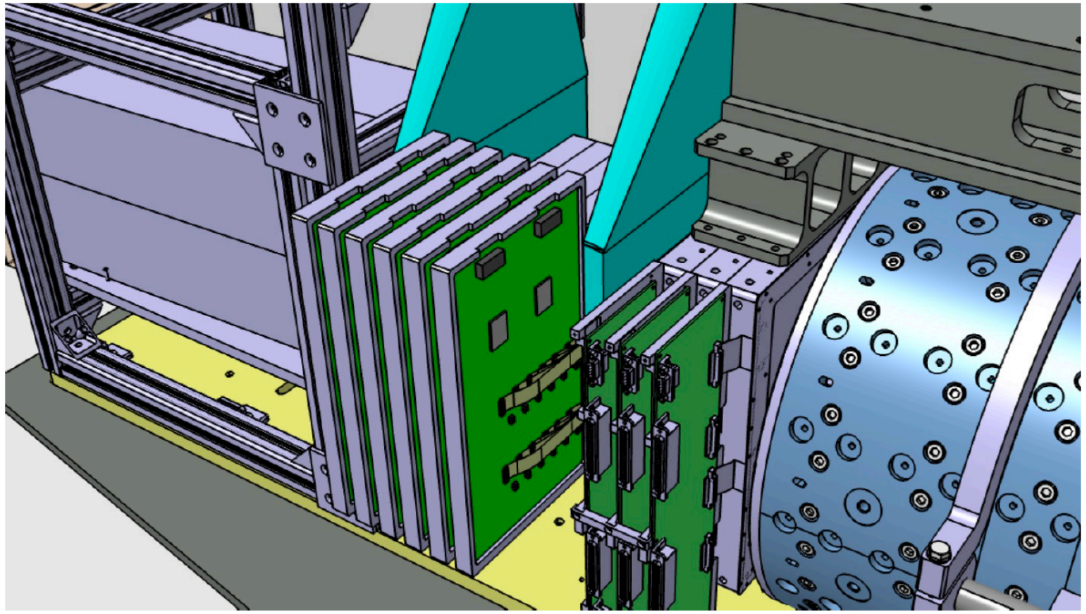
H. Abreu et al. "The FASER W-Si High Precision Preshower Technical Proposal" CERN-LHCC-2022-006 ; LHCC-P-023 https://cds.cern.ch/record/2803084

Pre-shower Upgrade Design

H. Abreu et al. "The FASER W-Si High Precision Preshower Technical Proposal" CERN-LHCC-2022-006 ; LHCC-P-023 https://cds.cern.ch/record/2803084

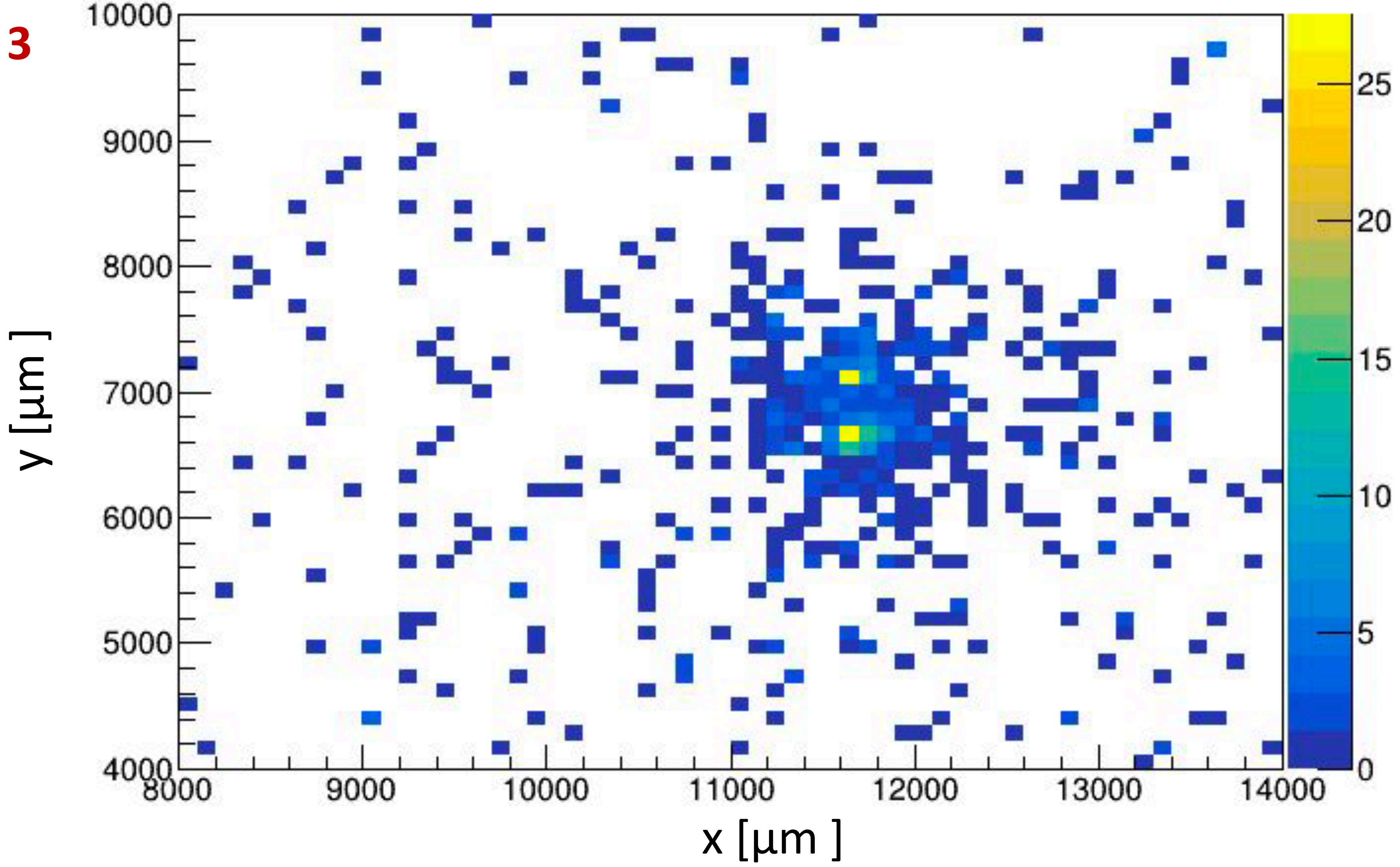
- 6 detector planes
- Each detector plane: **1 X0 of tungsten** + plane of **monolithic Si-pixel sensors**





EM Shower Development in a Pixeleted Detector

PLANE 3



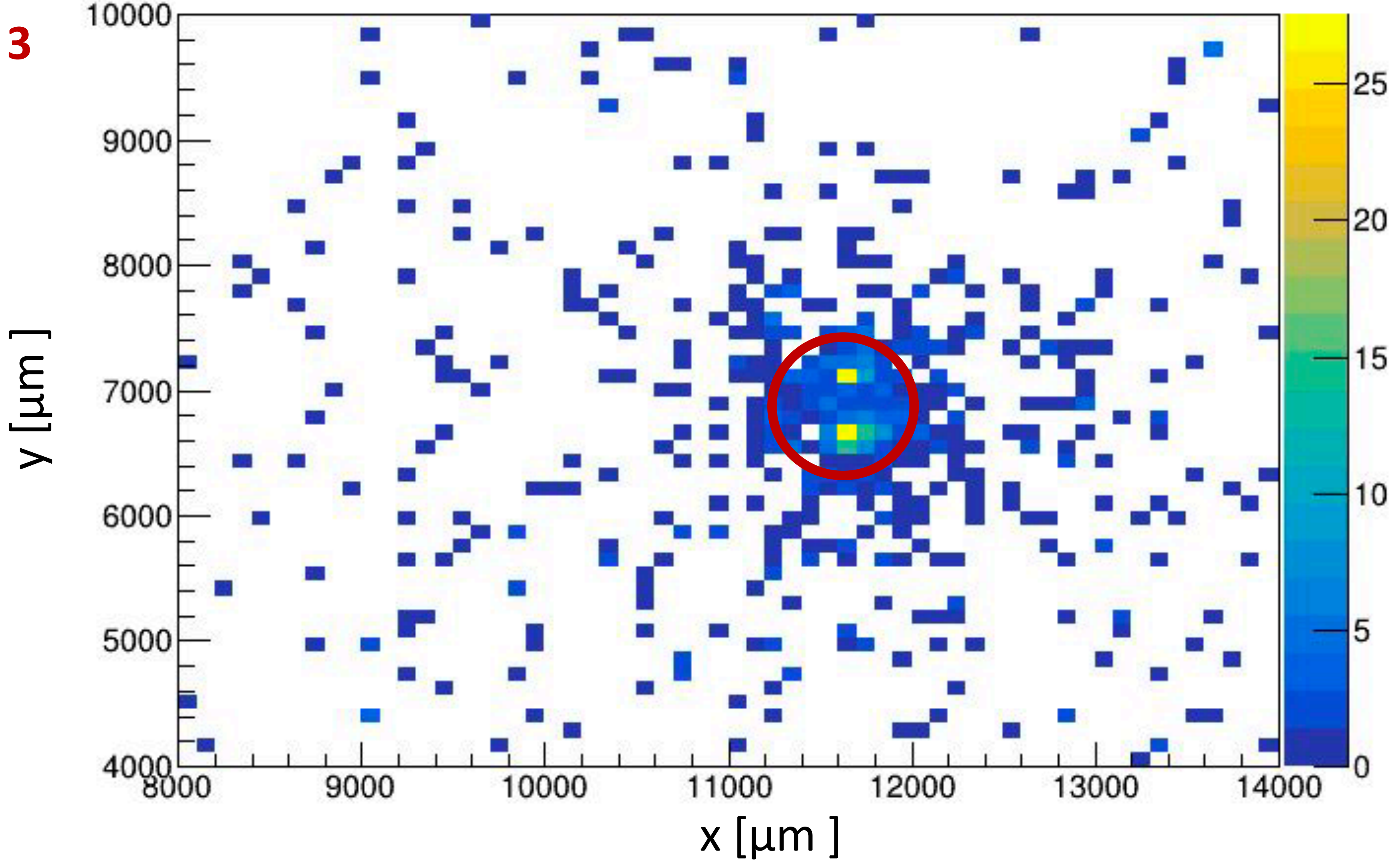
$E_{\gamma 1}$= 1 TeV
$E_{\gamma 2}$= 1 TeV

$d(\gamma 1, \gamma 2)$ = 500 μm

Events simulated using Allpixsquared

EM Shower Development in a Pixeleted Detector

PLANE 3



$E_{\gamma 1}$= 1 TeV
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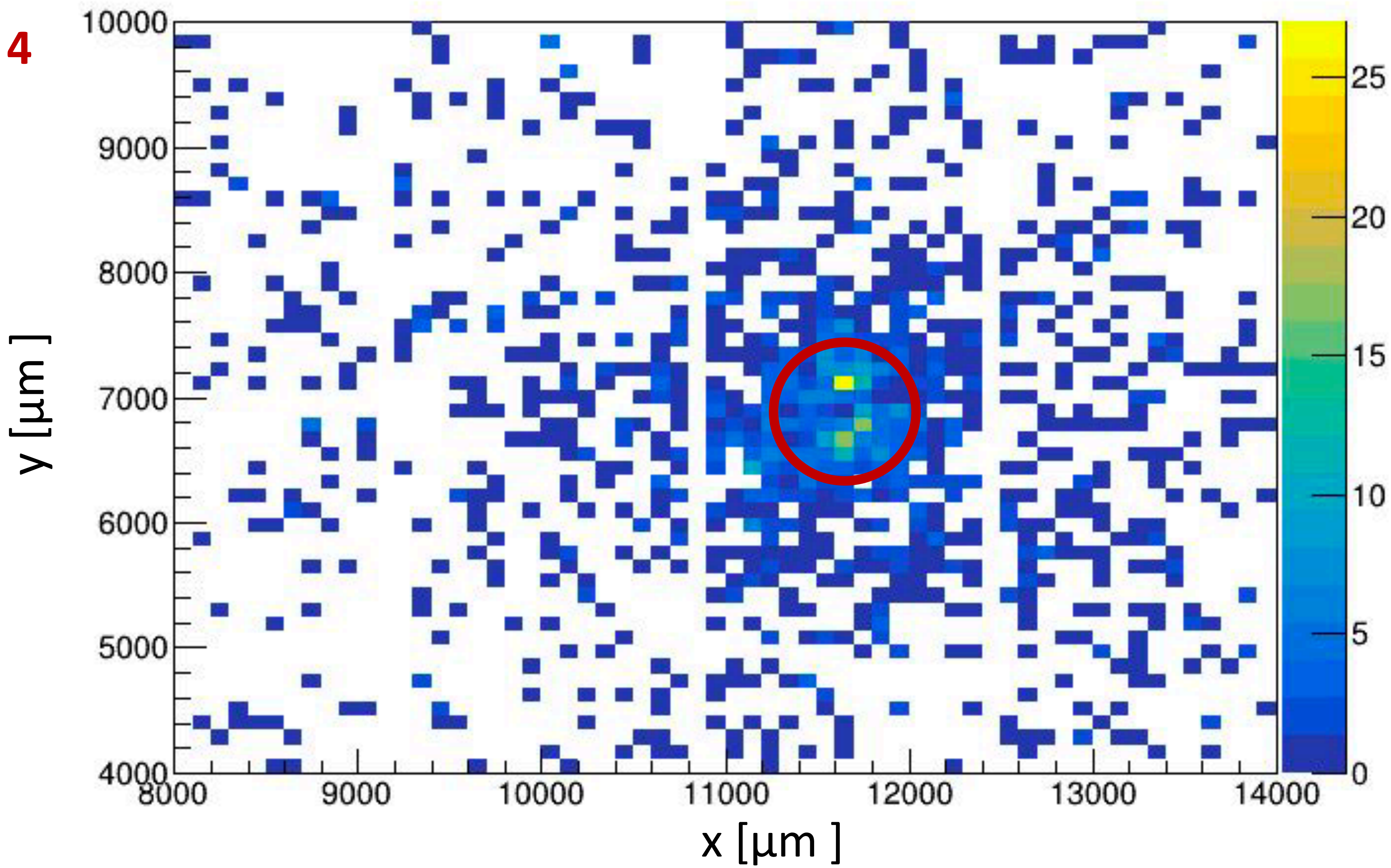
Events simulated using Allpixsquared

EM Shower Development in a Pixeleted Detector

PLANE 4



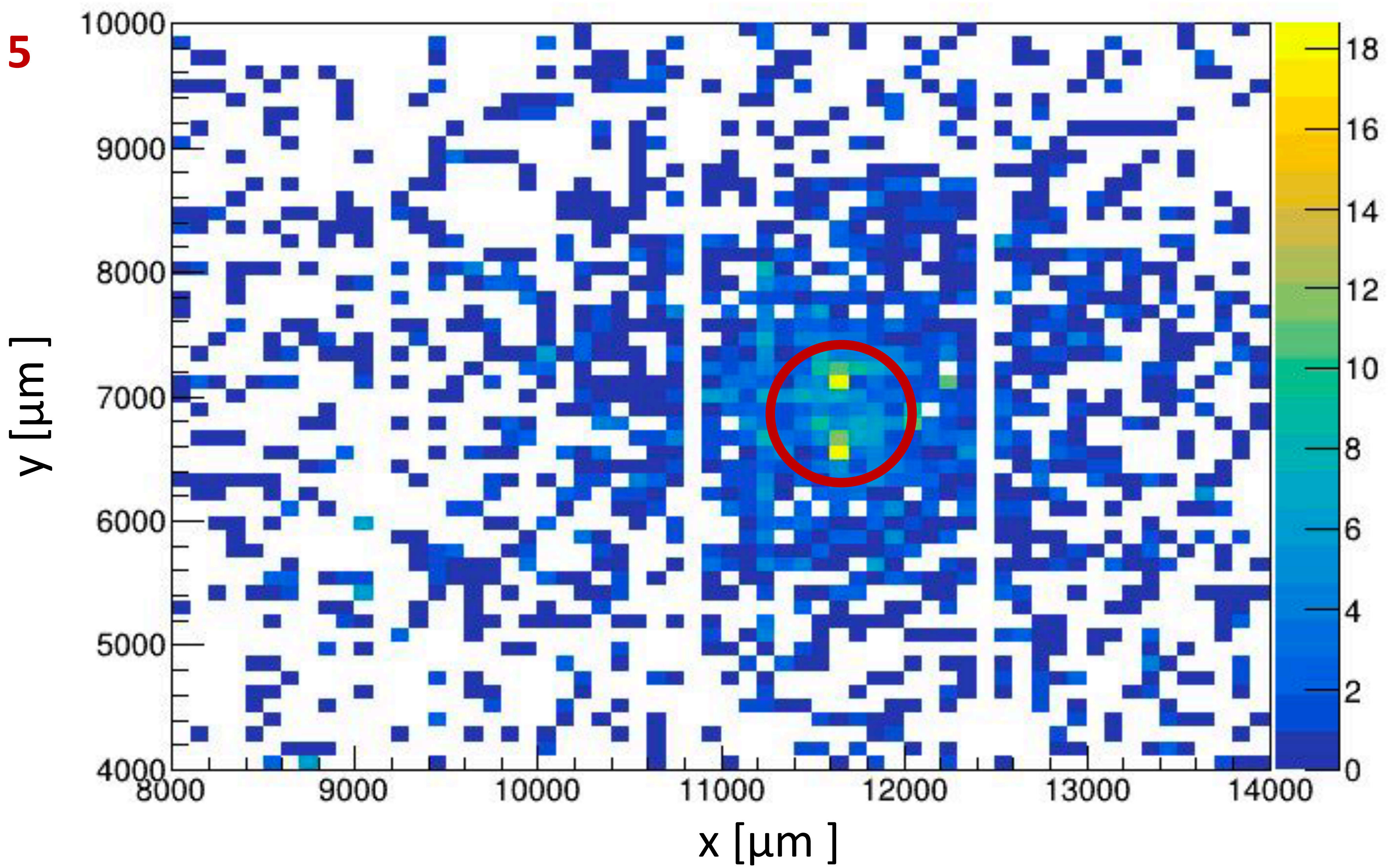
$E_{\gamma 1}$= 1 TeV
$E_{\gamma 2}$= 1 TeV

$d(\gamma 1, \gamma 2) =$
$500\ \mu m$

Events simulated using Allpixsquared

EM Shower Development in a Pixeleted Detector

PLANE 5



$E_{\gamma 1}$= 1 TeV
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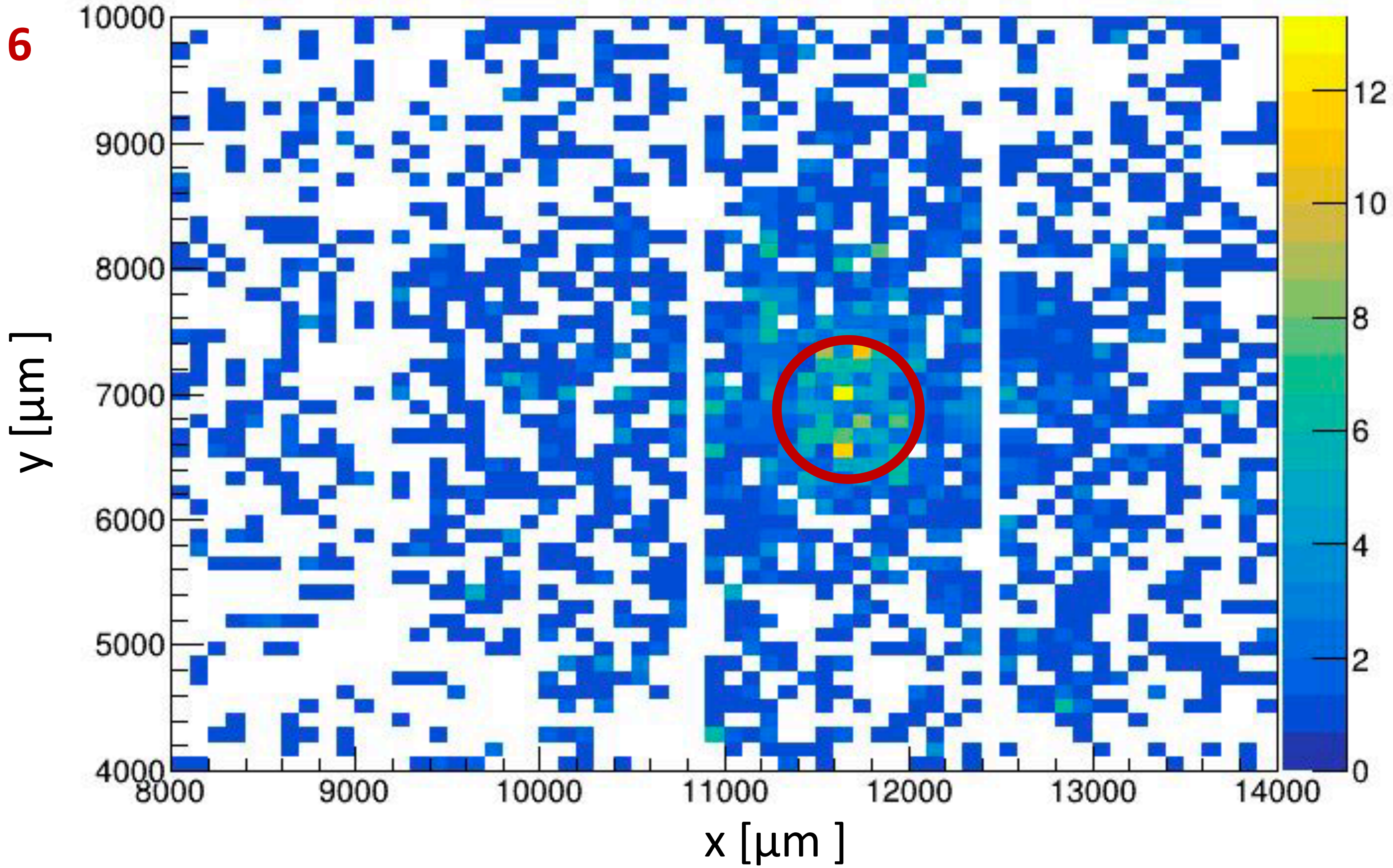
Events simulated using Allpixsquared

EM Shower Development in a Pixeleted Detector

PLANE 6



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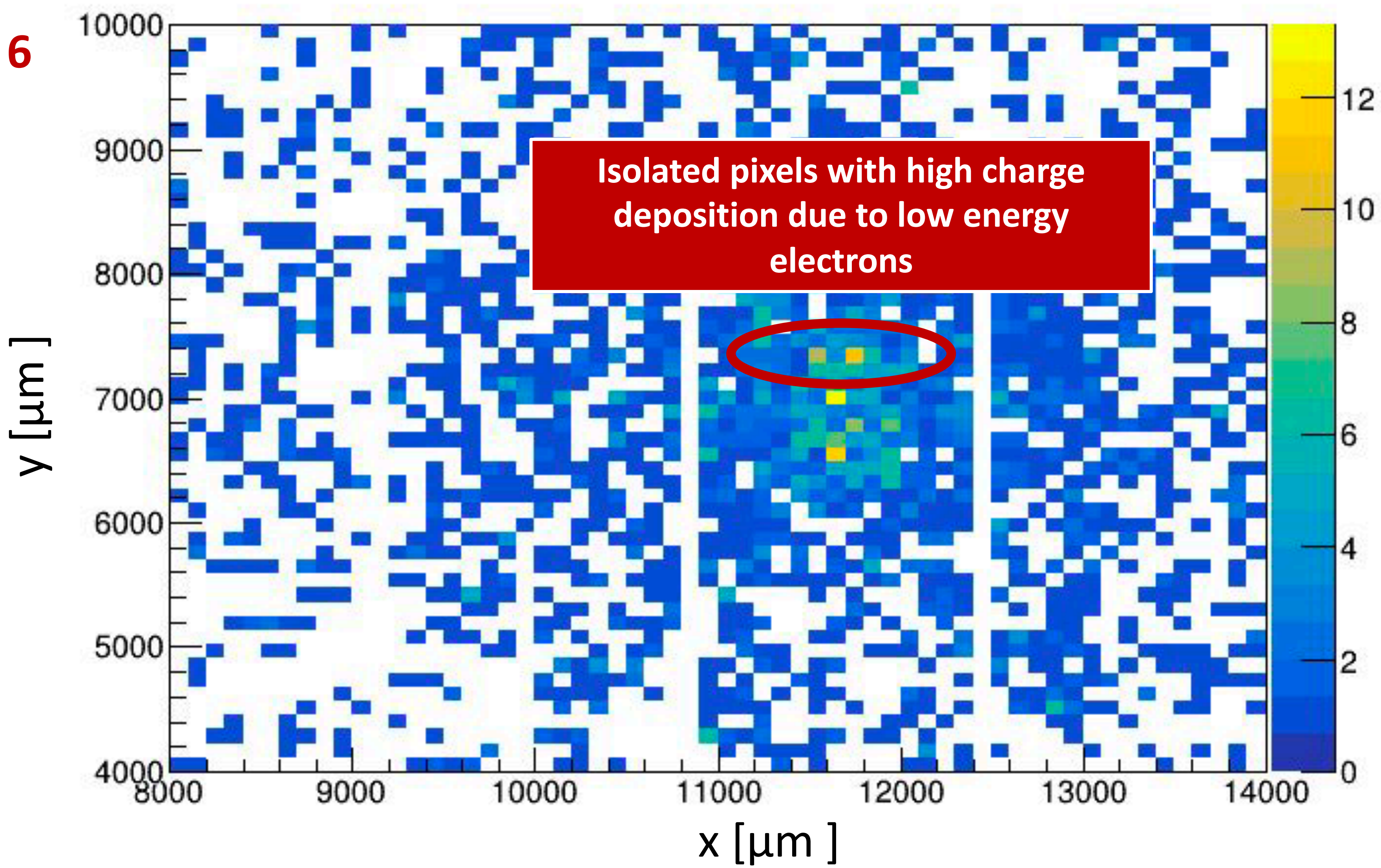
Events simulated using Allpixsquared

EM Shower Development in a Pixeleted Detector

PLANE 6



$E_{\gamma 1}$= 1 TeV
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d($\gamma 1, \gamma 2$) = 500 µm

Events simulated using Allpixsquared

F. Martinelli et al.
2021 *J. Inst.* **16** P12038
https://doi.org/10.1088/1748-0221/16/12/P12038

The FASER Small Prototype Chip

Purpose

study **different level of INTEGRATION OF THE FRONT-END** electronics inside the sensitive area of the pixels

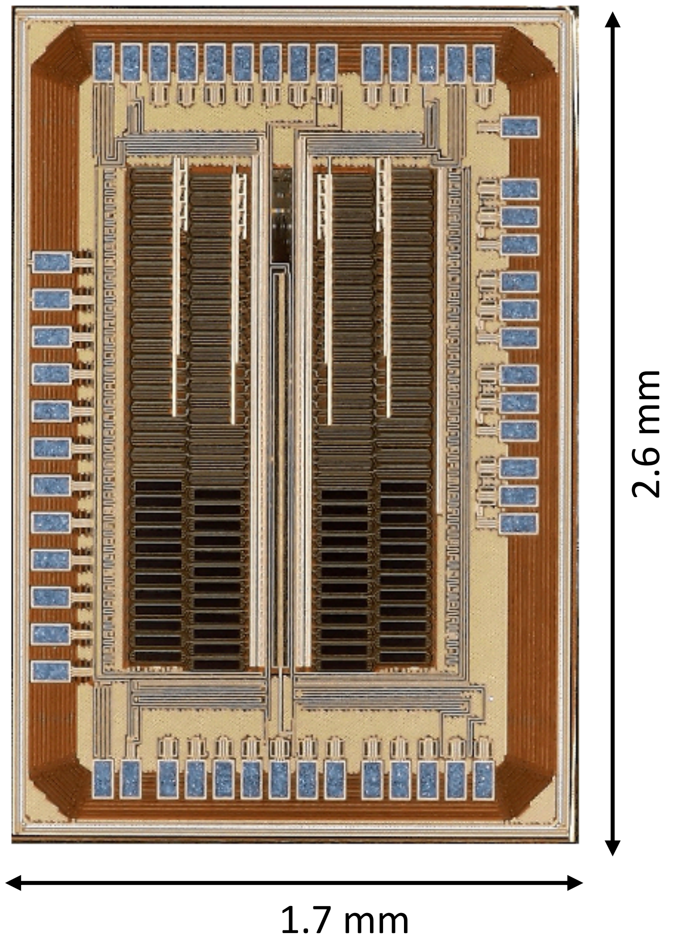
Final aim

identify the BEST FRONT-END CONFIGURATION for the pre-production chip of the FASER Pre-shower (submitted in June 2021)

200 µm x 50 µm PIXELS
shape to reduce the electric field at the edge of the sensitive areas

Tested in 2021

2 superpixels
16x4 pixels each



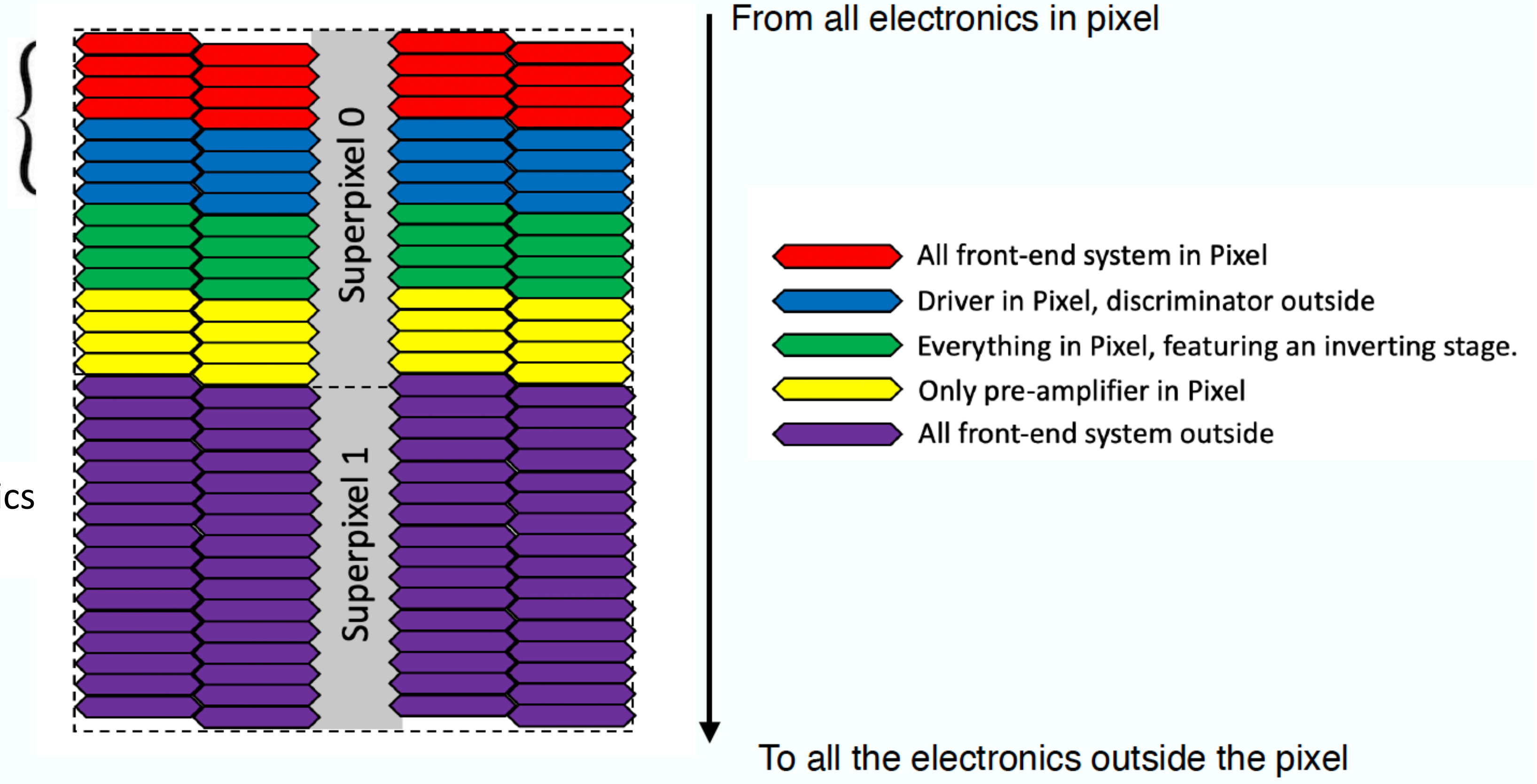
Small Prototype: Front-end Configurations

F. Martinelli et al.
2021 *J. Inst.* **16** P12038
https://doi.org/10.1088/1748-0221/16/12/P12038

5 Different front-end configurations

Configurations we would like to include

Backup configurations to still study electronics elements for the pre-production chip

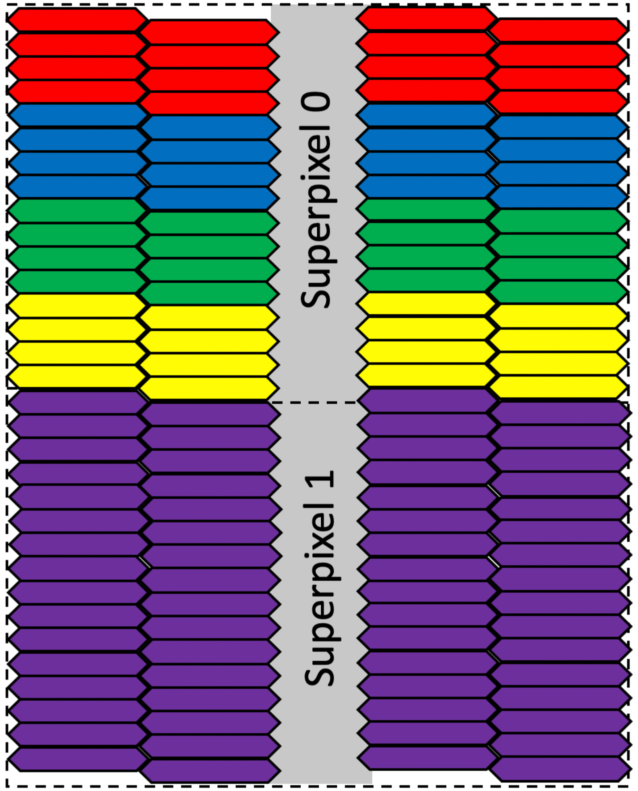


Small Prototype: Results and Comments

F. Martinelli et al.
2021 *J. Inst.* **16** P12038
https://doi.org/10.1088/1748-0221/16/12/P12038

- All front-end system in Pixel
- Driver in Pixel, discriminator outside
- Everything in Pixel, featuring an inverting stage.
- Only pre-amplifier in Pixel
- All front-end system outside

Configuration	σ_v [mV]	G_c [mV/fC]	ENC [e⁻]	$\sigma_{V_{th}}$ [mV]
All f.e. outside pixel	4.2 ± 0.2	159 ± 1.0	165 ± 9	32.3
Only pre-amp. in pixel	2.5 ± 0.1	96.8 ± 0.5	161 ± 9	26.9
All f.e. in pixel, inv. stage	6.9 ± 0.5	179 ± 1.0	241 ± 19	30.8
Pre-amp. and driver in pixel	3.8 ± 0.2	133.7 ± 0.6	178 ± 9	23.4
All f.e. in pixel	5.4 ± 0.4	148 ± 1.0	228 ± 20	27.1



- The **last two configurations** represent a good compromise between comptacness and performance
- Configurations integrated in the pre-production chip

FASER Pre-production Chip

FASER MAIN

128x64 pixels

Pre-amplifier + driver in pixel, discriminator outside

FASER V2

128x48 pixels

Everything integrated in pixel (discriminator also)

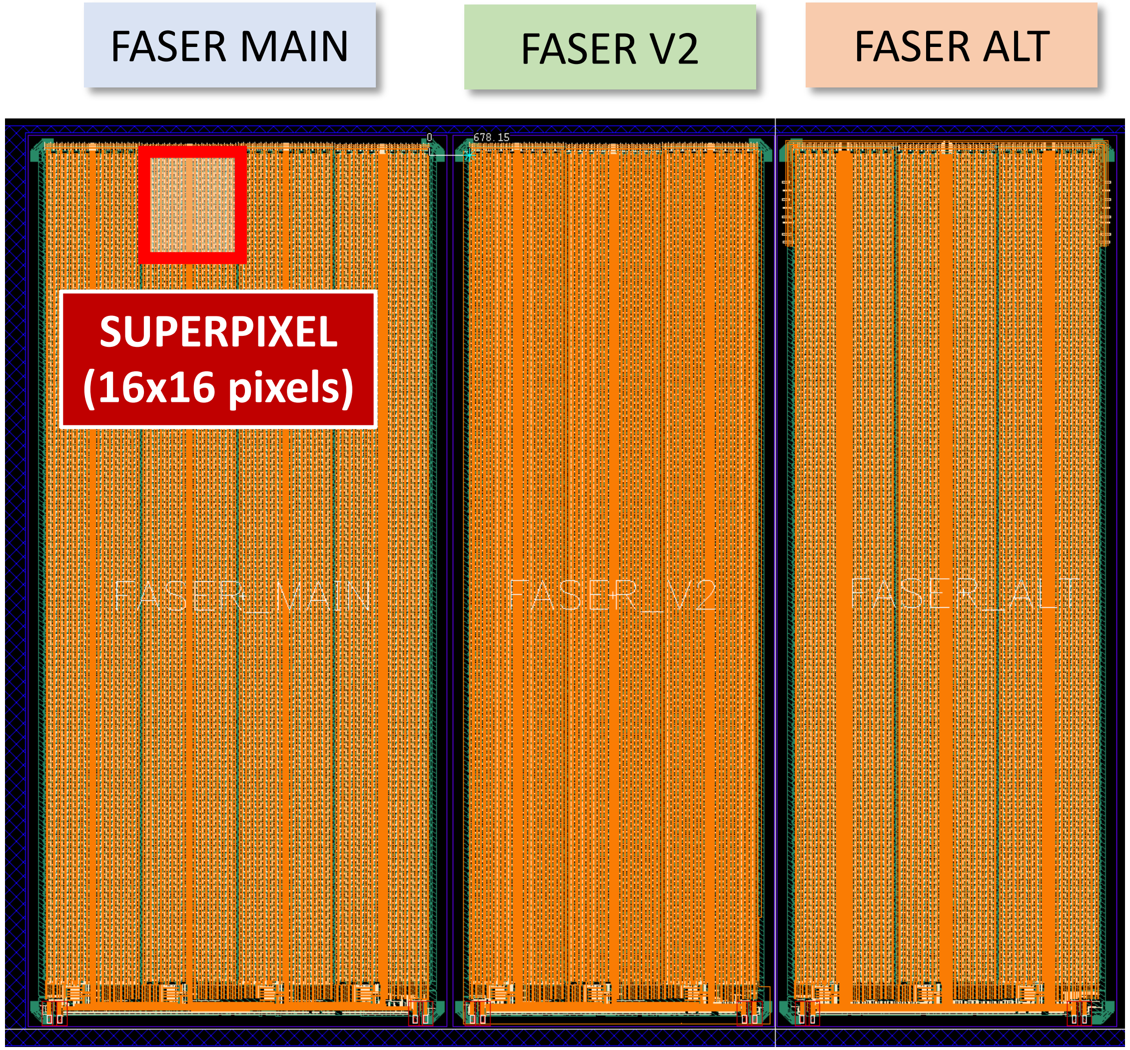
FASER ALT

128x48 pixels

Conservative configuration dedicated to the test of the digital readout

Disadvantage: much more dead area

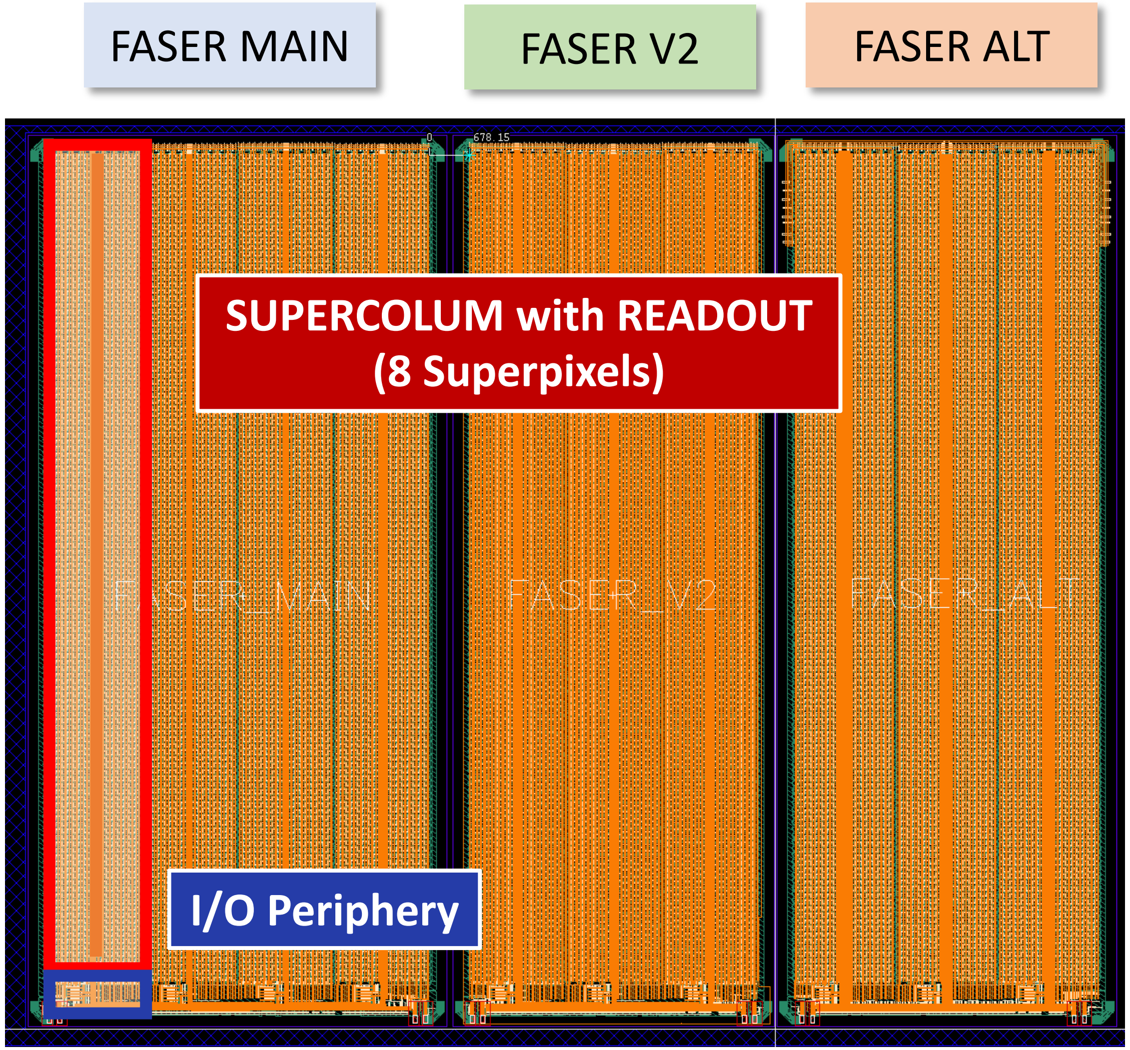
FASER Pre-production Chip



MODULAR ARCHITECTURE

Matrices divided in **super-pixels** and **super-columns**

FASER Pre-production Chip



MODULAR ARCHITECTURE

Matrices divided in **super-pixels** and **super-columns**

Monolithic ASIC Specifications

(*) *See [Théo Moretti's] and [Matteo Milanesio's] talks*

Main specifications	
Pixel Size	65 μm side (hexagonal) ~ 100 μm pitch
Pixel dynamic range	0.5 ÷ 65 fC
Cluster size	O(1000) pixels
Readout time	< 200 μs
Time resolution	< 300 ps
Power consumption	< 150 mW/cm^2

Selected technology: SG13G2, by IHP microelectronics.

ASIC design: University of Geneva, with support from KIT and CERN

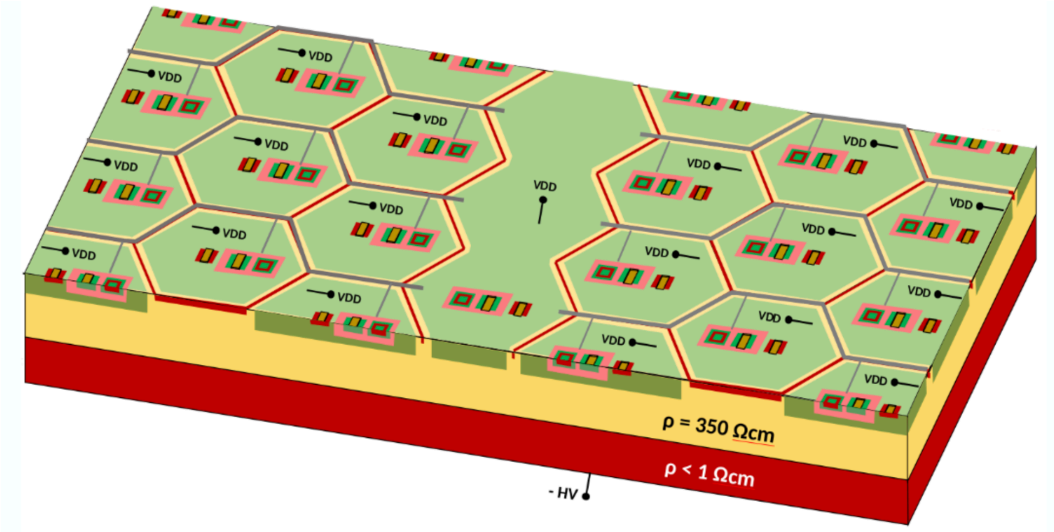
- Monolithic ASIC in **130nm SiGe BiCMOS** (*)
- Pixel size: **hexagonal pixels with 65 μm side** (~ 100 μm pitch)
- Chip size: 1.5 x 2.5 cm^2

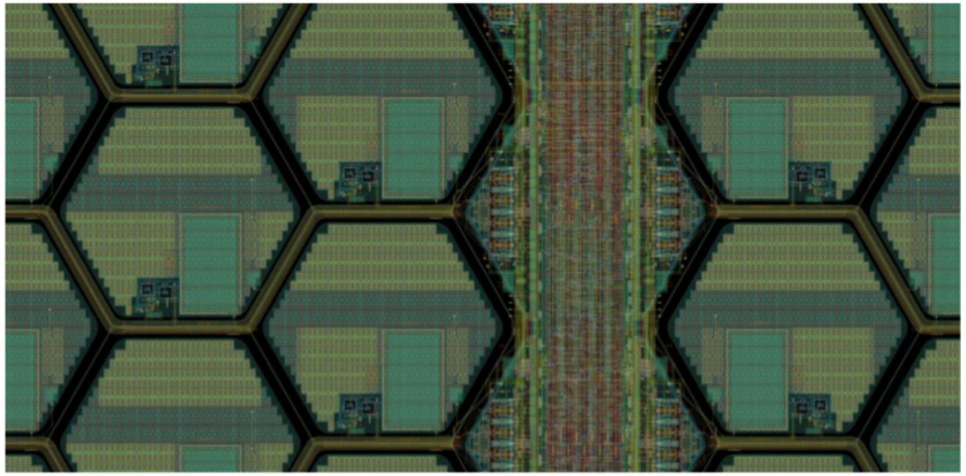
- **Local analog memories** to store the charge
- **Ultra fast readout** with no digital memory on-chip to minimize the dead area

In between an imaging chip and a HEP detector

Sensor Cross Section

- Low resistivity heavily p-doped substrate as a support
- Negative high voltage applied to the substrate

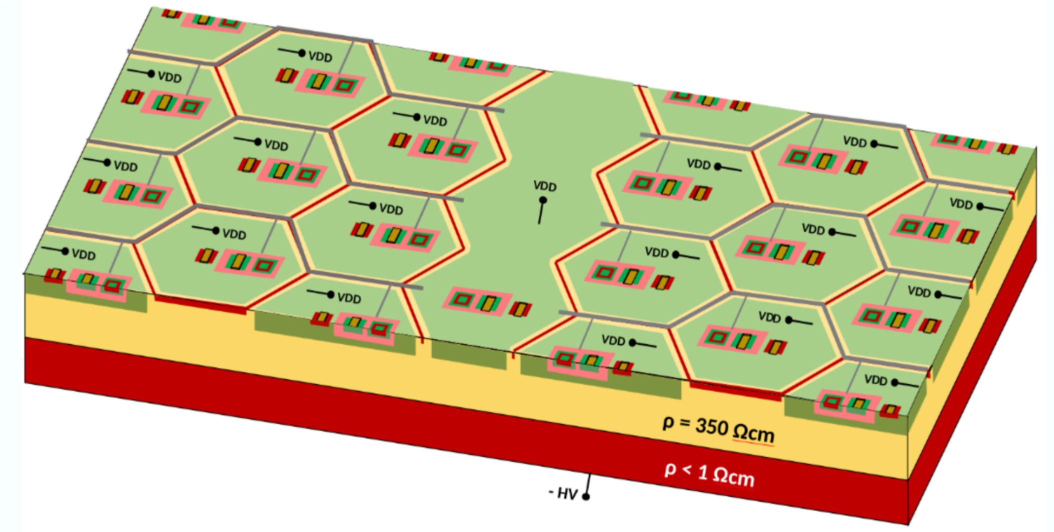


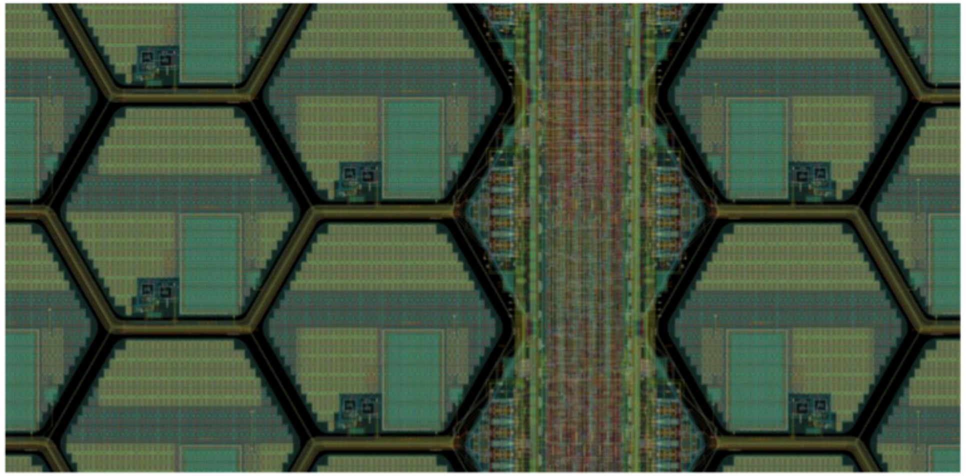


Sensor Cross Section

- Low resistivity heavily p-doped substrate as a support
- Negative high voltage applied to the substrate

- High resistivity 50 µm epitaxial layer





Sensor Cross Section

- Low resistivity heavily p-doped substrate as a support
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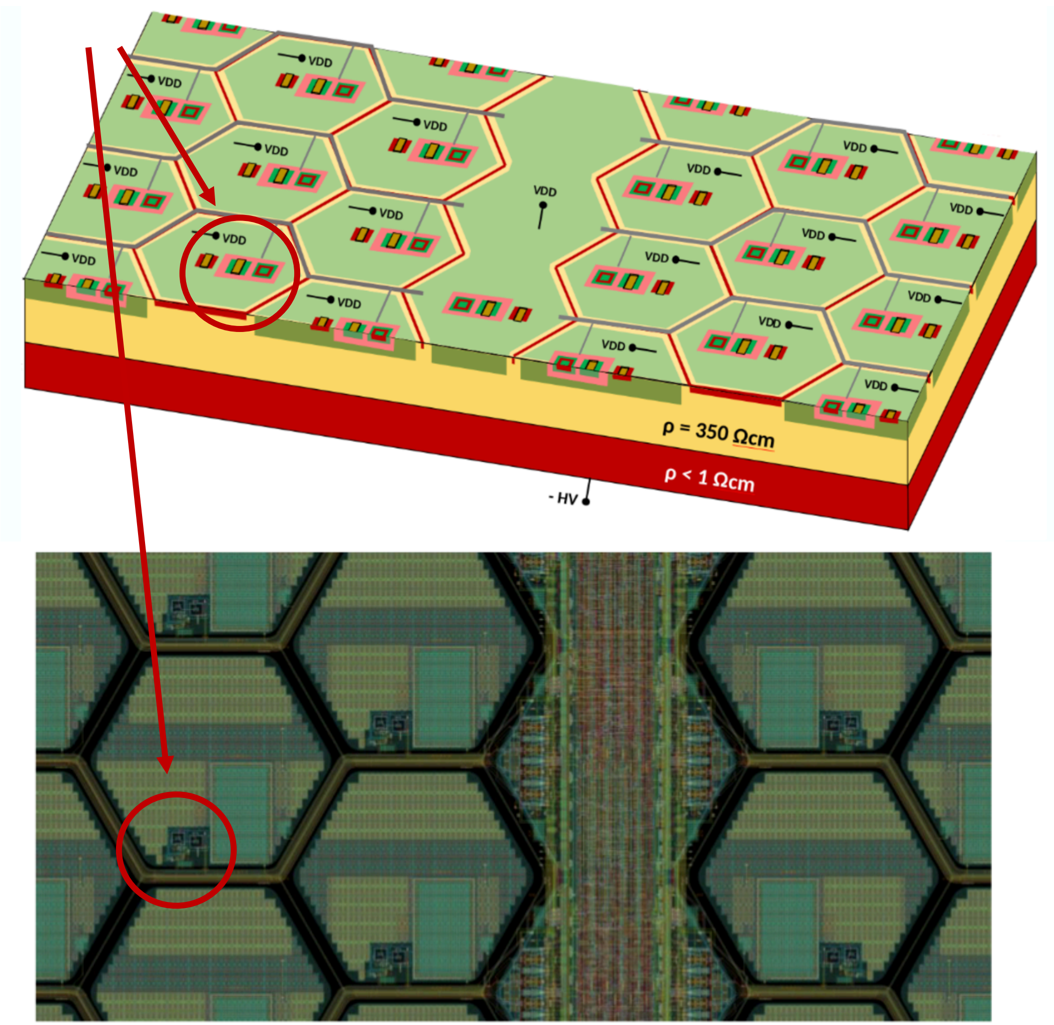
- High resistivity 50 µm epitaxial layer
- Triple – well design
- **Analog electronics inside the pixel**

ANALOG electronics



Sensor Cross Section

- Low resistivity heavily p-doped substrate as a support
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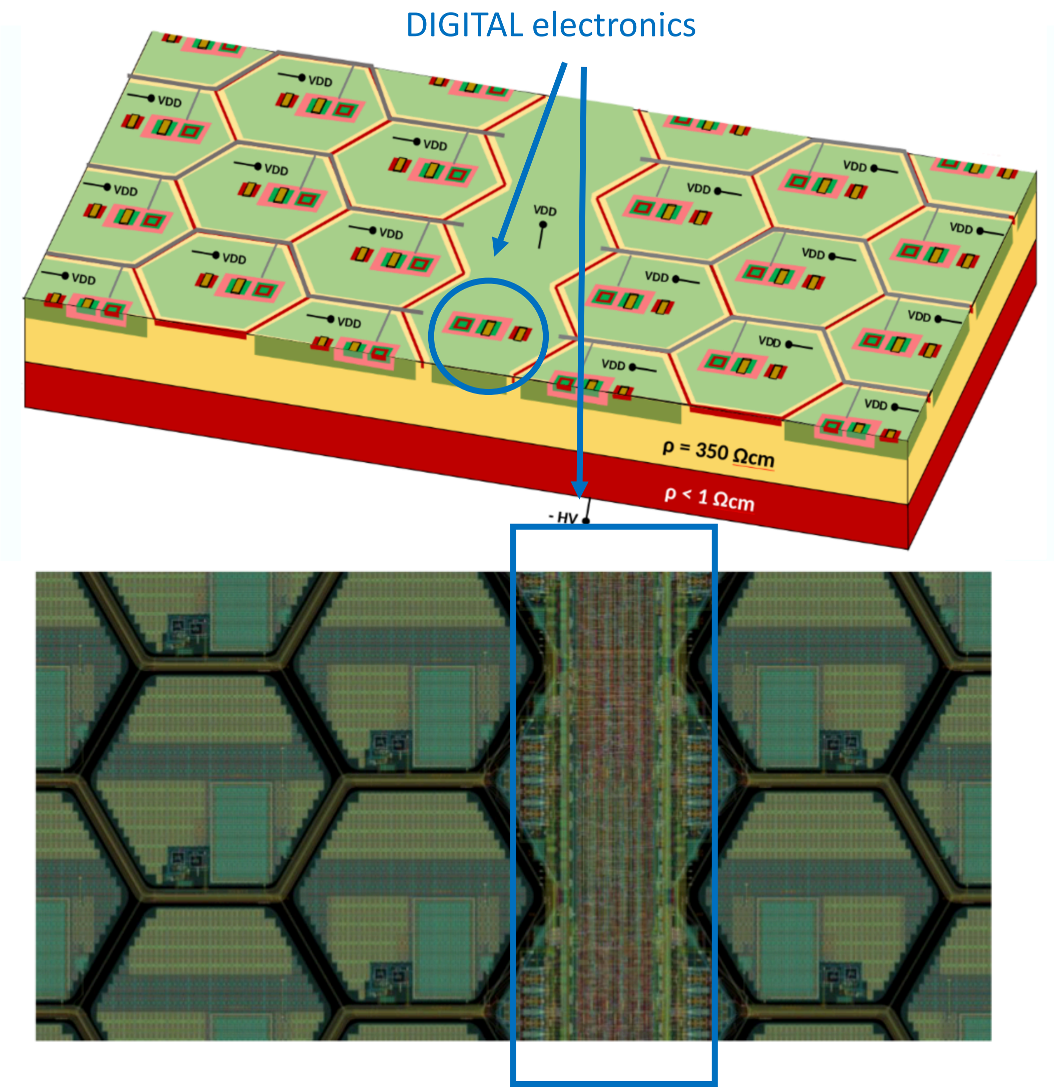
- High resistivity 50 µm epitaxial layer
- Triple – well design
- **Analog electronics inside the pixel**
- **Digital electronics outside the pixel**



Sensor Cross Section

- Low resistivity heavily p-doped substrate as a support
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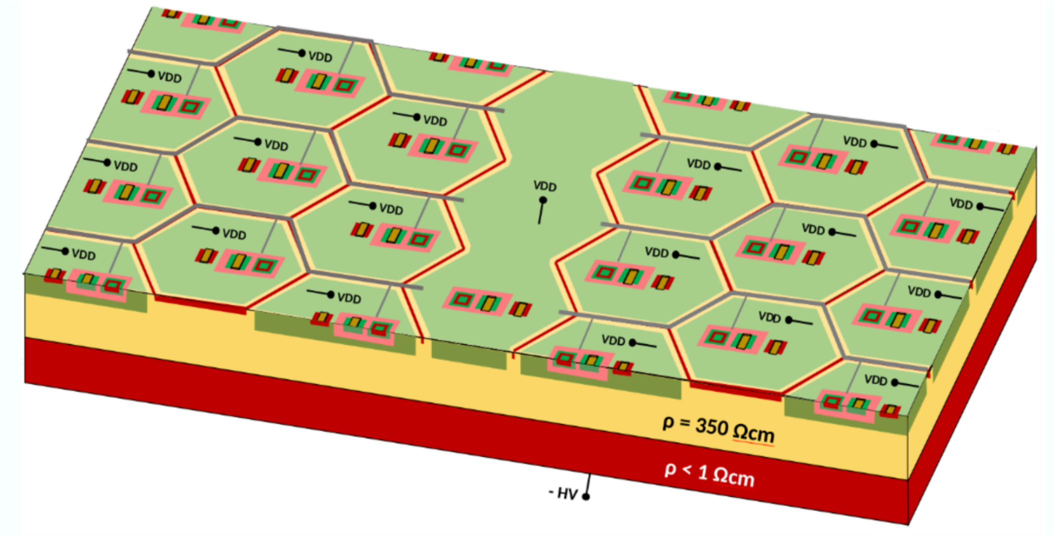
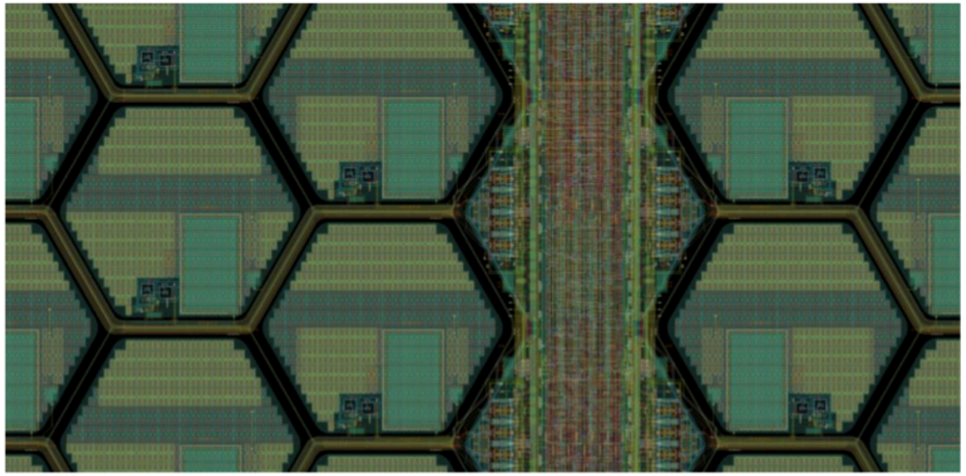
- High resistivity 50 µm epitaxial layer
- Triple – well design
- **Analog electronics inside the pixel**
- **Digital electronics outside the pixel**
- Electronics inside the guard ring isolated from substrate using a deep n-well
- Digital electronics in a separate well
- Positive low voltage applied to pixels and electronics deep n-wells





Sensor Cross Section

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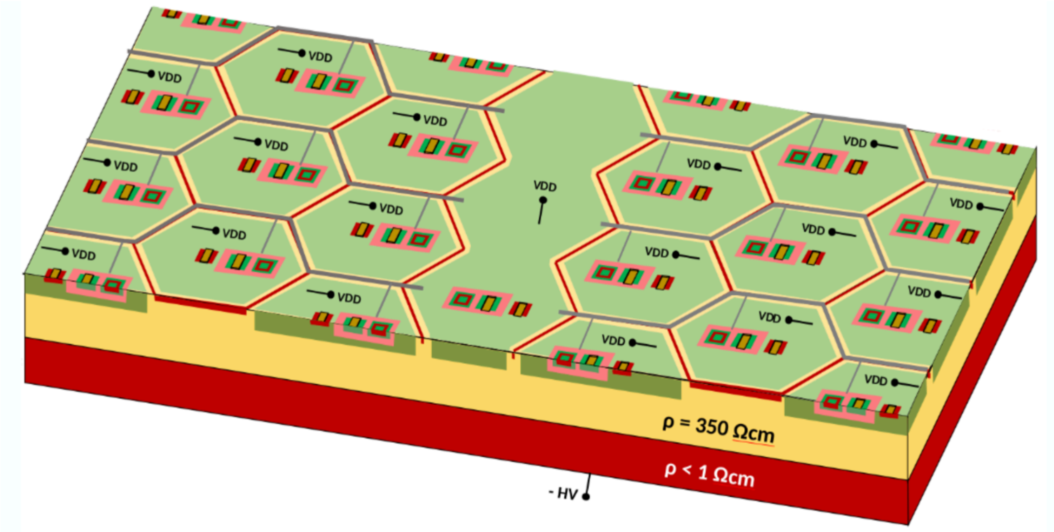
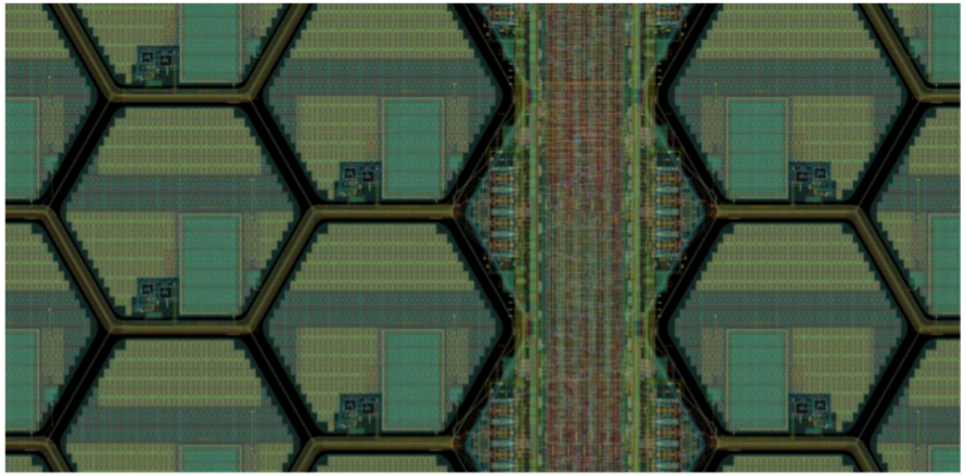
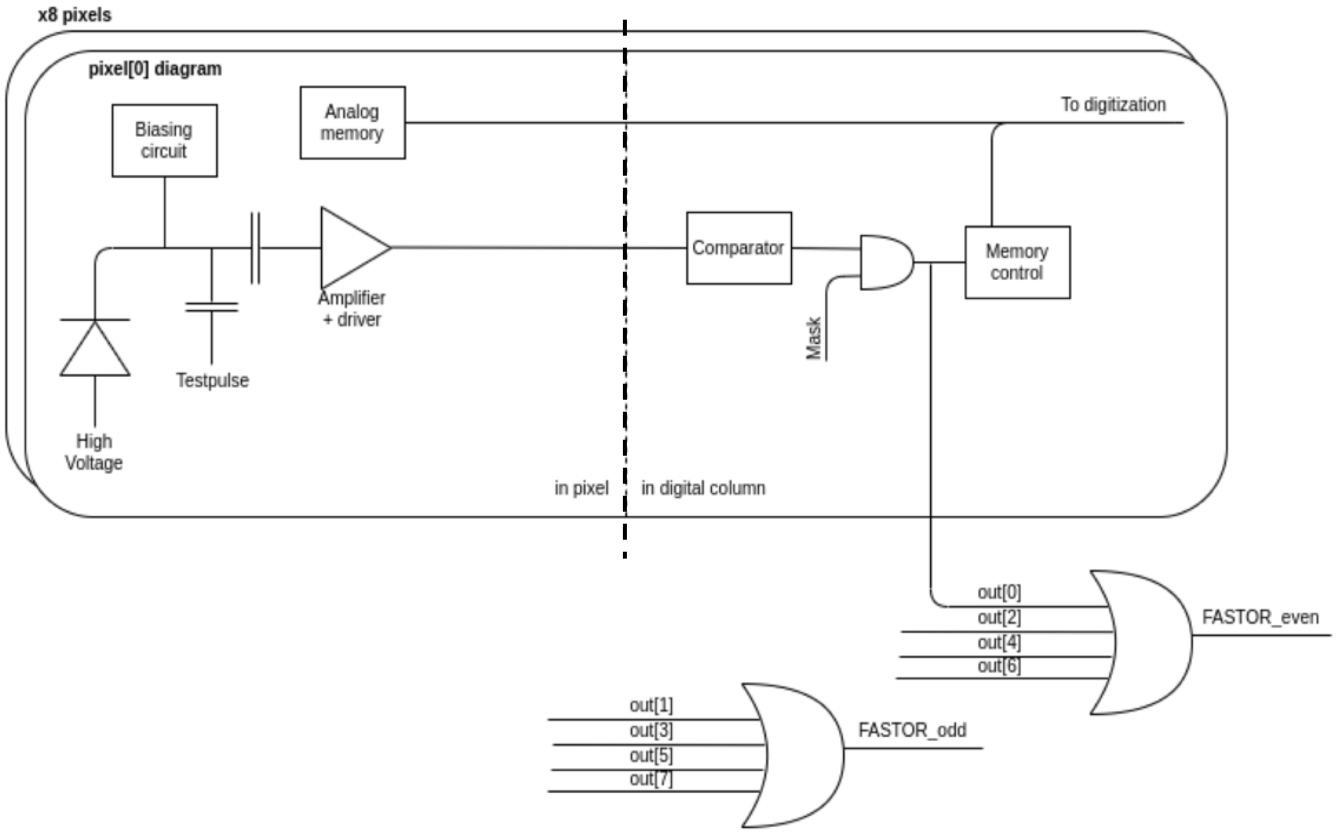
- **Analog electronics inside the pixel**
- **Digital electronics outside the pixel**
- Electronics inside the guard ring isolated from substrate using a deep n-well
- Digital electronics in a separate well
- Positive low voltage applied to pixels and electronics deep n-wells

- ≈ 6% dead area in the pixel matrix



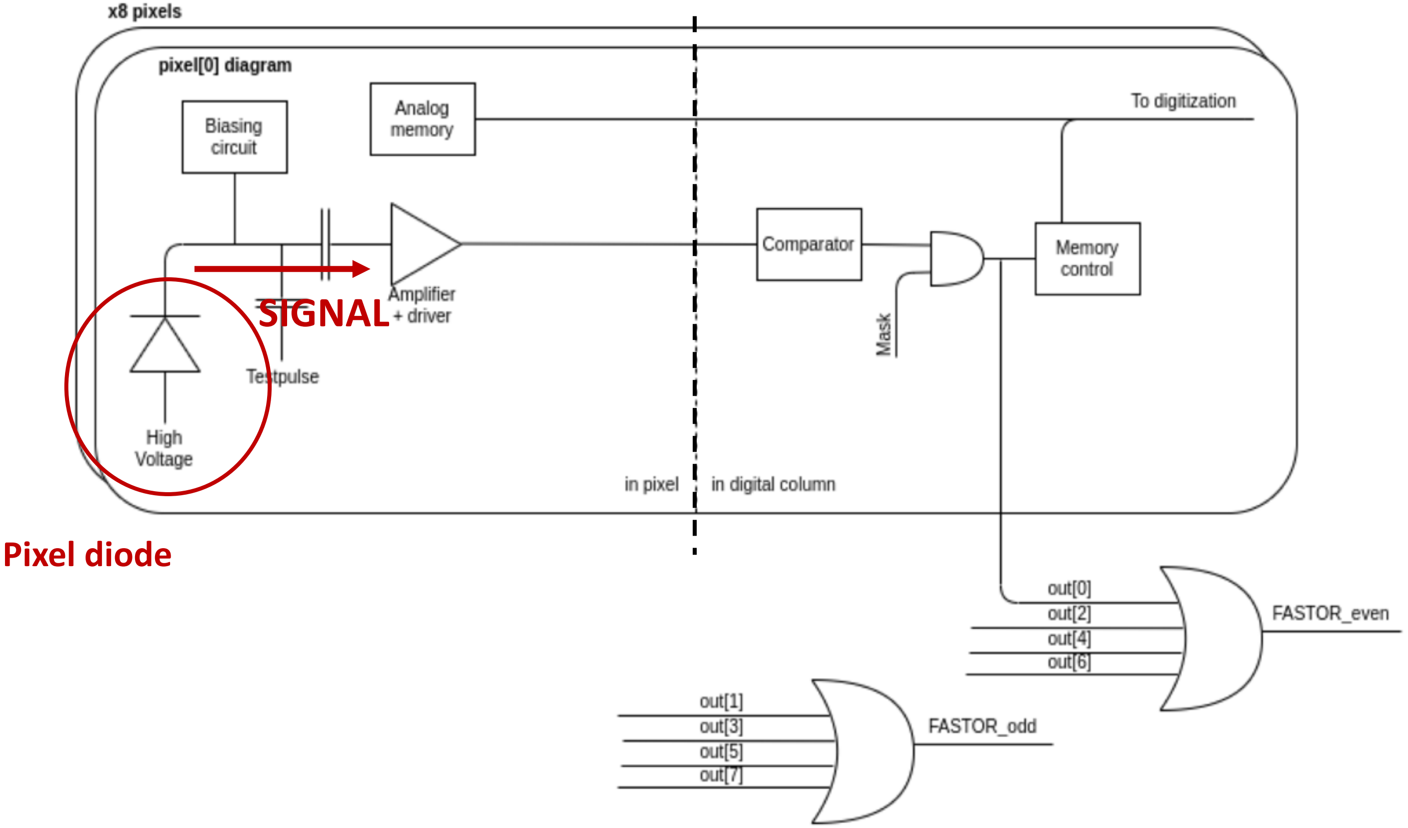


Pixel Row Structure



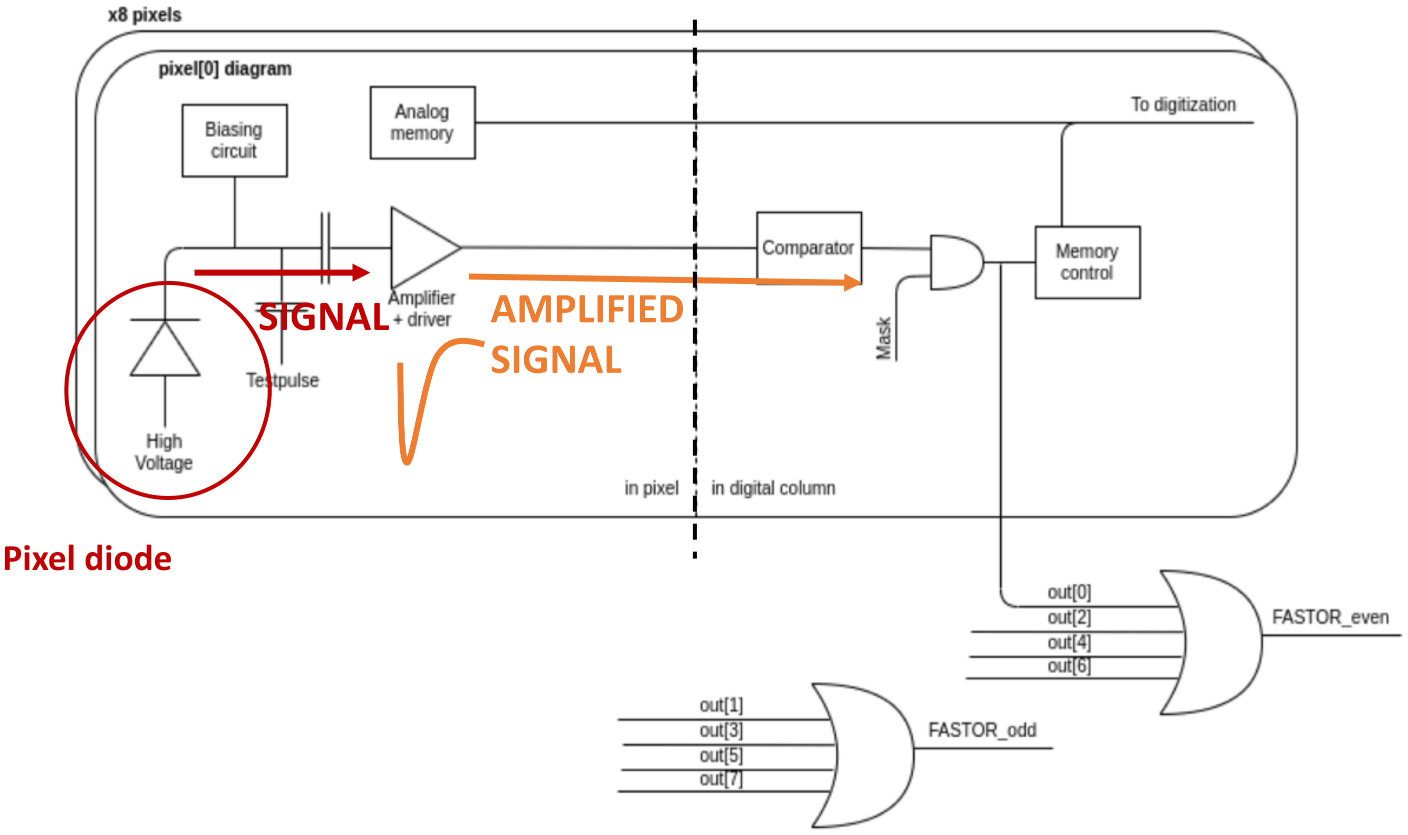
Pixel Row Structure

- When an hit arrives a signal is produced



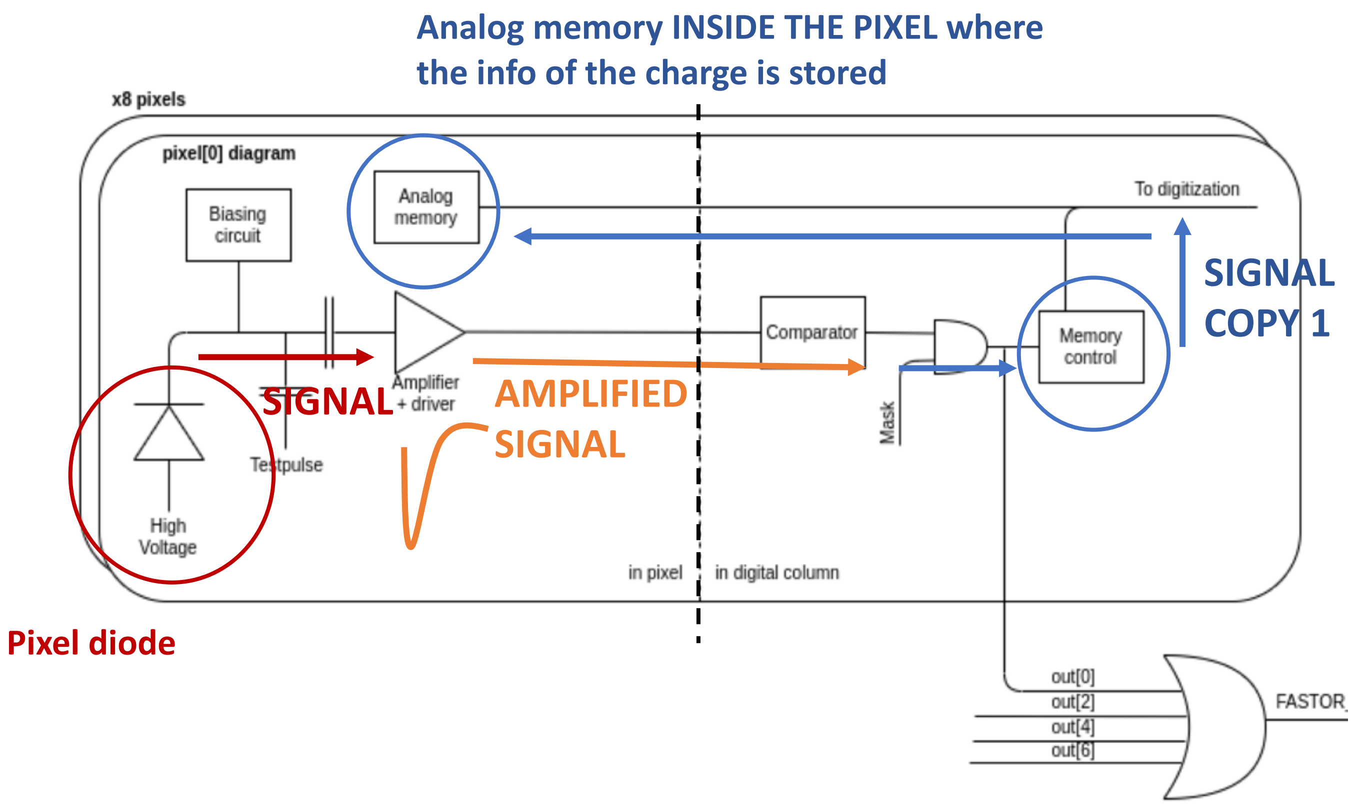
Pixel Row Structure

- When an hit arrives a signal is produced
- The signal gets amplified by the PRE-AMPLIFIER
- The signal is sent ouside the pixel to the COMPARATOR



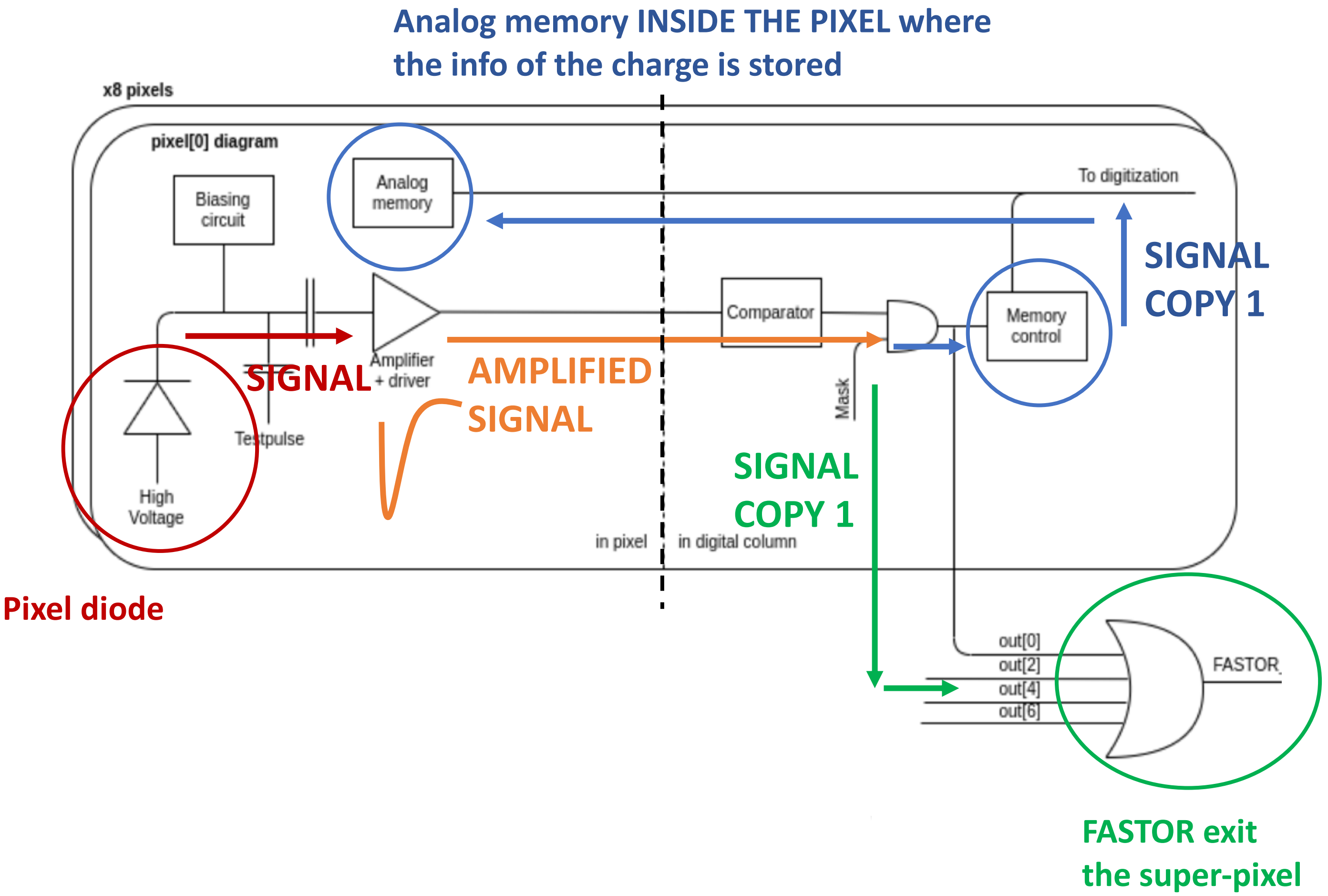
Pixel Row Structure

- When an hit arrives a signal is produced
- The signal gets amplified by the PRE-AMPLIFIER
- The signal is sent ouside the pixel to the COMPARATOR
- The output of the comparator is copied:
    - **COPY 1** goes to the MEMORY CONTROL
- **Memory Control** loads the analog memory inside the pixel if the charge is over threshold

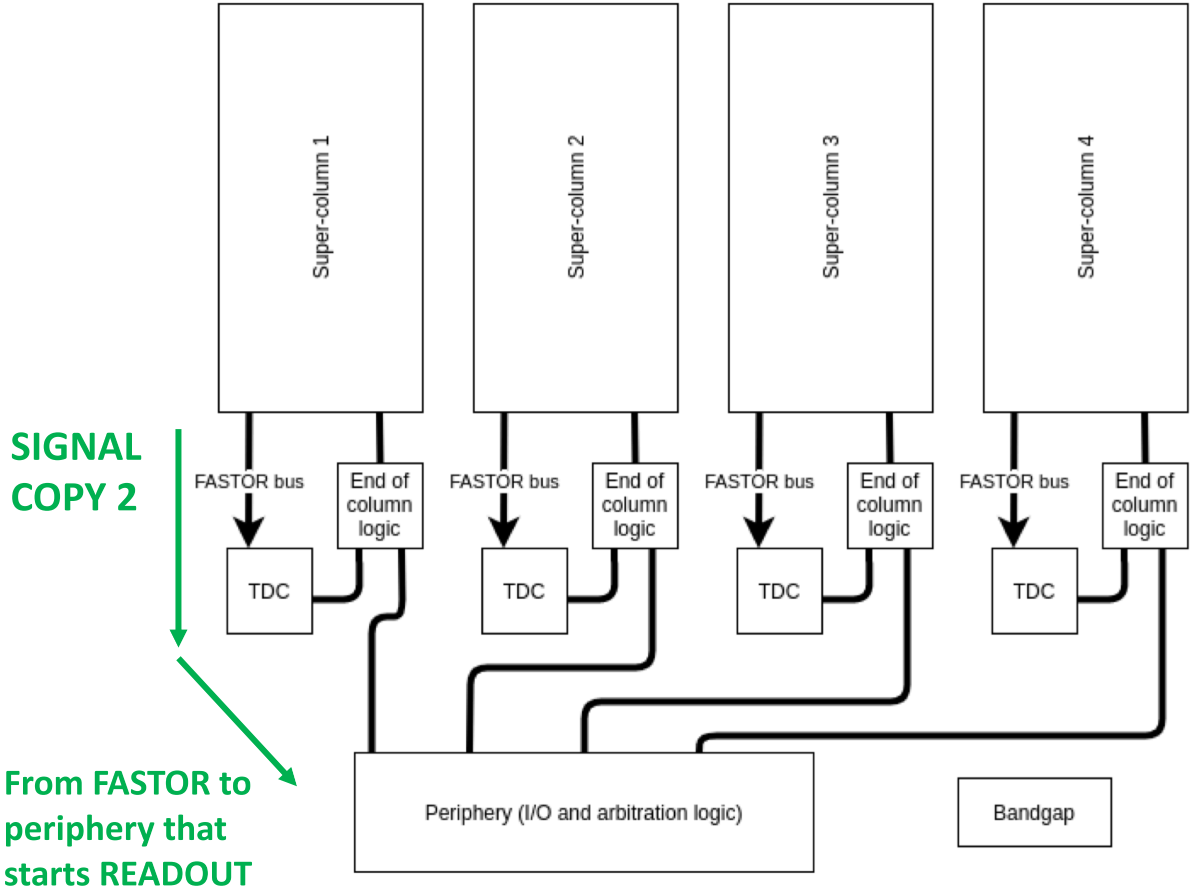


Pixel Row Structure

- When an hit arrives a signal is produced
- The signal gets amplified by the PRE-AMPLIFIER
- The signal is sent ouside the pixel to the COMPARATOR
- The output of the comparator is copied:
    - **COPY 1** goes to the MEMORY CONTROL
    - **COPY 2** goes to the FASTOR that will give the signal to start the Readout
- **Memory Control** loads the analog memory inside the pixel if the charge is over threshold

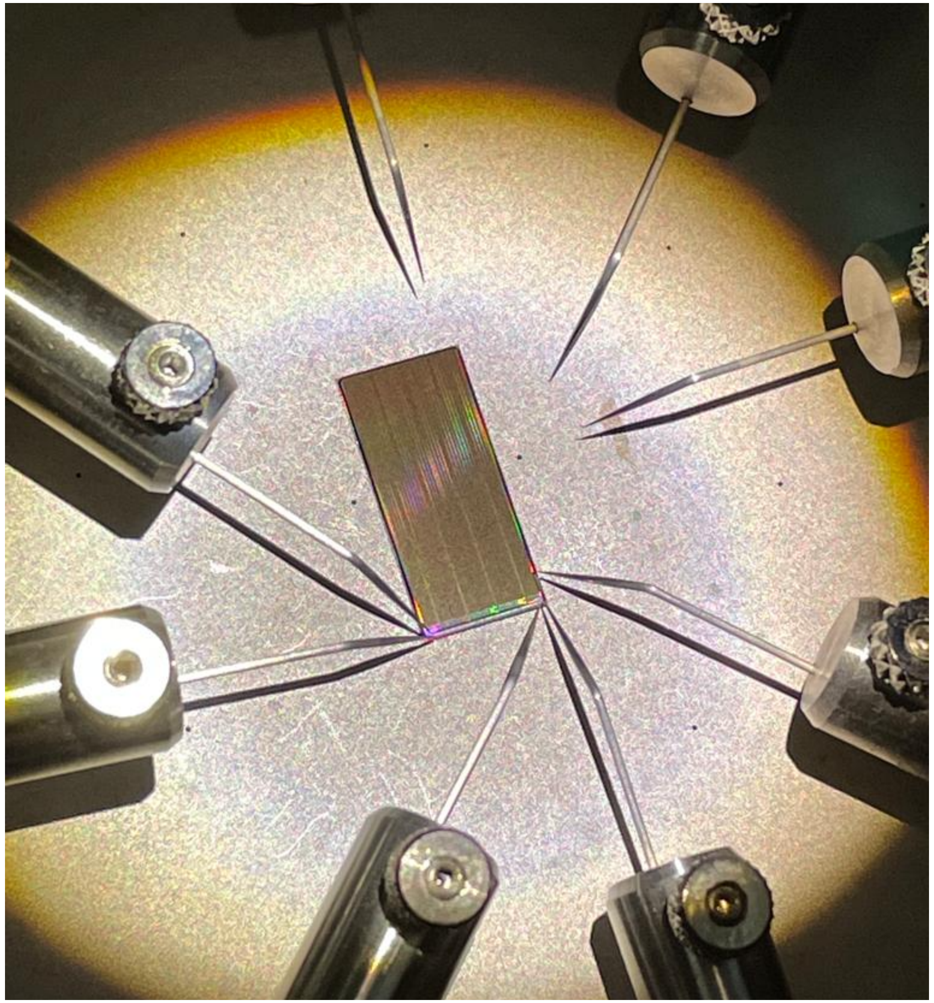


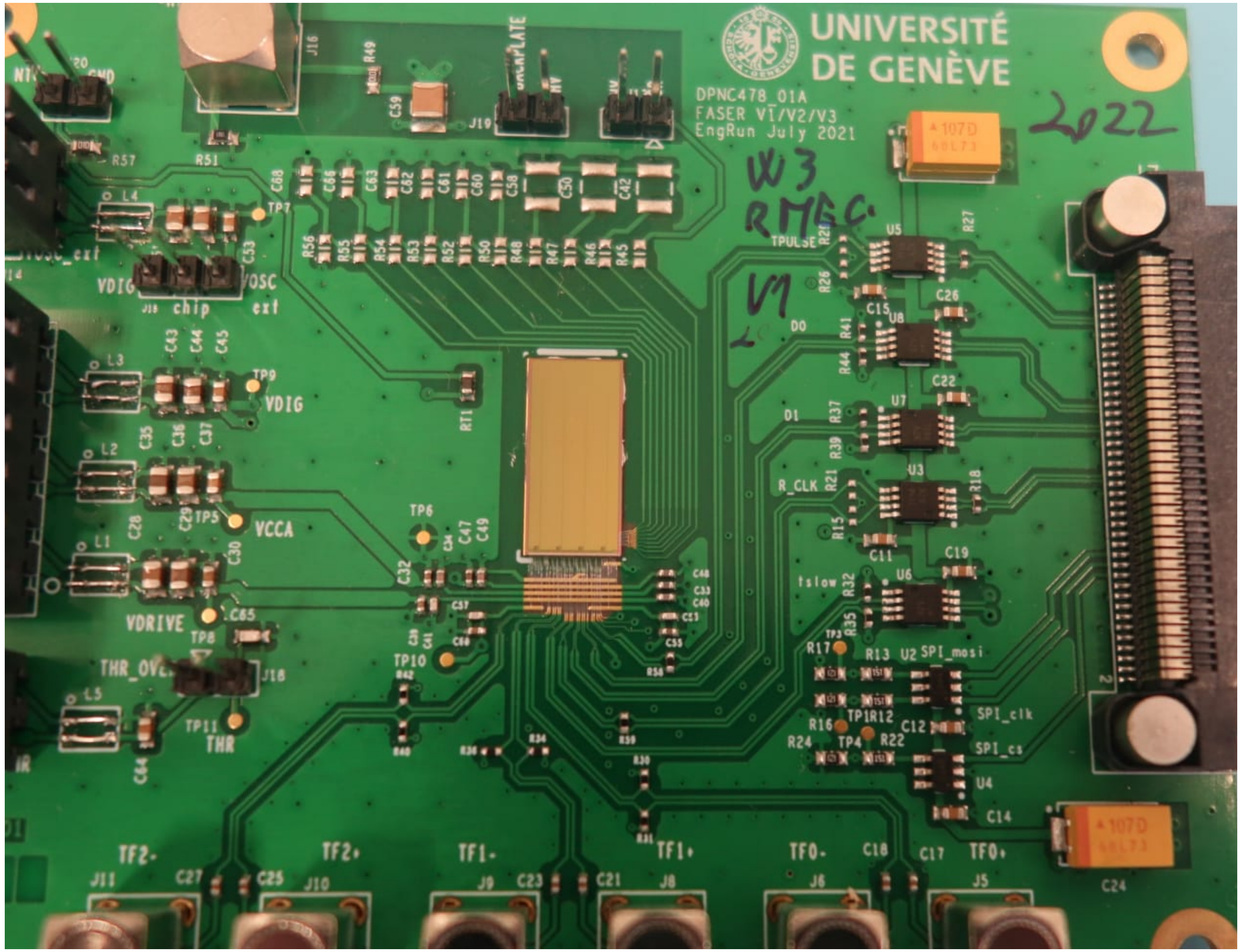
ASIC Structure and Readout



- A copy of the signal exit **IMMEDIATELY** the pixel through the FASTOR
- Each FASTOR send a signal to the perifery to start the READOUT
- To be sure we collected the charge entirely, the **perifery waits a bit before starting the READOUT**
- **Readout time max 200 µs**
- If in a super-pixel **zero FASTOR** are **active, zero bit are sent to the periphery (optimization)**

The Pre-production Chip – First Tests





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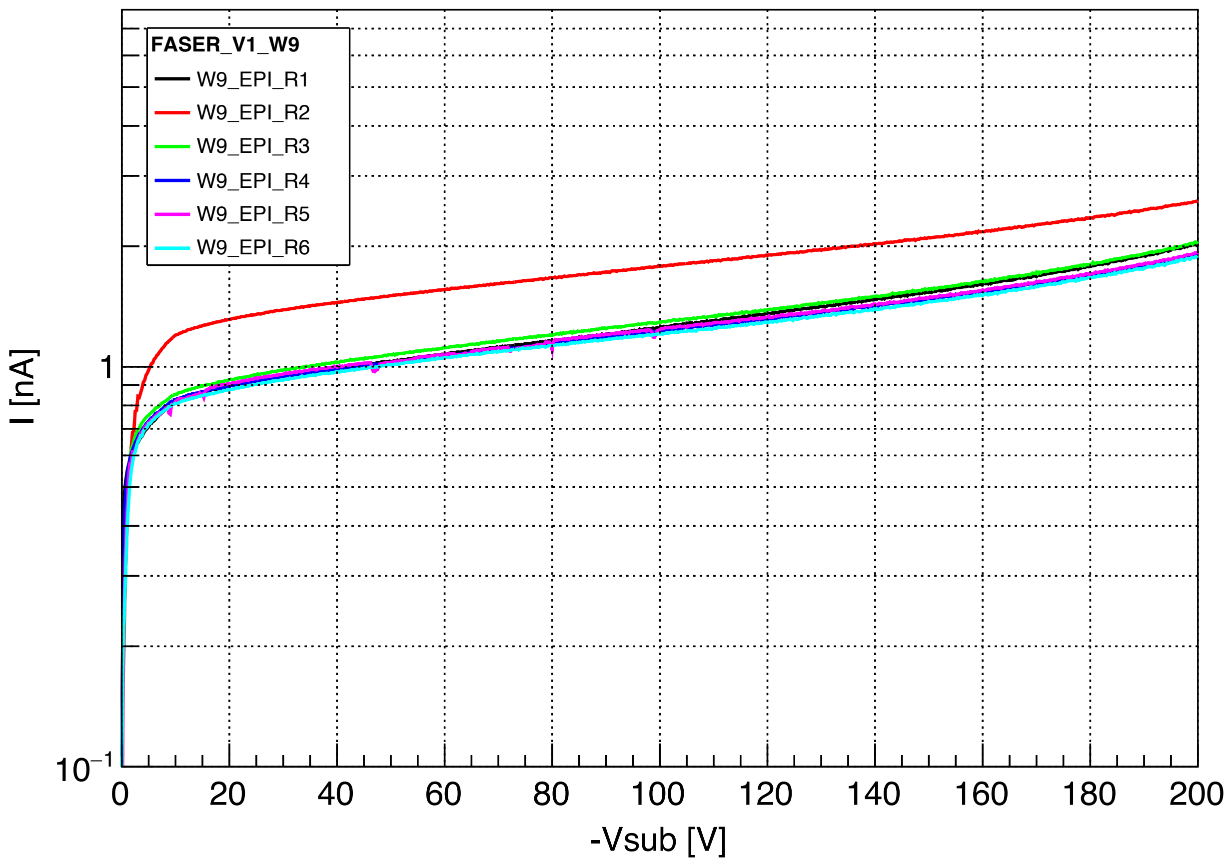
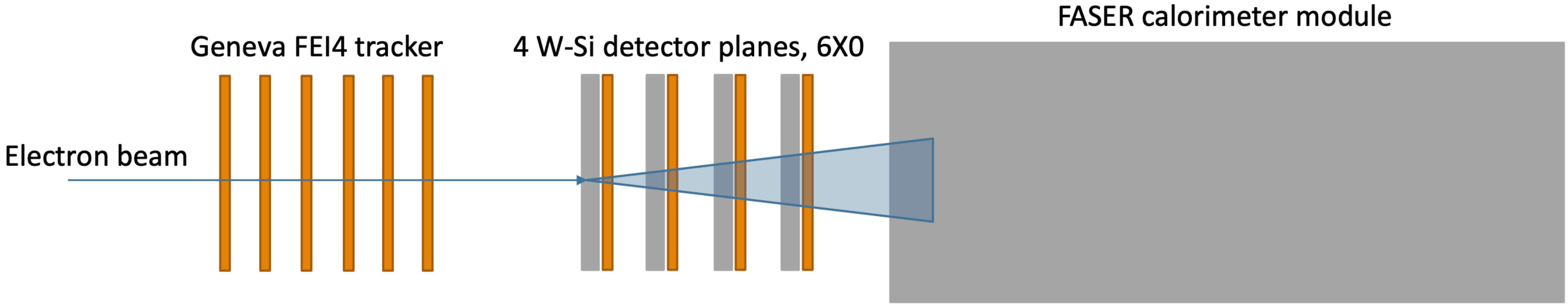


The chip can operate up to -200 V

Testbeam at SPS – H2 with electron beam

For FE-I4 Geneva Telescope:
Theo Moretti's and
Matteo Milanesio's talks
and
M. Benoit *et al.*
2016 *JINST* **11** P07003
https://doi.org/10.1088/1748-0221/11/07/P07003

- Test beam planned **end of August 2022**
- **Electron beam** with energy up to 250 GeV
- Measurement of the performance of the new FASER preshower pre-production ASIC
- **Combined performance** of the new **FASER preshower** and **FASER calorimeter module**
- Study the energy resolution and how to compensate the loss with the preshower



Summary

- New FASER preshower detector will **enable discrimination of photons** from LLPs decays

- Monolithic ASIC to distinguish clusters from **two ultra-collimated high-energy electromagnetic showers**
  - **Hexagonal pixels** with 65 μm side (≈ 100 μm pitch)
  - **Dynamic range, from 0.5 fC to 65 fC**
  - **Analog memories to store charge** information → read out many pixels at the same time

- **Test beam** with electron beam **end of August 2022**

- New pre-shower installed in ‘23/’24 winter break to **take data during LHC Run3**

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FASER

Thank you !

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BACKUP SLIDES

The LHC Forward Physics

- Most LHC detectors sensitive to transverse particles coming from head-on pp collisions
- **Large forward cross section currently wasted and not probed**

- Forward particles are **highly collimated**: only $\sim$ 1cm spread for 100 m longitudinal travel
- **A small detector far away could potentially see a large flux of Long-Lived Particles (LLPs) with very small background**

- ForwArd Search ExpeRiment
- Proposal submitted in 2018 and approved by Cern in March 2019

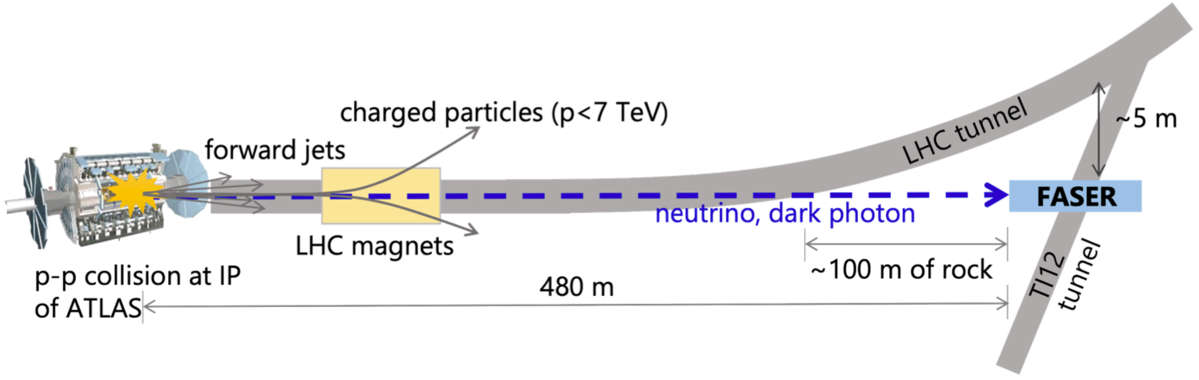
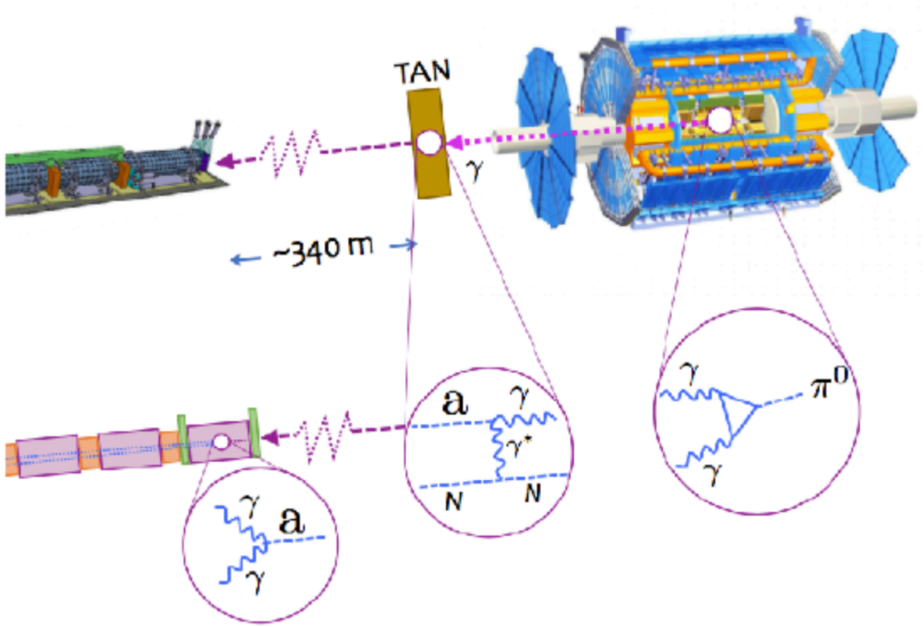
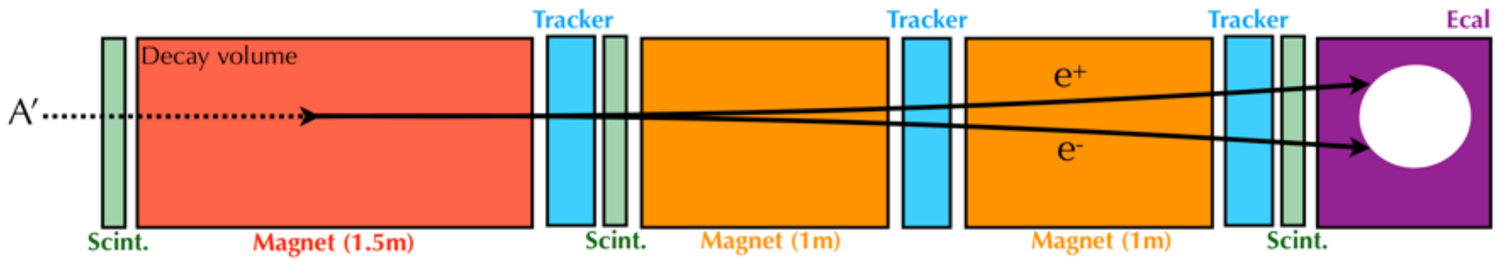


Figure: Location of FASER in the tunnel - schema is not in scale.

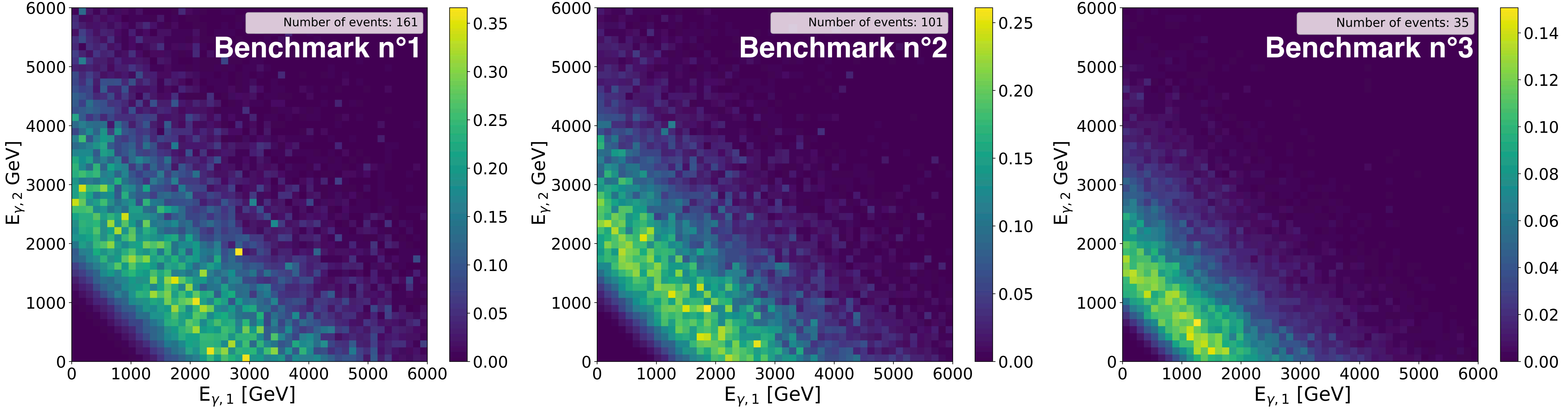
Primakoff Process

- ALPs can decay in two photons via $a\gamma\gamma$ coupling
  - Photons in the TeV range are produced at ATLAS IP
  - Collide with the TAN particle absorber
  - The ALPs are produced (via e.g. the Primakoff process)
  - ALPs decay to photon-pair within the FASER volume
  - The photons will then produce an electromagnetic shower



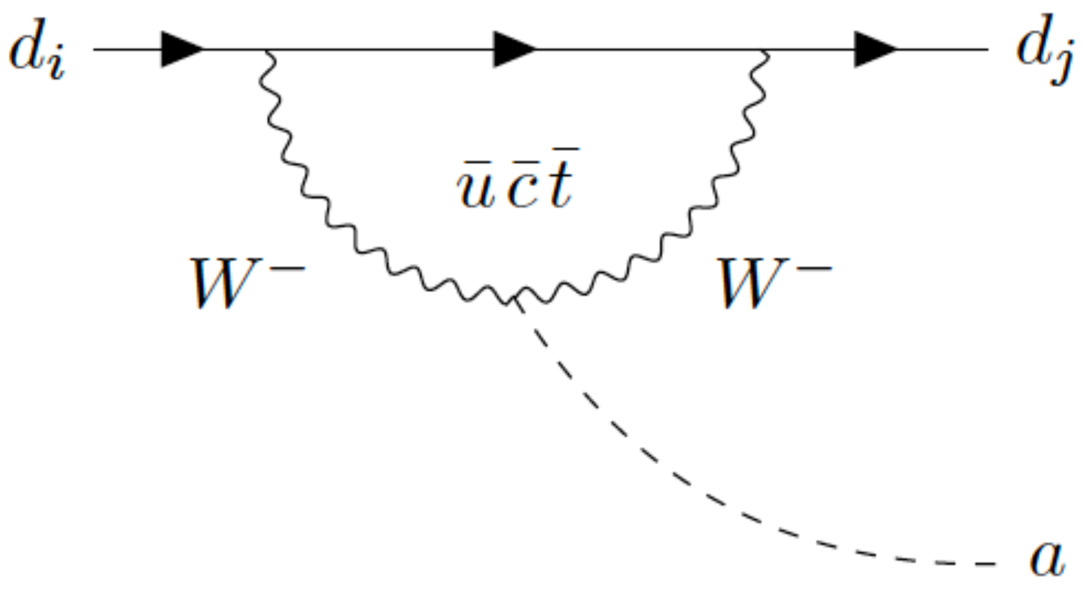


Di-photon Signal Energy Distributions



ALPs Production - FCNC

- Down type quark becomes an up type quark
- Emits a charged boson which will itself radiate an ALP
- It then interacts with the up type quark which changes flavor again to become a down type quark

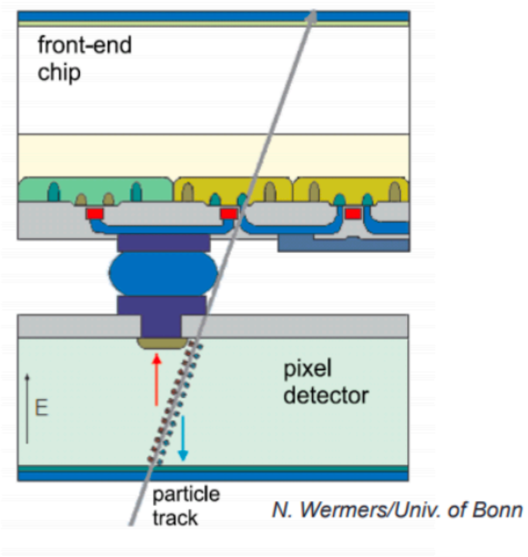


Hybrid VS Monolithic Pixel Detectors

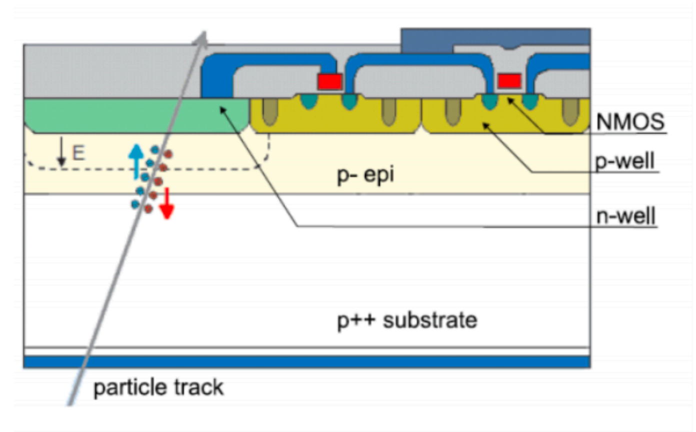
ATLAS

FASER

Hybrid Pixel Detector



Monolithic Pixel Detector (example)



cost ratio

Readout chip : sensor chip : bump bonding ≅ 1:2:7

PROS: better optimization of sensors and electronics

CONS: generally high production costs

Sensor integrated in the readout, **only CMOS processing**

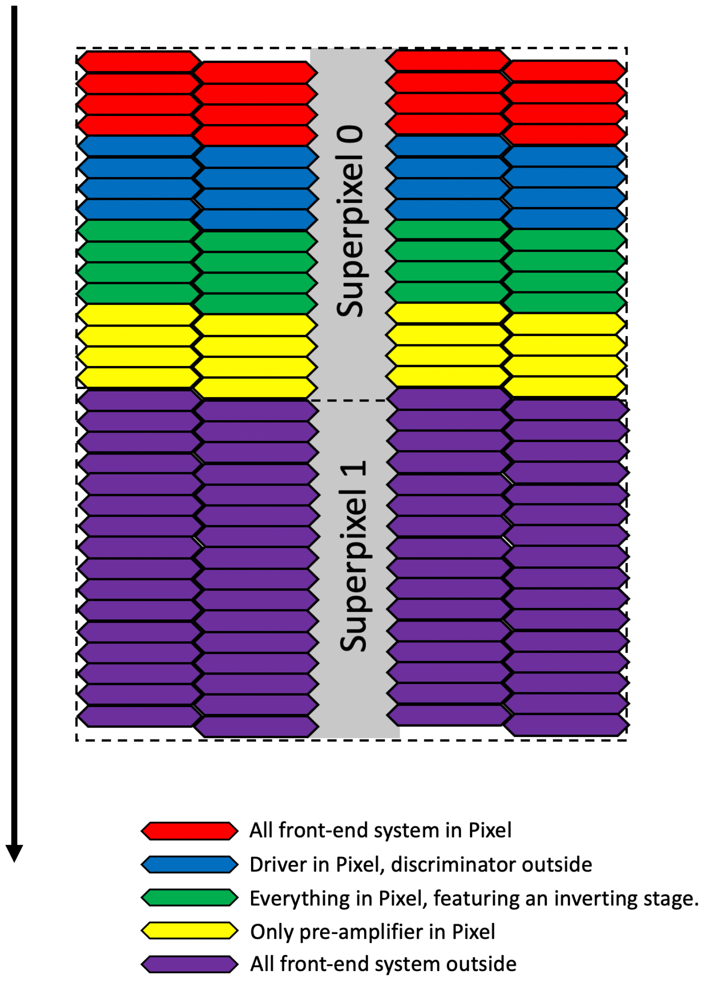
PROS: lower production costs

CONS: more difficult design

Prototype0 Results and Comments

Configuration	σ_v [mV]	G_c [mV/fC]	ENC [e$^-$]	$\sigma_{V_{th}}$ [mV]
All f.e. outside pixel	4.2 ± 0.2	159 ± 1.0	165 ± 9	32.3
Only pre-amp. in pixel	2.5 ± 0.1	96.8 ± 0.5	161 ± 9	26.9
All f.e. in pixel, inv. stage	6.9 ± 0.5	179 ± 1.0	241 ± 19	30.8
Pre-amp. and driver in pixel	3.8 ± 0.2	133.7 ± 0.6	178 ± 9	23.4
All f.e. in pixel	5.4 ± 0.4	148 ± 1.0	228 ± 20	27.1

	Advantages	Disadvantages
All outside the pixel	1. Low ENC due to amplifiers 2. High gain due to low capacitance	1. Large dead area 2. Bad scaling
Amplifier inside	1. Low ENC	1. Low gain due to amplifier + driver coupling 2. Bad scaling
Inverting stage	1. Highest gain	1. Worse ENC 2. Additional line for inverting stage
Amplifier + driver inside	1. Good compromise	
All inside	1. Best use of pixel area	1. Largest ENC (but still acceptable)



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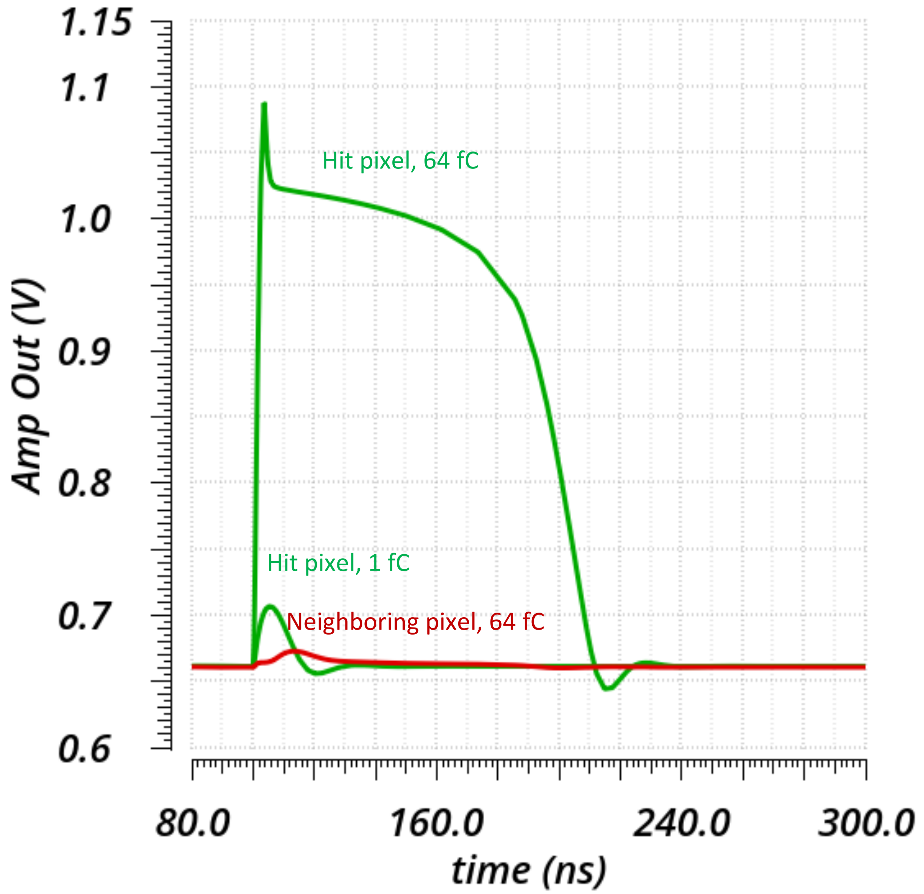
2021 *J. Inst.* **16** P12038
https://doi.org/10.1088/1748-0221/16/12/P12038

Signal Routing and Crosstalk Suppression

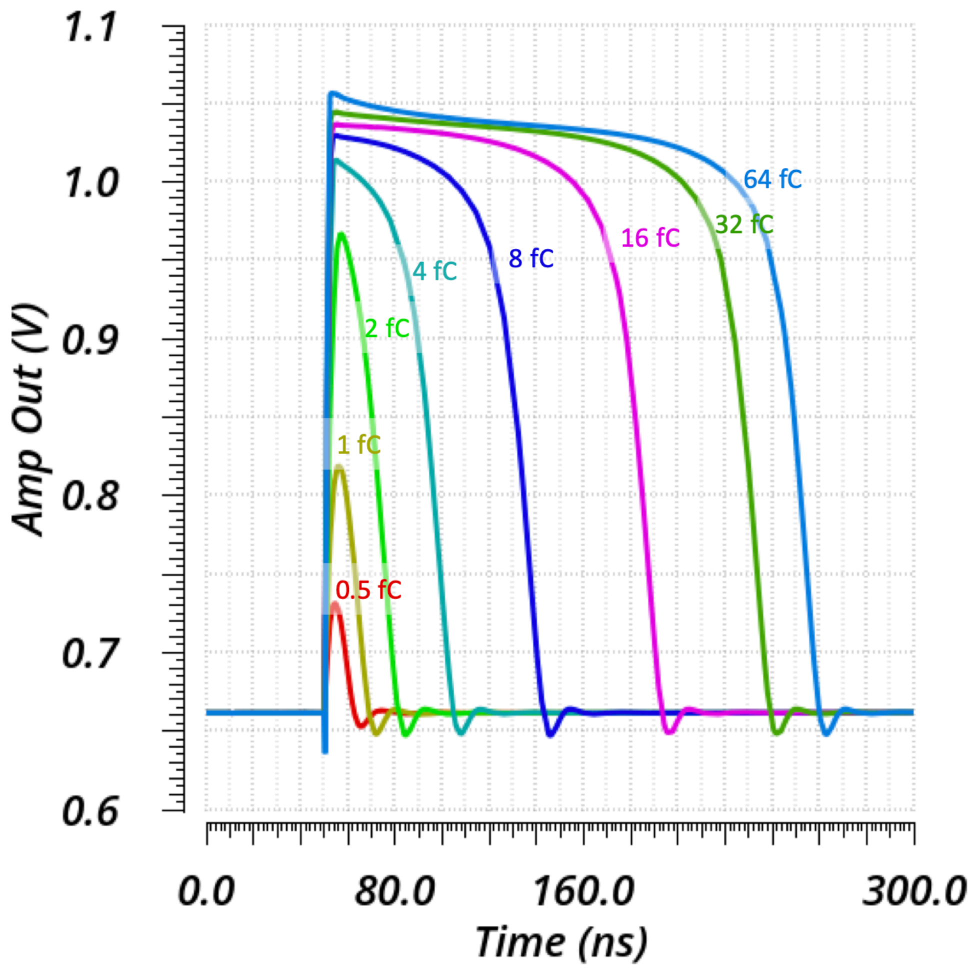
- Signal routed in a **shielded bus** to **minimize crosstalk between neighboring pixels**
- Big signal produced by a 64 fC charge (in green)
- Signal induced in the neighbouring pixel (in red)
    - **Crosstalk is supressed but not eliminated**
    - The signal produced by a 1 fC charge is small but still bigger than the induced signal
    - Threshold set accordingly to 0.5 – 1 fC



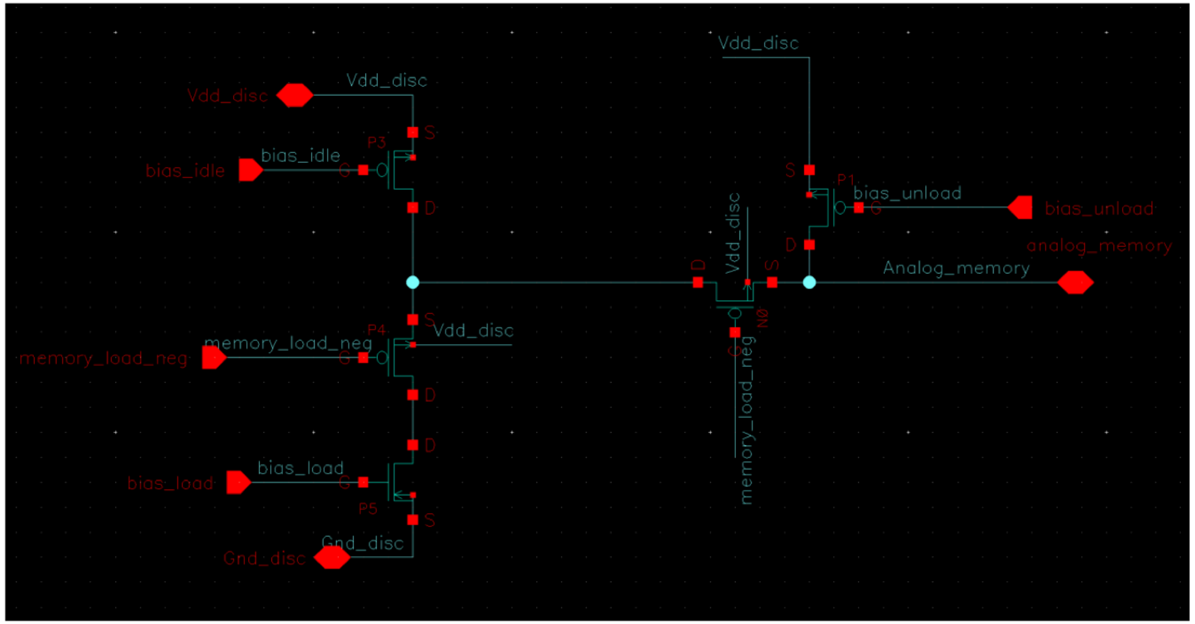
Amplification Stage

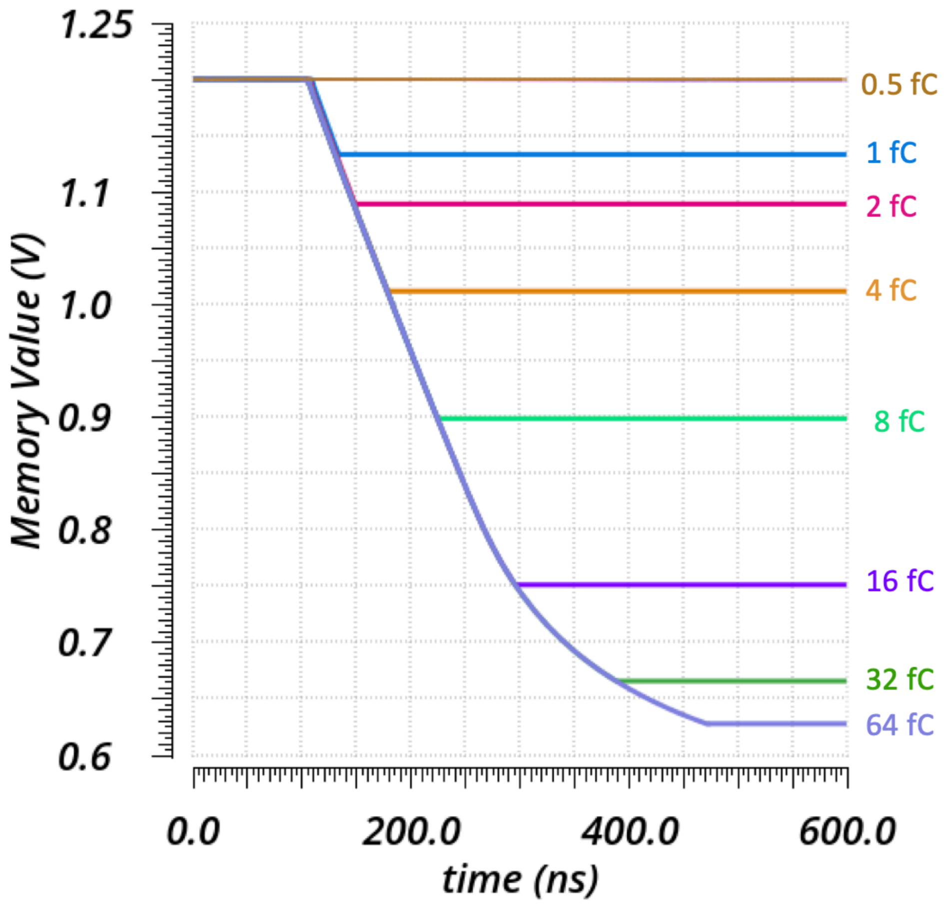
- Since we want to measure high charges we convert the charge information to Time Over Threshold
- **For different charges, if the charge increases also the TOT increases but not linearly (almost logarithmic relation)**
- **Saturation at 64 fC (intrinsic saturation of the pixel)**

Simulation data



Memory Control and Analog Memories





- Current leakage even if the switch is opened. It takes 200 µs to degradate the memory value of 30 mV (= 1 bin of our ADC).

After 200 µs we still measure something but we are less precise

Di-Photon Reconstruction Efficiencies

$E_{\gamma 1}$= 1 TeV
$E_{\gamma 2}$= 1 TeV