ACEOLE Project

Data Acquisition, Electronics, and Optoelectronics for LHC Experiments

José Pedro Cardoso

Biography

Age: 37
Nationality: Portugese
Education: M.Sc in Electrical and Computer Engineering
B.Sc in Electronics and Telecommunications Engineering
Interests: IC Design, Software Design, Microcontrollers, Computer Networking and Linux
Fellow since: 1st of June 2009

Near Future

With ACEOLE Marie Curie's Programme, I had the opportunity to work at CERN and get access to a high level education and training, such as : MEAD courses, Conference's Courses and PhD. After this 3 year step, I will be ready to face the market with highly increased technical background, that prepared me to become a team leader, sharing my knowledge with younger researchers.

Project

The goal: Auto-Calibration Self-Test Low-Phase Noise Radiation Tolerant PLL.

A set of robust ASIC building blocks and functions need to be developed to meet the requirements of front-end electronics and detector readout systems of future experiments upgrades of the existing detectors. The project aims to design, characterize and qualify one or more low-power, ASIC building blocks or functions using a new commercial 130 nm CMOS technology. These circuits shall adopt structural and functional radiation tolerant design techniques in order to make them robust to total dose and single event phenomena. Modern microelectronic CAD tools and mixed-signal, semi-custom and full-custom VLSI design methods will be adopted in the design of a radiation tolerant Phase-Locked Loop (PLL) with very low phase noise characteristics. The device will be part of a future Timing Trigger and Control system for SLHC and it will be used, amongst other applications, to drive high speed transceivers, high precision digital-to-analogue converters and high resolution time-to-digital converters.

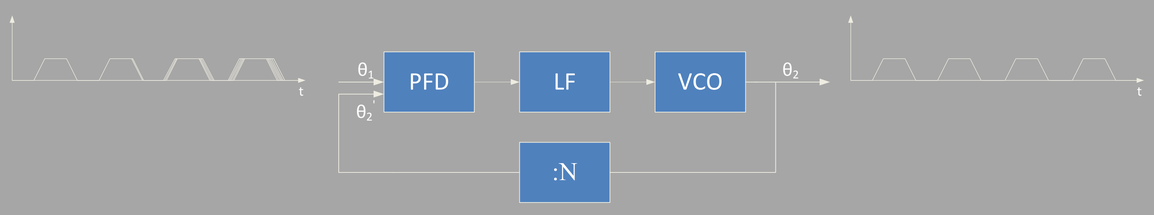
Work

The main circuit will be divided into two major parts:
- **PLL** (Phase Frequency Detector, Loop Filter, VCO, Prescaler, Lock detector and Automatic Oscillation Amplitude Control)
- **Testing Blocks** (Calibration, Frequency Measurement, Jitter Measurement, Fuse Bank and controller), which are a part of a Built-In Self Test (BIST) structure

PLL

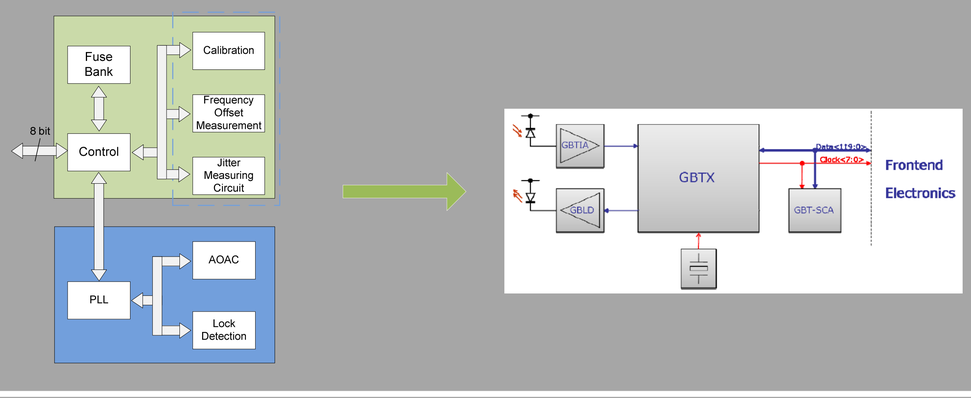
Phase Locked Loop (PLL) is a circuit, which compares the phase of an input signal (reference signal) with the signal generated by the internal *Voltage Controlled Oscillator* (VCO). The PLL includes Lock Detection and Automatic Oscillation Amplitude Control.

How does it work ?
- A jittered signal is applied to the PLL
- The PLL will act as a filter for the noisy input signal, maintaining the phase error constant.
- An output clock signal is thus obtained that tracks the average or the input signal phase but displays very low phase noise.



BIST

The functions performed by the BIST structure are the following:
- Calibration – Auto-Calibration of the PLL and Re-Calibrate when needed
- Frequency Offset Measurement – deviation's detection on the central frequency
- Jitter Measurement – measures the jitter of a desired signal



Status

- The Design of a Low-Phase Noise VCXO to be integrated on the PLL has already started
- Until the end of the year all the main blocks will be finished:
  - *Phase Locked Loop*
  - *Testing Circuitry*
  - *Fuse Bank*
- This circuit will be integrated on the GBTX project, which will do its tape-out during January 2011

Training

- On-Job Training

State-of-the-art, Cadence software training and Matlab Modelling of a PLL

- Technical Training

- 29th of June - 1st of July 2009 - "PLLs, VCOs and Frequency Synthesizers", MEAD's course organized by Ecole Polytechnique Fédérale de Lausanne (EPFL),
- 14th of September 2009 - Short-course, during ESSCIRC 2009, on "Nanoscale CMOS analog design from devices to system".

Other

"Leaders in Science" – Self-Confidence Building Trainning

EUROTRAINING

Secondment

PhD in "Electrical and Computer Engineering"

Institution: "Faculdade de Engenharia da Universidade do Porto" (FEUP)

The doctoral program is divided as follows:
- one year of courses
- two years of research

First year
- "Microelectronic and Microelectromechanical technologies
- "Test and Design for Testability
- "Digital Communications Systems
- "Seminars

Universidade do Porto FEUP Faculdade de Engenharia

TRAINING FOR EUROPE
13 – 17 SEPTEMBER 2010

This research project has been supported
by a Marie Curie Early Initial Training Network Fellowship
of the European Community's Seventh Framework Programme
(PITN-GA-2008-211801-ACEOLE)

CERN MARIE CURIE ACTIONS PEOPLE