ACEOLE Project

Data Acquisition, Electronics, and Optoelectronics for LHC Experiments

Timo Tick

Work package 1:

Pixel Detector Systems for Particle Tracking and Imaging

Biography:

Age: 31
Nationality: Finnish
Education: D.Sc. (engineering)
Fellowship: 1.12.2008 – 31.11.2011

Training:

On the job training: Integrated Circuit (IC) fabrication techniques, wafer level packaging technologies and flip chip bonding techniques training at VTT Micronova silicon processing facility in Espoo, Finland
Training in silicon pixel detector technology, detector read out electronics design as well as thermal simulation training at CERN

Conferences: Electronics Components and Technology Conference 2009 (ECTC), San Diego, California.
Topical Workshop for Electronics in Particle Physics 2010, Aachen, Germany

Languages: French courses at CERN

General description of work:

Background:

CERN has developed pixel detectors for high-precision measurement of particle tracks in experiments at the LHC and other domains such as medical imaging and materials analysis. Key technological challenges in the development of next generation detectors are:

- Reduction of the thickness of the detector material, as this material distorts the physics interactions
- Development of low-cost interconnection techniques to allow covering of large areas with hybrid pixel detector arrays

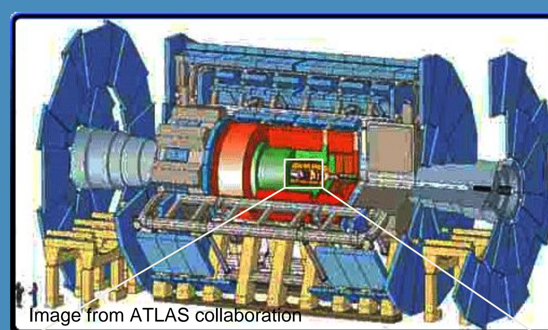


Image from ATLAS collaboration

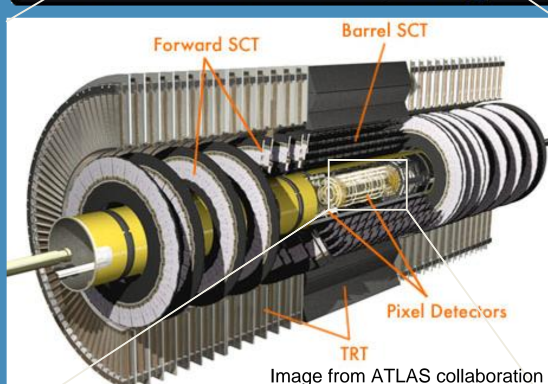
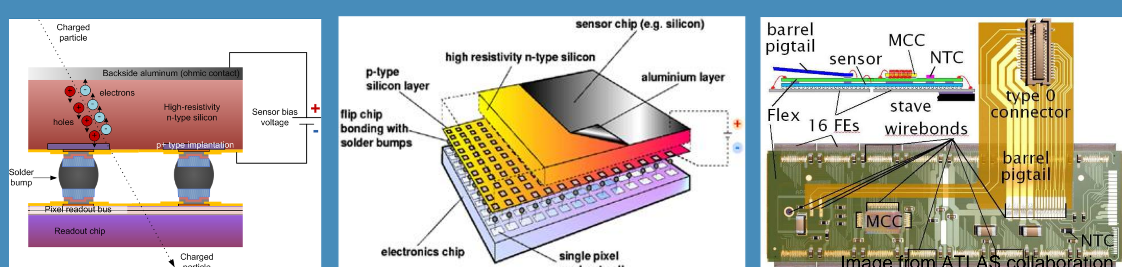


Image from ATLAS collaboration

Objectives:

- Study of moderately large area Pixel detector tIling solutions
- Design of low-mass detector assemblies suitable for tiling moderately large areas of pixel arrays
- Construction and evaluation of demonstrator assemblies implementing the most promising tiling solutions for particle tracking and/or photon counting applications



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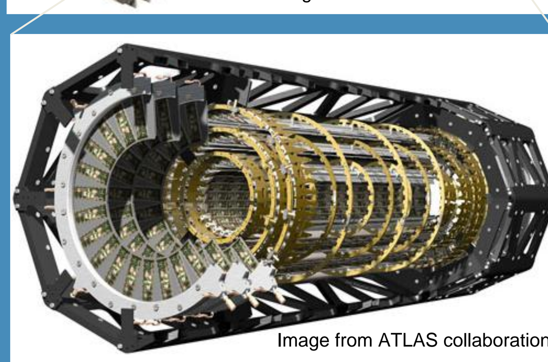
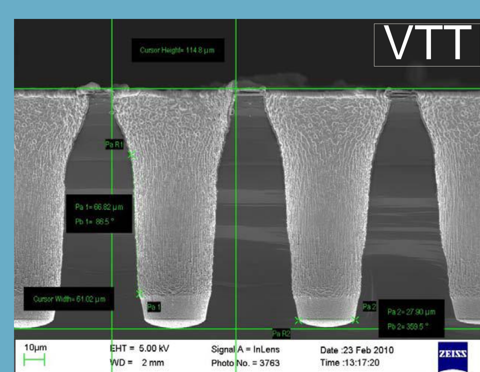


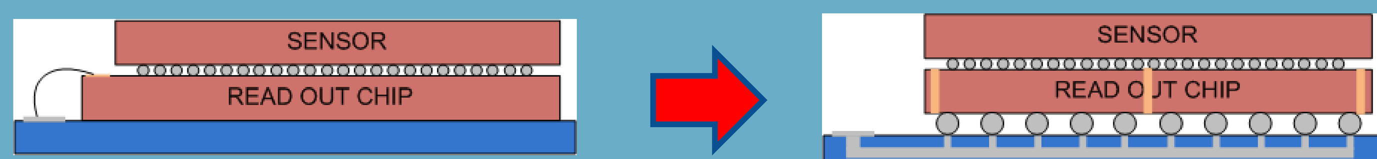
Image from ATLAS collaboration

Specific description of work:

Through Silicon Via (TSV) process development:

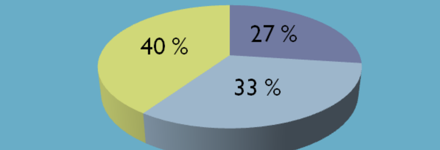
- TSV is an electrical contact between the front (active) side and the back side of a silicon chip
- The use of TSV's will allow large area seamless tiling of pixel detector chips
- Joint development project with ACEOLE partner VTT with a goal to develop a TSV process that is suitable for HEP detector chips

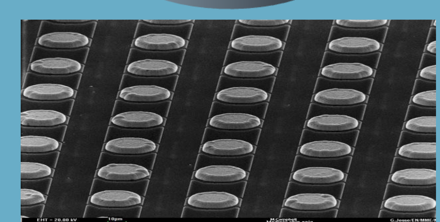




Development and evaluation of low cost wafer bumping and bonding technology:

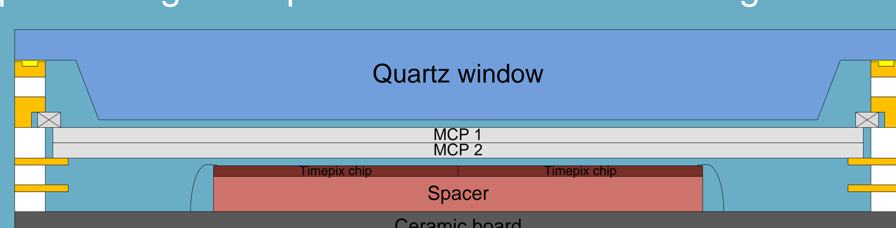
- Hybrid pixel detector consists of a Read Out Chip (ROC) and a Sensor Chip (SC)
- Every pixel of the SC is connected to corresponding read out circuitry on ROC with micro solder bumps (~ 20 μm) with Flip Chip (FC) bonding
- Current bump fabrication technology is too expensive for the volumes typical to HEP detector projects
- Goal of the project is to identify and evaluate low cost techniques for wafer bumping and FC bonding
  - Identifying potential industrial partners – creating a supply network
  - Evaluating their processes/equipment

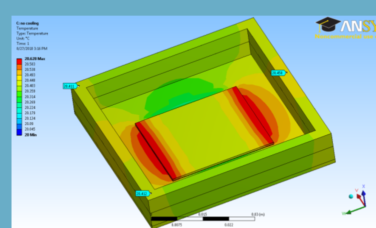




Micro Channel Plate Hybrid Photon Detector (MCP-HPD) prototype for Medipix collaboration:

- Goal of the project is to build a Hybrid Photon Detector (HPD) prototype that uses Timepix chips, is tileable with high sensitive area fraction and can be used to for performance evaluation
- Prototype is designed to use processes and technology that are compatible with the image intensifier industry manufacturing lines
- Potential applications: Cherenkov ring imaging and adaptive optics sensor
- Engineering challenges are the compatibility of materials and processes to vacuum processing and operation and thermal management





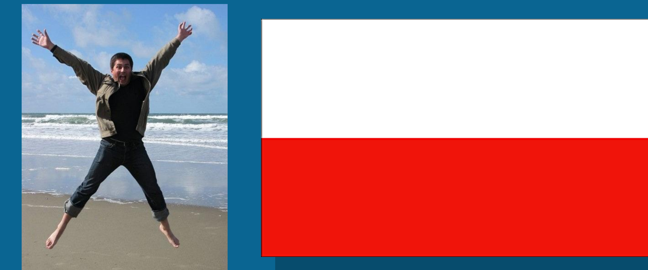
Michał Bochenek

Work package 3:

On-detector Power Management Schemes

Biography:

Age: 27
Nationality: Polish
Education: M.Sc. in nuclear physics, Ph.D. (in progress)
Fellowship: 1.10.2008 – 30.09.2011

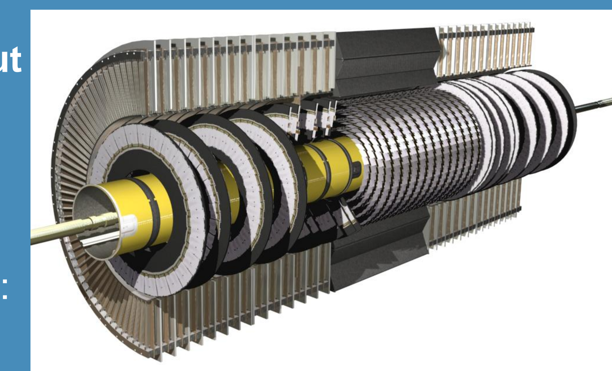


Training:

- Hardware:
  - Operational Amplifiers: Theory & Design; TU Delft, Delft, The Netherlands
  - Adaptive Power Management; San Francisco, CA, United States
  - Low-voltage and Mixed Signal CMOS Circuit Design; San Francisco, CA, United States
  - EIROforum School of Instrumentation; CERN, Geneva, Switzerland
  - Low-Power, Low Voltage Analog IC Design; EPFL, Lausanne, Switzerland
- Software:
  - Introduction to Analogue IC Design: Schematic entry and simulation; RAL, United Kingdom
  - Introduction to Analogue IC Design: Layout and post layout verification; RAL, United Kingdom
- Conferences and workshops:
  - International Solid State Circuits Conference (ISSCC); San Francisco, CA, United States
  - TWEPP-09 Topical Workshop on Electronics for Particle Physics; Paris, France
  - TWEPP-10 Topical Workshop on Electronics for Particle Physics; Aachen, Germany
- Languages:
  - French courses

General description of work:

After the LHC luminosity upgrade, **the number of front-end readout channels** in the ATLAS Semiconductor Tracker **will be increased** by one order of magnitude. Therefore, a **new solution** for powering the readout electronics **has to be elaborated**.



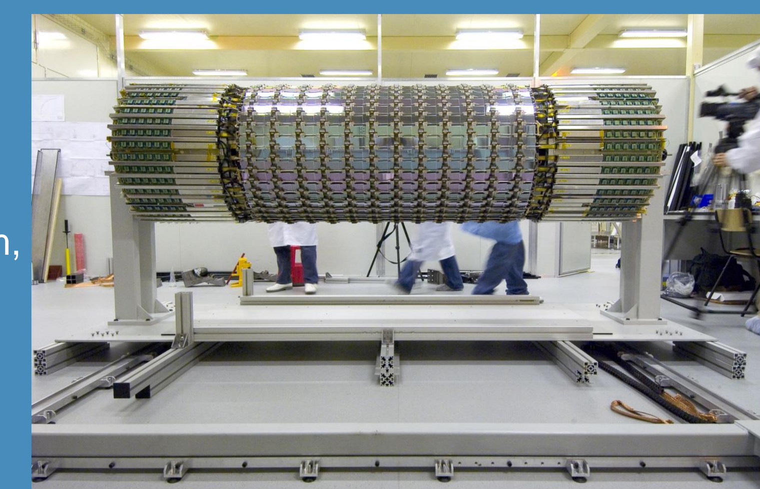
Two main approaches for power distribution under development are:

- the **serial powering** of a chain of modules,
- the parallel powering scheme using **DC-DC conversion**.

In either case switched-capacitor converters on the front-end chips will be needed!

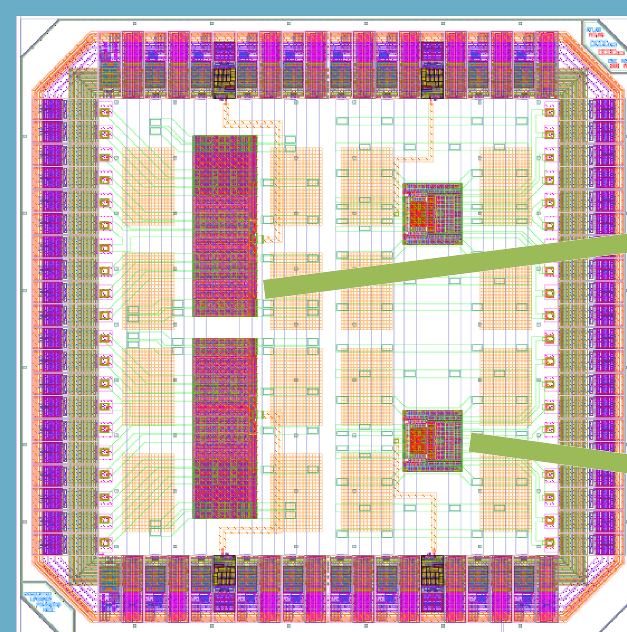
Objectives:

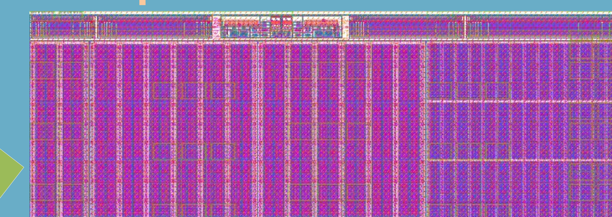
- Design a prototype building block for the powering system,
- Check its electrical, functional and radiation characterization,
- Integration of the optimized building block into the full tracker demonstrator ASIC and then the tracker demonstrator module



Specific description of work:

Switched capacitor DC-DC converter design:





The 2x2 mm^2 "DCDC013" chip consists of four switched capacitor DC-DC converters:

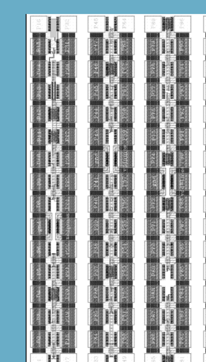
- Two voltage doublers,
- Two step-down converters.

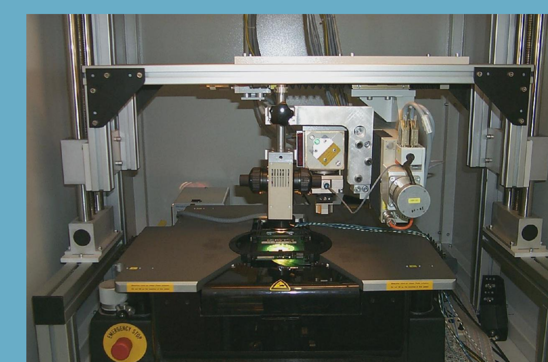
Designed in the IBM CMOS 130nm technology

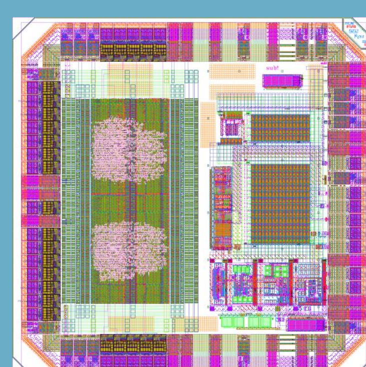
Irradiation tests of the CMOS devices at room and low temperature:

TID90 and **TID3** are the test chips, designed to evaluate the radiation tolerance of **90 nm** and **130 nm** technology for high energy physics applications.

The chips contain of individual **transistors**, **resistors** and **parasitic elements,** which allow for monitoring the **degradation induced by radiation**.







Assembly of the SEULogic chip:

The 2x2 mm^2 "SEULogic"chip consists of two main parts:

- Shunt regulator for the serial powering scheme,
- Purely digital part (will be used for testing 130 nm design kit digital flow).

Designed also in the IBM CMOS 130nm technology

TRAINING FOR EUROPE

13-17 SEPTEMBER 2010

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