

Analog FE ASIC

Upgrade of the front end electronics of the
LHCb calorimeter

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Calorimeter upgrade meeting – CERN – October 5th 2010

- I. Introduction
- II. Preamplifier
- III. Channel architecture
- IV. Technology issues
- V. Status and plans

I. Introduction: what's new ?

- If everybody was at the last meeting
 - This could be the last slide
 - Else
 - We'll go through the talk and come back at the end
- After first prototype submission and last meeting (22th June)
 - Design documentation
 - Test preparation (see Edu's talk)
 - Some thinking on alternatives to clipping
- Informal discussion with M. Newcomer at TWEPP
 - LAPAS chip for ATLAS LAr calorimeter
 - Interested in our design
 - They will include the scheme on a comparative between different CMOS and BiCMOS topologies (Student work)

I. Introduction: requirements

- Requirements as agreed during last year (PM gain 1/5):

	Value	Comments
Energy range	0-10 GeV/c (ECAL) Transverse energy	1-3 Kphe / GeV Total energy
Calibration	4 fC / 2.5 MeV / ADC cnt	4 fC input of FE card: assuming 25 Ω clipping at PMT base 12 fC / ADC count if no clipping
Dynamic range	4096-256=3840 cnts :12 bit	Enough? New physic req.? Pedestal variation? Should be enough
Noise	$\ll 1$ ADC cnt or ENC < 5 -6 fC	< 0.7 nV/ $\sqrt{\text{Hz}}$ \longrightarrow
Termination	50 \pm 5 Ω	Passive vs. active
AC coupling	Needed	Low freq. (pick-up) noise
Baseline shift Prevention	Dynamic pedestal subtraction (also needed for LF pick-up)	How to compute baseline? Number of samples needed?
Max. peak current	4-5 mA over 25 Ω 1.5 mA at FE input if clipping	50 pC in charge
Spill-over correction	Clipping	Residue level: 2 % \pm 1 % ?
Spill-over noise	\ll ADC cnt	Relevant after clipping?
Linearity	$< 1\%$	
Crosstalk	$< 0.5\%$	
Timing	Individual (per channel)	PMT dependent

See talk about noise in June's meeting:

<http://indico.cern.ch/materialDisplay.py?contribId=1&sessionId=0&materialId=slides&confId=59892>

I. Introduction: active line termination

- Electronically cooled termination required:

- 50 Ohm noise is too high
- e. g. ATLAS LAr (discrete component)

- Common gate with double voltage feedback

- Inner loop to reduce input impedance preserving linearity and with low noise
- Outer loop to control the input impedance accurately

$$Z_i \approx \frac{1/g_{m1}}{G} + R_{C1} \frac{R_1}{R_1 + R_2}$$

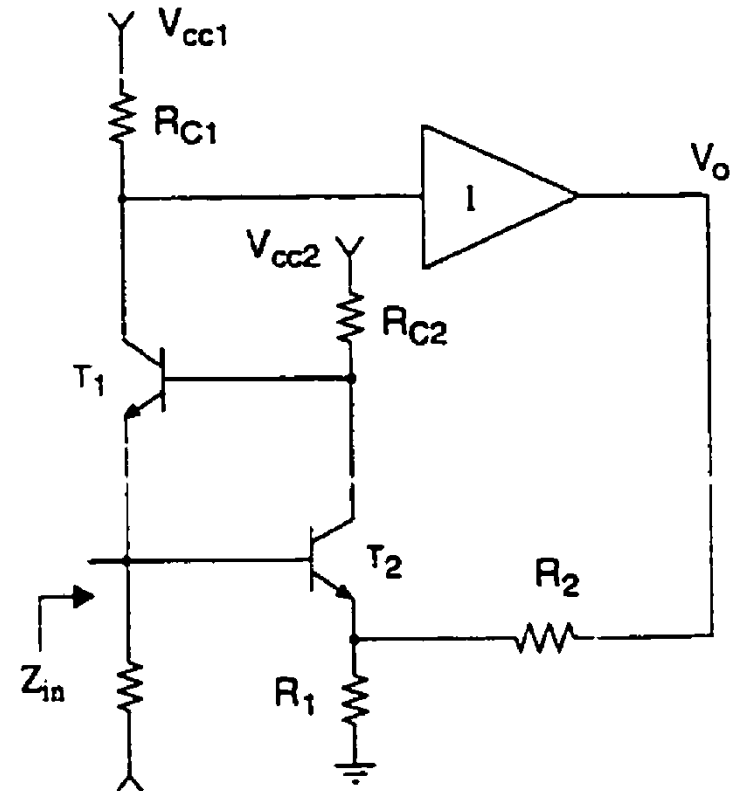
- Transimpedance gain is given by R_{C1}

- Noise is $< 0.5 \text{ nV}/\sqrt{\text{Hz}}$

- Small value for R_1 and R_2
- Large g_{m1} and g_{m2}

- Need ASIC for LHCb

- 32 ch / board: room and complexity



I. Introduction: LAPAS chip for ATLAS LAr upgrade

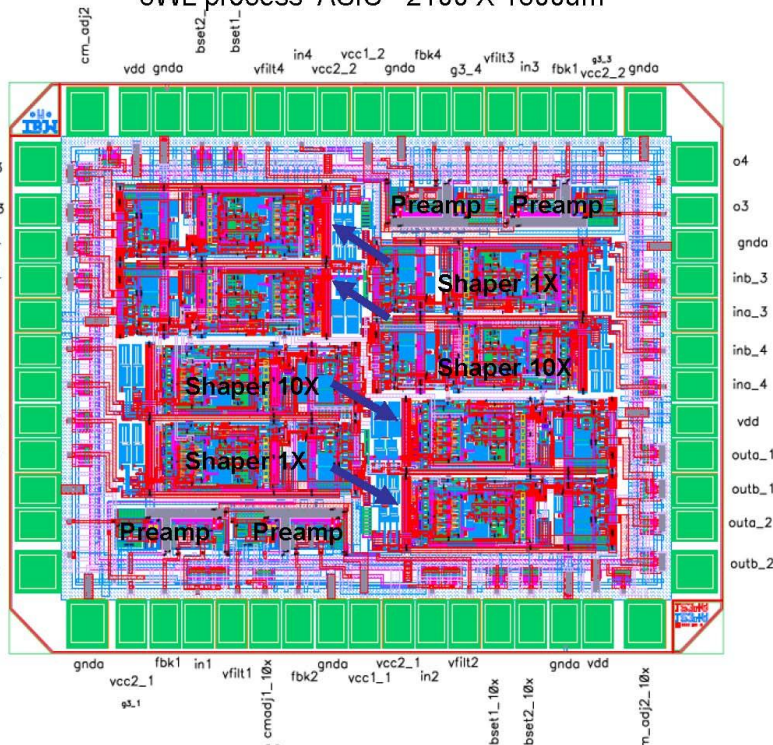
- TWEPP 09

LAPAS: A SiGe Front End Prototype for the Upgraded ATLAS LAr Calorimeter

Mitch Newcomer

On Behalf of the ATLAS LAr Calorimeter Group*

LAPAS: Liquid Argon PreAmplifier Shaper
8WL process ASIC 2100 X 1800um

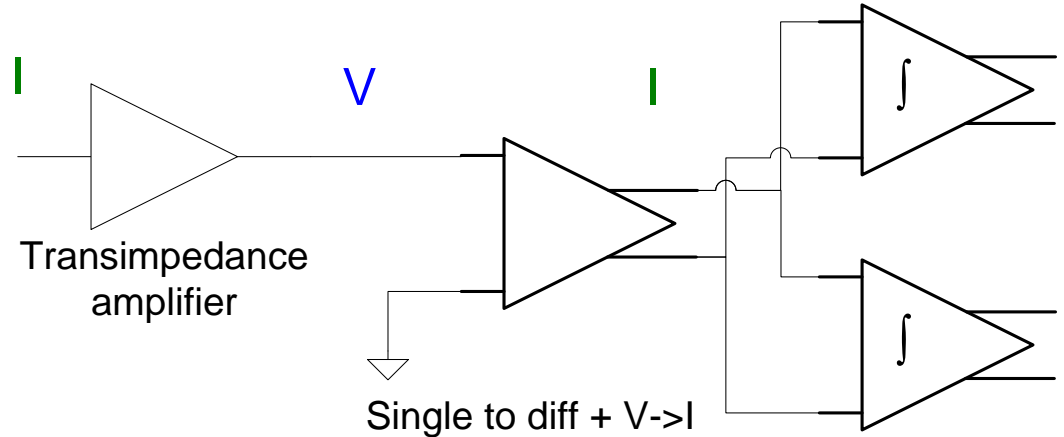


Special Acknowledgment of the significant contributions of Emerson Vernon, Sergio Rescia (BNL) and Nandor Dressnandt (Penn) to this work.

I. Introduction: voltage output versus current output

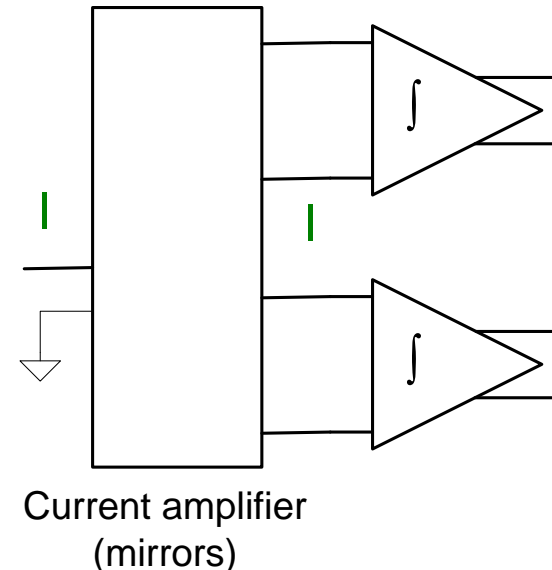
• Voltage output:

- Pros:
 - Tested
- Cons:
 - I (PMT) $\rightarrow V$ and $V \rightarrow I$ (integrate)
 - Larger supply voltage required
 - External components
 - 2 additional pads per channel



• Current output ("à la PS")

- Pros:
 - "Natural" current processing
 - Lower supply voltage
 - All low impedance nodes:
 - Pickup rejection
 - No external components
 - No extra pad
- Cons:
 - Trade-off in current mirrors: linearity vs bandwidth



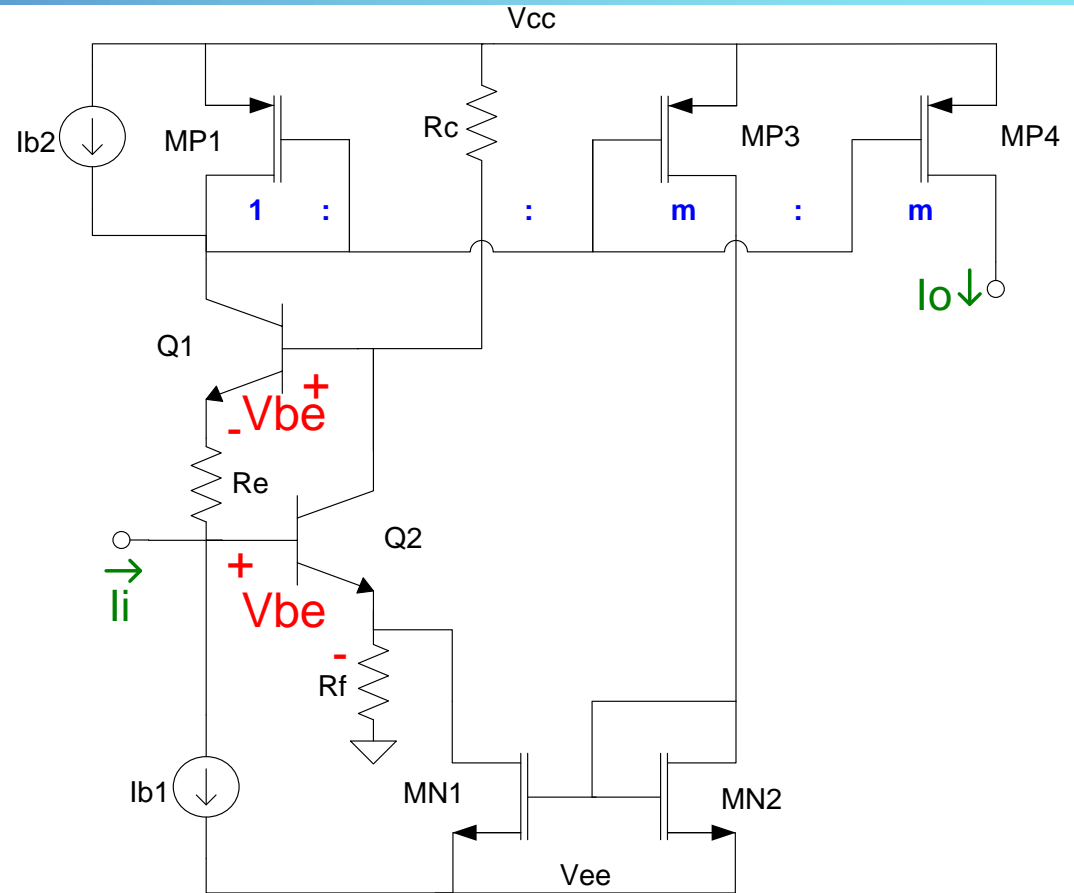
II. Preamplifier: current output / mixed feedback

- **Mixed mode feedback:**
 - Inner loop: lower input impedance
 - Voltage feedback (gain): Q2 and Rc
 - Outer loop: control input impedance
 - Current feedback: mirrors and Rf
- Variation of LAr preamplifier
- Current gain: m
- Input impedance

$$Z_i \approx \frac{1/g_{m1} + R_e}{g_{m2} R_c} + m R_f$$

- **Problem:**

- Voltage feedback for the super common base needs 2 Vbe (about 1.5 V !)
- Small room for current mirrors with 3.3 V
 - Need cascode current mirrors
 - 5 V MOS available: but poor HF performance



II. Preamplifier: current output / current feedback

- **Current mode feedback:**
 - Inner loop: lower input impedance
 - Current feedback (gain): mirror: K
 - Outer loop: control input impedance
 - Current feedback: mirror: m

- **Current gain: m**

- **Input impedance**

$$Z_i \approx \frac{1/g_{m1} + R_e}{1 + K} + \frac{K}{1 + K} m R_f$$

- **Current mode feedback used**

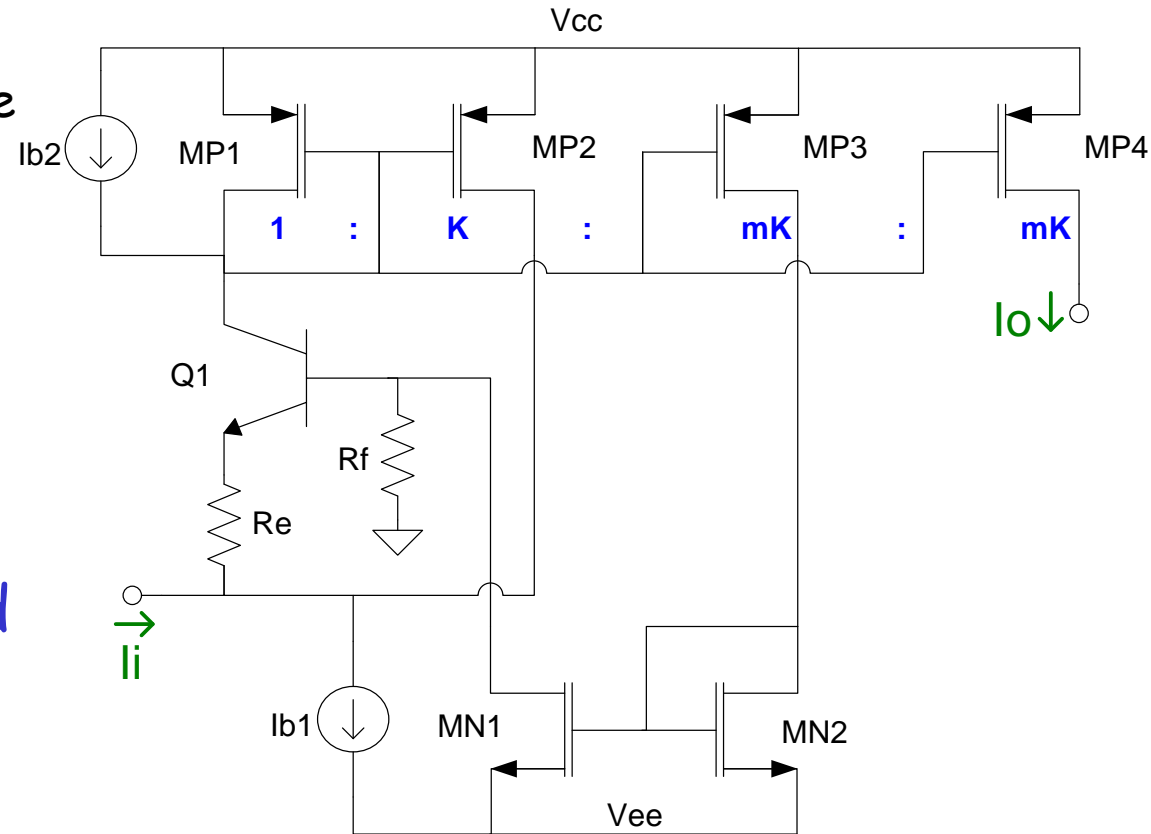
- Optical communications
- SiPM readout

- **Low voltage**

- Only 1 Vbe for the super common base input stage

- **Better in terms of ESD:**

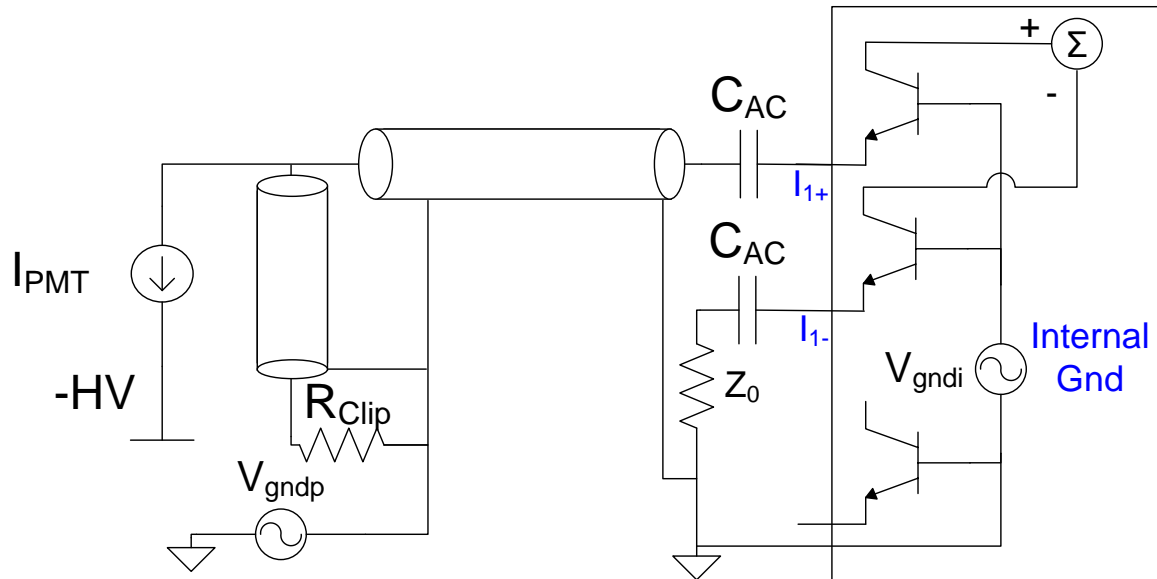
- No input pad connected to any transistor gate or base



POWER < 10 mW

II. Preamplifier: pseudo-differential input

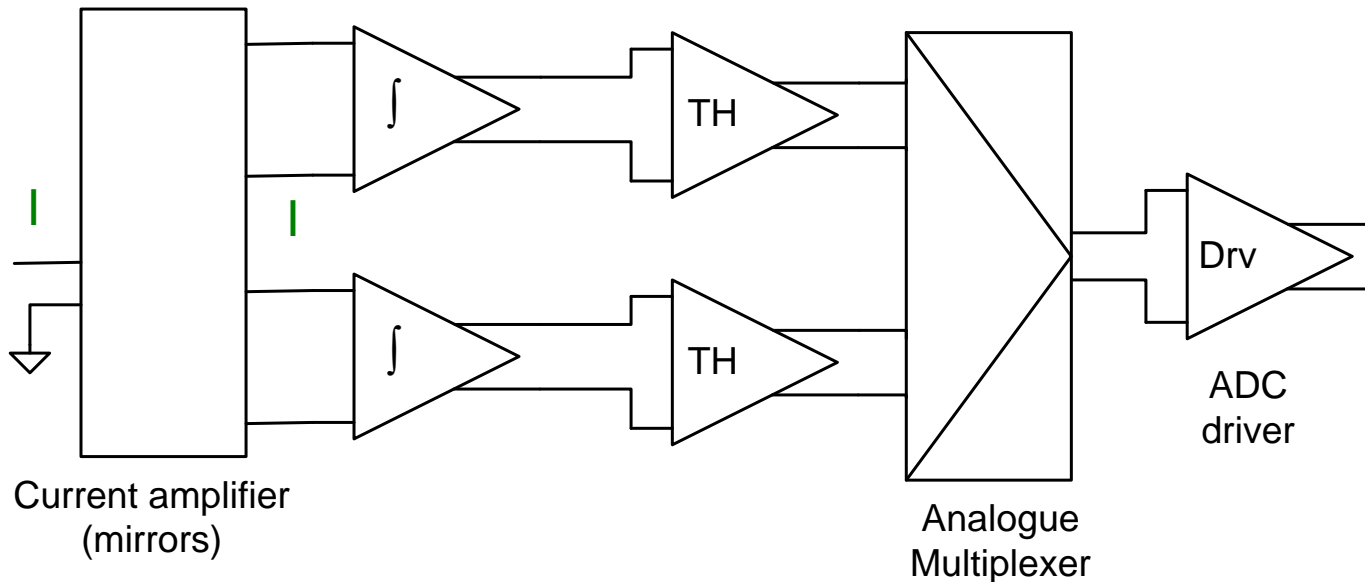
- Pseudo-differential input attenuates ground (and CM) noise in FE:
 - Mitigates V_{gndi} (conducted) noise (attenuation depends on matching)
 - Symmetrical chip/PCB layout also mitigates capacitive coupling (xtalk, pick-up)



- Drawback: uncorrelated HF noise $\times \sqrt{2}$
 - Predictable and stable effect
- Current mode preamplifier makes easier pseudo differential input:
 - Current: 2 pads per channel
 - Voltage (external component): 6 pads per channel

III. Channel architecture

- Current mode amplifier
- Switched integrator
 - Fully differential Op Amp
- Track and hold
 - ADC has already got one, really needed? Clock jitter...
 - 12 bit: flip-around architecture (same Fully Diff OpAmp?)
- Analogue multiplexer
- ADC driver
 - Depends on ADC input impedance: resistive or capacitive ?



IV. Technology issues: choice of technology

- **SiGe BiCMOS is preferred:**

- SiGe HBTs have higher g_m/I_{bias} than MOS: less noise, less Z_i variation
- SiGe HBTs have higher f_t (>50 GHz): easier to design high GBW amplifiers

- **Several technologies available:**

- IBM
- IHP
- AMS BiCMOS 0.35 μm

	IBM	IHP	AMS
HBT f_t	> 100 GHz	190 GHz	60 GHz
CMOS	0.13 μm	0.13 μm	0.35 μm
Cost [€/mm ²]	> 3 K	> 3 K	1 K

- **AMS is preferred**

- Factor 2 or 3 cheaper
- Too deep submicron CMOS not required / not wanted:
 - Few channels per chip (4 ?)
 - Smaller supply voltage
 - Worst matching
- Radiation hardness seems to be high enough (to be checked)

IV. Technology issues: radiation tolerance

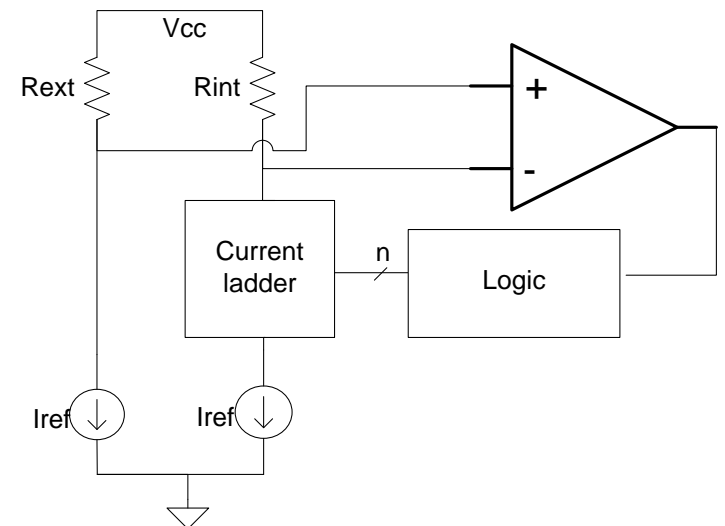
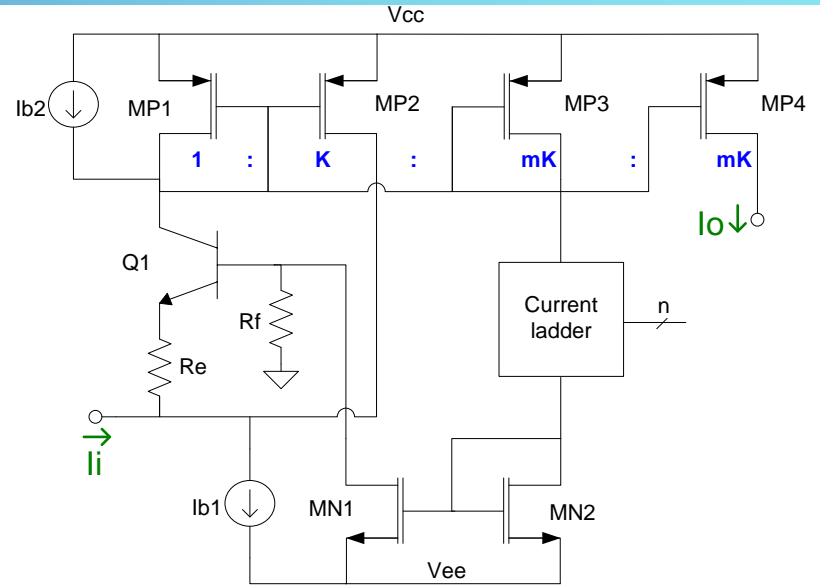
- Requirements:
 - Dose in 5 years (TID): 10-20 krad/s
 - Neutron fluence?
- AMS SiGe BiCMOS 0.35 um should be ok:
 - Omega studies about ILC calorimeters...
 - ATLAS: CNM studies: <http://cdsweb.cern.ch/record/1214435/files/ATL-LARG-SLIDE-2009-337.pdf>
- Radiation tolerance should be taken into account at design:
 - Cumulative effects:
 - Use feedback (global or local): minimal impact of beta degradation.
 - Not rely on absolute value of components, use ratios but:
 - Effect on current mirrors?
 - Transient events:
 - Guard rings for CMOS and substrate contacts: avoid SEL.
 - Majority triple voting: SEU hardened logic (if any) .

IV. Technology issues: effect of process variations

- Input impedance is the key point
- Two types of parameter variation simulated
 - Mismatch between closely placed devices (local variation component to component)
 - No problem: 1 % level
 - Process variation (lot to lot):
 - Problem: 10-30 % level !! (uniform distribution)
 - Pessimistic: experience tell that usually production parameters are close to the typical mean values
- In principle process variation affects whole production (1 run)
 - Could be compensated with an external resistor in series / parallel with the input
- Variation wafer-to-wafer or among distant chips in the same wafer:
 - Can not be simulated
 - Higher than mismatch and lower than process variation
 - According to previous experience: 2-3 % sigma: BUT NO WARRANTY
- Should we foresee a way to compensate it?
 - Group (2-3) chips and:
 - Different pcb (2 - 3 different external resistor values)
 - Tune a circuit parameter
 - Automatic tuning

IV. Technology issues: effect of process variations

- Input impedance controllable by:
 - Tune feedback resistor R_f
 - Difficult: small value (R_{on} of the switch)
 - Tune second feedback current
 - Binary weighted ladder (3 bits?): simple
- How control current ladder control?
 - Group ASICs a fix the value, set by:
 - External jumper
 - Slow control: dig interface required
 - Automatic tuning
 - Reference voltage
 - Reference currents: external or band gap
 - External resistor
 - Wilkinson or SAR ADC style logic



V. Status and plans

• Prototyped in June AMS run:

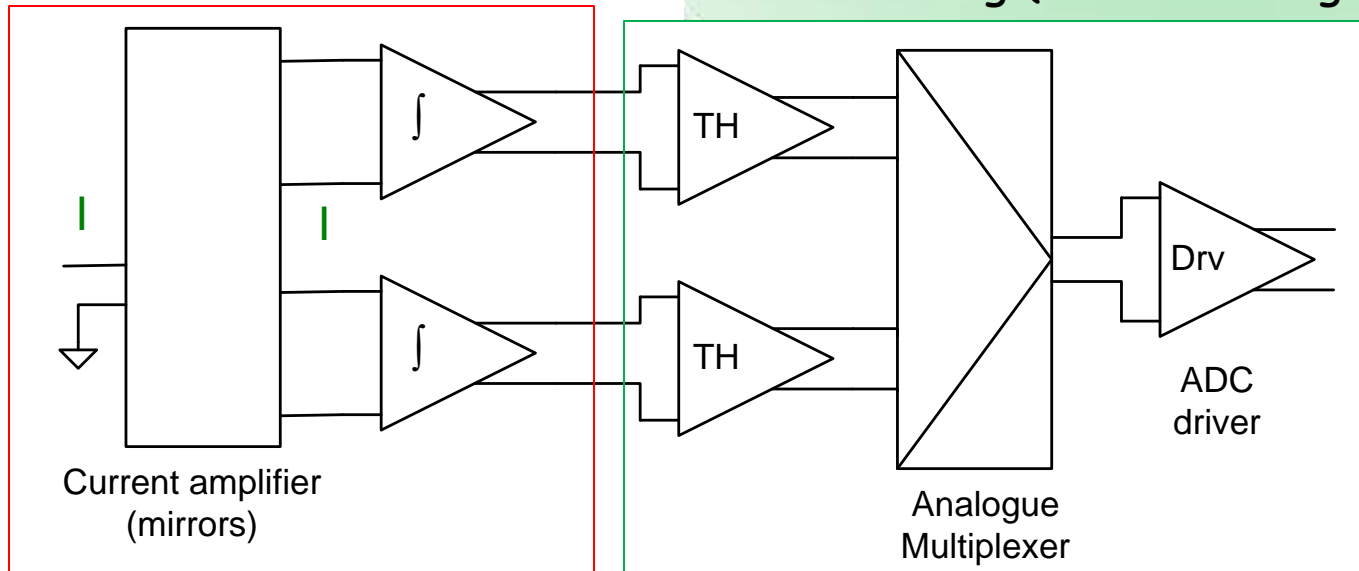
- Low noise current amplifier:
 - Basic schemes
- Integrator:
 - High GBW fully differential OpAmp
 - Could be used in other stages



See Edu's talk

• To be tested in future runs:

- Compensation of process variation of amplifier's input impedance
- Track and hold (if needed)
- Analogue multiplexer
- ADC driver
 - ADC needs to be characterized
- Common blocks:
 - Clock generation
 - Biasing (CMOS band gap already exists)



V. Status and plans: concluding remarks

- A current mode amplifier with cool termination seems feasible:
 - Current feedback preferred
 - Current mirrors with active cascode topologies
 - Linearity better than 0.5 % for 2 mA peak input current
 - BW > 300 MHz
- Noise seems ok:
 - Gain such that 50 pC @ PMT \Rightarrow 2 V @ Integrator Output
 - Single ended preamp and no pedestal subtraction: 250 uV rms
 - Differential preamp and no pedestal subtraction: 330 uV rms
 - Differential preamp and dynamic pedestal subtraction: 500 uV rms (1 ADC count)
- Simulation results in Edu's talk

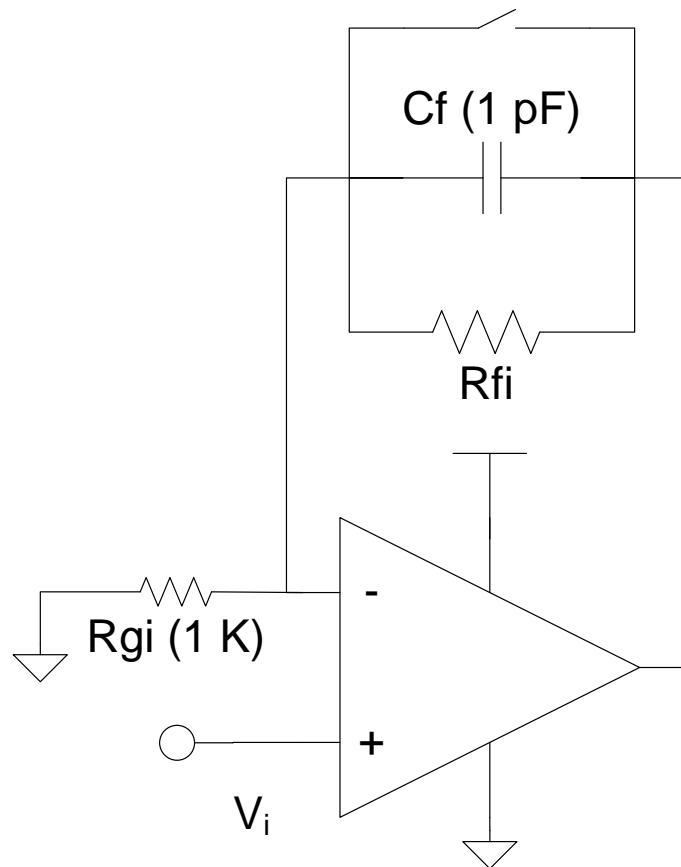
V. Status and plans: concluding remarks

- It looks ok, however it is just calculation and simulation for the moment
 - Matching may affect linearity
 - Simulated, but at the end it depends on layout
 - A dramatic effect is not expected...
- To keep in mind...
 - Integrated solution gives some security margin
 - Still possible to modify PM base
 - How to do clipping? Gaussian shaping? Digital spill over correction (as in PS) ?
 - *As differential as possible* for a single ended sensor
- Cost...
 - If an engineering run can be shared with other projects
 - Cost of < 15€/ch for the analog seems feasible (without ADC)

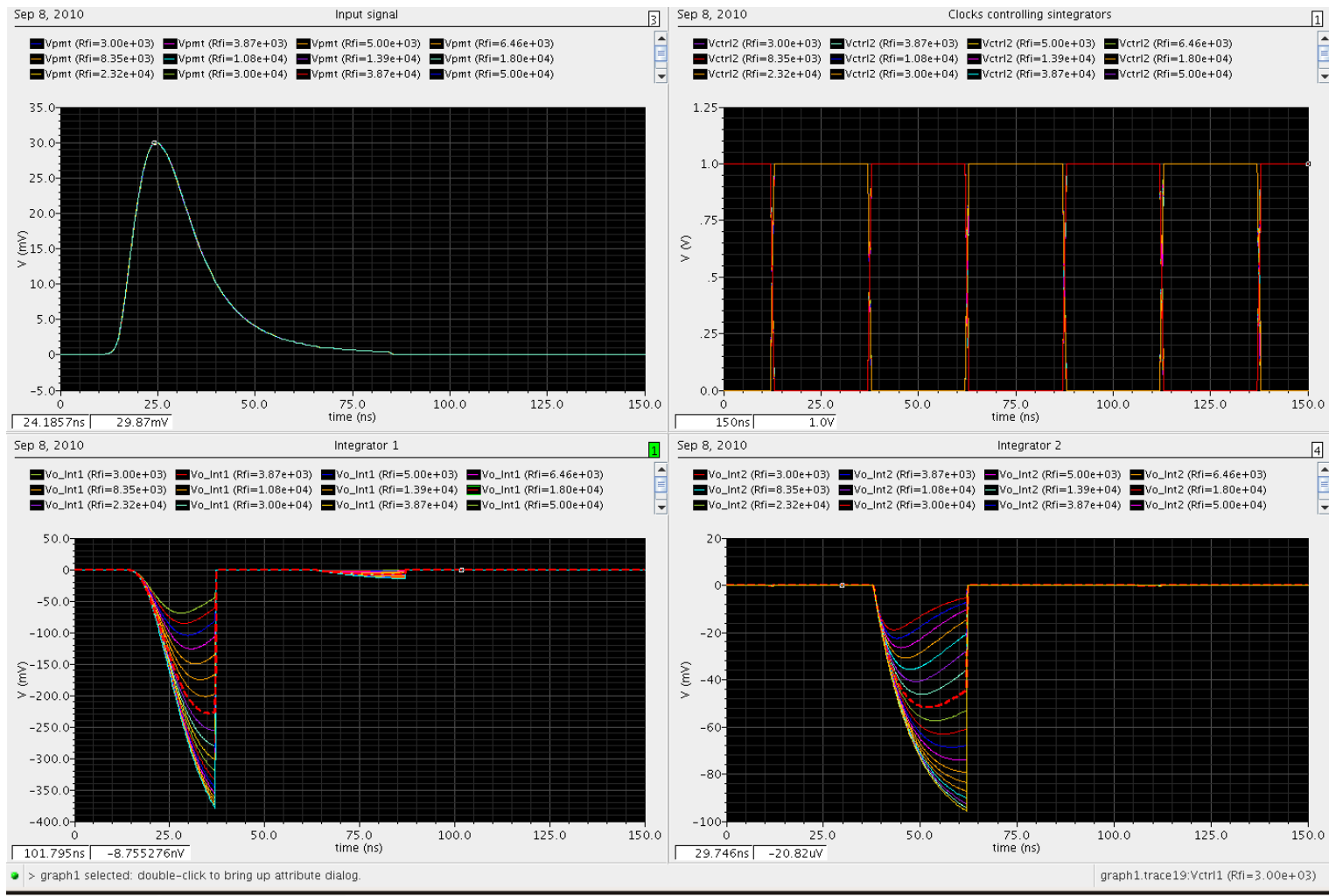


BACK-UP

- Possible alternative to delay line clipping or gaussian shaping
 - Jacques' idea



• Possible alternative to delay line clipping or gaussian shaping



- Possible alternative to delay line clipping or gaussian shaping

