



Analog FE ASIC: first prototype

Upgrade of the front end electronics of
the LHCb calorimeter

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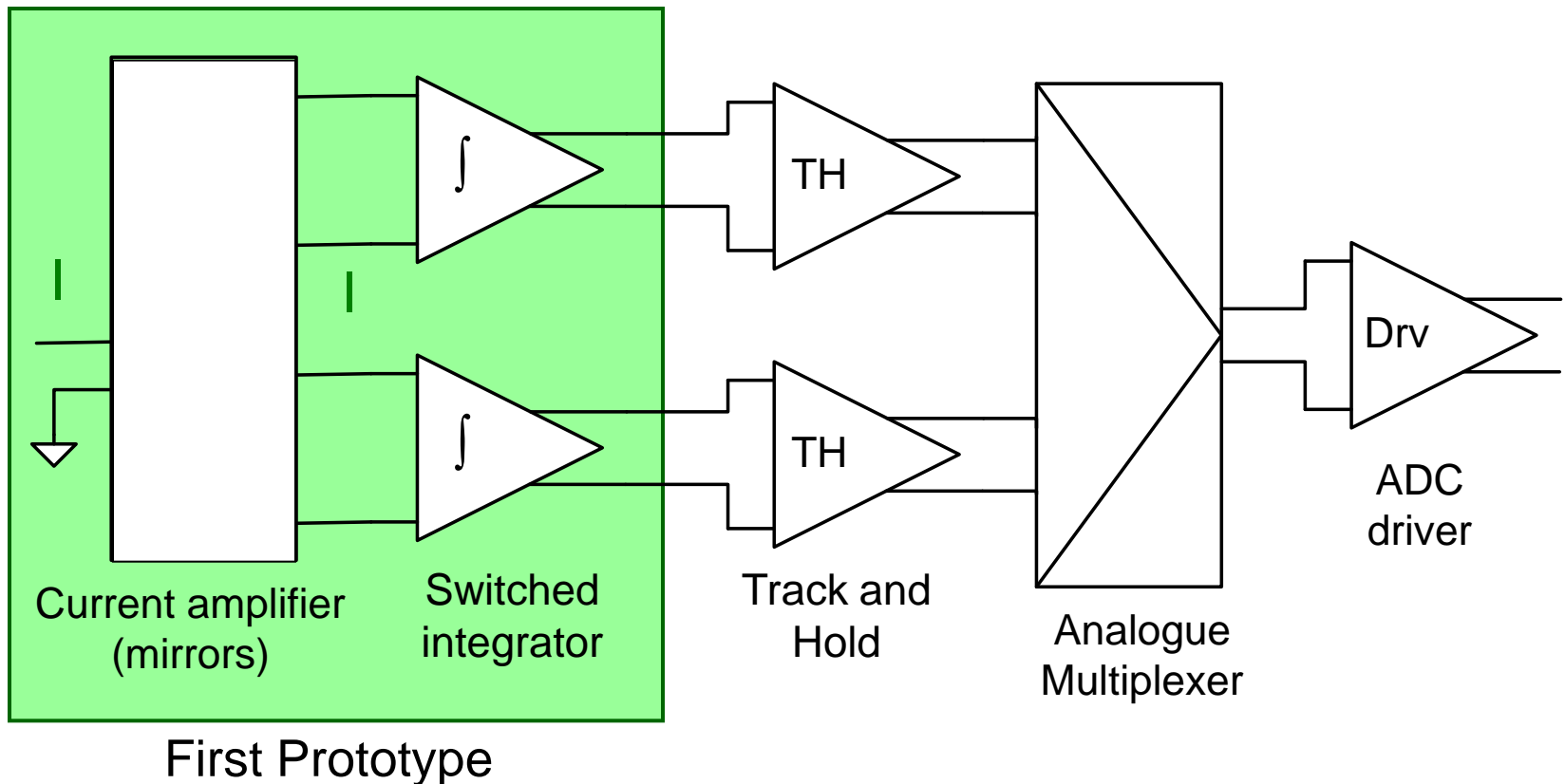
Calorimeter upgrade meeting – CERN – October 5th 2010

Outline

- (1) Introduction
- (2) Current Mode Preamplifier
- (3) Integrator
 - FDOA
 - Switched Integrator
- (4) Linearity
- (5) Noise
- (6) IC Implementation Details

Introduction

- ECAL analogue FE IC: channel architecture

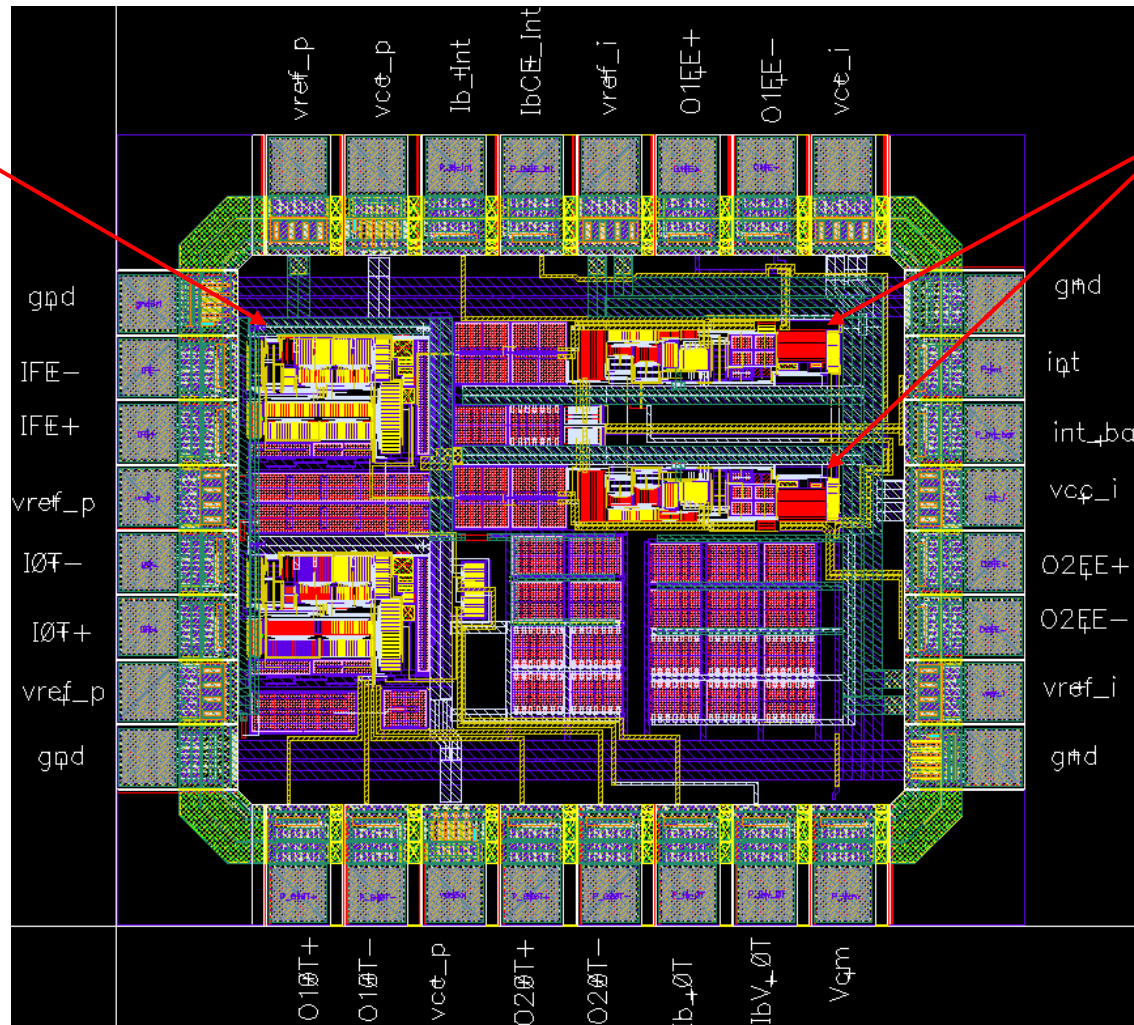


Introduction

- IC sent: ICECAL

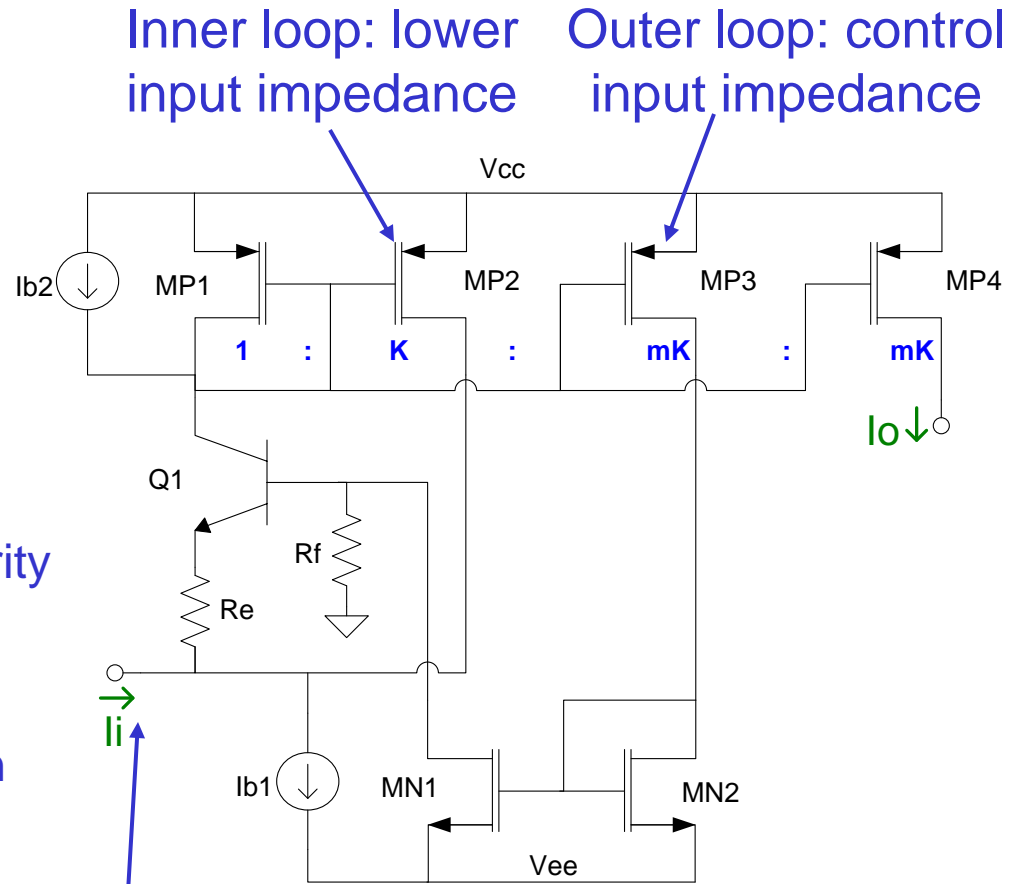
Current preamp

Integrators



Current mode preamplifier

- Pros:
 - “Natural” current processing
 - Lower supply voltage
 - All low impedance nodes:
 - Pickup rejection
 - No external components
 - No extra pad
- Cons:
 - Trade-off in current mirrors: linearity vs bandwidth
- Low voltage
 - Only 1 V_{be} for the super common base input stage
- Better in terms of ESD:
 - No input pad connected to any transistor gate or base

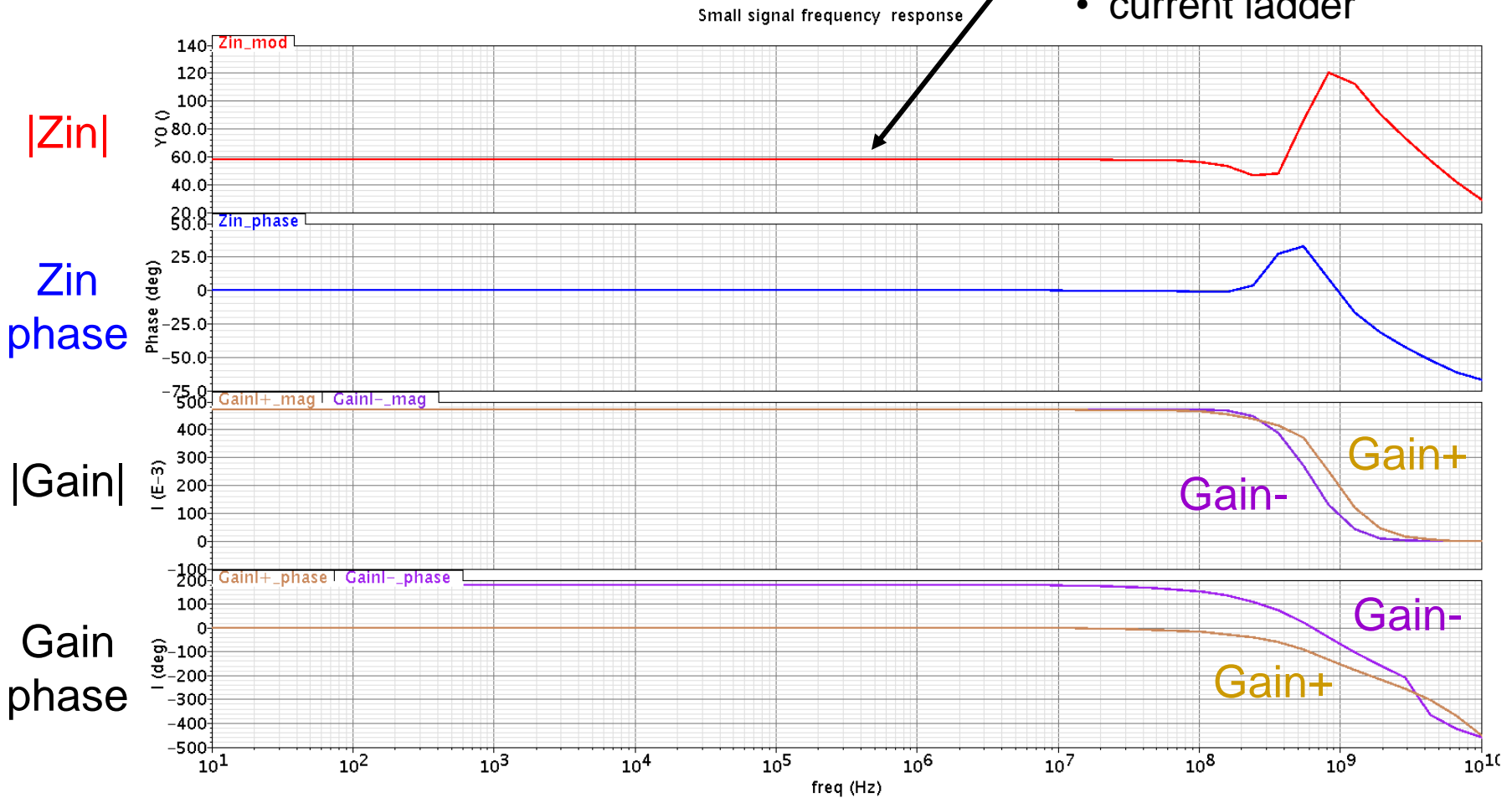


$$Z_i = \frac{1/g_{m1} + R_e}{1 + K} + \frac{K}{1 + K} mR_f$$

Current mode preamplifier

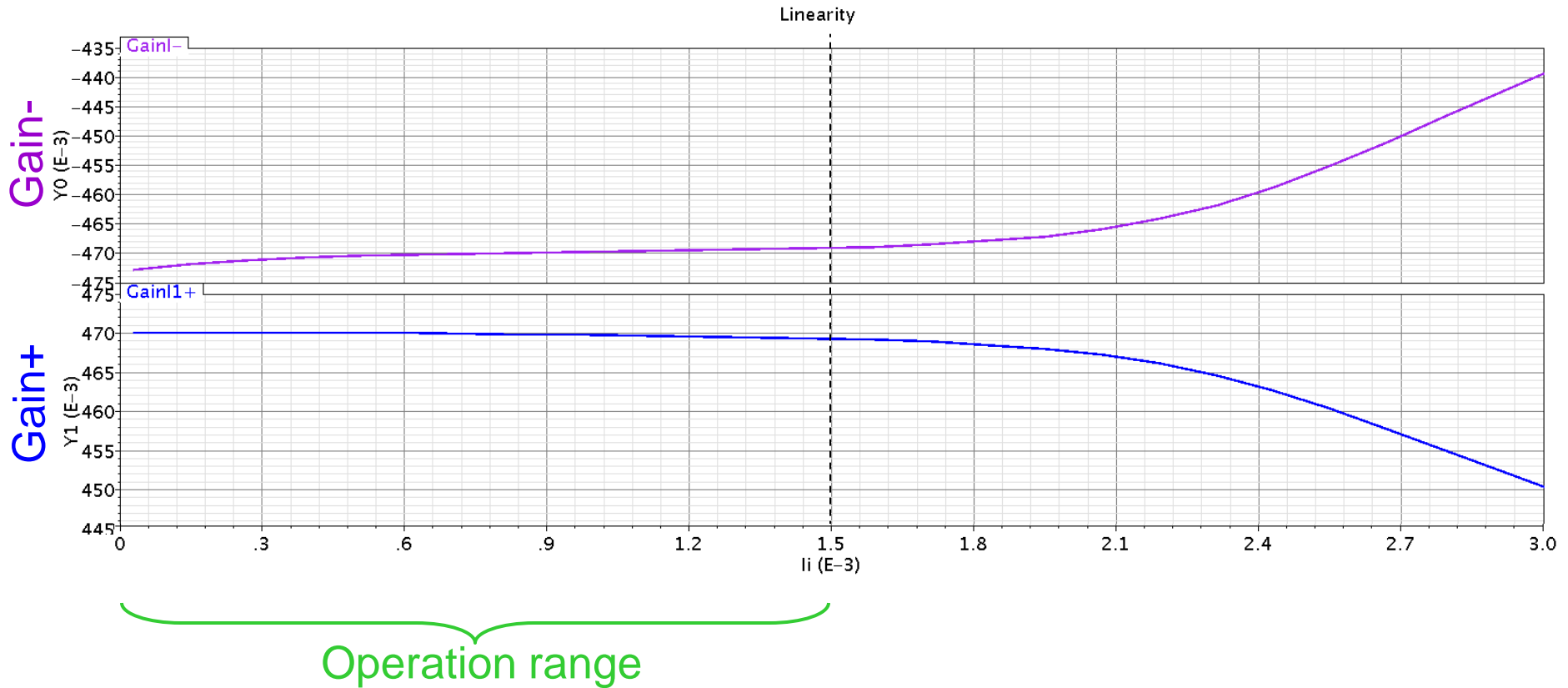
- Simulations based on the extracted RC

- Possible compensations:
- Parallel R
 - current ladder



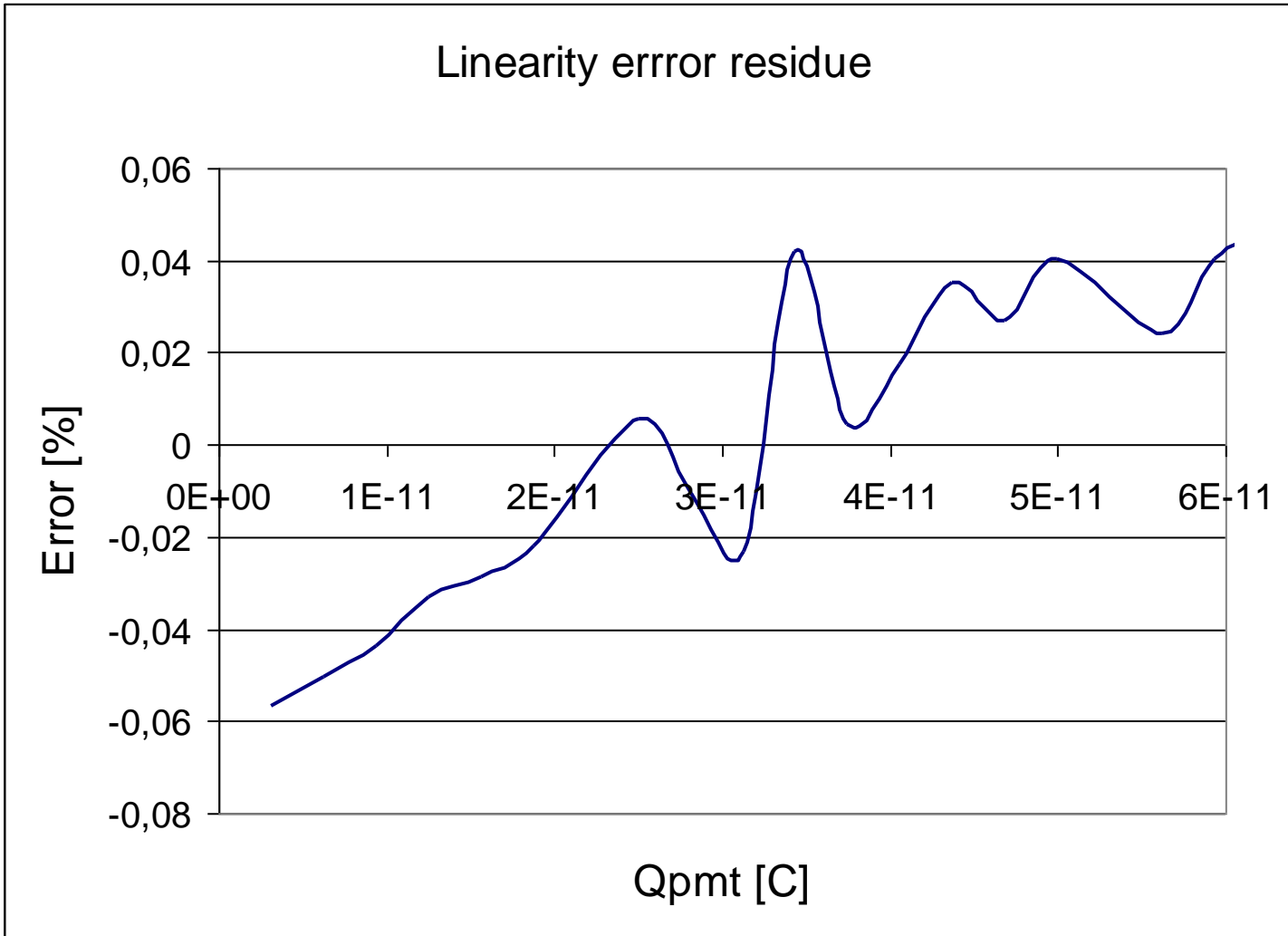
Current mode preamplifier

- Simulations based on the extracted RC: linearity vs. $I_{i,peak}$



Current mode preamplifier

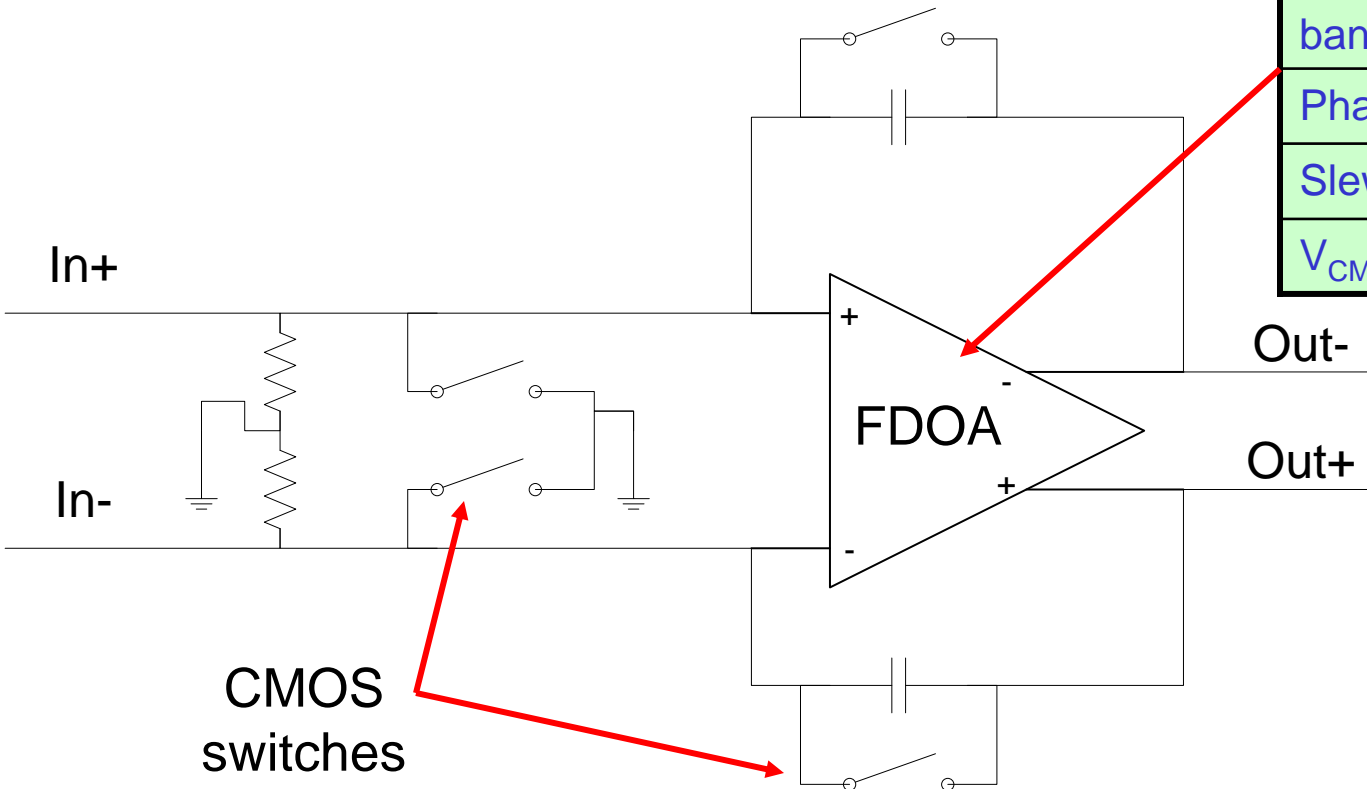
- Linearity error after integration (ideal) vs input charge



Integrator

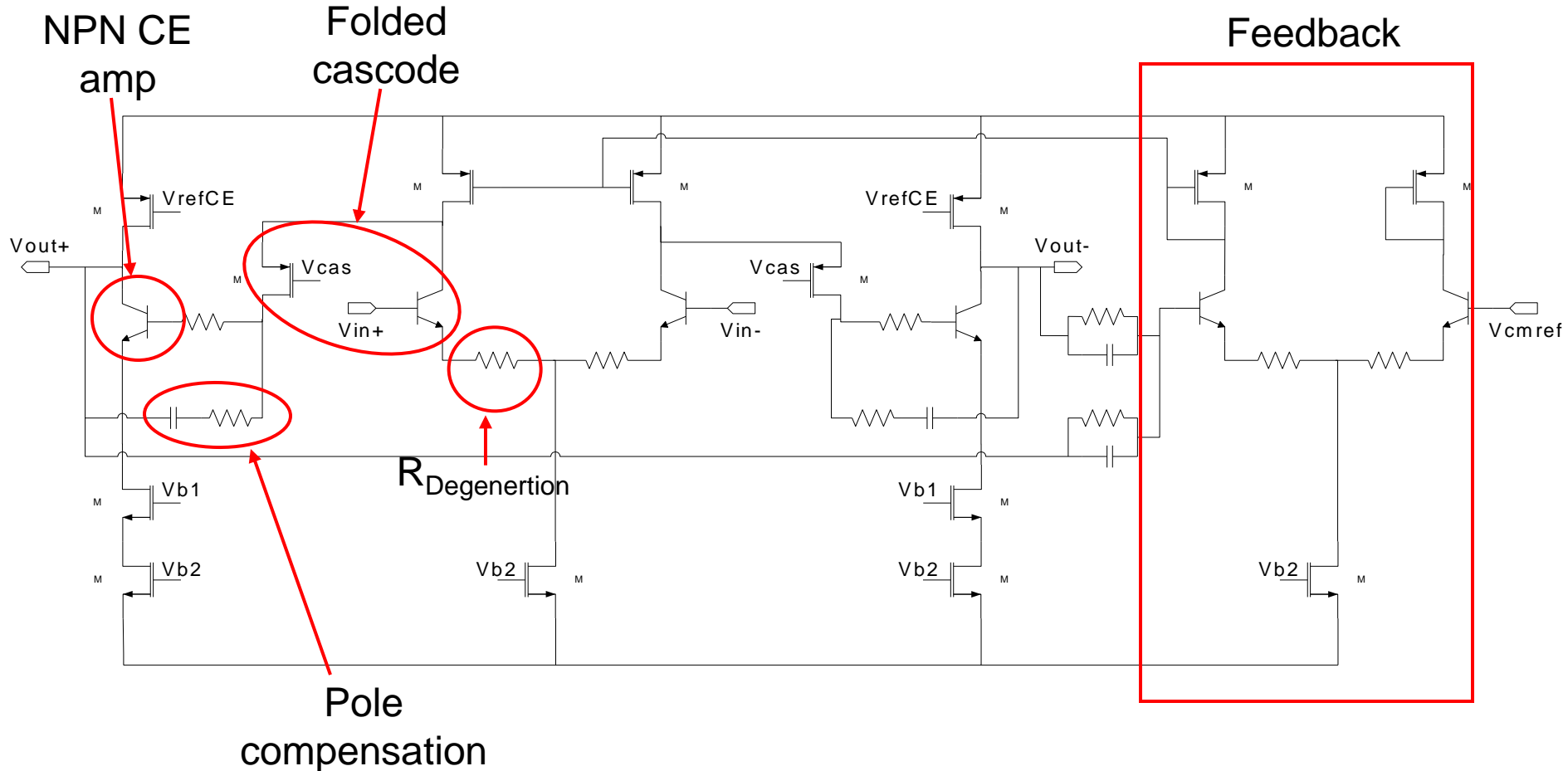
- Switched integrator architecture

FDOA specifications	
Parameter	Value
Gain bandwidth	500 MHz
Phase margin	> 65°
Slew rate	> 2 V/μs
V_{CM}	1.65 V



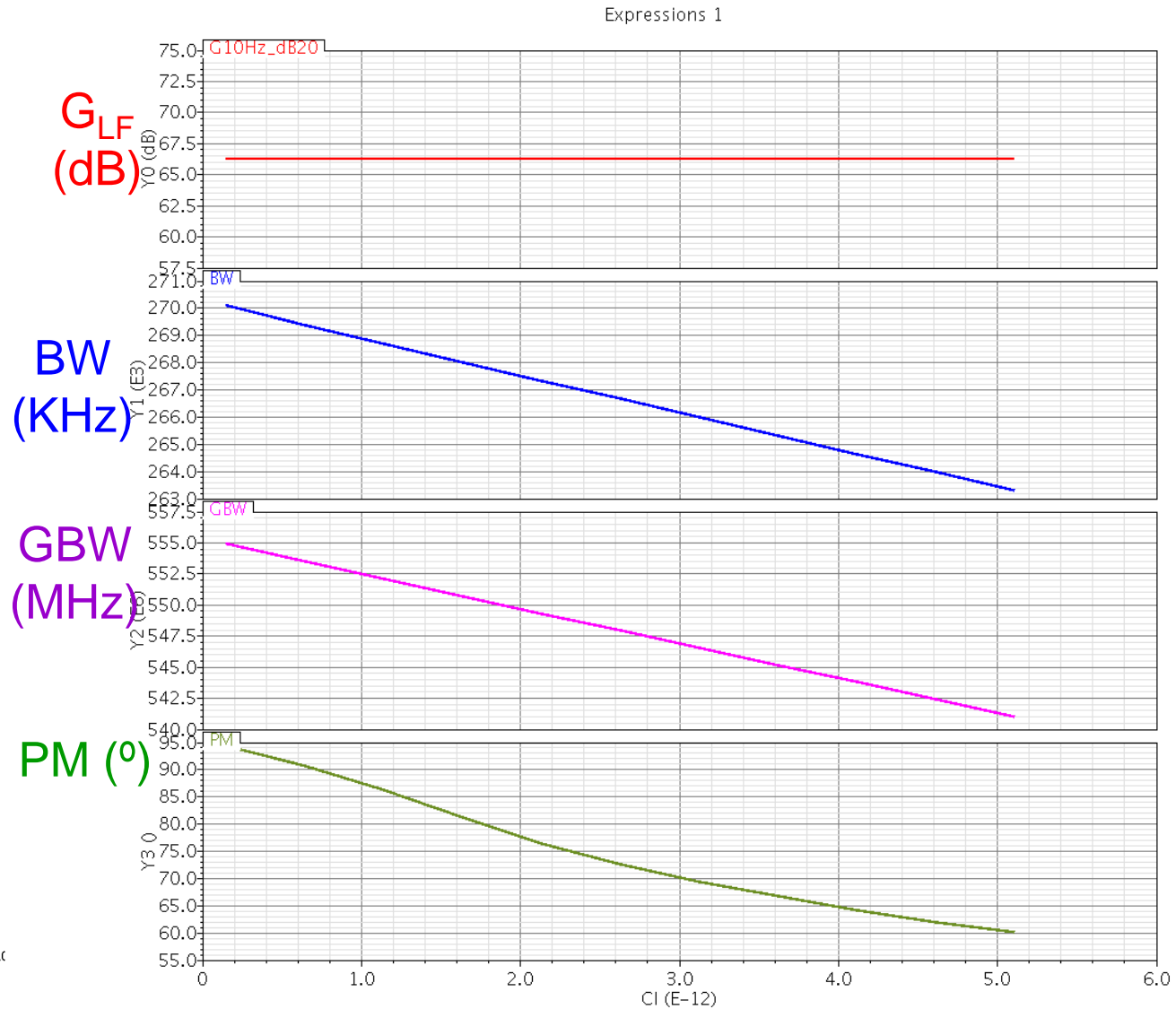
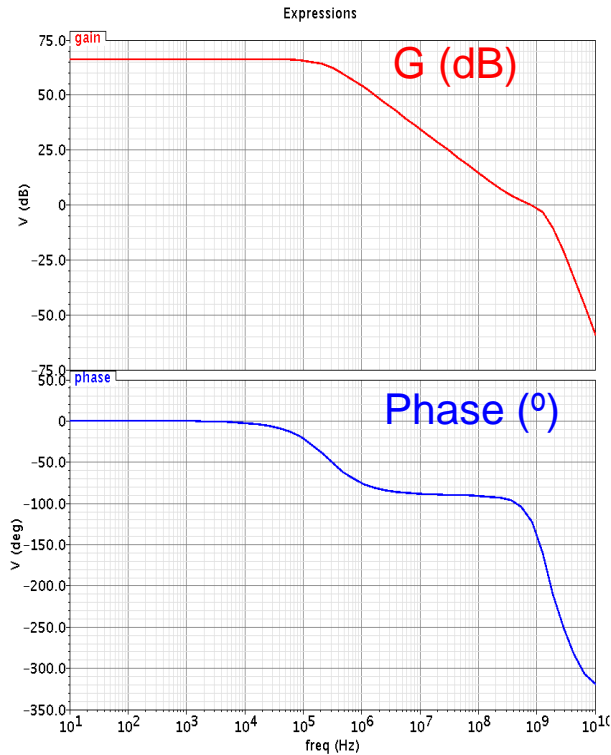
FDOA: design

- Fully differential Operational Amplifier



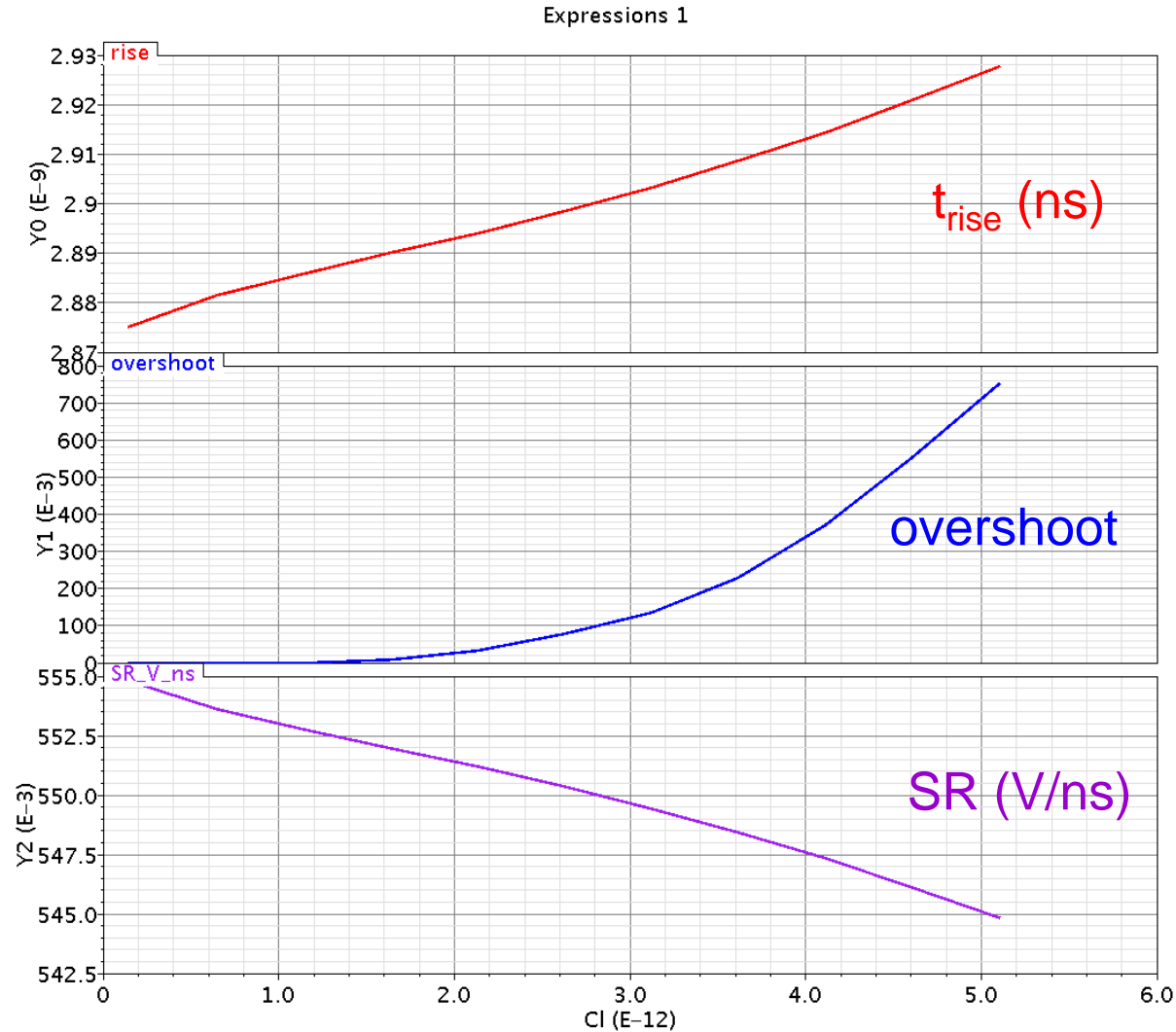
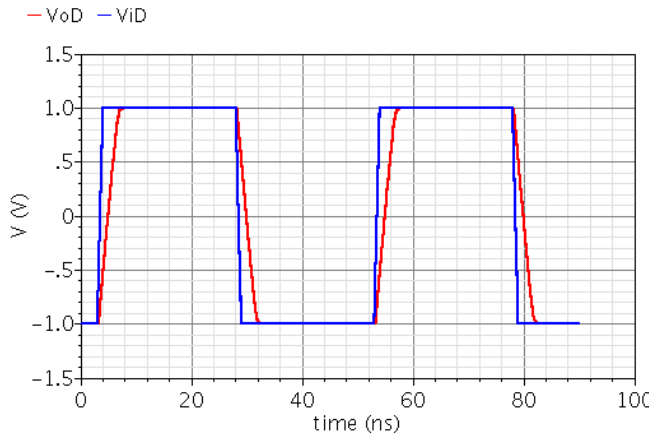
FDOA: open loop post layout simulations

- $I_{bCE} = 900\mu A$
- Load capacitor between 150fF and 5.1pF



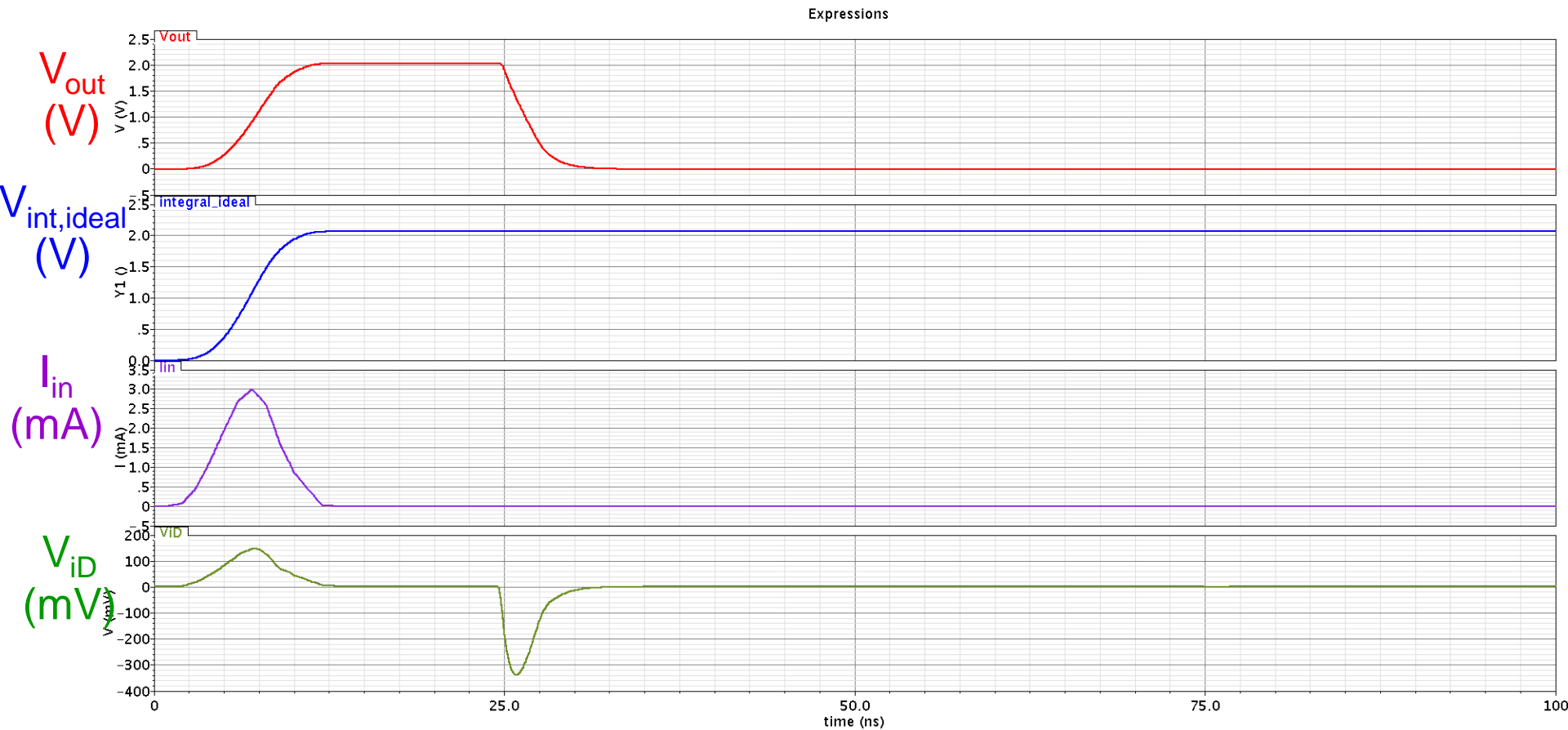
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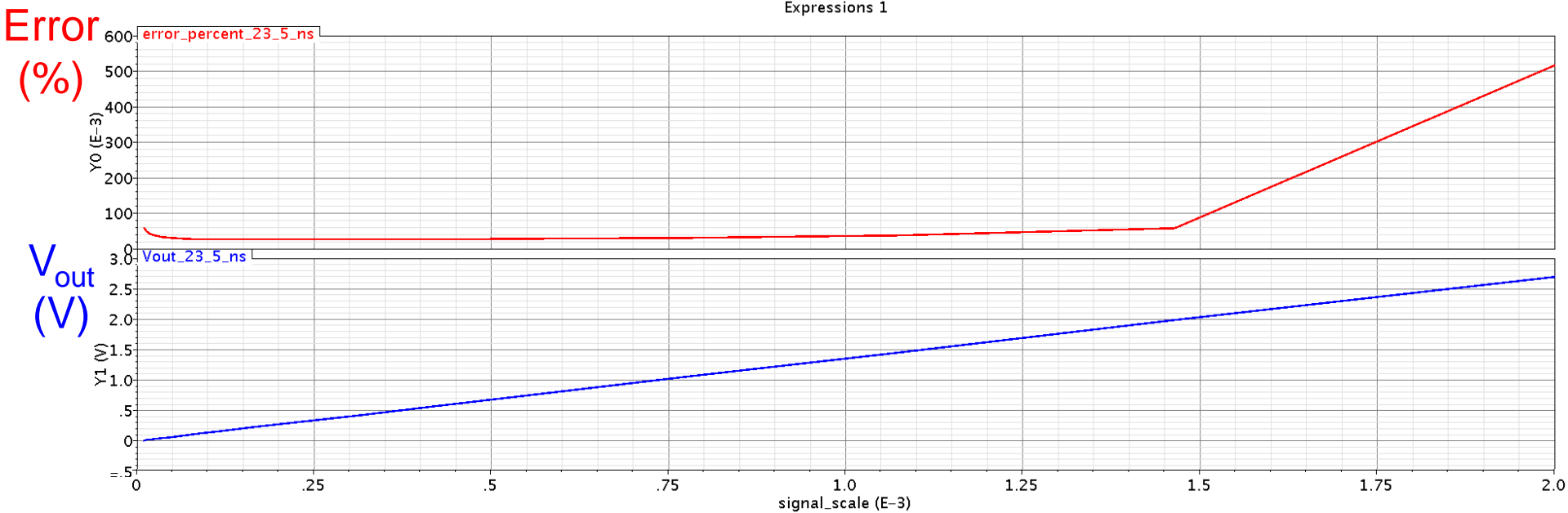
Integrator: pulse response

- Simulations based on extracted RC
- $C_1 = 5\text{pF}$



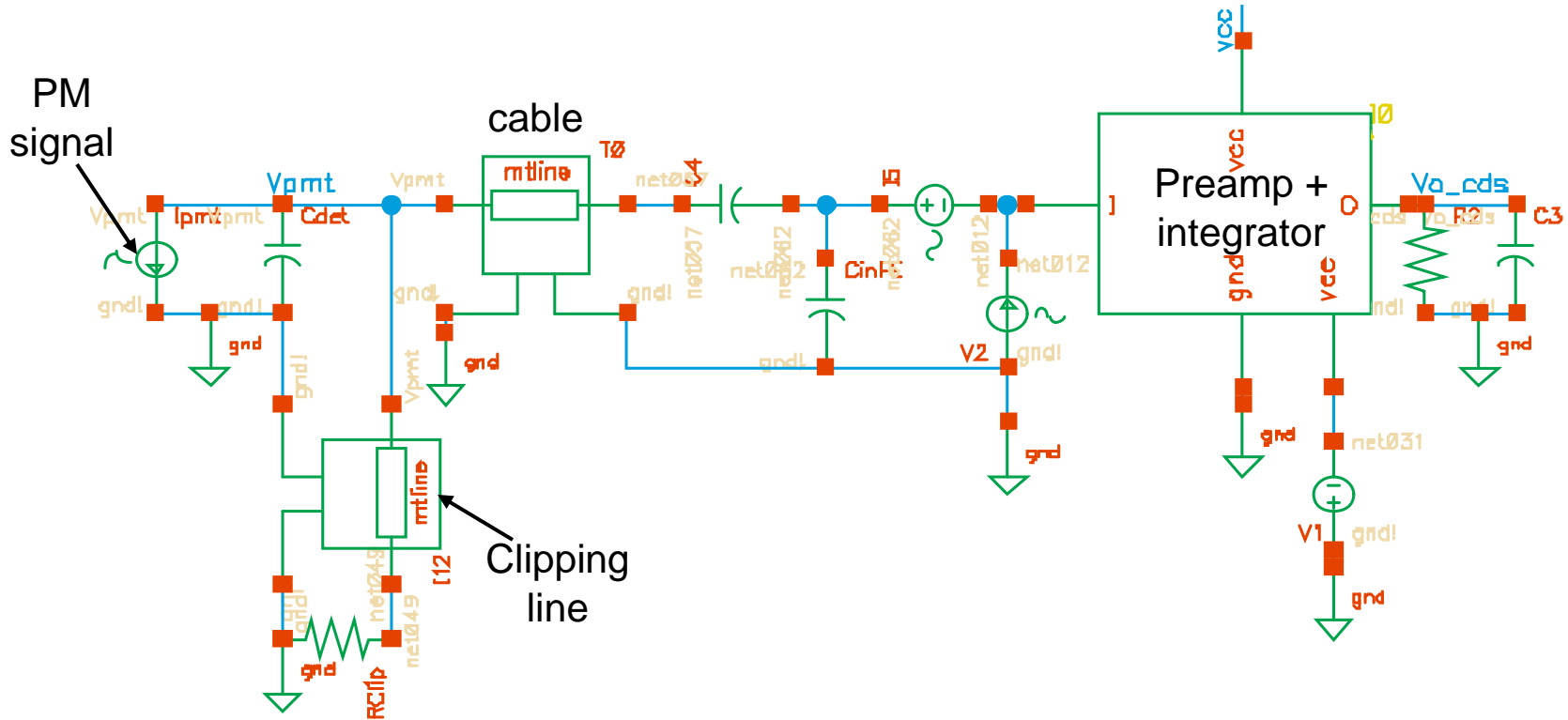
Integrator: Linearity

- Simulations based on extracted RC
- $C_1 = 5\text{pF}$



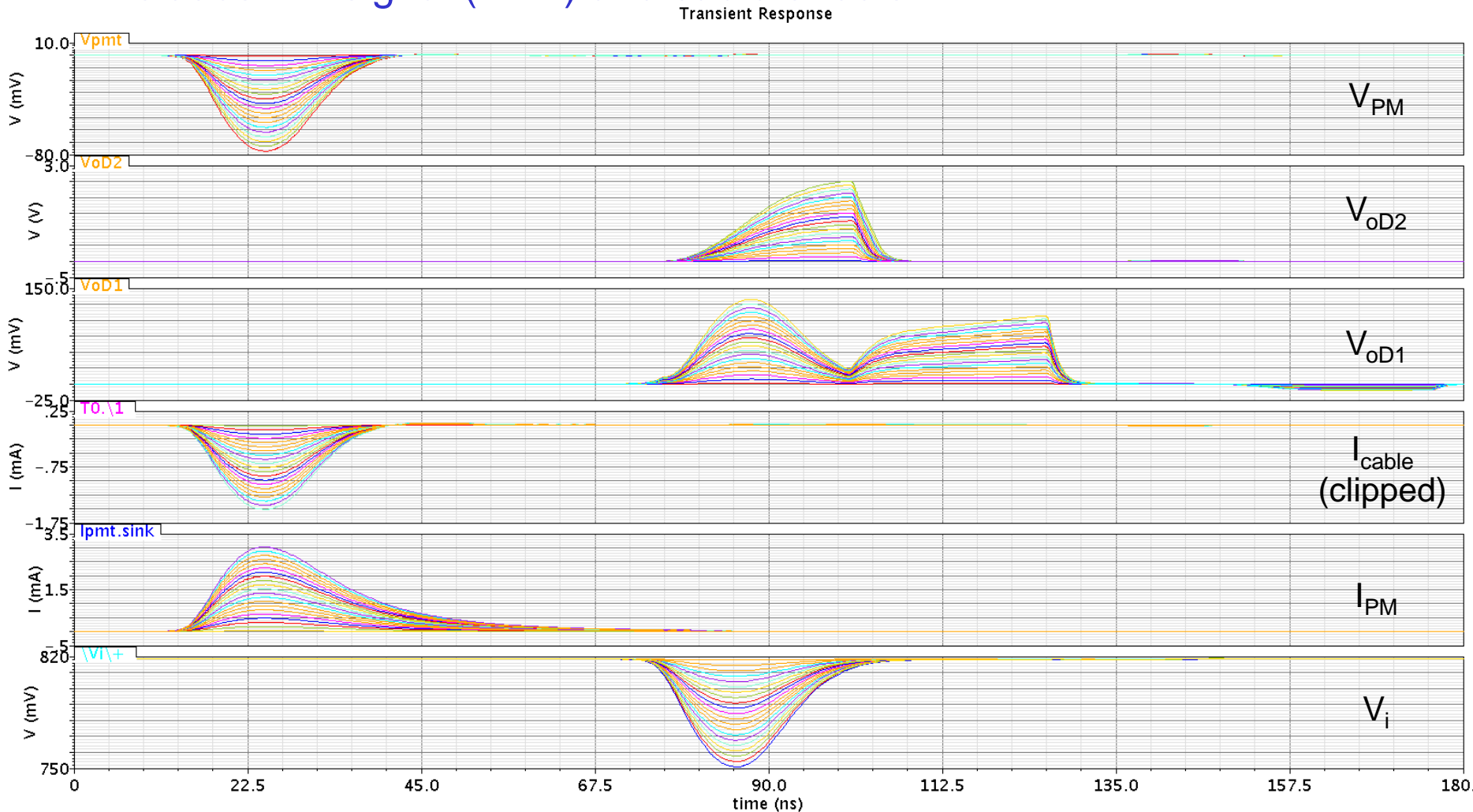
Front End simulations (Preamp+integrator)

- Simulations based on extracted RC of complete IC
- Includes PM signal (TDR) and cable effects

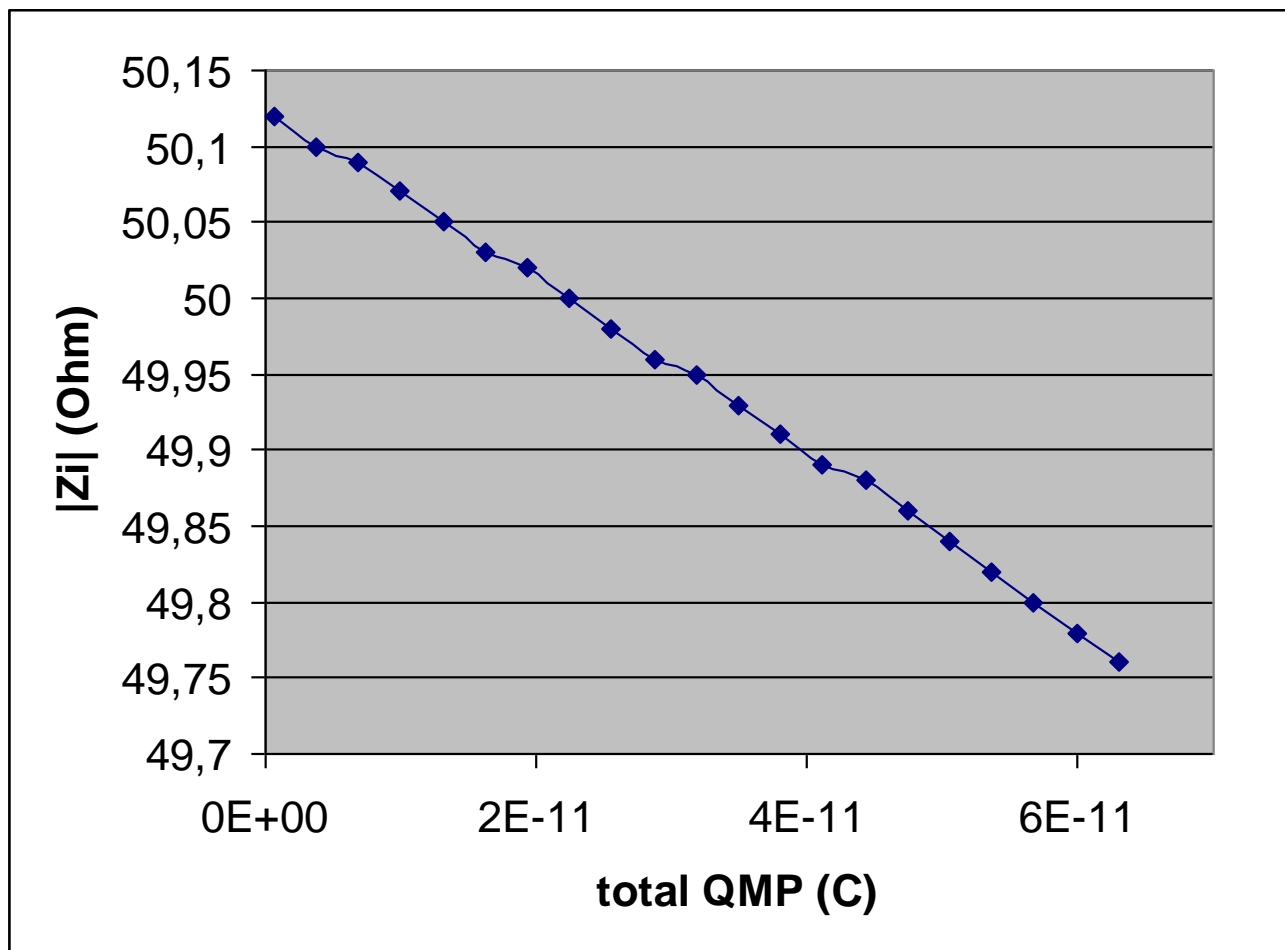


Front End simulation (Preamp+integrator)

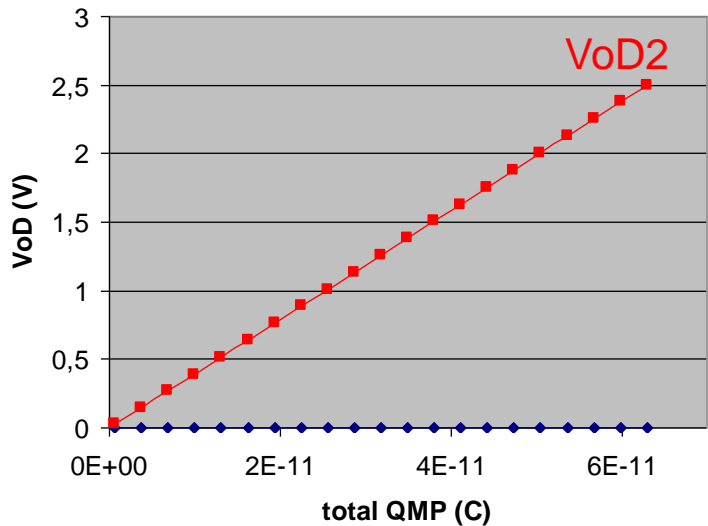
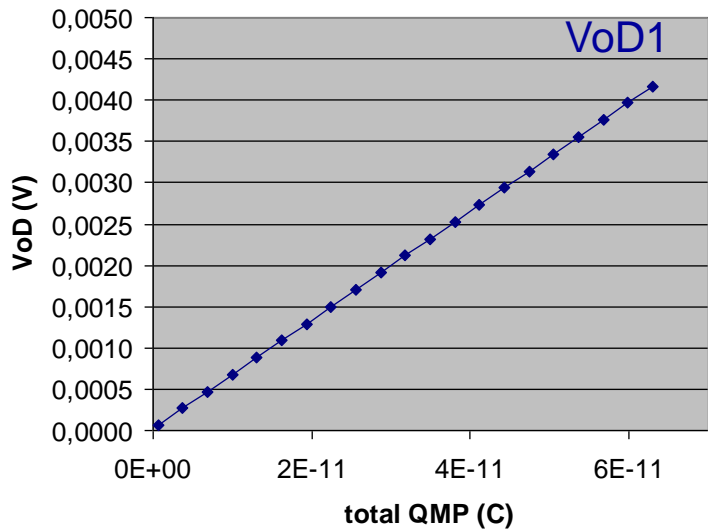
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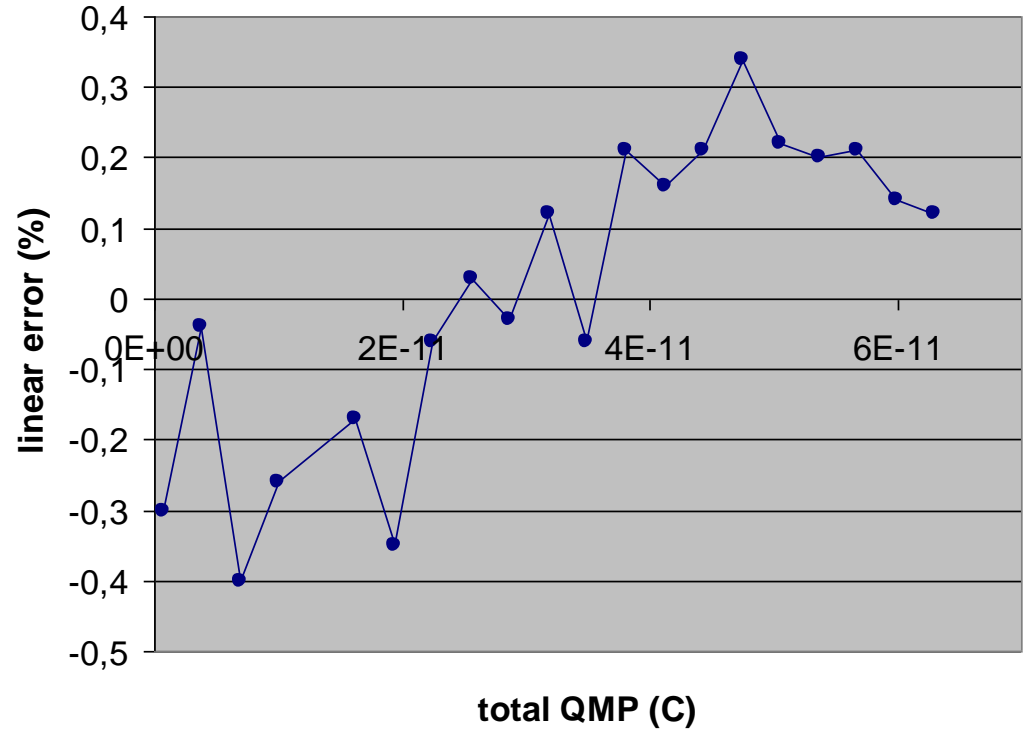
Dynamic deviation of the input impedance



Front End simulation: linearity

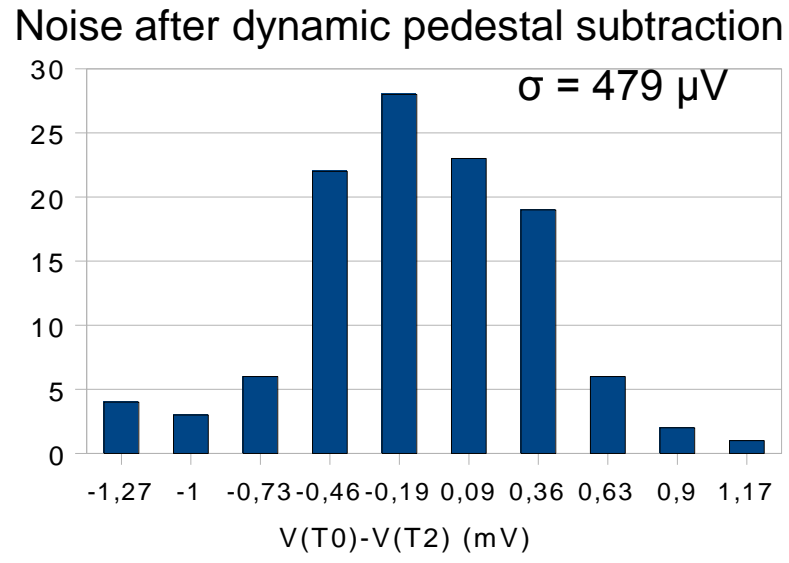
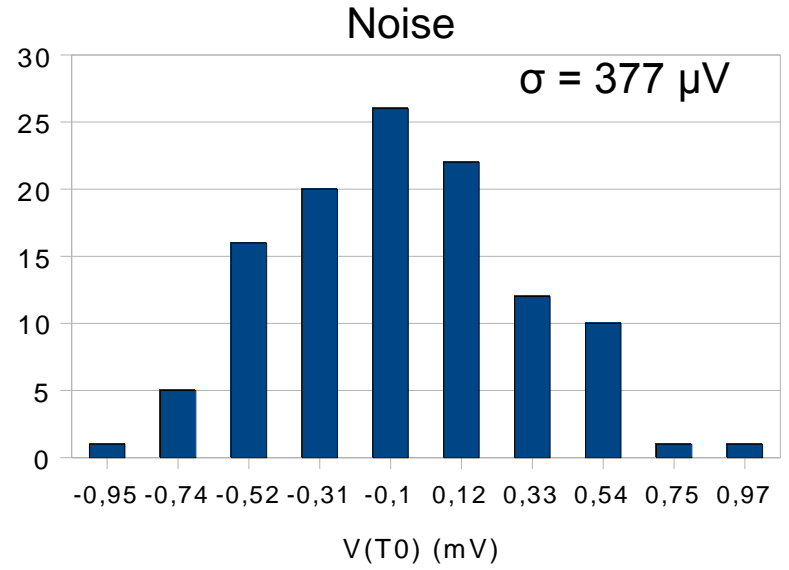
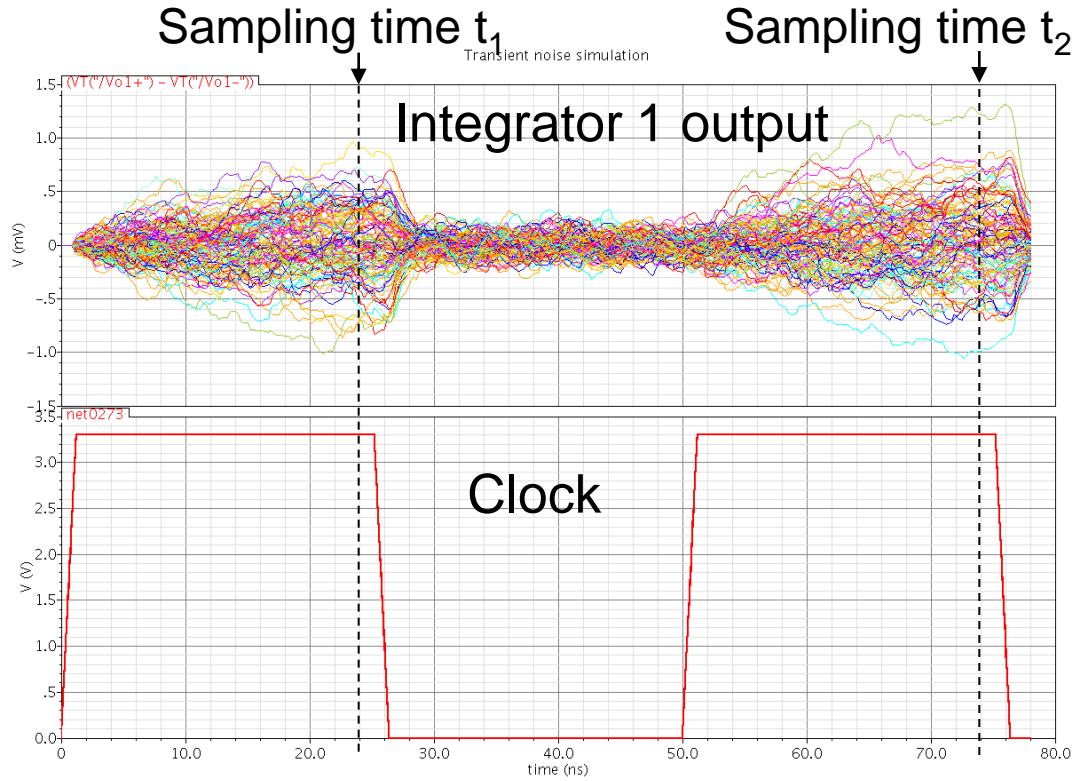


Linear error



Front End simulation: noise

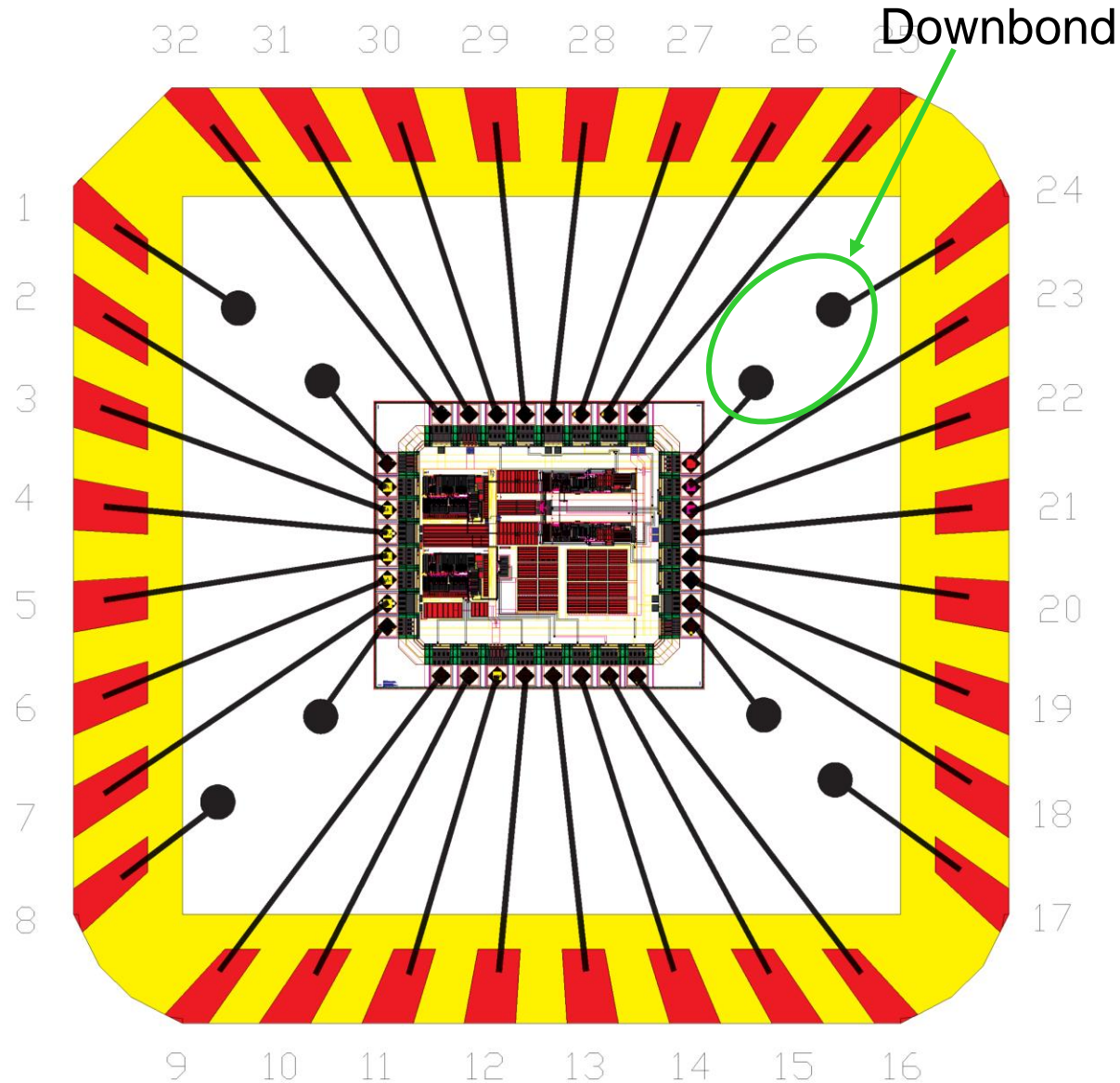
- Transient noise analysis



- Noise at output: distribution of $V(t_2)$
- Noise after dynamic pedestal subtraction: distribution of $V(t_1) - V(t_2)$

IC Implementation details

- AMS SiGe BiCMOS s35
- QFN package
 - Substrate connected to central pad (gnd)
- When taking into account the bonding parasitics:
 - $3 * \text{nominal } L \Rightarrow \text{danger of ringing}$
- Solutions:
 - Include R in series with decoupling capacitor of V_{ref}
 - Increase number of gnd pins
 - Downbonds for gnd



Prototype test PCB

- PCB designed for tests
 - 4 layers
 - 2 socket compatible
 - About 8x9 cm
- Chips arrived on 1st October.

