RAD-HARD BANDGAP VOLTAGE REFERENCE IN LFOUNDRY

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From a CPPM's student internship project in 2019

Specifications

1.8 V in LFoundry

Voltage reference	VREF = 1 V	VREF deviation	ΔVREF = 0.01 V
Supply voltage	VDD = [1.5, 2] V	Current consumption	ICC = 70 µA
PSRR	-25 dB	Maximal leakage current	ISTB = 0.01 nA
Operating temperatures	T = [-45, 90] °C	Radiation hardness specifications	TID = 80 MRads
Temperature variation	ΔT=0.2%	Radiation specifications	NIEL = 1.5*10^15 neq/cm²

Focus on [-20, 60] °C.
ATLAS working point: -10 °C.

General schematic

Autobias & Startup

Unbalancing the zero current state in the beginning and supply current

CTAT & PTAT Branches

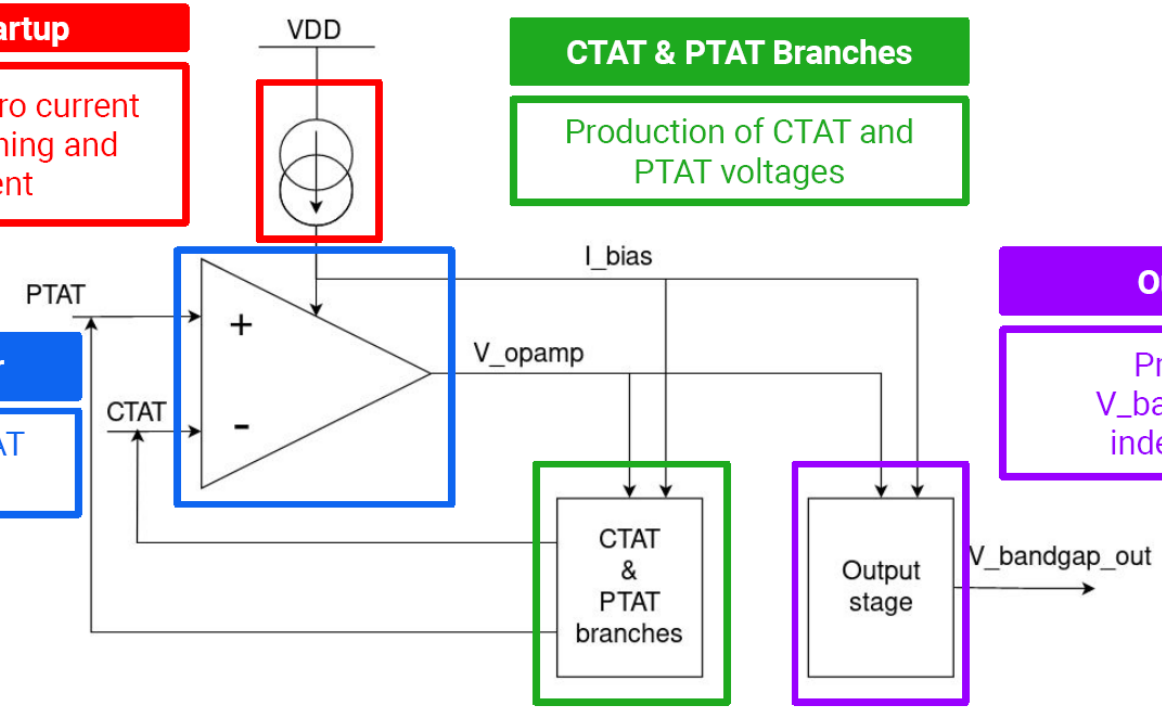
Production of CTAT and PTAT voltages

Output stage

Production of V_bandgap_output independent to T

Operational amplifier

Balance CTAT and PTAT voltages

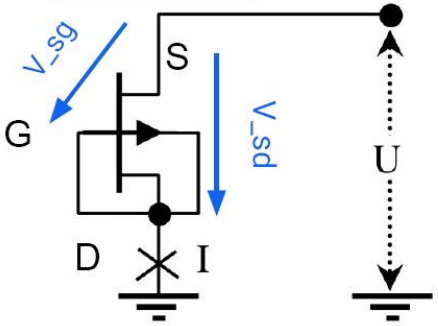


DTMOS transistor

(Dynamic-Threshold Metal-Oxide-Silicon transistor)

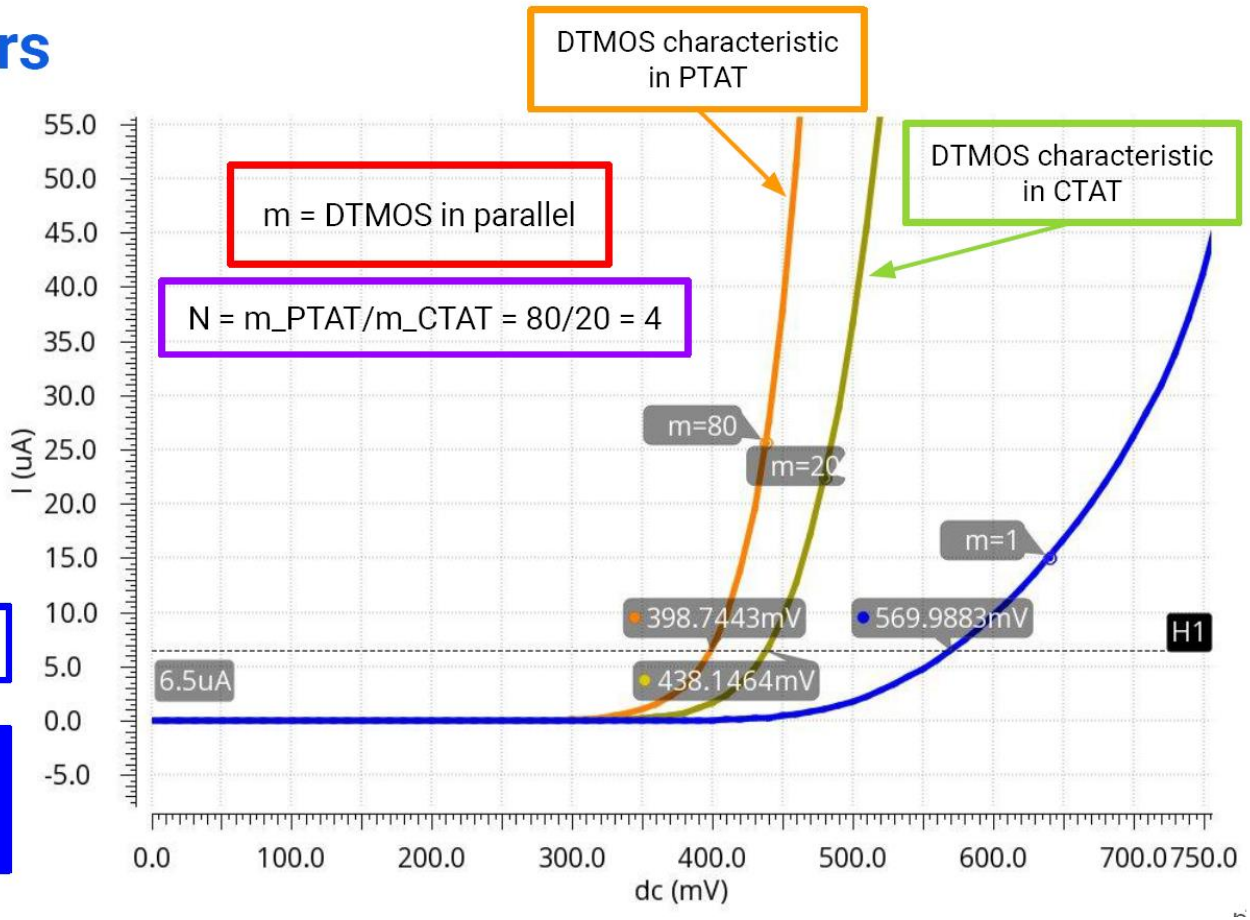
DTMOS transistors

W = 3 um
L = 0.6 um



At 6.5 uA the DTMOS is biased

Bias current set to 6.5 uA to design the Autobias and startup circuit



[1] Annema,JM.(1999). Low-Power Bandgap References Featuring DTMOST's. IEEEJournal of Solid State circuits,34.
[2] Gromov,V.(2004). Development of the Bandgap Voltage Reference Circuit, Featuring Dynamic Threshold MOS Transistors(DTMOST's) in 0.13um CMOS Technology. 10thWorkshop on Electronics for LHC and Future Experiments,333-339.

Layout dimension

The bandgap cell dimension is ~600µm x 600µm
(pads and guarding included)

The cell was designed and test in 2021 but does not work.

Need to be resubmit with minor modifications (psub layer).