LFoundry SEU-tolerant memory (RD50_MPW2) test at RBI facilities

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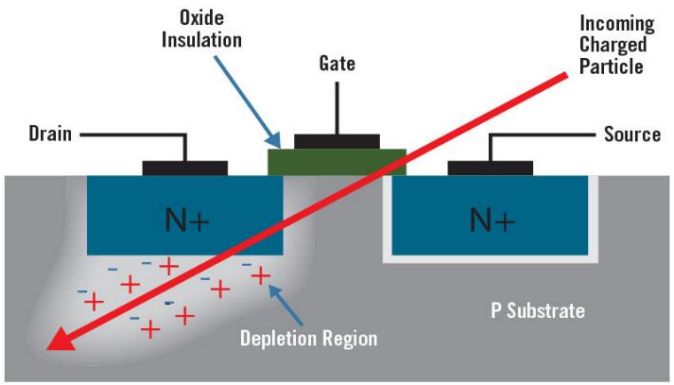
Special thanks to Pierre Barrillon, Denis Fougeron, Aneliya Karadzhinova-Ferrer, Rogelio Palomo, Milko Jaksic, Marlon Barbero

Single Event Upset (SEU) mechanism

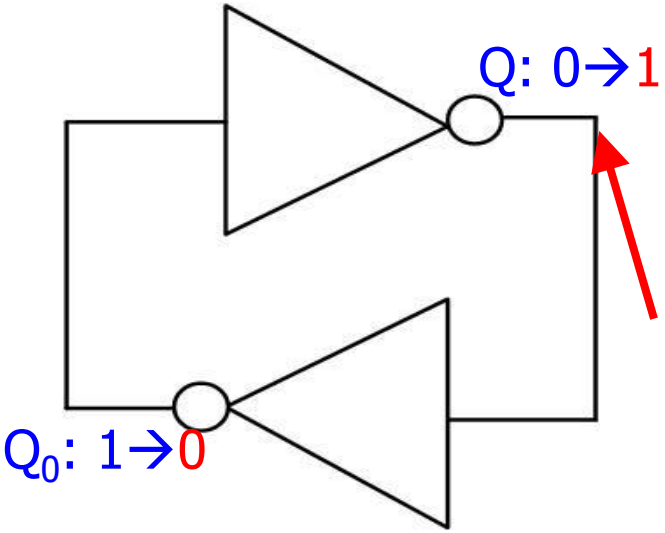
Energetic particle strikes → Creates ionization path with free e^- and holes



↓ Single Event Effect (SEE)

↓

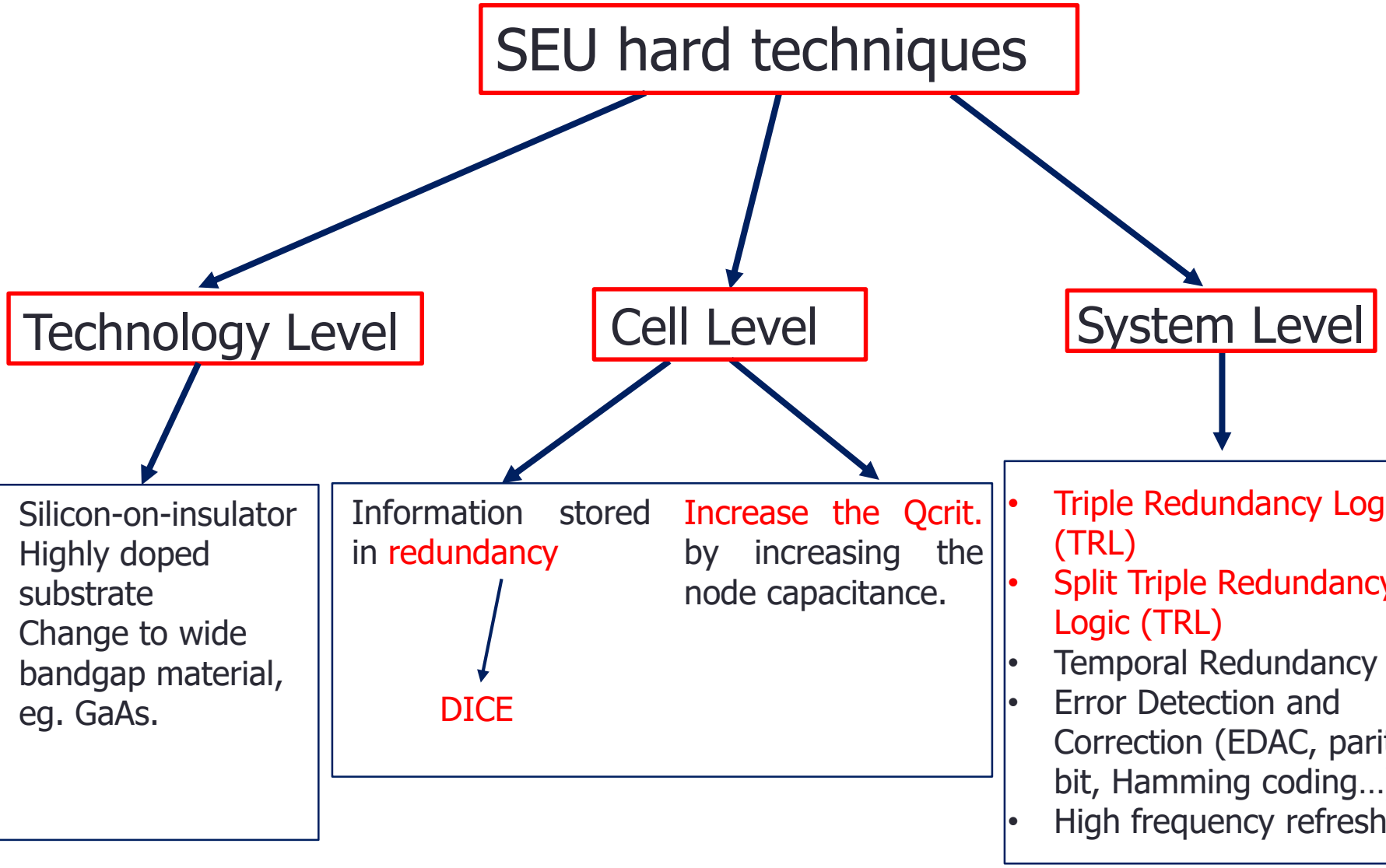
← Single Event Upset (SEU)



A particle strike
Bit Flip !!!

SEUs occur in memories (SRAMS,SDRAMS) and sequential logics!

SEU Hardening techniques



SEU tolerant memory for particle physics experiments

Particles deposit sufficient charge in small region of silicon. The charge might flip the state of a memory bit (SEU= Single Event Upset). For example, according to the HL-LHC and ATLAS detector specifications (for inner layer), we expect to get 0.2-0.5 GHz/cm² particle flux.

The main objective of the project is to design and compare SEU tolerant memories in several comparable technologies and nodes (AMS and TSI 180 nm HV, TowerJazz 180nm CIS, LFoundry 150nm). (The LATCH standard cell as a reference)

Measuring the cross section of 1-bit memory, allows to estimate the effect of the tolerance to SEU.

$$\sigma(\mathrm{BER/cm^2}) = \frac{N_{errors}}{\phi * Nlatches}$$

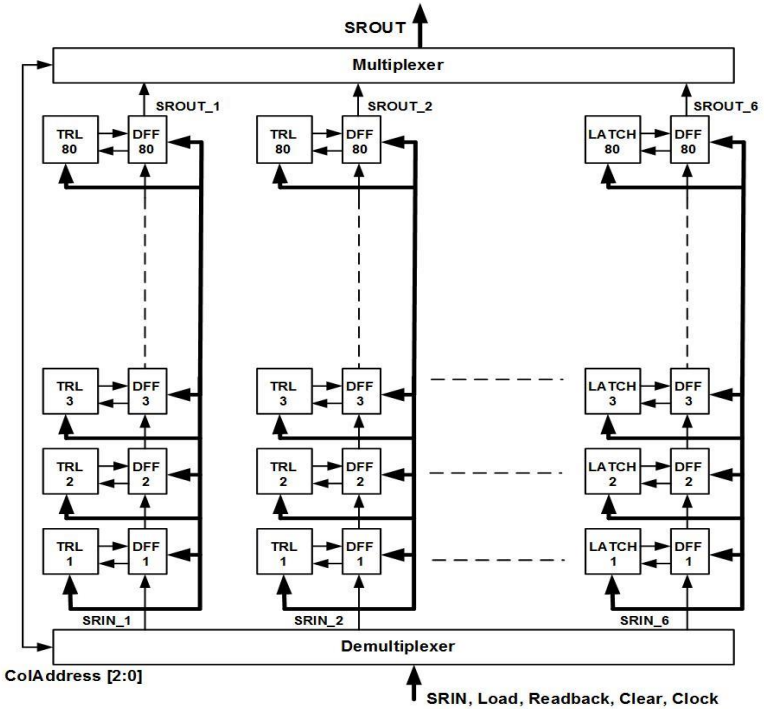
With BER (Bit Error Rate)= N_{error}/N_{latchs}

SEU tolerant test chips

- 4 SEU tolerant chips in 3 different technologies. Data from all latches can be collected and their behavior directly compared during irradiation tests

- The SEU chip is sub-divided in several columns (Typically 80 cells per kind of memories)

- Custom patterns are written and read through a shift register in synchronization with the beam.
- Custom pattern can be '000' (called 0->1) or '111' (called 1>0) writing. The reading should be same if no errors



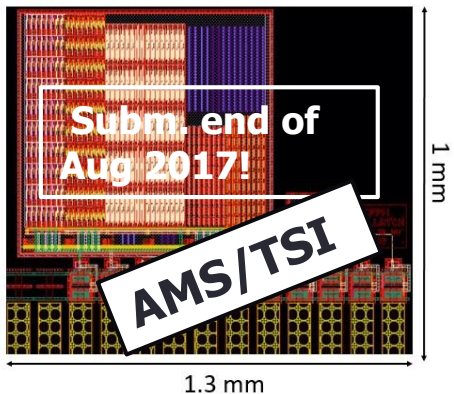
Sequence:

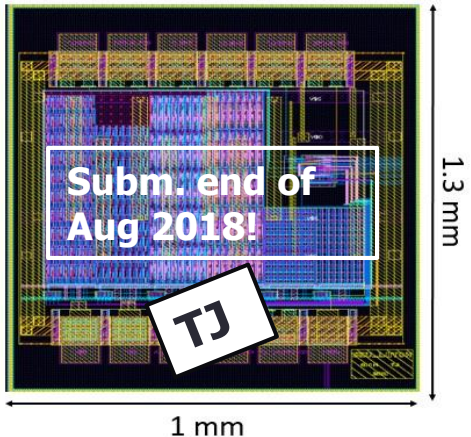
→ Put data into SR
→ Write into memory
→ Wait for the beam
→ Data back into SR
→ Read through the SR
→ Cal. # of errors

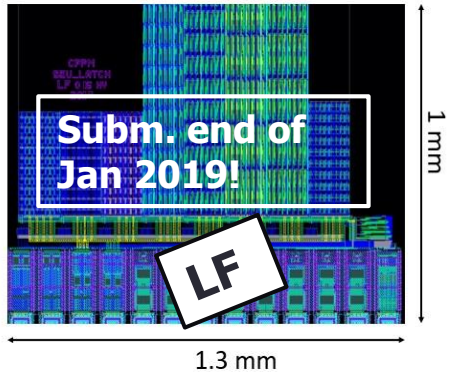
SEU tolerant memories (technology level)

Different flavors of memories:

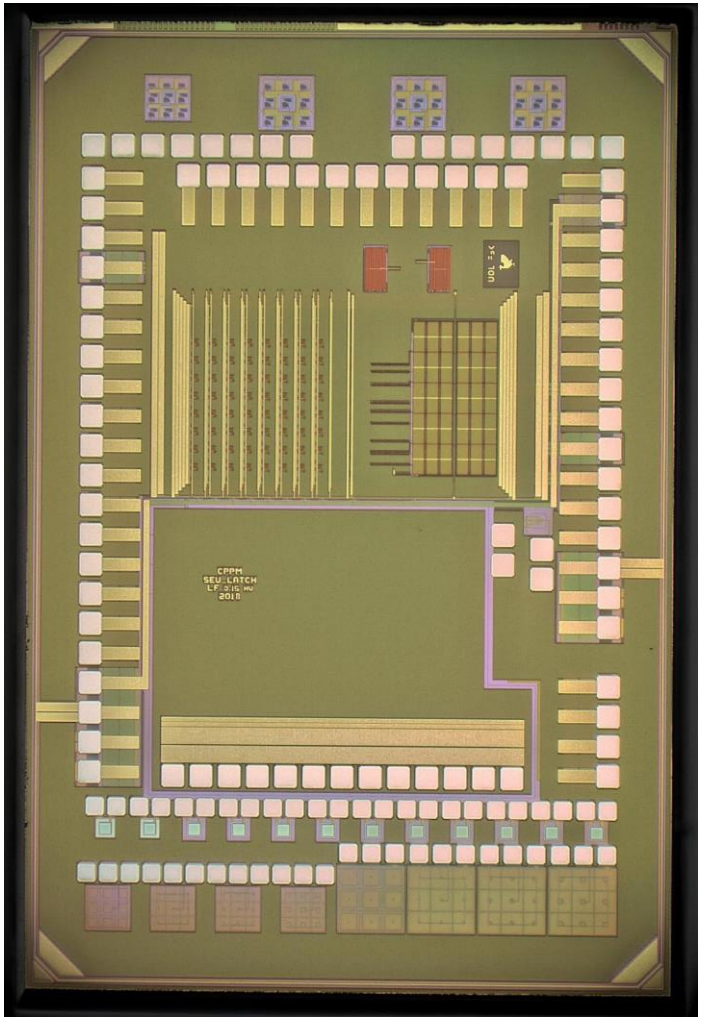
Column	AMS/TSI 180nm	TJ 180nm	LF 150nm
8	EMPTY	EMPTY	Standard cell
7	Triplication with DICE cell	Triplication with DICE cell	DICE cell
6	Triplication with Standard cell	Triplication with Standard cell	eDICE cell (enhanced)
5	Split Triplication with Standard cell	Split Triplication with Standard cell	Triplication with Standard cell
4	Split Triplication with Standard cell	Split Triplication with DICE cell	Triplication with DICE cell
3	Standard cell	Standard cell	Split Triplication with Standard cell
2	DICE cell	DICE cell	Split Triplication with DICE cell
1	EMPTY	EMPTY	SRAM

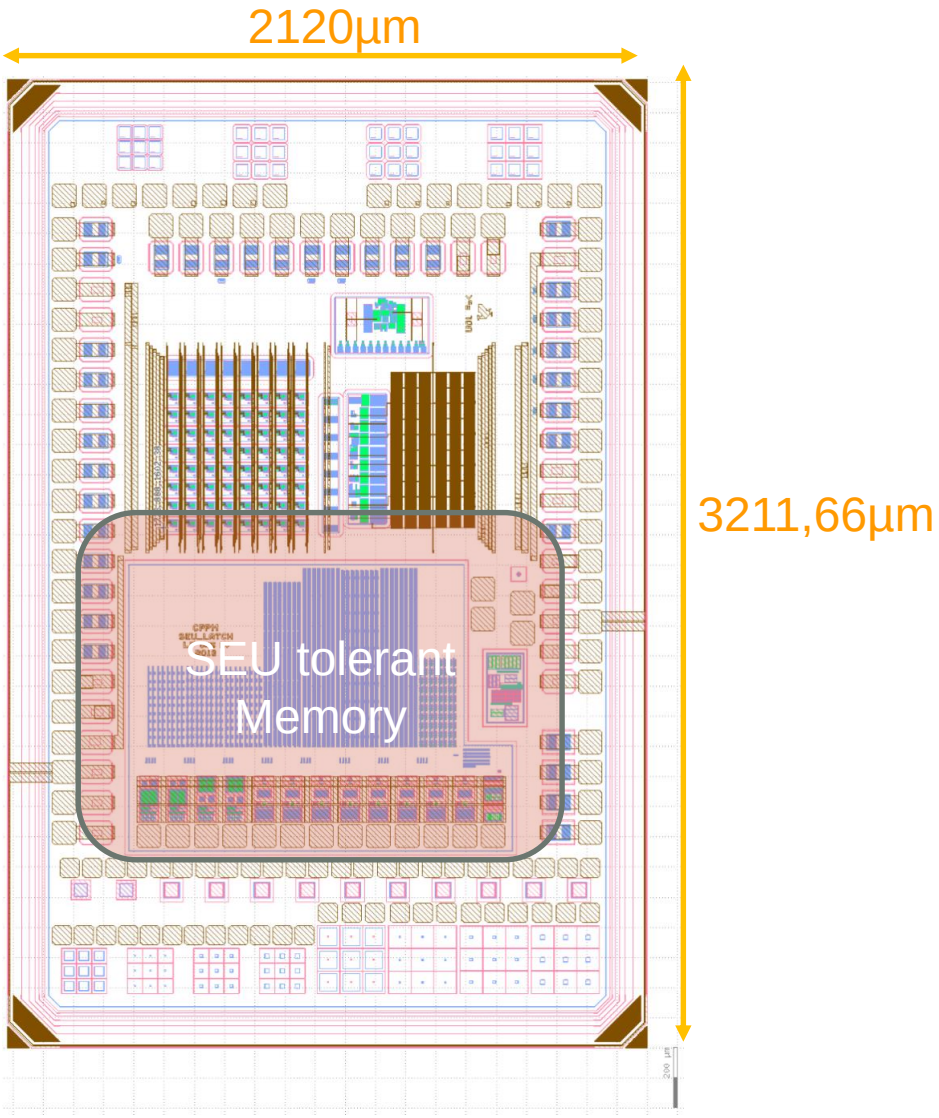






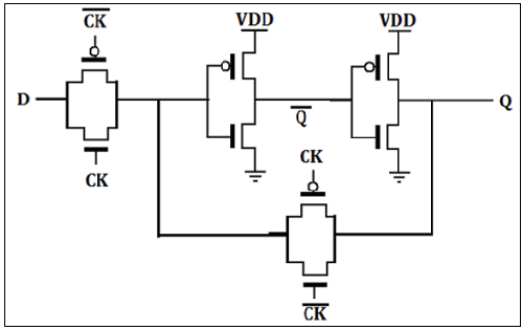
RD50-MPW2 Scope & Design Layout



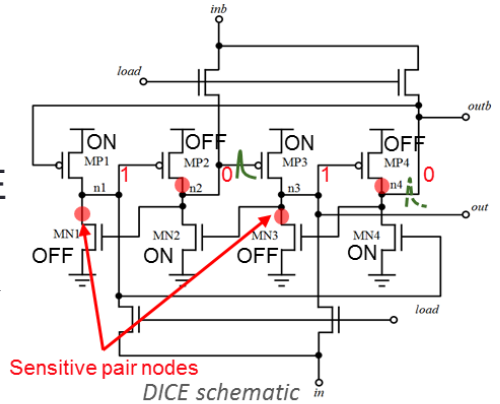


LFoundry Latch(s) description

- Standard cell "DF_X2" from the "lf15adlvt9s" library



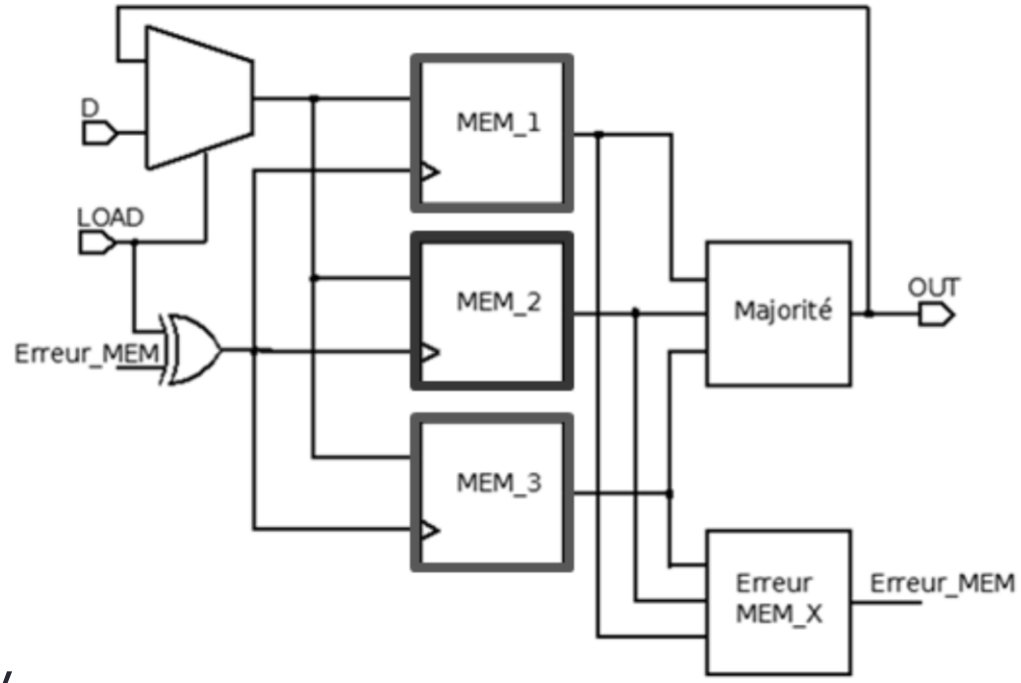
- DICE "Dual Interlocked Storage Cell" (full custom cell)
- DICE latch structure is based on the conventional cross coupled inverters:
  - The charges deposited by a ionising particle strike one node can't be propagated due to the stability of this architecture.
  - If 2 sensitive nodes (corresponding to the OFF transistors drain area) are affected simultaneously, the immunity is lost and the DICE latch is upset
- Enhanced DICE "Dual Interlocked Storage Cell" (full custom cell)
  - The distance between the 2 sensitive nodes (corresponding to the OFF transistors drain area) is bigger to increase the immunity



DICE schematic
(example of a stored data = 1)

Triple redundancy Architecture description

- Triple redundancy with a feedback correction commanded by a latch error detection.



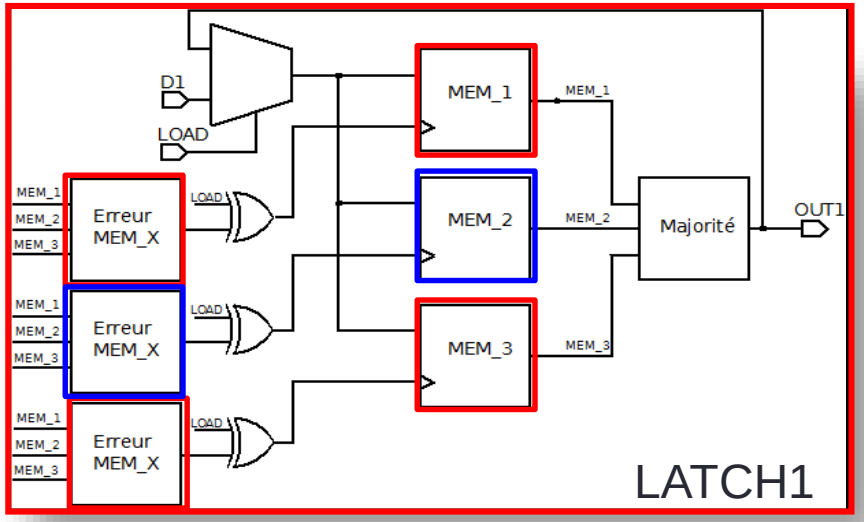
- MEM_x made by
  - Standard cell "DF_X2" from the "lf15adlvt9s" library

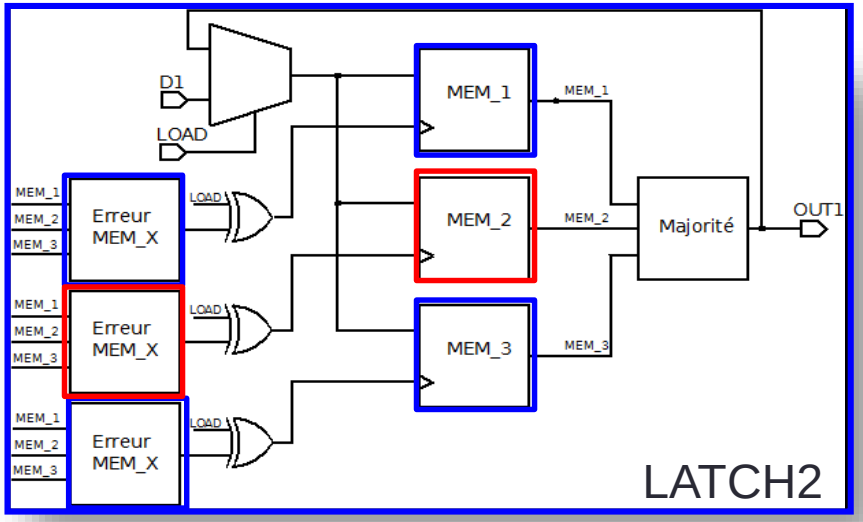
or

  - DICE "Dual Interlocked Storage Cell" (full custom cell)

Triple redundancy Architecture description (new approach)

SPLIT Triple redundancy with 2-bit to separate sensitive nodes





MEM_x made by

Standard cell "DF_X2"
from the "lf15adlvt9s" library

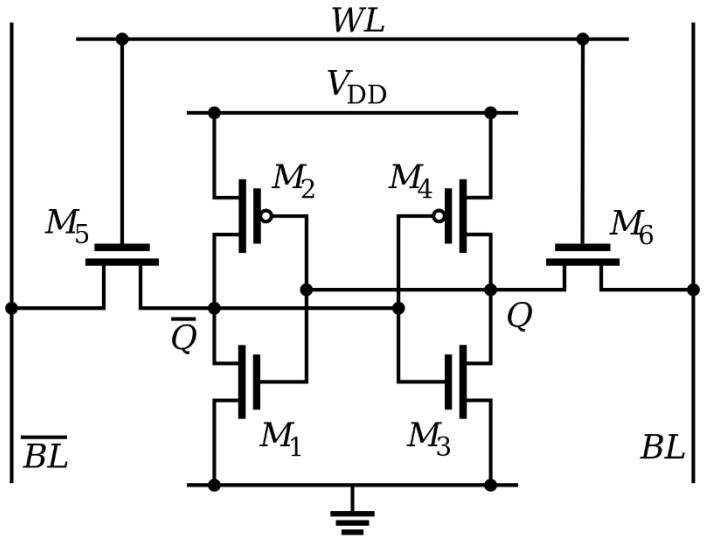
or

DICE "Dual Interlocked Storage Cell"
(full custom cell)

Latch(s) description

- SRAM memory (static RAM)

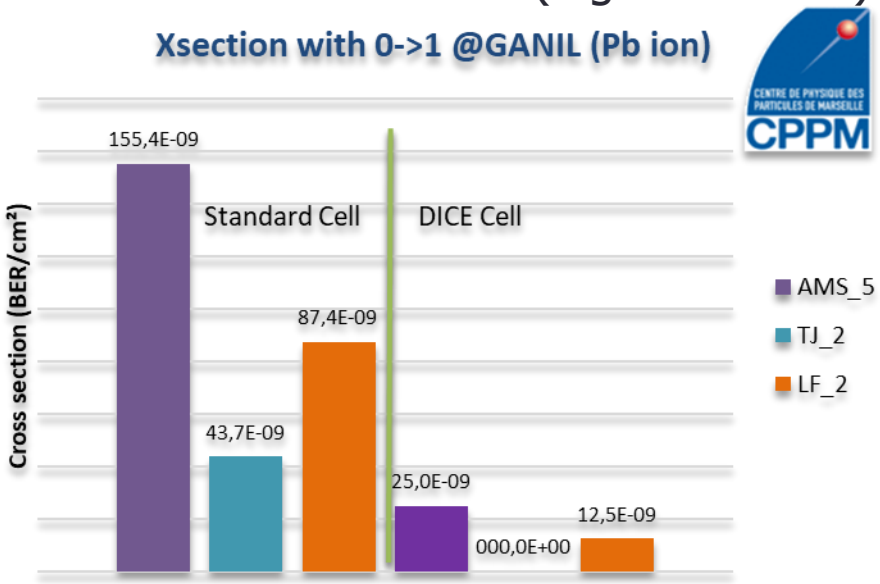
Full custom 6T CMOS RAM cell

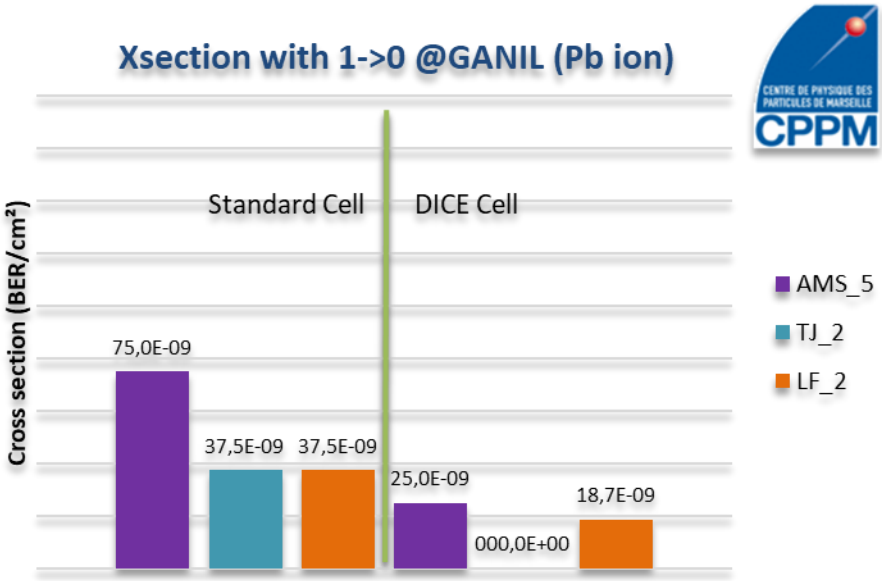


Comments

- To decrease the SEU sensitivity, we need to
  - Add redundancy on sensitive nodes (DICE and Triplication)
  - To increase the distance between sensitive nodes (enhanced DICE and SPLIT Triplication)
  - Or both

- The AMS, TJ, and LF chips were already tested (CERN, GANIL) with an equivalent LET at saturation results (high threshold)

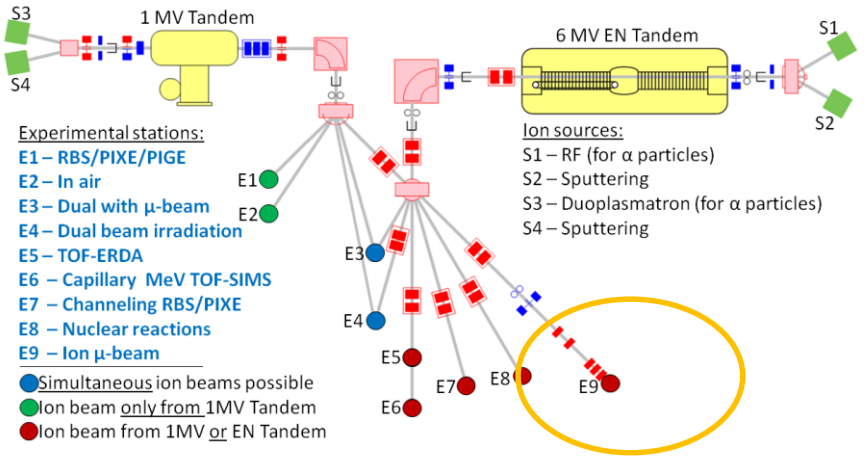




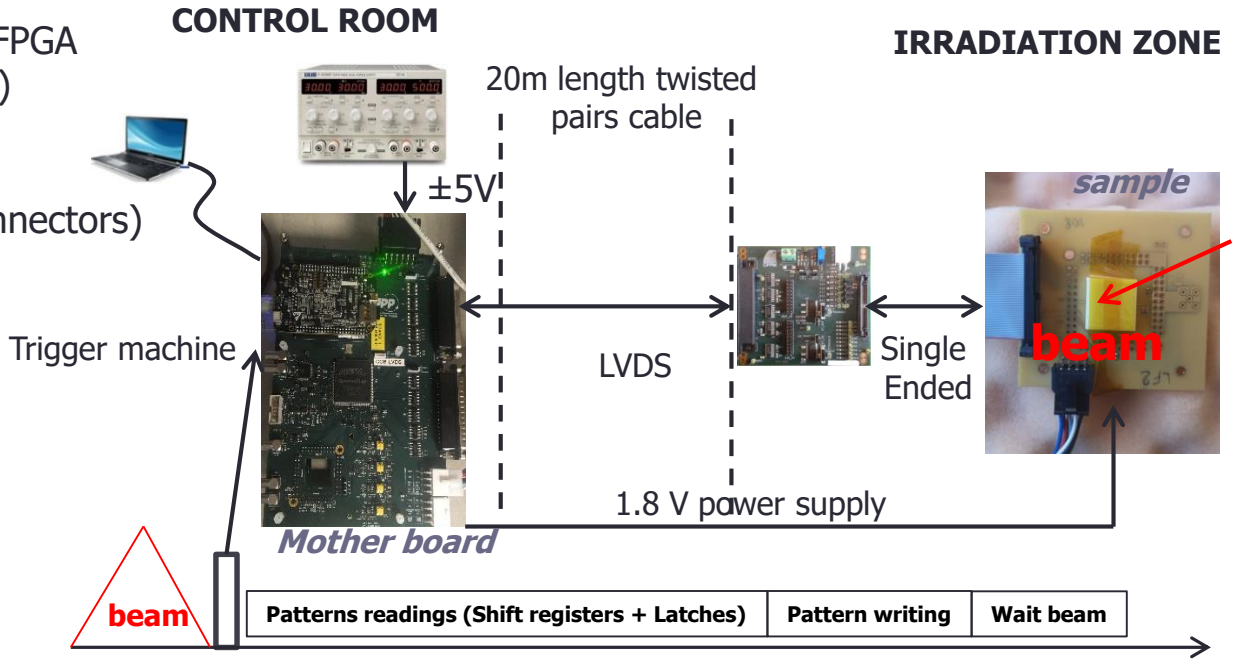
SEU Memory under wide GANIL Pb ion beam (LET = 73 MeV.cm²/mg)
Standard cell less tolerant than DICE cell for all technologies

Experimental Setup for LF chip at RBI

- **6MV Tandem Van de Graff at RBI**
  - E9 : Ion µbeam line, beam size 10 µm²
  - C12 Heavy ion at 21 Mev (LET ~5MeV/cm²/mg)
  - Flux estimated : 500E9 part/sec
  - one LF chip were installed



- **Mother board V3**
  - NanoPC BeagleBone card + FPGA
  - Flexible programming (VHDL)
  - Digital signals
    - 40 TTL signals
    - 32 LVDS signals (DB-37 connectors)
  - Analog channels
    - 4 SAR ADC (16 bits)
    - 10 DAC (16 bits)
  - Lab tests + irradiation tests

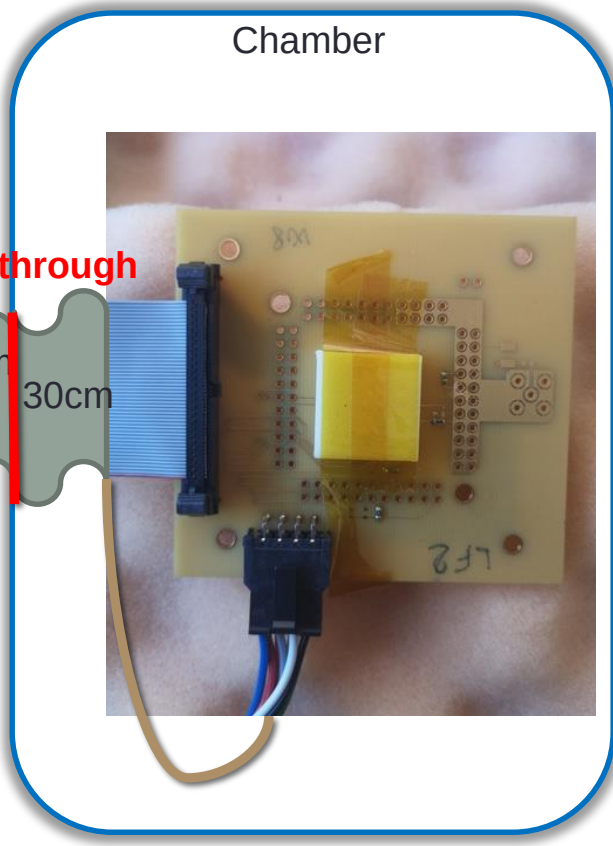


Setup from CPPM

2 DUT boards are working well (the Global Memory has no errors).
The software (Beaglbone) is managed manually (no trigger signal)

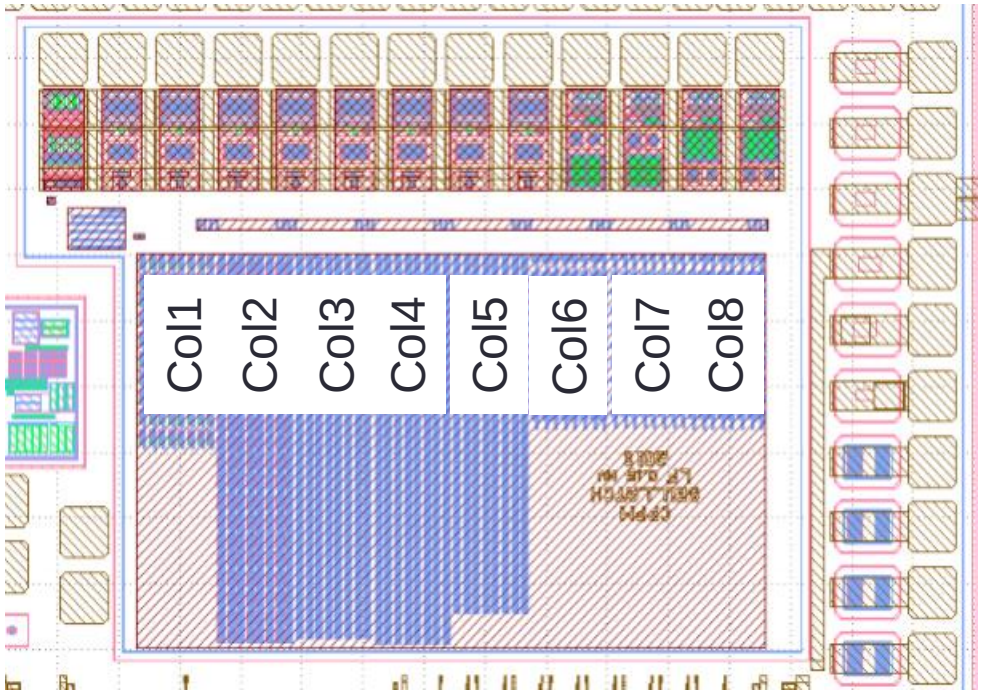
The PROTO65N board should be V3 or V4.
Firmware is not compatible with the downgraded version (V2 etc)

The intermediate board (single-end vs LVDS) is placed closed to the chamber



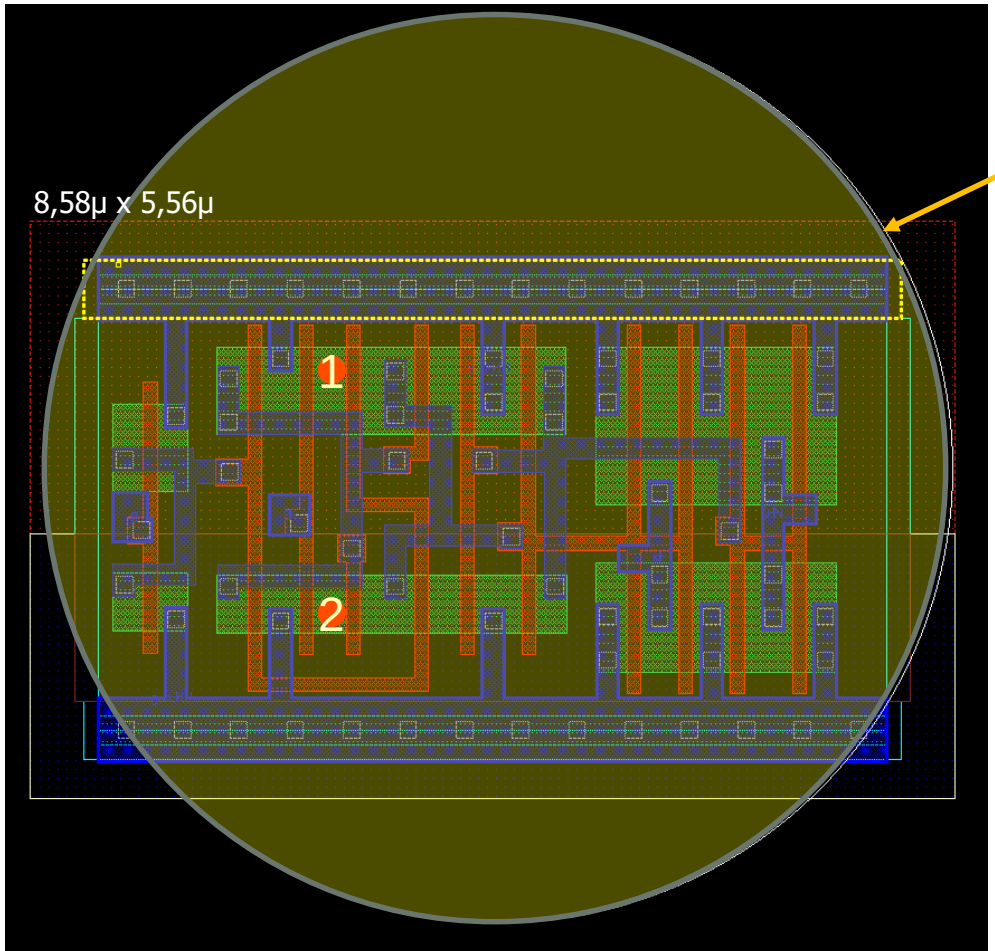
CPPM's Memory : columns position

Column	LF 150nm (N°2)
8	Std cell
7	DICE cell
6	eDICE cell (enhanced)
5	1-bit TRL with Std cell
4	1-bit TRL with DICE cell
3	Split TRL with std cell
2	Split TRL with DICE cell
1	SRAM



Col 8 : STANDARD LATCH : LX_X2

To fire the latch, two points can be separately hit on the drain side of the PMOS or the NMOS transistors.

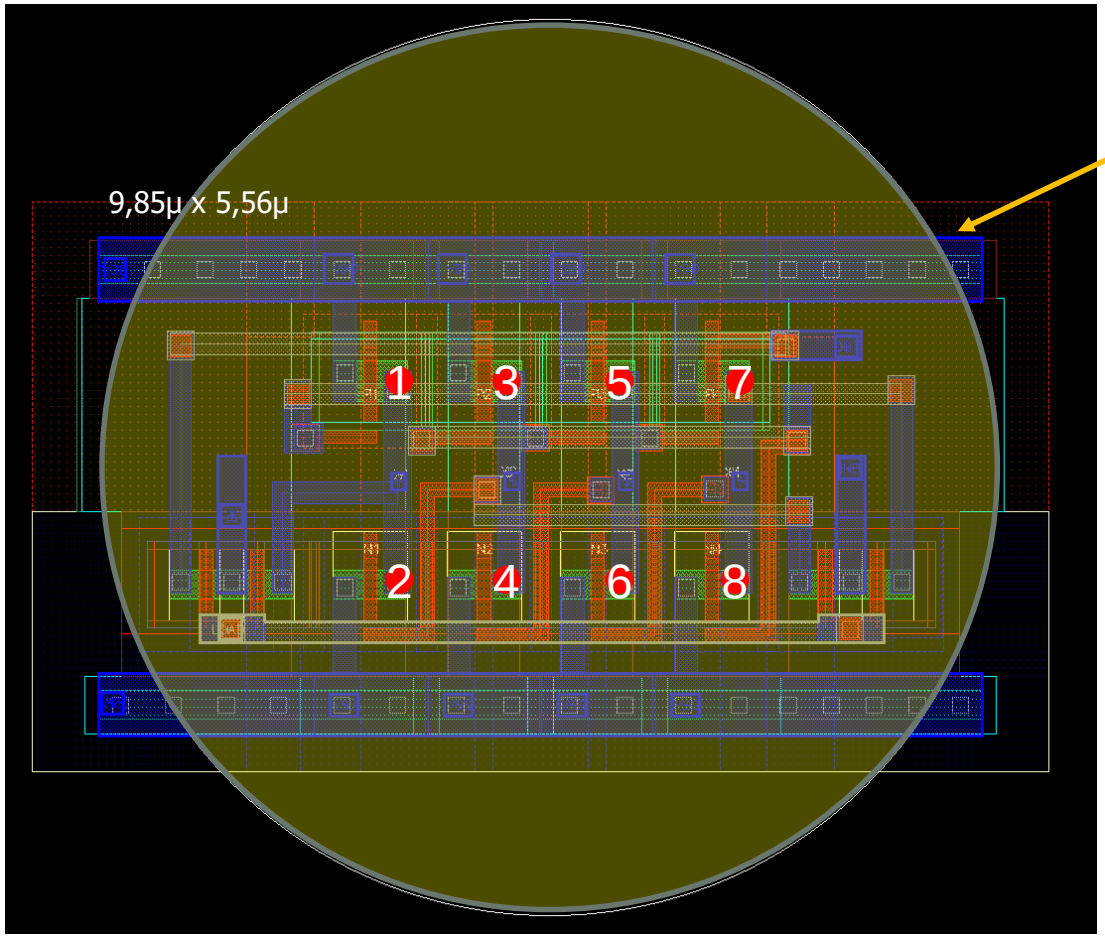


10µm² Spot size

Because the beam size is bigger than 1µm² @RBI, we will hit the whole cell

Col 7 : CUSTOM LATCH : CPPM_DICE_LF

To fire the latch, height points can be separately hit on the drain side of the PMOS or the NMOS transistors.

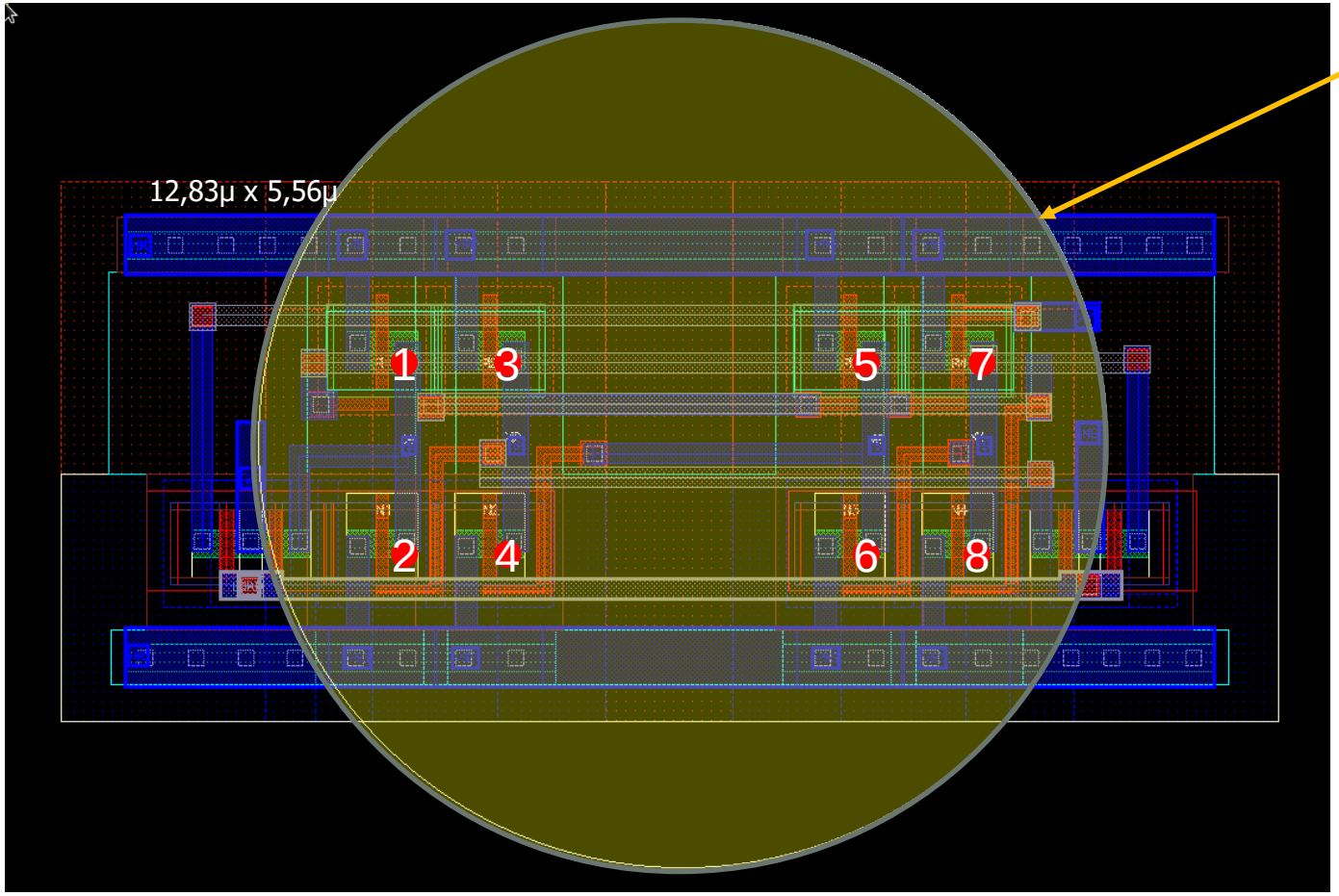


10µm² Spot size

Because the beam size is bigger than 1µm² @RBI, we will hit the whole cell

Col6 : CUSTOM LATCH : CPPM_eDICE_LF

To fire the latch, height points can be separately hit on the drain side of the PMOS or the NMOS transistors.

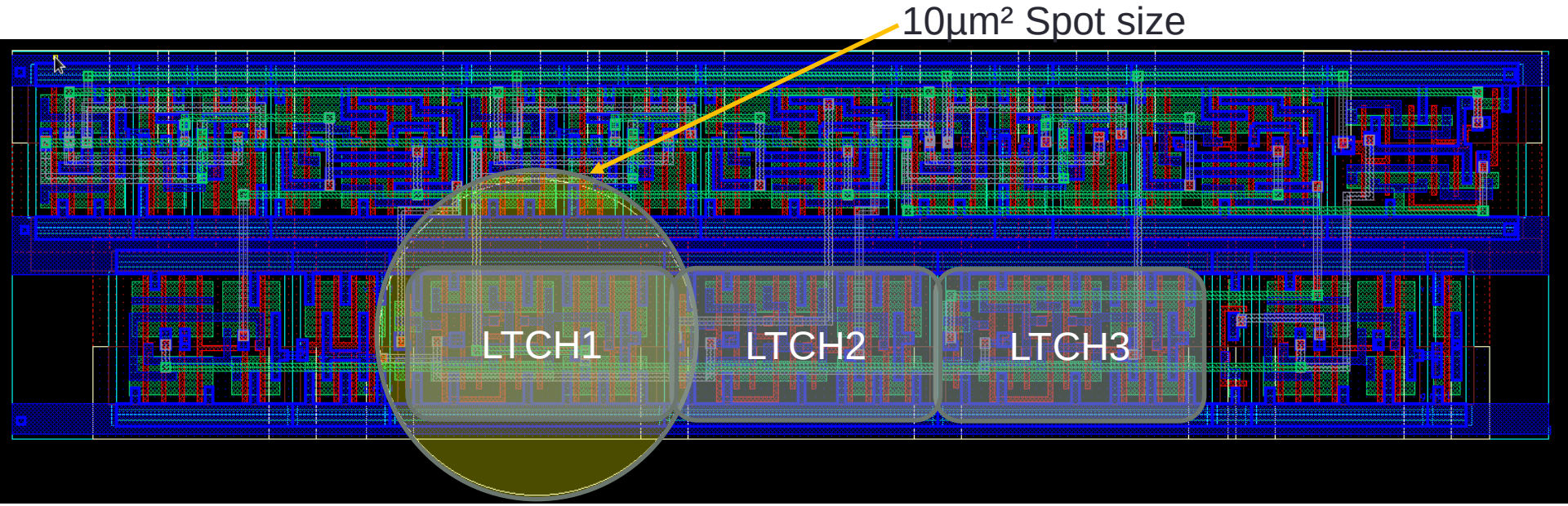


10µm² Spot size

Because the beam size is bigger than 1µm² @RBI, we will hit the whole cell

Col5 : STANDARD LATCH (LX_X2) : TRipLication

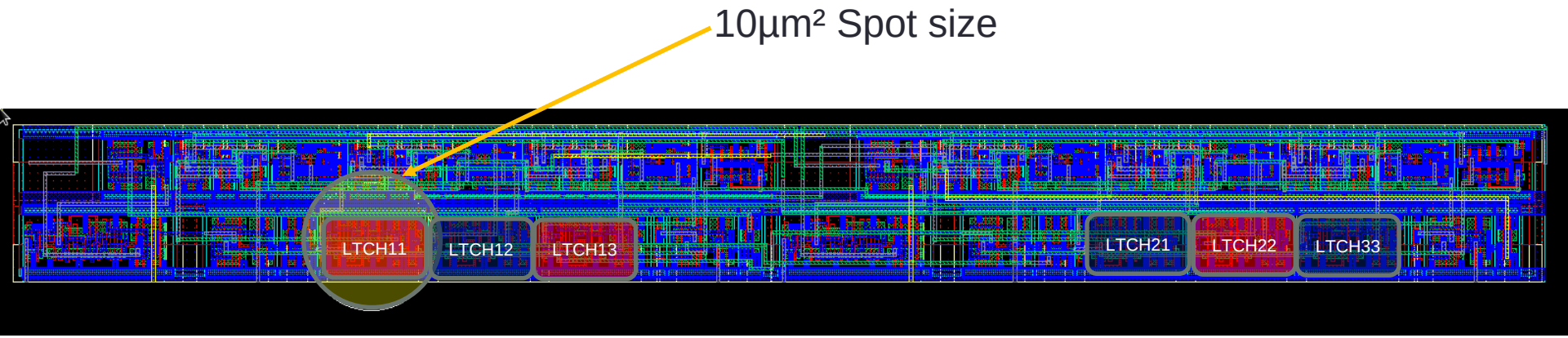
To fire one of the three latch, two points can be separately hit on the drain side of the PMOS or the NMOS transistors.



Because the beam size is bigger than 1µm² @RBI, we will hit one whole cell on three

Col3 : STANDARD LATCH (LX_X2) : SPLIT TRipLication

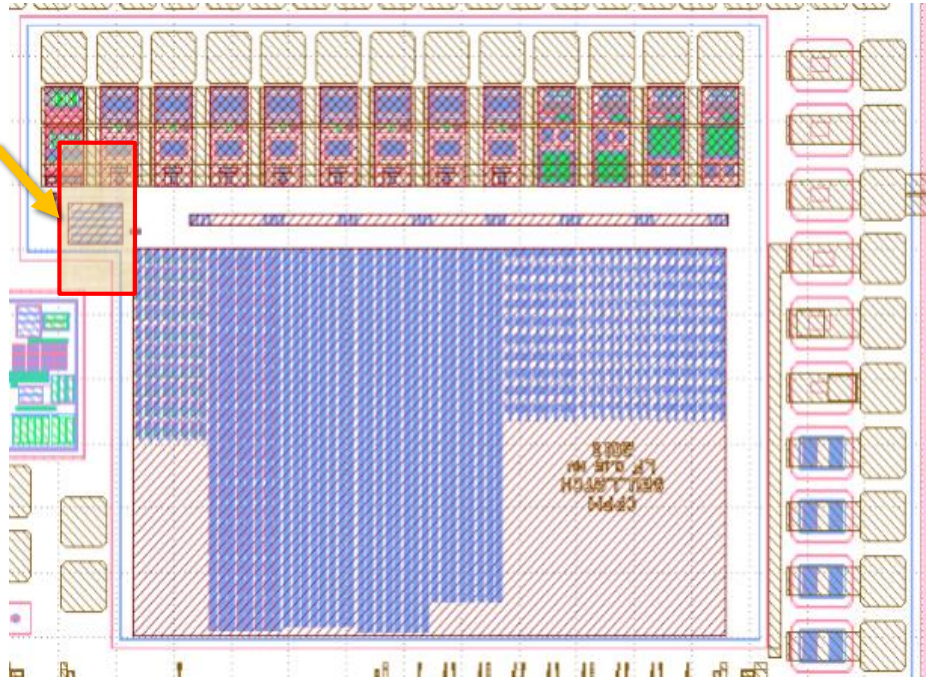
To fire one of the three latch, two points can be separately hit on the drain side of the PMOS or the NMOS transistors.



Because the beam size is bigger than 1µm² @RBI, we will hit one whole cell on six

Results : Global Nodes

The beam size is a spot of 10µm².
The beam scans the actual window by 121µsec/pixel.
The map size is 128 x 128 pixels
The window is covered in 1.98sec
LET = 5 MeV-cm2/mg



The scanned beam was applied on the *global signals generator* area for 60sec (30 loops)

Flux (part/sec/cm²) :

- For '000' loading the flux is 606.1E+9
- For '111' loading the flux is 538.8E+9

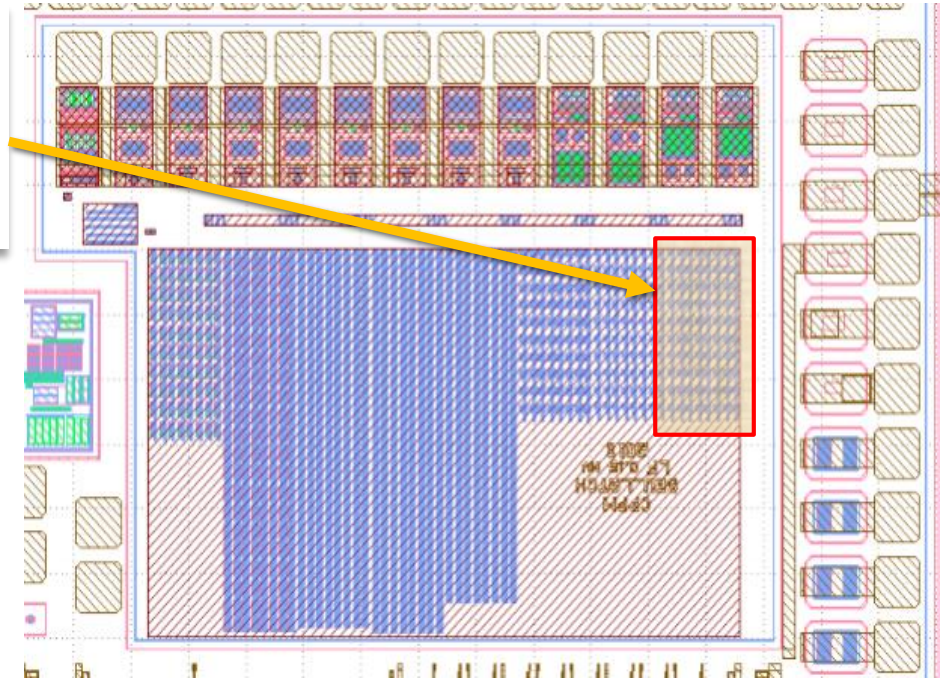
SET (Single Event Transient) appeared
When loading '000' on Shift Register :
Col 6, Col 5, Col 4
When loading '111' on Shift Register :
Col 7, Col 6, Col 4, Col 3, Col 2

No way to discriminate the source of the SET
Conclusion :
The chip is sensitive to SET. Need to be hardened

Global Signal Generator includes
Clock : to cadence the Shift Register
Data : to feed the Shift Register
Load : to load data on Latch
ReadBack : to read-back data from latch to Shift Register
Enable : to enable the output buffer

Results : Standard Cell

The beam size is a spot of 10µm².
The beam scans the actual window by 121µsec/pixel.
The map size is 128 x 128 pixels
The window is covered in 7.45sec
LET = 5 MeV-cm2/mg



The scanned beam was applied on the *Standard Cell* area area for 60sec (8 loops)

Flux (part/sec/cm²) :

- For '111' loading the flux is 3.64E+11

- Standard cell "DF_X2"
  from the "lf15adlvt9s" library

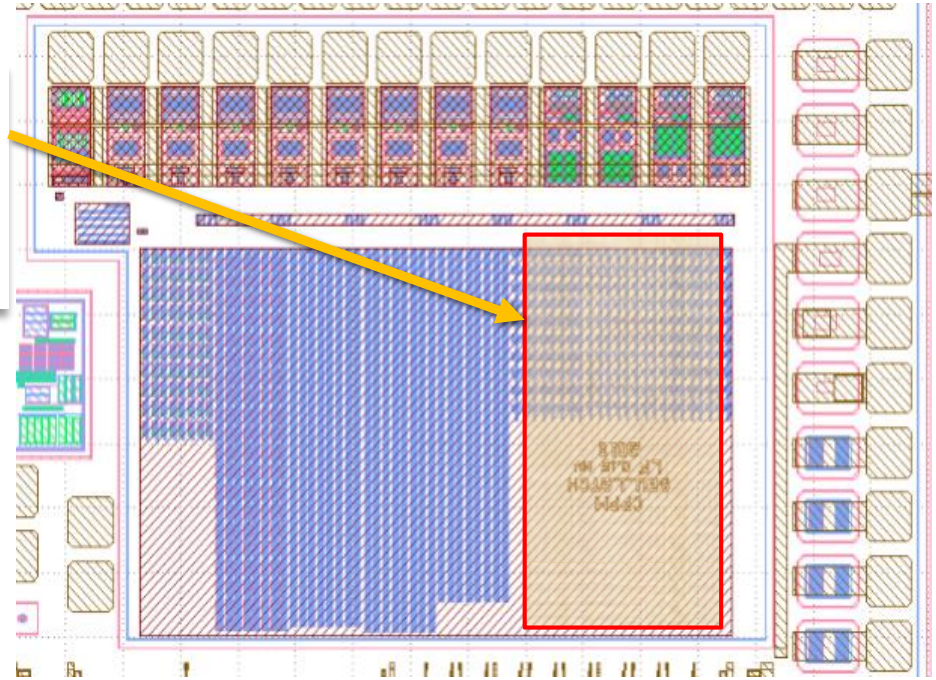
SEE (Single Event Upset) appeared
When loading '111' on Shift Register :

Cross section : 240.6E-15 err/cm²

Conclusion :
Because of low LET, the cross section value (240.6E-15 err/cm²) is lower than expected on saturated state (18.7E-9 err/cm²)

Results : Dice cell

The beam size is a spot of 10µm².
The beam scans the actual window by 121µsec/pixel.
The map size is 256 x 256 pixels
The window is covered in 7.92sec
LET = 5 MeV-cm2/mg



The scanned beam was applied on the global signals generator area for 600sec (75 loops)

Flux (part/sec/cm²) :

- For '000' loading the flux is 1.01E+12
- For '111' loading the flux is 4.66E+12

- Customed DICE cell

SEE (Single Event Upset) appeared

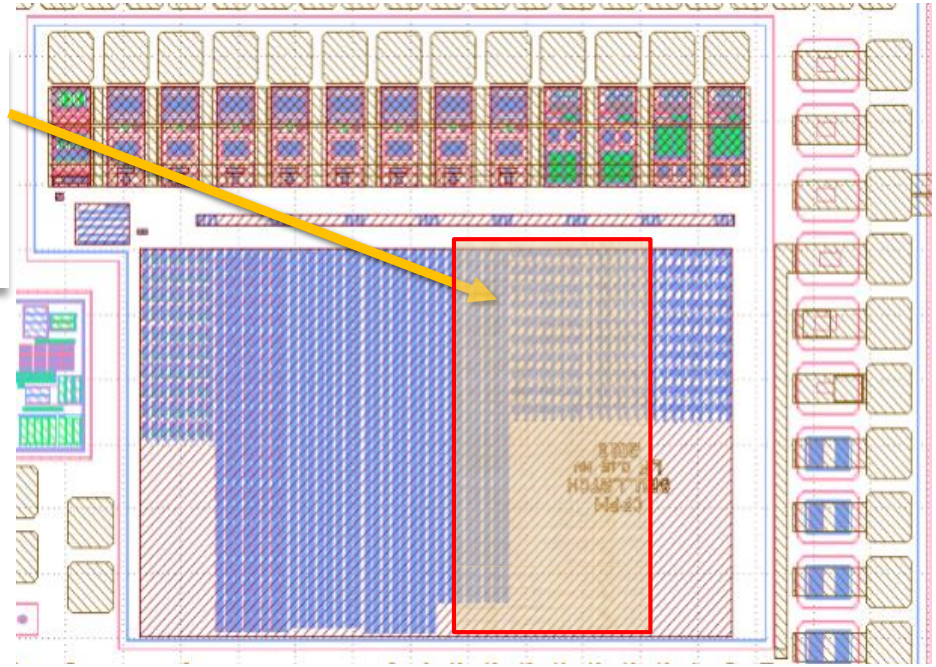
When loading '000' on Shift Register :
Cross section : 259.3E-15 err/cm²

When loading '111' on Shift Register :
Cross section : 8.1E-15 err/cm²

Conclusion :
Because of low LET, the cross section value
when loading '000' (259.3E-15 err/cm²) is lower than expected on saturated state (12.5E-9 err/cm²)
- when loading '111' (8.1E-15 err/cm²) is lower than expected on saturated state (18.7E-9 err/cm²)

Results : eDice cell

The beam size is a spot of 10µm².
The beam scans the actual window by 121µsec/pixel.
The map size is 256 x 256 pixels
The window is covered in 7.92sec
LET = 5 MeV-cm2/mg



The scanned beam was applied on the global signals generator area for 600sec (75 loops)

Flux (part/sec/cm²) :

- For '111' loading the flux is 3.7E+12

- Customed DICE cell

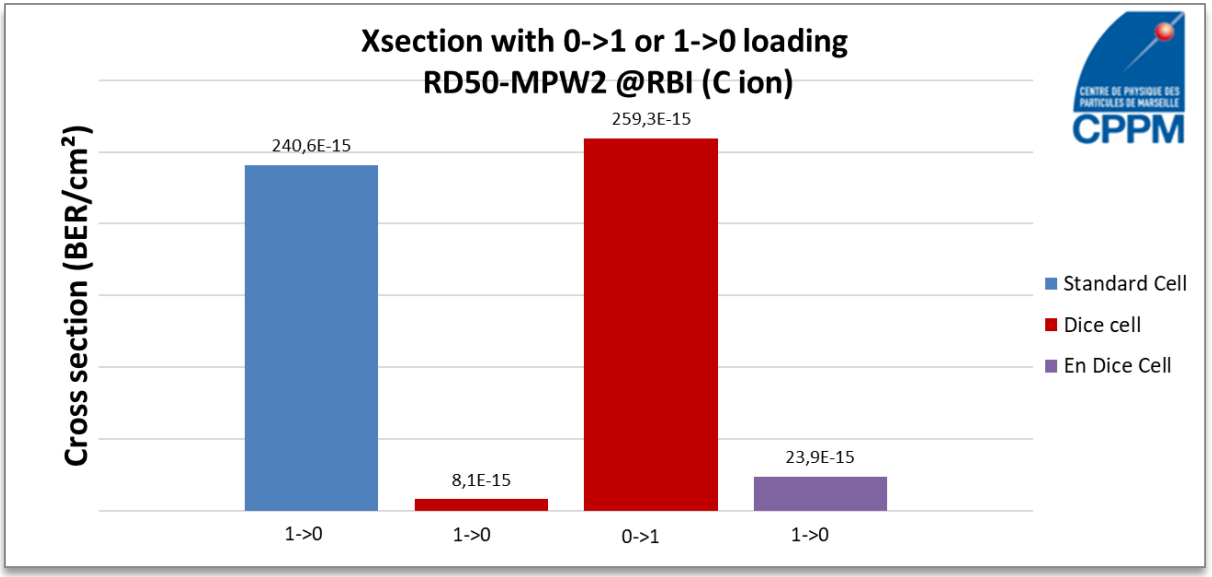
SEE (Single Event Upset) appeared
When loading '111' on Shift Register :
Cross section : 23.9E-15 err/cm²

Conclusion :
The eDICE cell has roughly the same results than the DICE cell

RESULTS

- The SEU Tolerant memory is sensitive to SET. Global nodes should be hardened
- The LF standard cell shows some SEU results at low LET threshold, but cannot be compared from GANIL test (made at high LET threshold), and not with Protons beam @CERN

- The Standard cell is less tolerant than the DICE (eDICE) cells. No real benefice of the eDICE



- Only single LATCH have results. The Triplication cells need more time to get error or else the beam size is to small to hit several latches in the same time.

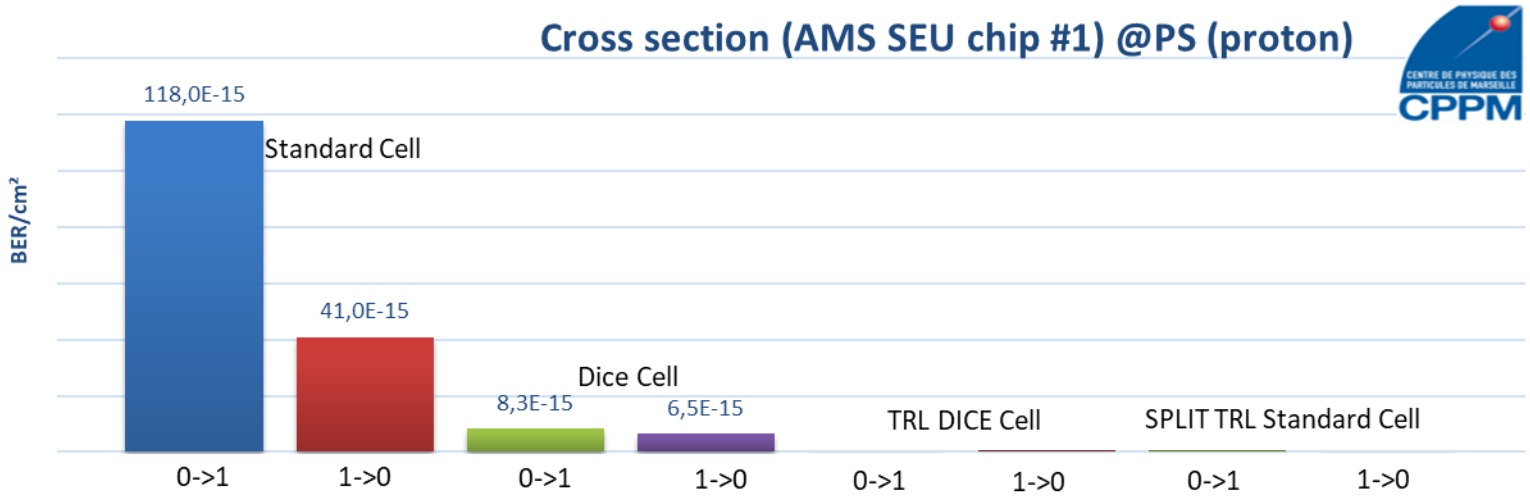
Conclusion

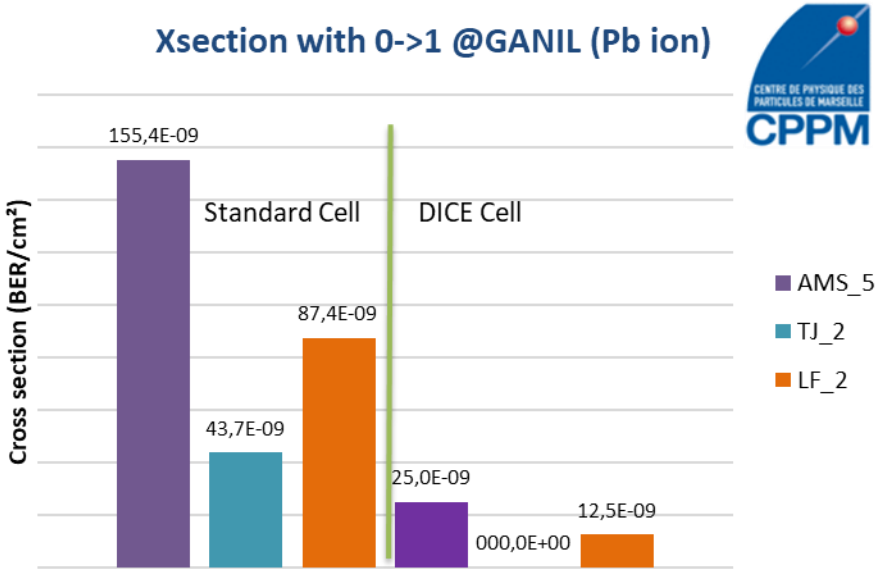
- The SEU tolerant memory from the RD50-MPW2 chip was tested under a C_{12} ion at 21 Mev (LET ~5MeV/cm²/mg) on the RBI Ion µbeam line with a beam size of 10 µm². The µbeam line is able to reach 1µm² beam size by using an other ion than the C_{12} one
- The µbeam is scanned under a fixed area, in order to cover a bigger surface (speed few 1-2µm/µsec)

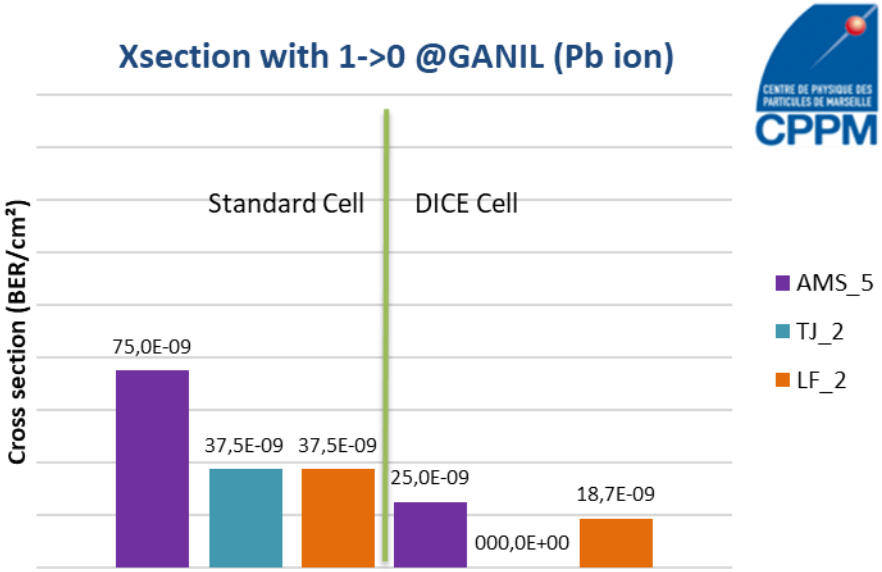
- To compare with other technologies (AMS, TSI, TJ), the test should be done with wide beam and higher LET (saturation) with more time exposure

- The µbeam approach will be very interesting to study the cell itself (single one : Std or DICE) and not the Triplication architecture.

BACKUP


Cross section (AMS SEU chip #1) @PS (proton)
BER/cm²
118,0E-15
Standard Cell
41,0E-15
8,3E-15
Dice Cell
6,5E-15
TRL DICE Cell
SPLIT TRL Standard Cell
0->1
1->0
0->1
1->0
0->1
1->0
0->1
1->0


Xsection with 0->1 @GANIL (Pb ion)
Cross section (BER/cm²)
155,4E-09
Standard Cell
DICE Cell
87,4E-09
43,7E-09
25,0E-09
000,0E+00
12,5E-09
AMS_5
TJ_2
LF_2


Xsection with 1->0 @GANIL (Pb ion)
Cross section (BER/cm²)
Standard Cell
DICE Cell
75,0E-09
37,5E-09
37,5E-09
25,0E-09
000,0E+00
18,7E-09
AMS_5
TJ_2
LF_2