CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE CPPM

Aix-Marseille université

SMALL SENSOR DIODES WITH LFOUNDRY 150NM

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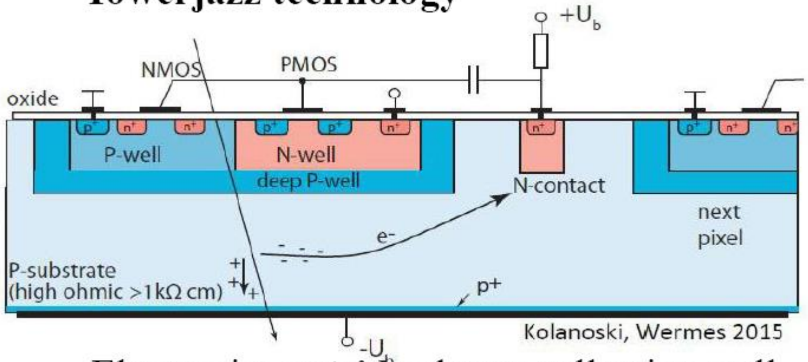
29 july 2021

Motivations

- Two design approaches

"Small Collection Diode" design:

Towerjazz technology



Electronics **outside** charge collection well

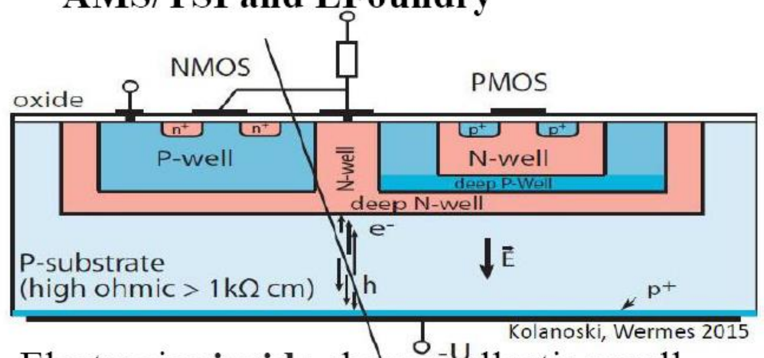
PROS: **Small sensor capacitance → Low power consumption and noise**

CONS: **Long drift distances → Less radiation hard**

$$ENC^2_{thermal} \propto \frac{4}{3}\frac{kT}{g_m}\frac{\mathbf{C_d^2}}{\tau}$$

"Large Collection Diode" design:

AMS/TSI and LFoundry



Electronics **inside** charge collection well

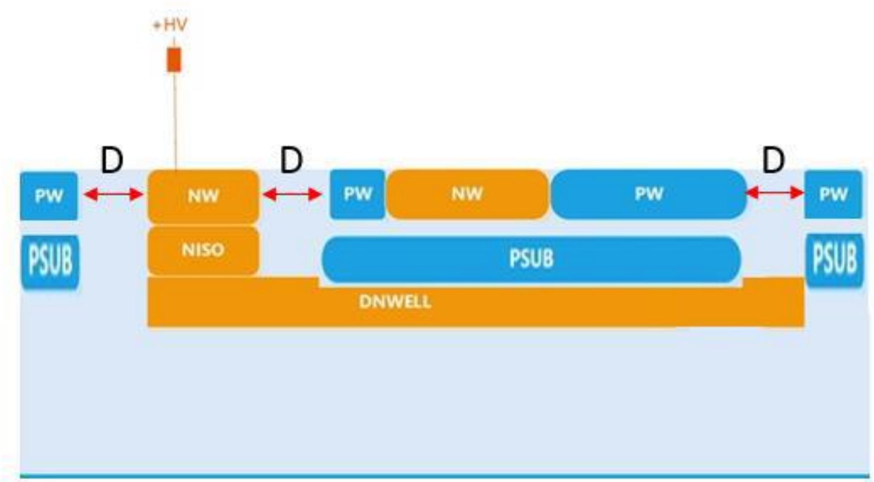
PROS: **Short drift distances→ Radiation tolerant**

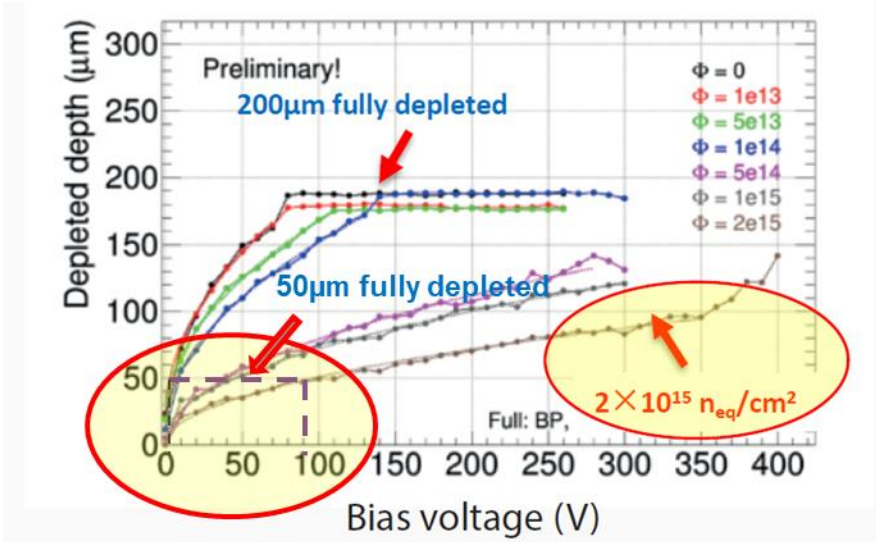
CONS: **Large sensor capacitance → Noise & speed (power) penalties**

$$\tau_{CSA} \propto \frac{1}{g_m}\frac{\mathbf{C_d}}{C_f}$$

New Rad-Hard Small pixel approach

- Let think to reach a pixel size of 50µm x 50µm x 50µm
  - 50µ x 50µ square and 50µ depth
  - From ~10V (no Irrad) to 90V ($2x10^{15}$ neq/cm²)
  - With Backside Metallization
  - Less restrictive guardings
  - Uniform drift field

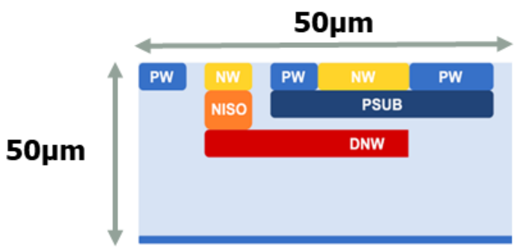




I.Mandić, et al., DOI: 10.1016/j.nima.2018.06.062

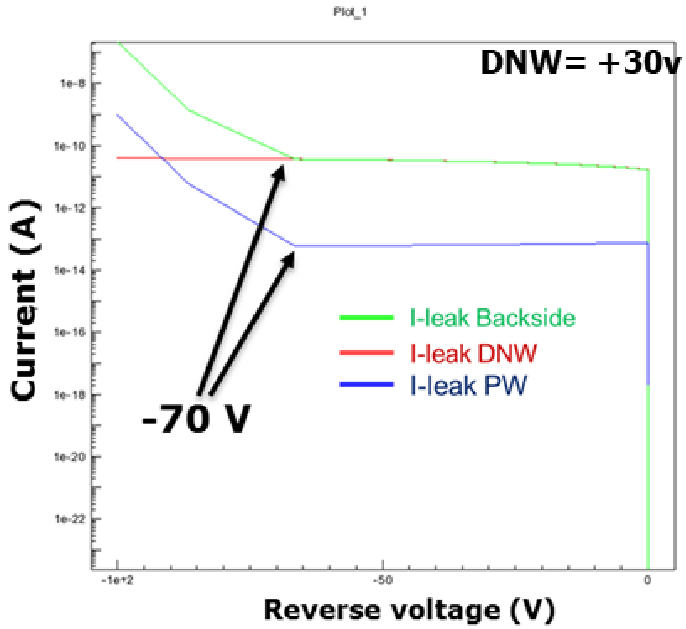
D= distance (very important parameter)

How to reach HV=100V?



Smaller size of the pixel (50µm× 50µm x 50µm)

The total Voltage potential (top to bottom) at **100 V** is achieved and the substrate is fully depleted (50µm)



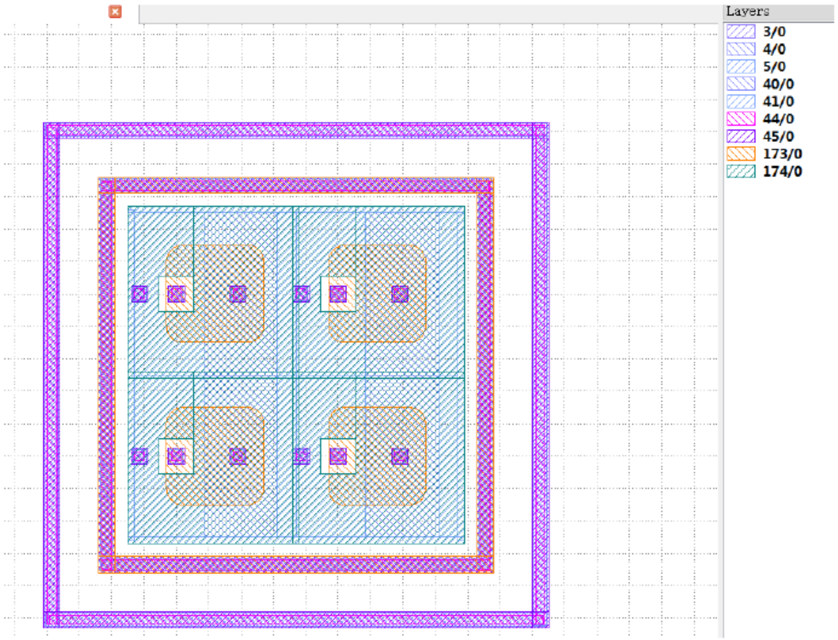
By applying Voltage on TOP and Bottom

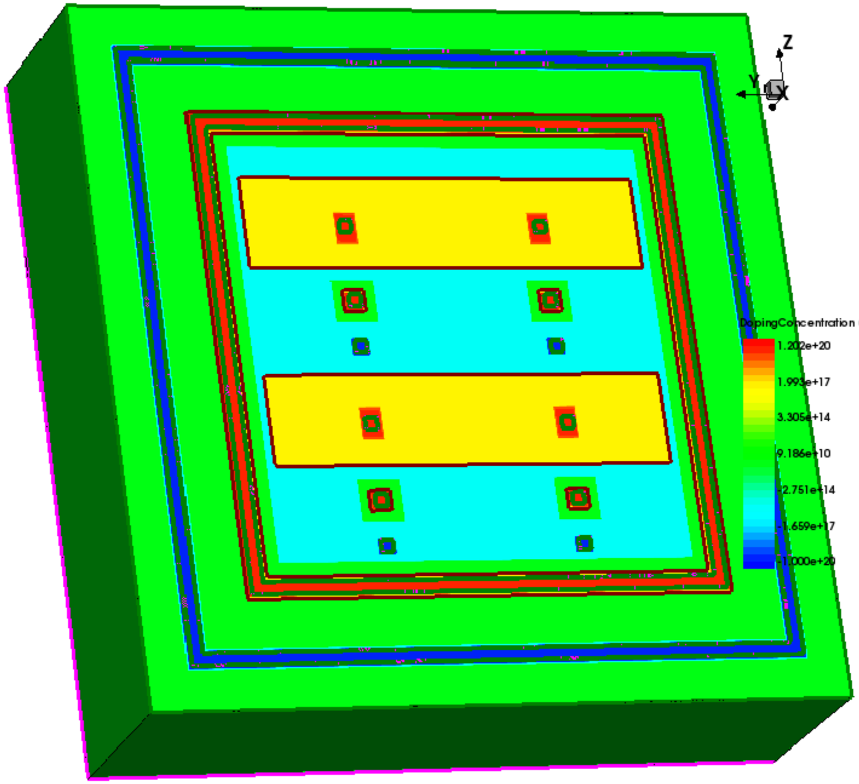
And the thickness should be 50µm if we want to keep the pixel efficiency

All TCAD simulations come from TCAD profile from foundry and all results were validated by Lfoundry.

TCAD 3D Simulation

- Matrix 2x2



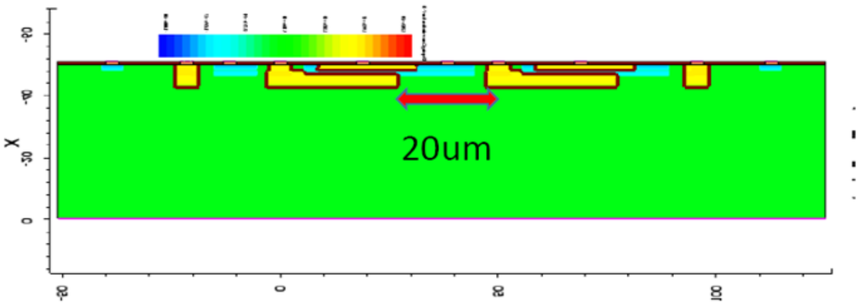


TCAD 3D Simulation

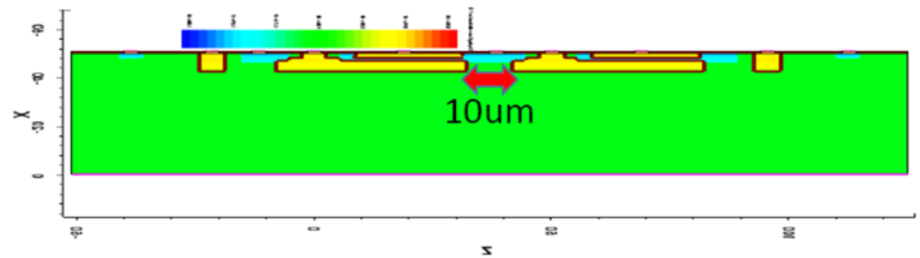
4 structures according the distance between pixels (DNW gap)

Bigger is the DNW area, higher is the BV, but higher is the capacitance

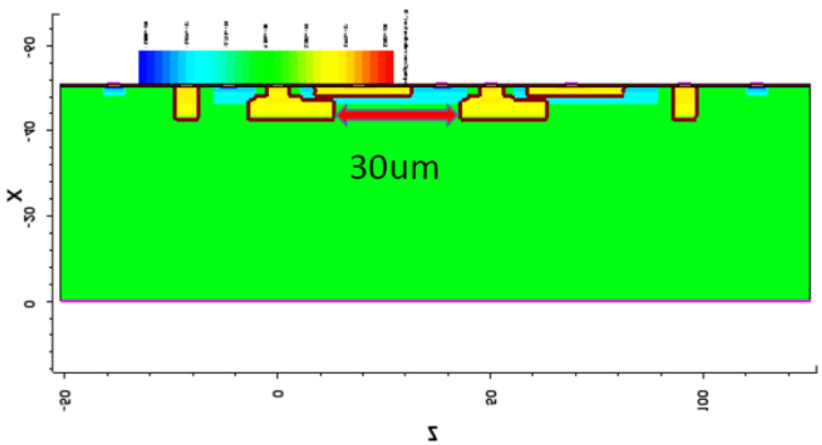
Trade-off between DNW area and capacitance value



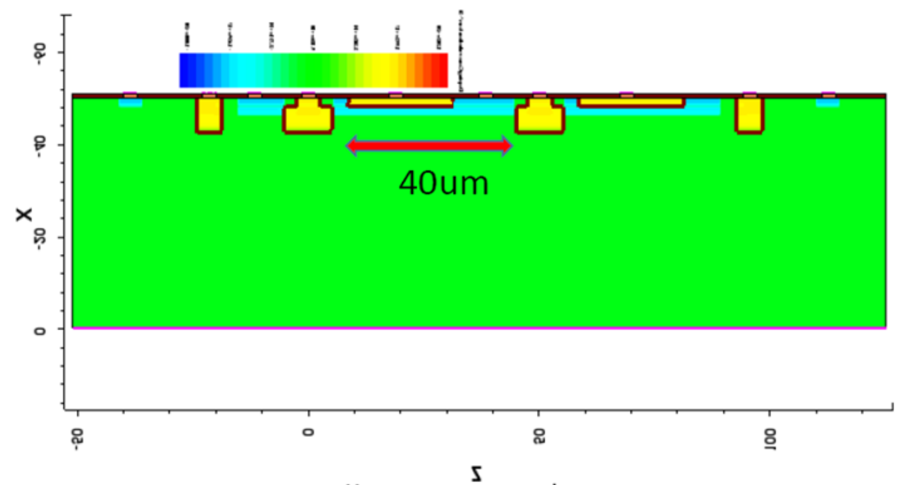
Dnwell area:30um*30um



Dnwell area:40um*40um



Dnwell area:20um*20um



Dnwell area:10um*10um

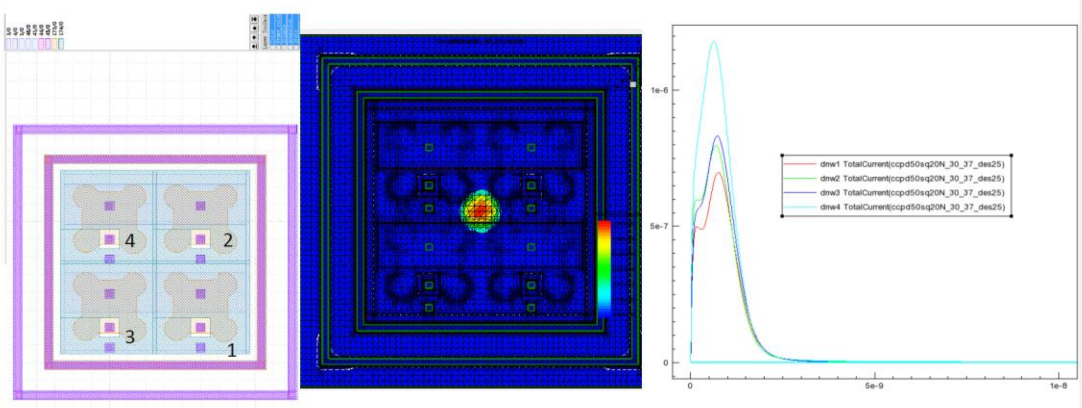
TCAD simulations

The study also shows that the pixel corners represent a weak point, since the distance between DNW is at its maximum. This means a higher probability for a punch-through between the PSUB layer and the substrate.

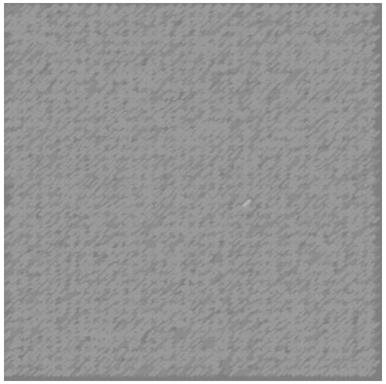
To resolve this problem, four diode structures were proposed:

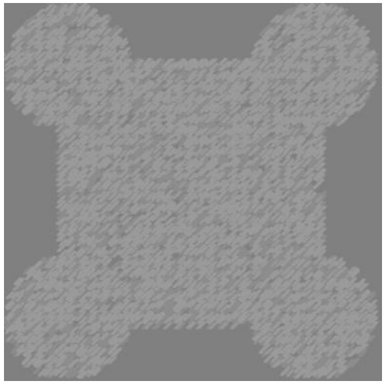
- Square (as a reference)
- Mickey ear square (to minimize the distance)
- Hexagonal (where the maximum distance between DNW is constant)
- Hollow Hexa (to minimize the Capacitance)

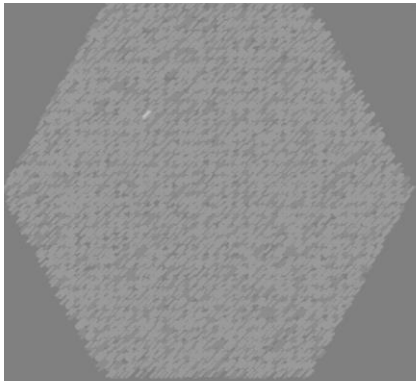
MIP simulation



Small sensor diodes flavors


Square


Mickey

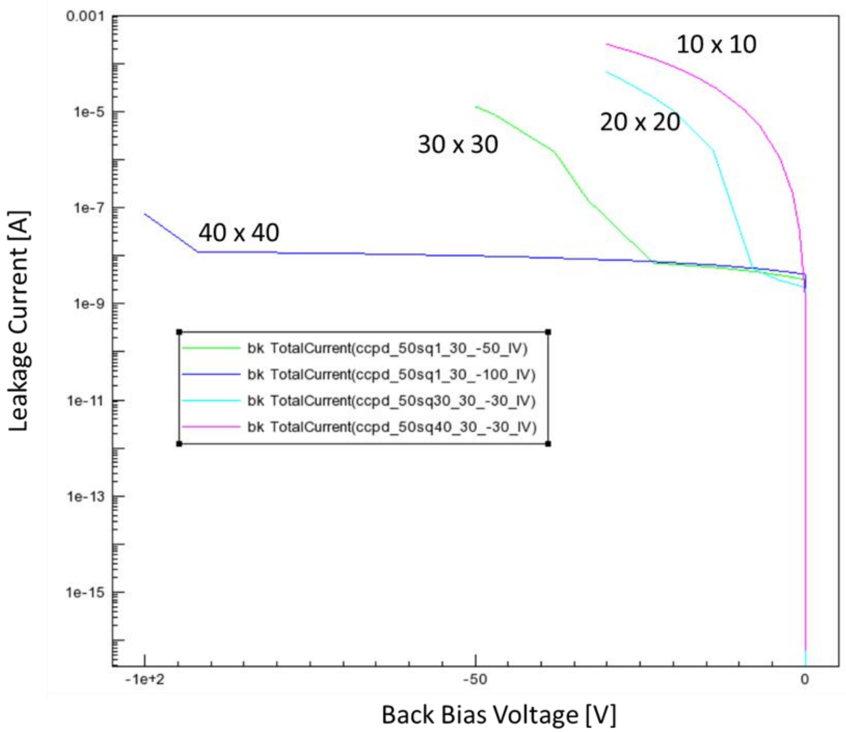

Hexa


Hollow Hexa

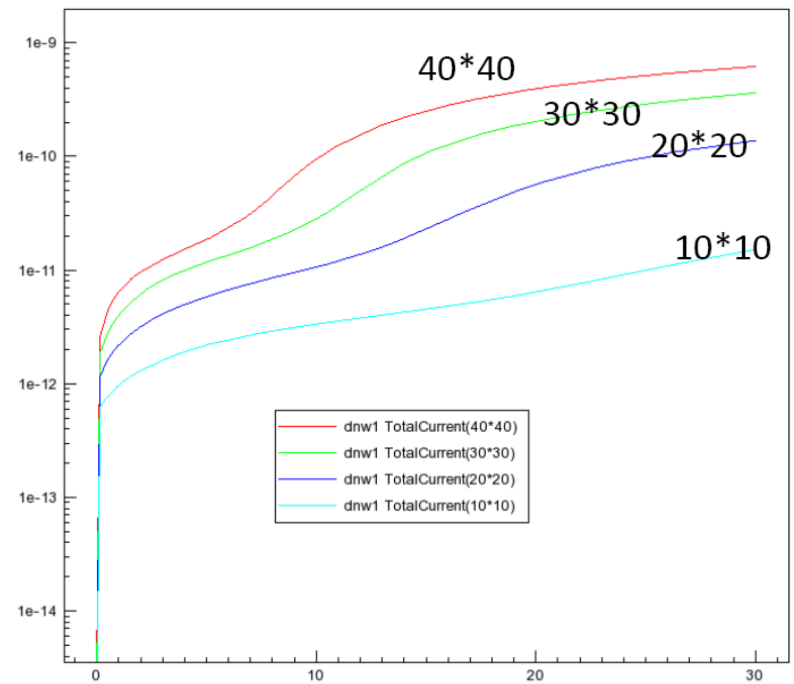
DNW structure	Capacitance [fF]	Breakdown voltage [V] (Back Bias)
Square 40 x 40	126	-100
Mickey 30 x 30	107	-70
Hexagone 30	77	-66
Hollow Hexa 30	55	-66

From TCAD simulation

TCAD simulations

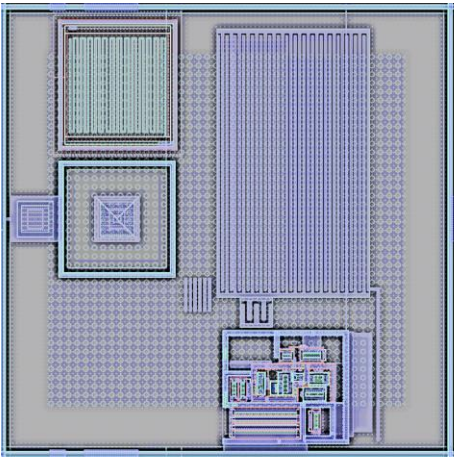


10nA/4px global leakage current for different diode (DNW) sizes, for a top bias @30 V (3kohms substrate)

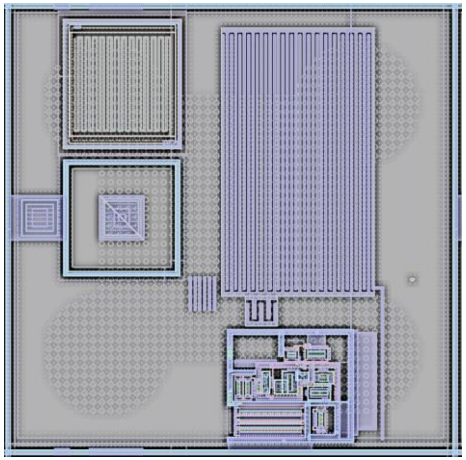


5nA/4px leakage current for different diode (DNW) sizes, for a bottom bias @0 V (3kohms substrate)

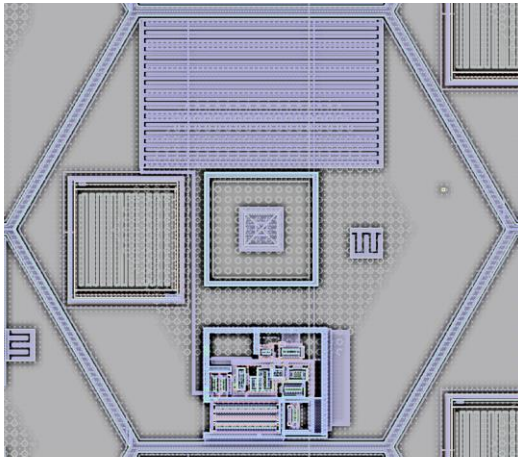
Small pixels flavors front-end



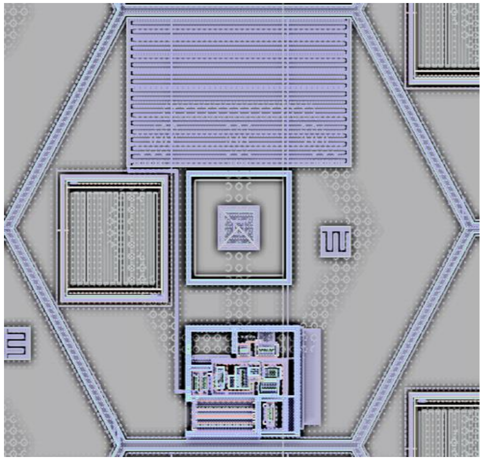
Square



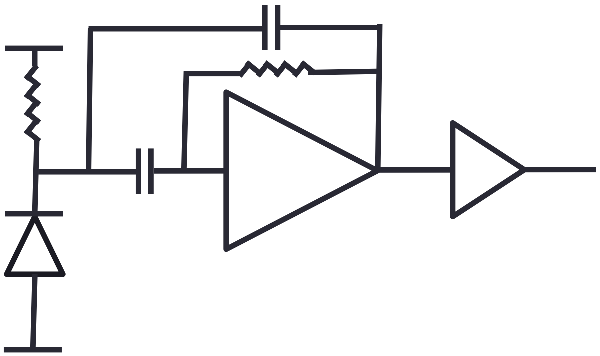
Mickey



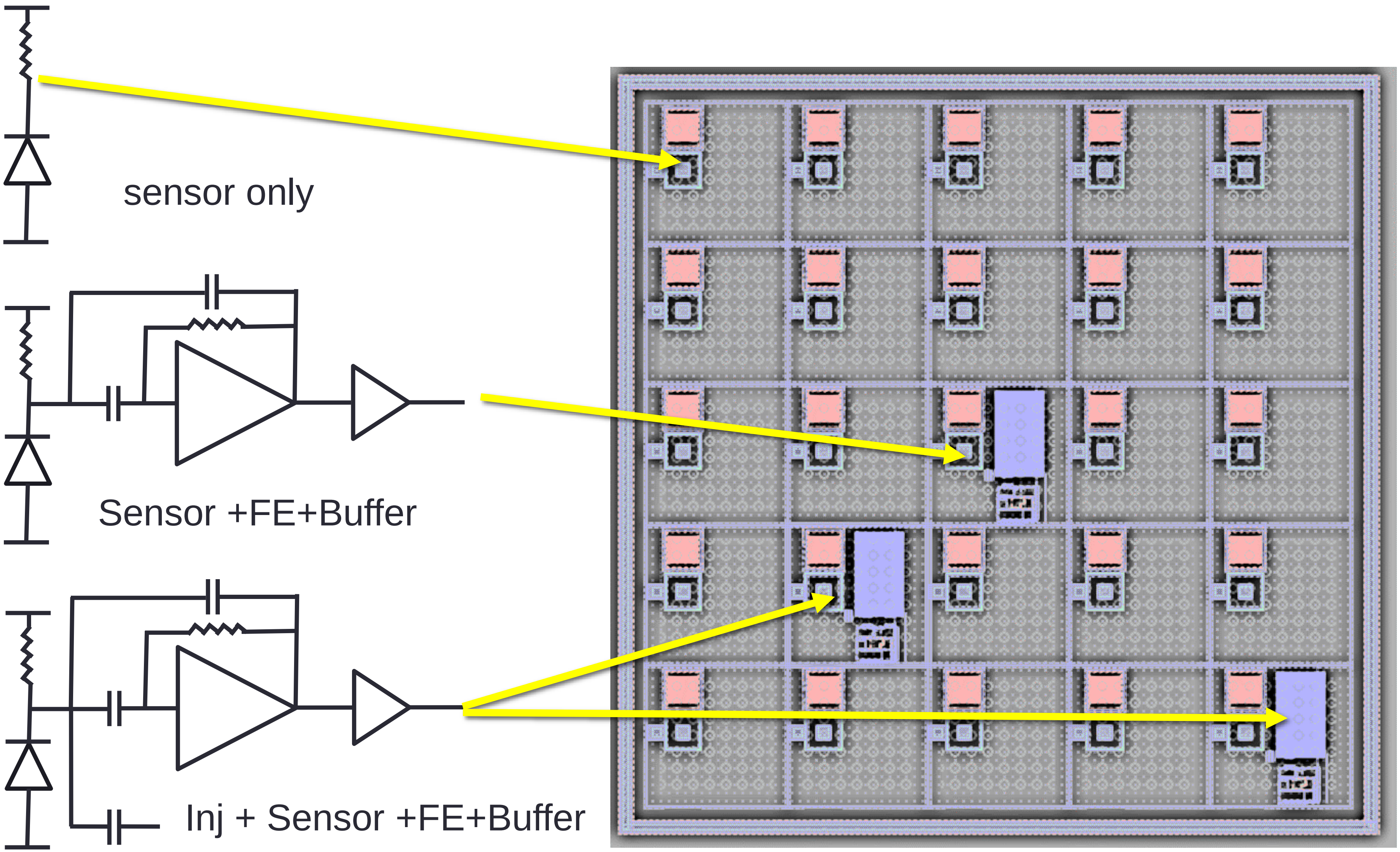
Hexa



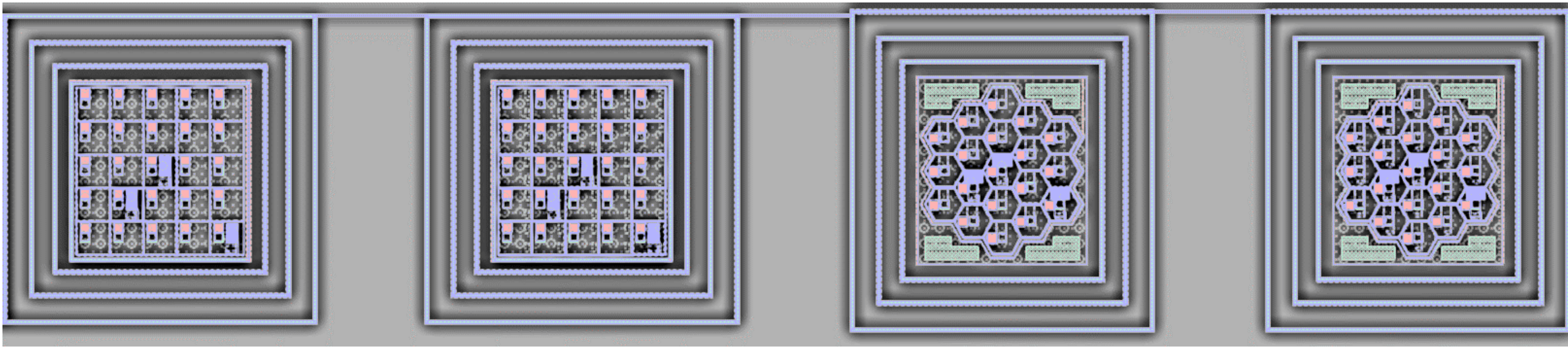
Hollow Hexa



Small pixels matrix (25 “square” pixels)



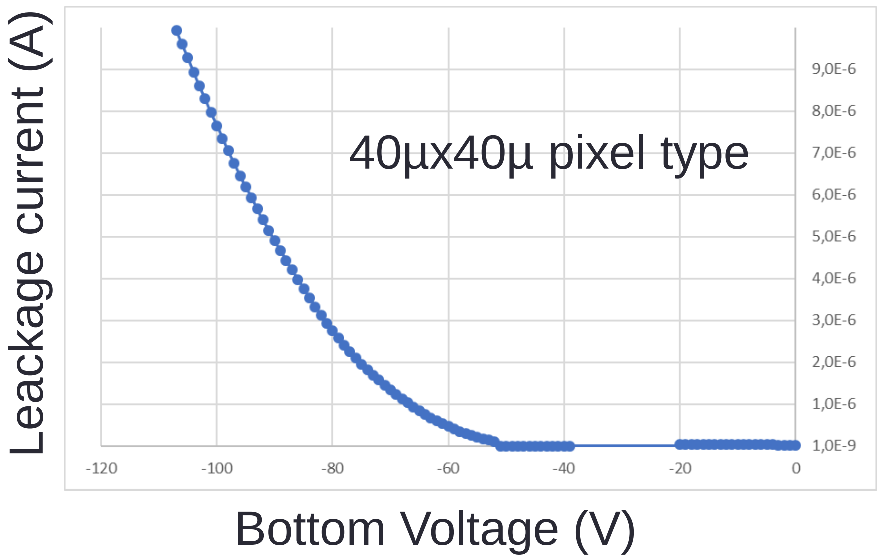
Small pixels test chip

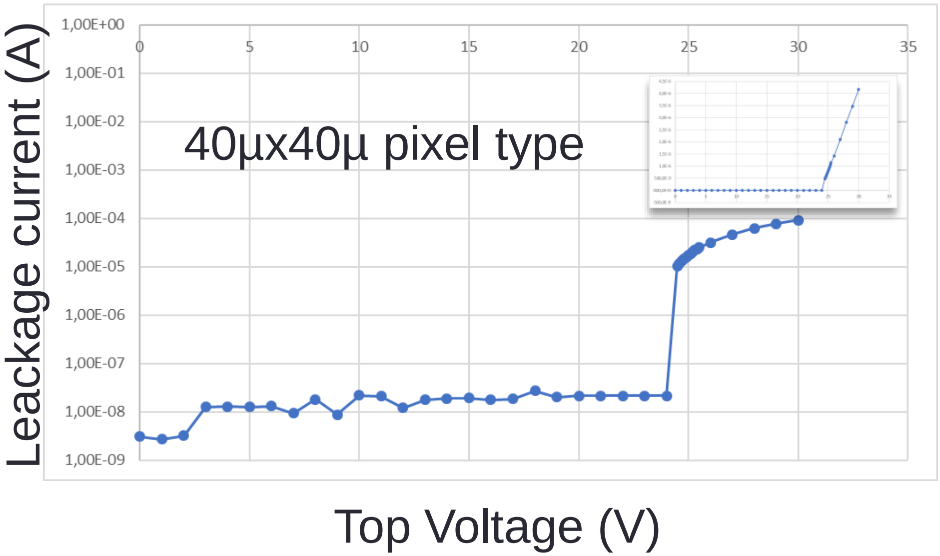


25 « Square » pixels | 25 « Mickey » pixels | 19 « Hexa » pixels | 19 « Hollow Hexa » pixels

- This test chip is a part of the LF-MONOPIX2.
- The tape-out was in may 2020.
- Delivering chip : end of 2020 (wafer thickness 700µm, 200µm, 100µm, 75µm)
- Test features to do (with and without radiations)
  - E-TCT
  - Analog readout of the pixels

1st Sensor Results (700µm)





30nA/4px global leakage current for different diode (DNW) sizes, for a top bias @24 V

BV at 54V (2kohms substrate)

10nA/4px leakage current for different diode (DNW) sizes, for a bottom bias @0 V

BV at 24V (2kohms substrate)

The total Voltage potential (top to bottom) at **78 V** is achieved

Summary

- Small sensor DMAPS (fully depleted with uniform drift field) can be designed by using LF 150nm without any process modification

- A 50µm x 50µm pixel size test chip was designed on 2020
- Leakage current, BV voltage, MIP simulation were simulated by using doping profile. All simulations were reviewed by the LFOUNDRY
- The pixel contains analog Front-end, to help the sensor measurement

- The test chip with several pixel flavours is under evaluation. The wafer resistivity is 2kohms with 700µm, 200µm, 100µm, 75µm thickness

- The small sensor proof of concept is done. Need additional test
  We need contribution for the test, especially on E-TCT test.

- Can we plan to design a small matrix for the RD50-MPW3?
  We will be happy to get contribution for the pixel readout design

BACKUP

Brainstorming

Objective Of a new submission

1. **Characterize New Diodes**
   - C, $I_{leakage}$, Radiation hardness
   - Could be done with the submitted testchip

2. **Reach low noise, low threshold Front-End + discriminator**
   - Must choose one-type of photodiode before testing (risk?)
   - R&D on front-end + Disc (what is spec?)
   - To be realistic, FE must not occupy whole area of 50 x 50 μm^2 (how much occupancy?)

3. **Do Monopix-like pixel**
   - Integrate Digital: BX, digital storage, readout… etc
   - Digital on Top
   - Ambitious project: how much time, how many resources