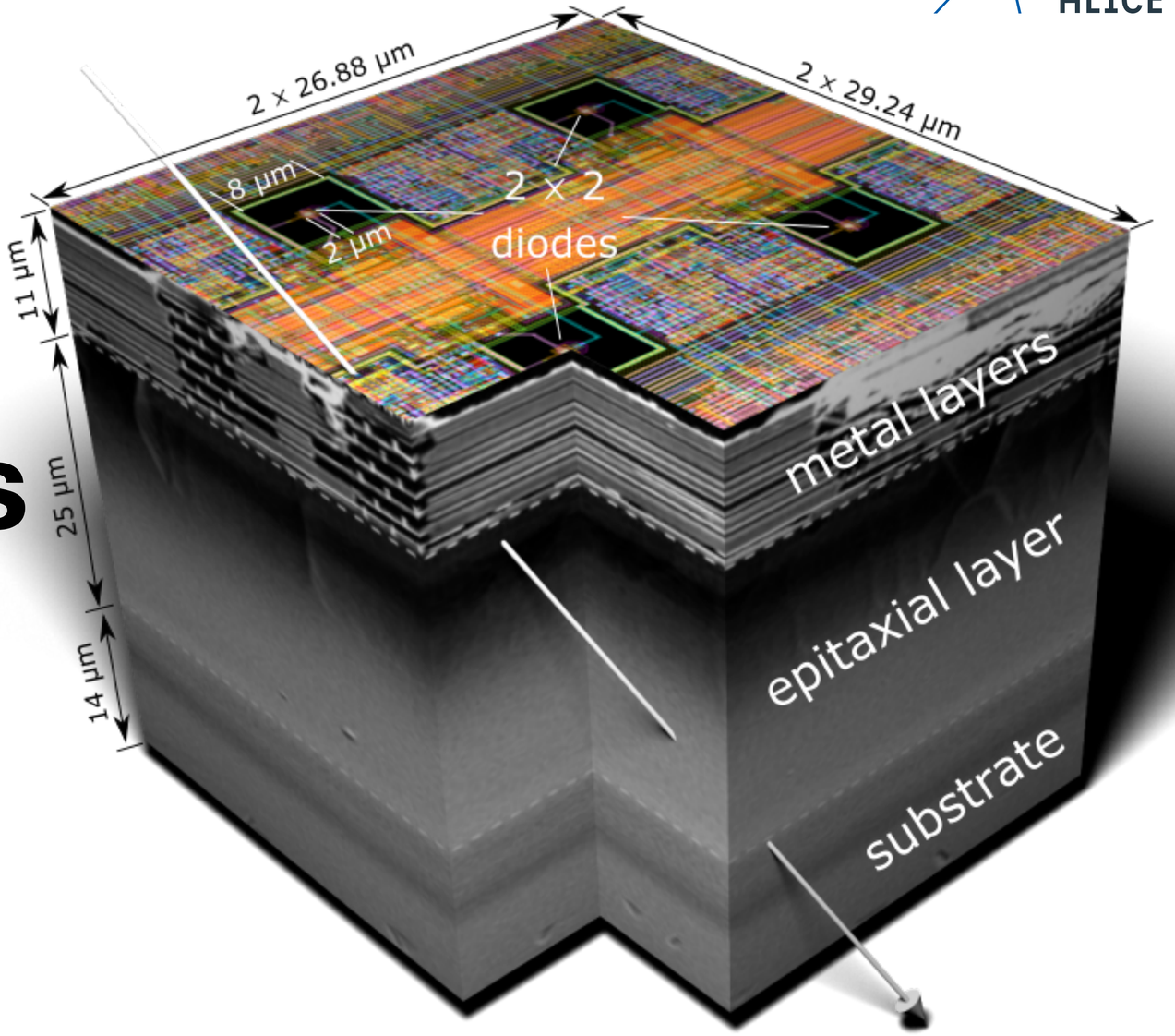
Silicon pixel sensors

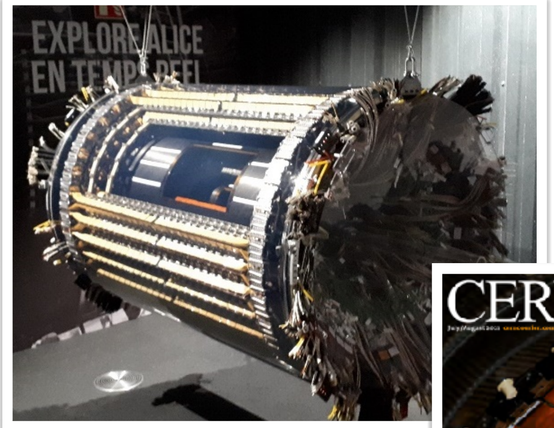
ALICE 3 workshop

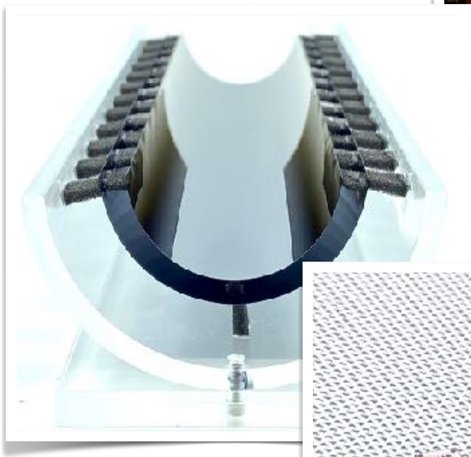


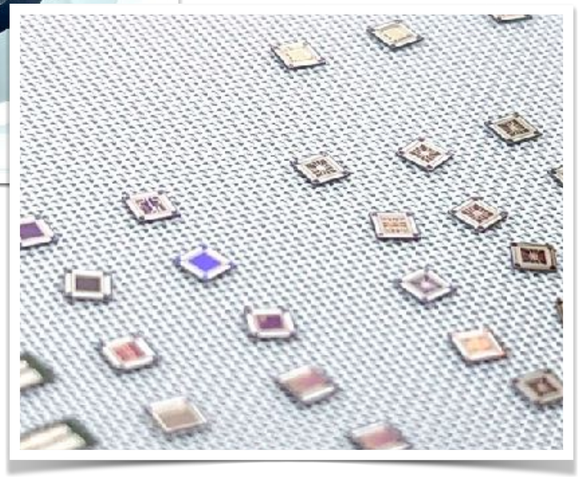
Magnus Mager (CERN), October 19th 2021

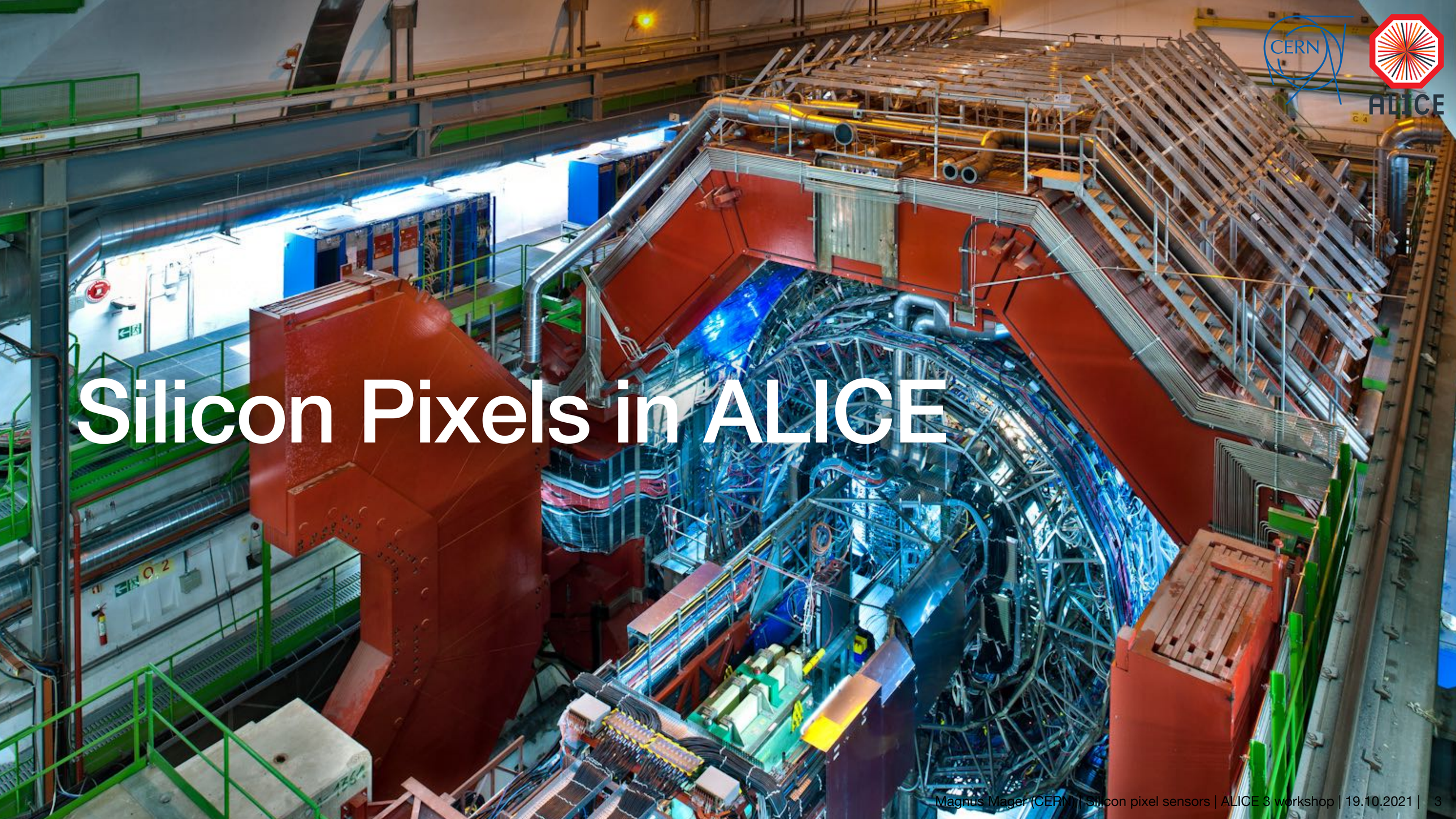
Outline

- Overview of silicon pixels in ALICE
  - ALICE ITS1, now dismounted
  - ALICE ITS2, *the* large scale application of MAPS
  - ALICE ITS3, the “current future” of MAPS
  - ALICE 3, scaling it up by another order of magnitude
- Monolithic Active Pixel Sensors (MAPS)
  - main achievements within ALICE R&D for ITS2
  - the ALPIDE chip
  - ALICE “offspring” targeting timing and radiation hardness
- R&D fronts (selection)
  - bent + large scale sensors
  - moving from 180 to 65 nm CMOS process
- Summary & Outlook







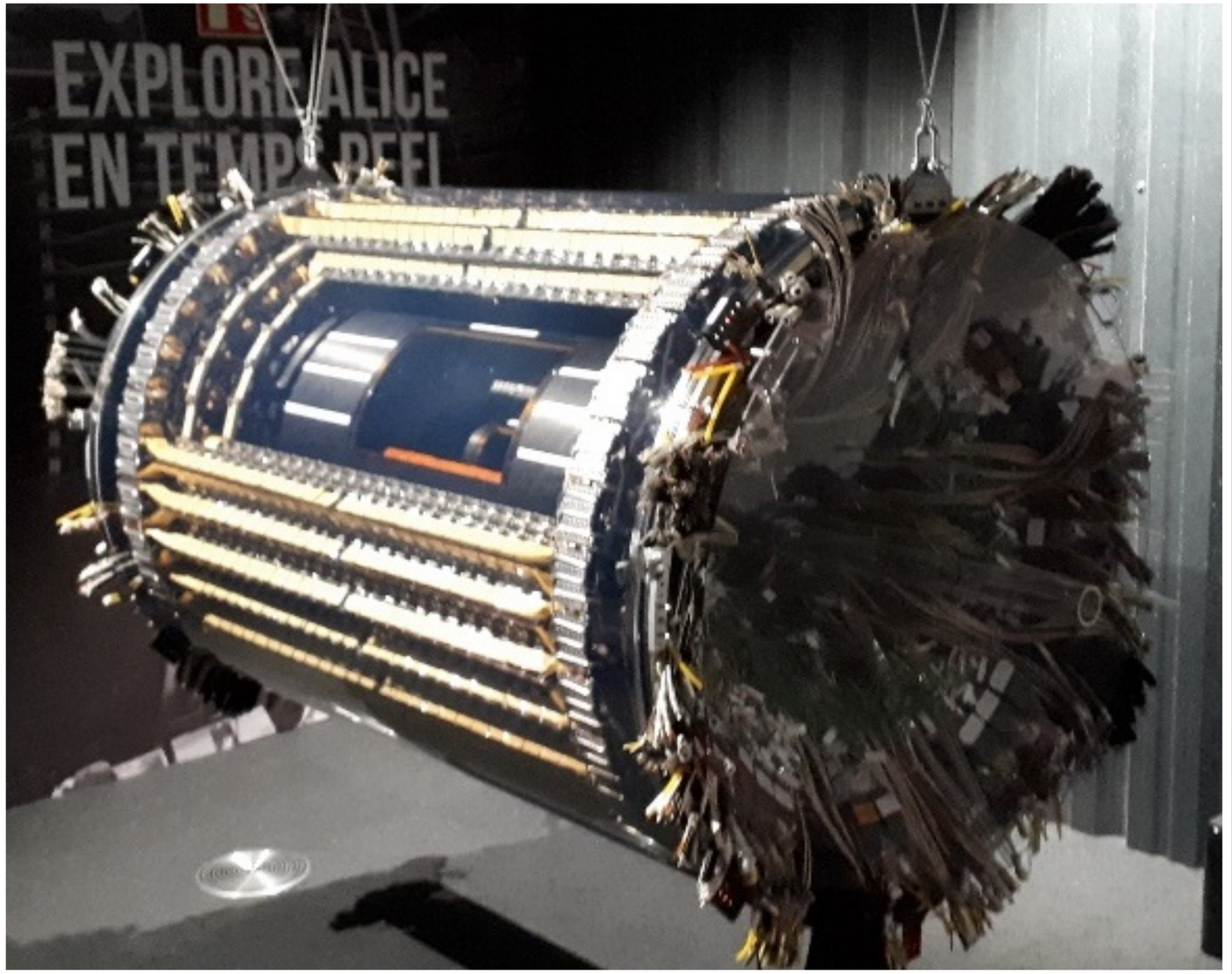


Silicon Pixels in ALICE

Silicon pixels in ALICE

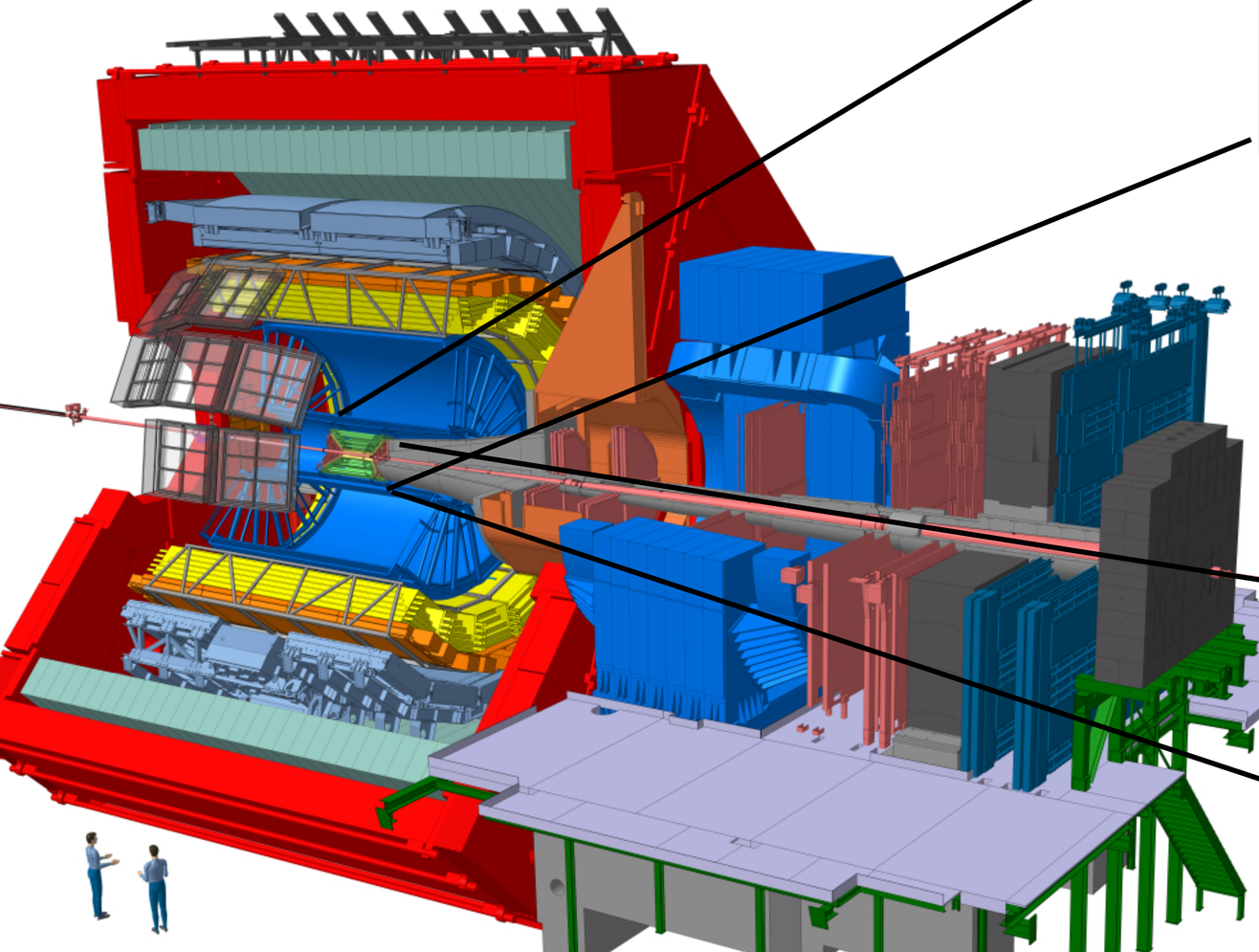
1. Hybrid (innermost layer of first ITS)

- Since the very beginning ALICE uses silicon pixels
- Hybrid detectors in Run 1
- Essential ingredient for its physics output
  - secondary vertex reconstruction
- Today: the first ITS is decommissioned and on display in the ALICE exhibition at P2

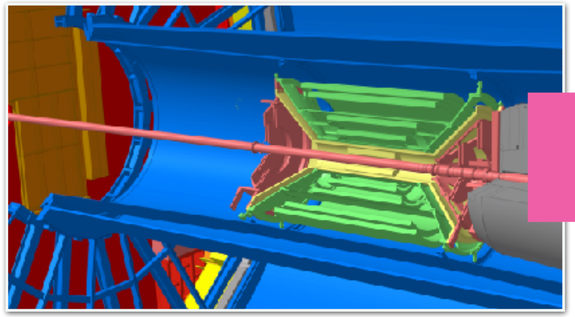


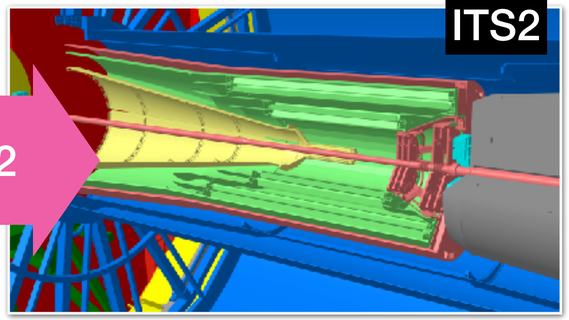
Silicon pixels in ALICE

LS2 upgrades with Monolithic Active Pixel Sensors (MAPS)



Inner Tracking System





LS2

6 layers:
- 2 hybrid silicon pixel
- 2 silicon drift
- 2 silicon strip

Inner-most layer:
- radial distance: 39 mm
- material: $X/X_0 = 1.14\%$
- pitch: $50 \times 425\ \mu m^2$

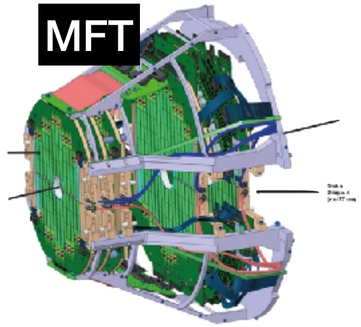
rate capability: 1 kHz

7 layers:
- all MAPS
- 10 m^2, 24k chips, 12.5×10^9 Pixels

Inner-most layer:
- radial distance: 23 mm
- material: $X/X_0 = 0.35\%$
- pitch: $29 \times 27\ \mu m^2$

rate capability: 100 kHz (Pb-Pb)

Muon Forward Tracker

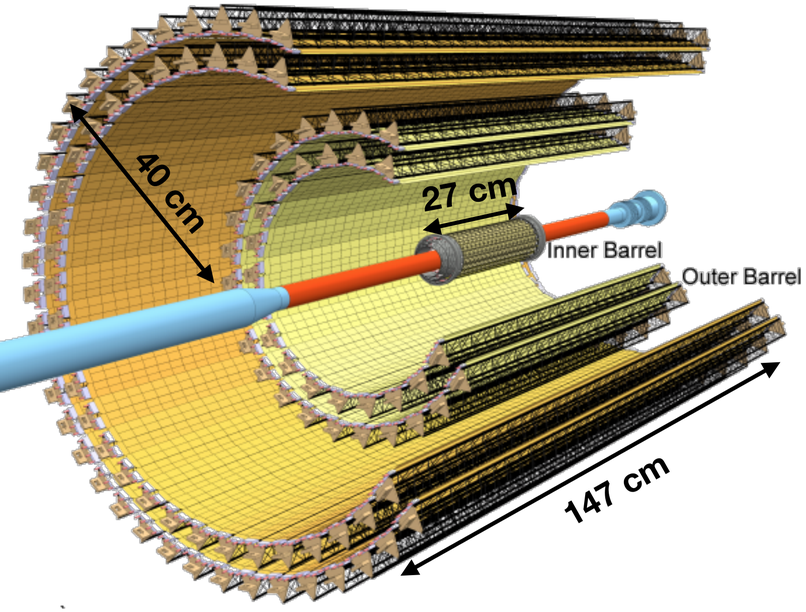


new detector

5 discs, double sided:
- based on same technology as ITS2

Silicon pixels in ALICE

2. Monolithic CMOS (7 layers, LS2 upgrade, “ITS2”)

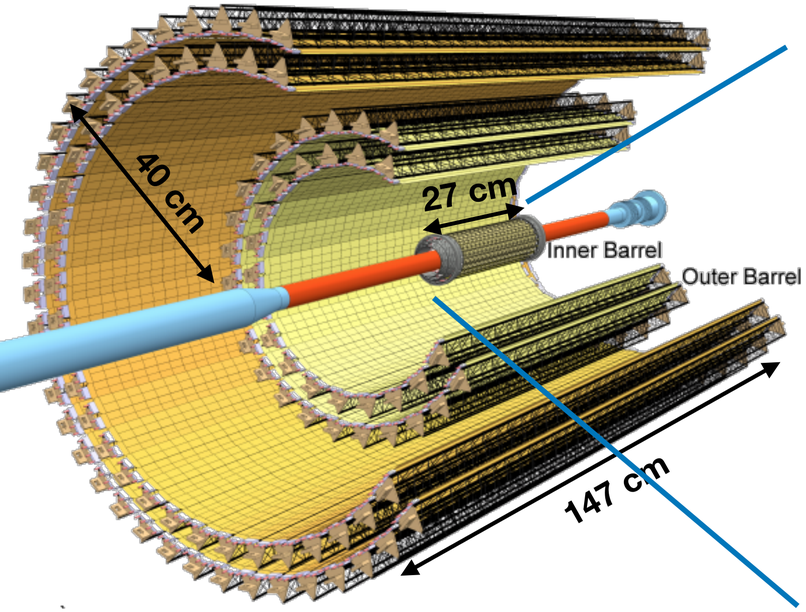


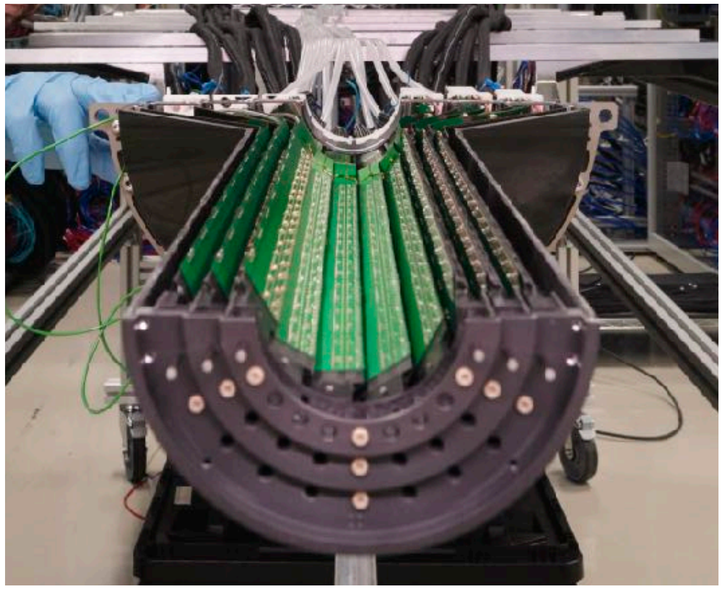
- 10 m^2 active area
- 12.5×10^9 pixels
- Installed and under final commissioning

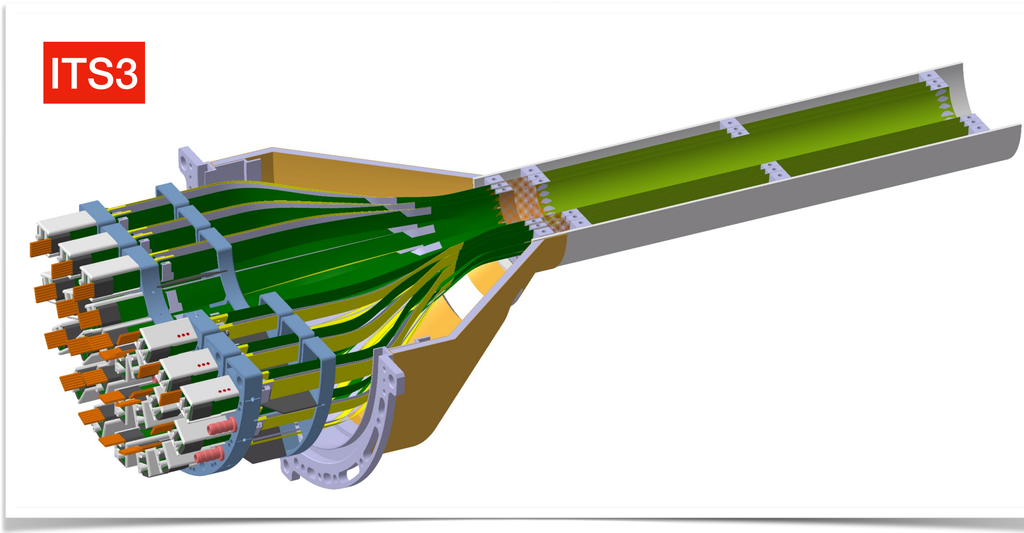
- By far largest detector of this kind
- Fully developed within the collaboration
  - including the silicon
  - R&D started some 10 years ago
- Construction involved >10 institutes

Silicon pixels in ALICE

a closer look at ITS2 and motivation for ITS3





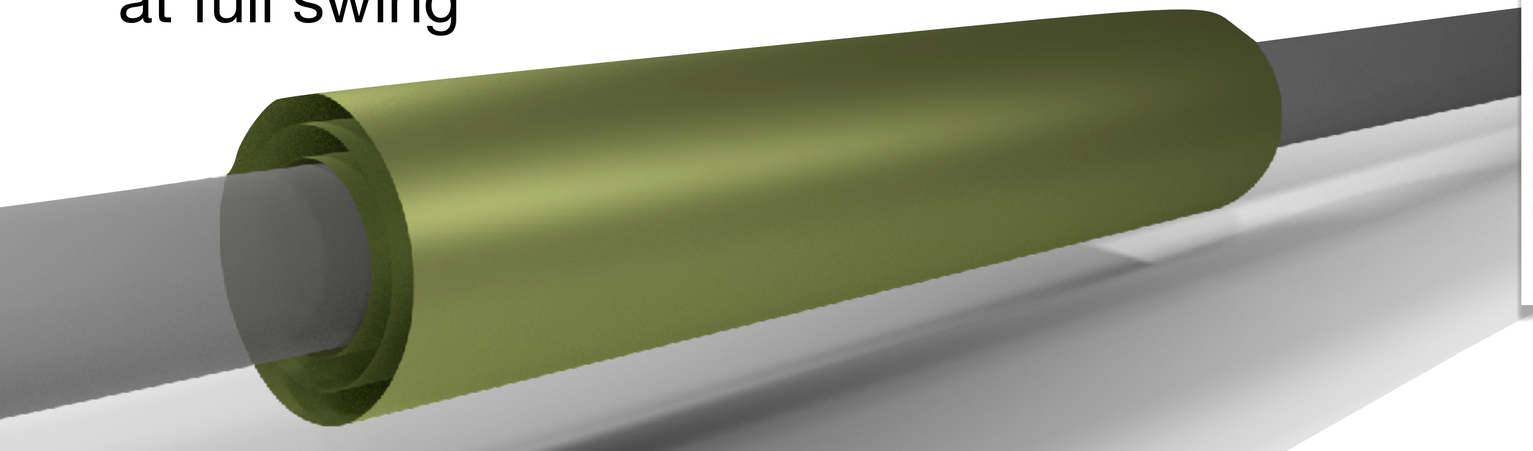


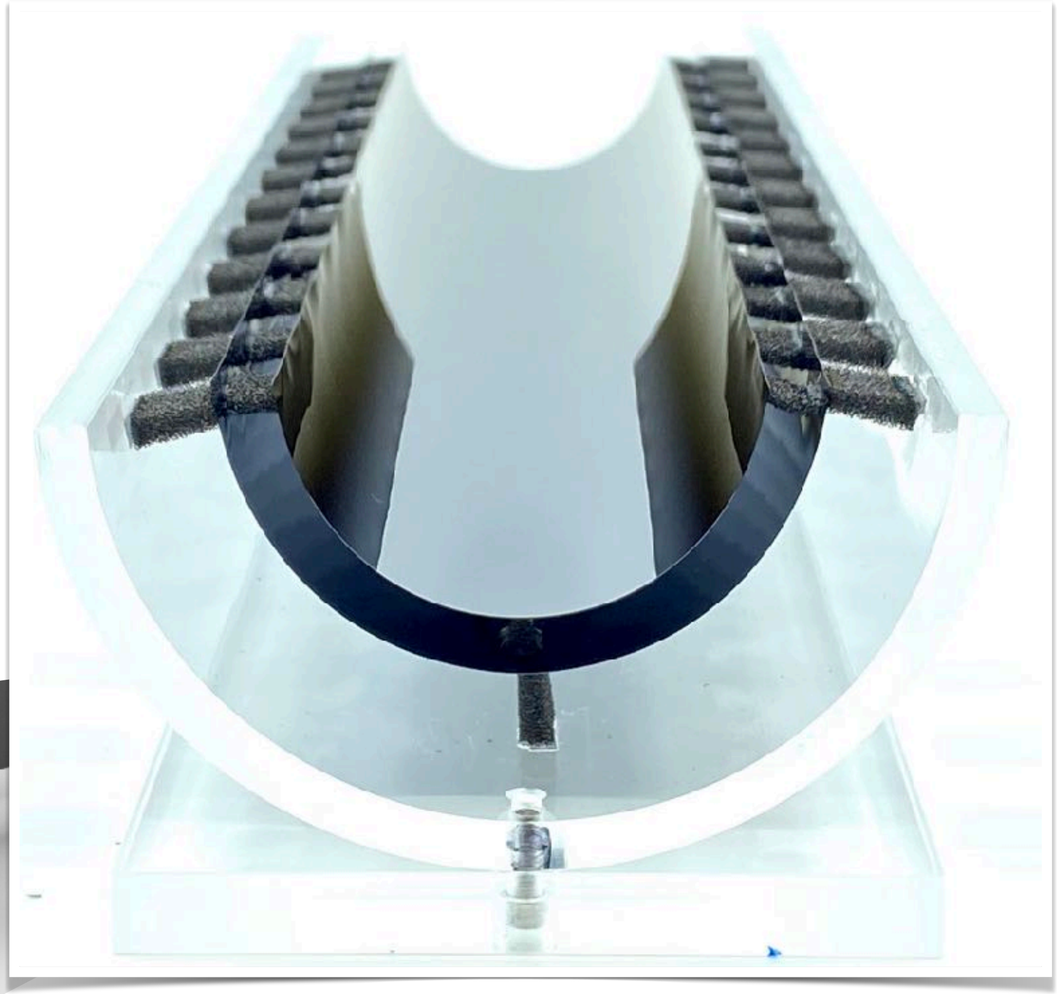
- ITS2 will provide:
  - pointing resolutions of 15 µm (in rφ and z) at transverse momenta of 1 GeV/c
  - tracking efficiencies of above 90% for particles with transverse momenta larger than 200 MeV/c
- The Inner Barrel is ultra-light but still rather packed → further improvements seem possible
- **Proposal:** replace detector staves (tiled by several chips) **by wafer-scale sensors that are bent around the beam pipe**

Silicon pixels in ALICE

3. Waver-scale, bent (inner 3 layers, LS3 upgrade, “ITS3”)

- Replacement of inner-most tracking layers
- Based on **wafer-scale, bent silicon** layers
  - new detector technology, achieving an order of magnitude lower material budget
  - main concrete drive to explore CMOS technologies (TJ **65 nm**)
- R&D endorsed by LHCC in 2019 and running at full swing

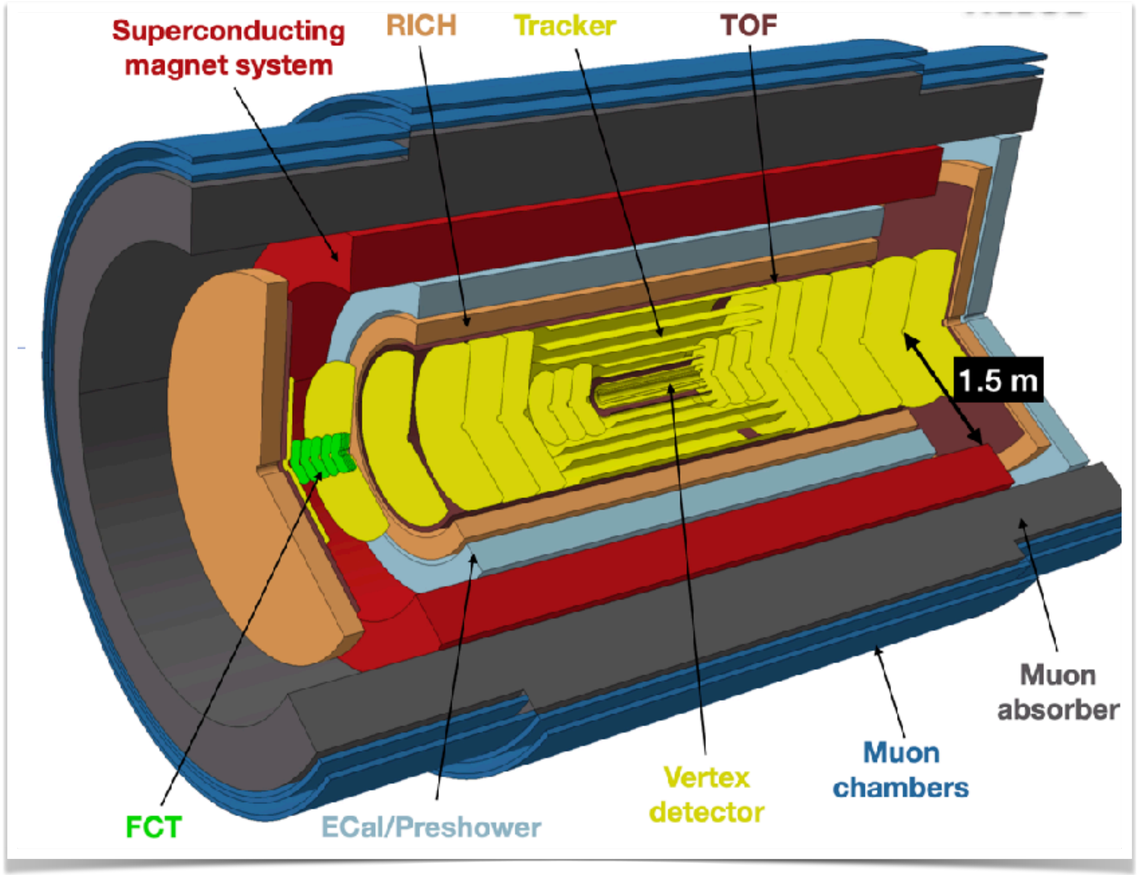




Silicon pixels in ALICE

4. large-scale + in vacuum (LS4 upgrade, ALICE 3)

- For ALICE 3, the goal is to produce an O(60-70 m^2) silicon tracker (yellow part)
- It will comprise two parts
  - in-vacuum tracker
  - outer tracking layers
- Builds upon the experience and knowledge gained from ITS2 and ITS3
  - bent sensors for inner-most layers
  - optimised modules for outer layers
- The scale of the undertaking requires us to go industrial/commercial: **CMOS MAPS are ideal**



see Jochen Klein's presentation on Monday

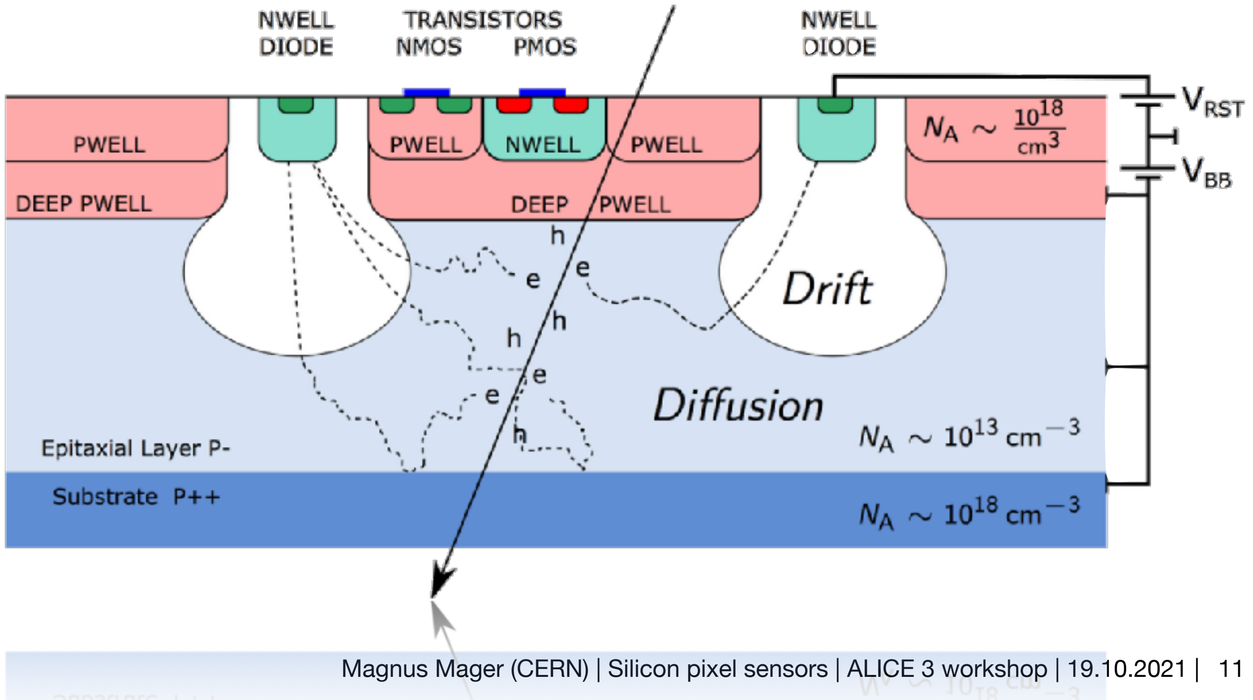
Silicon pixels in ALICE

key aspects for ALICE 3

- Low power consumption: 20-70 mW/cm^2
  - essential to keep material budget low (dominated by power distribution and heat removal)
  - builds upon **ALPIDE** development (introducing low-power in-pixel front-ends)
  - needs improvement to meet timing requirements O(100 ns) and higher data rates
  - benefits from deeper sub-micron technologies (move from 180 nm to **65 nm**, perhaps even further)
- Bent, wafer scale sensors
  - achieve the lowest possible material budget figures (no/minimal support, good hermiticity by design)
  - allow to be as close as possible to the beam (“non-flat” geometries)
  - builds on **ITS3**
- Radiation hardness: O(10^{15} 1 MeV/cm^2 n_{eq}) NIEL
  - orders of magnitude higher (at 5 mm) than ITS2 or ITS3
  - builds on ITS2 offspring development (**process modifications**)

This is challenging, but within reach today

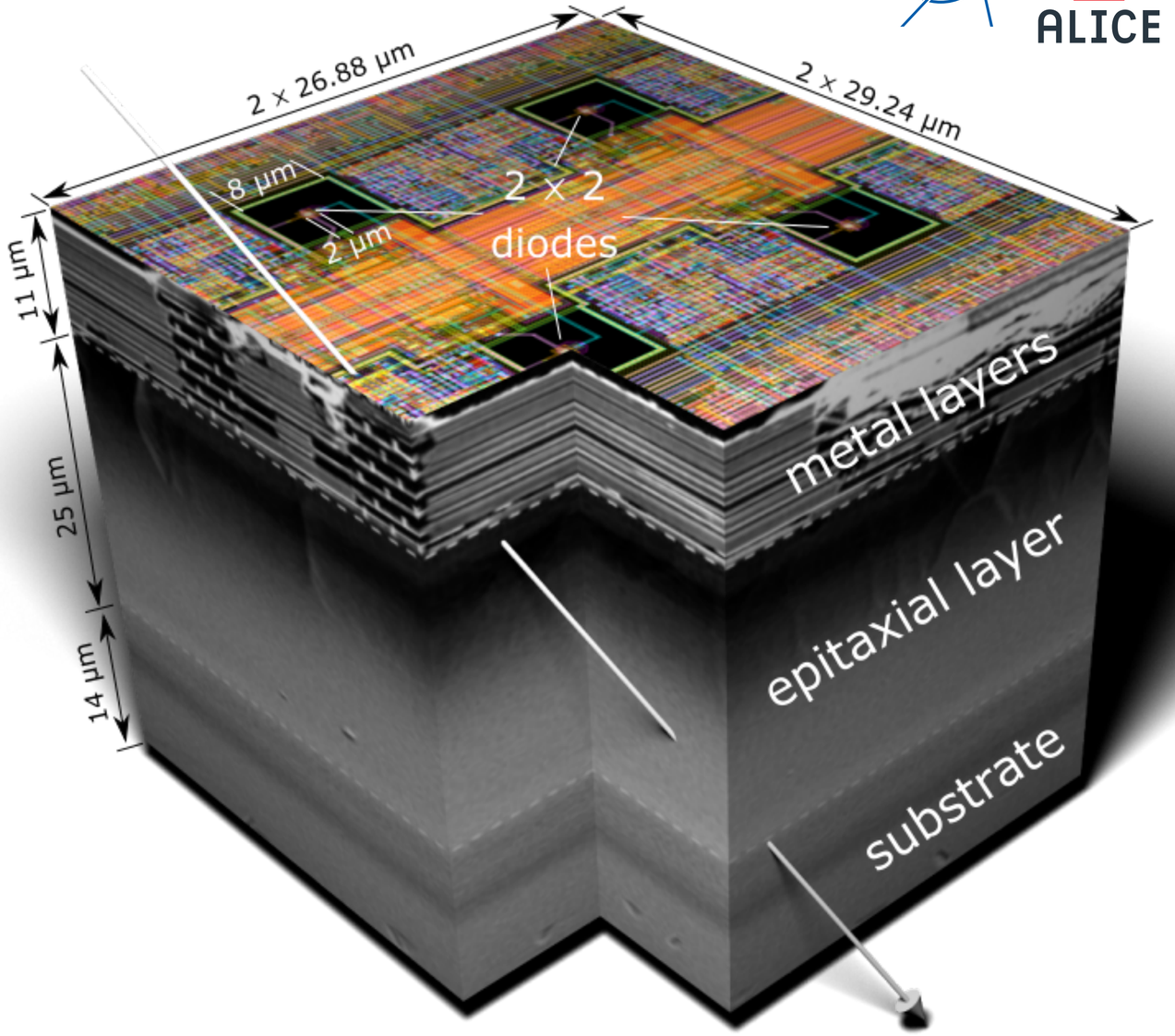
Monolithic Active Pixel Sensors (MAPS)



MAPS working principle (1)

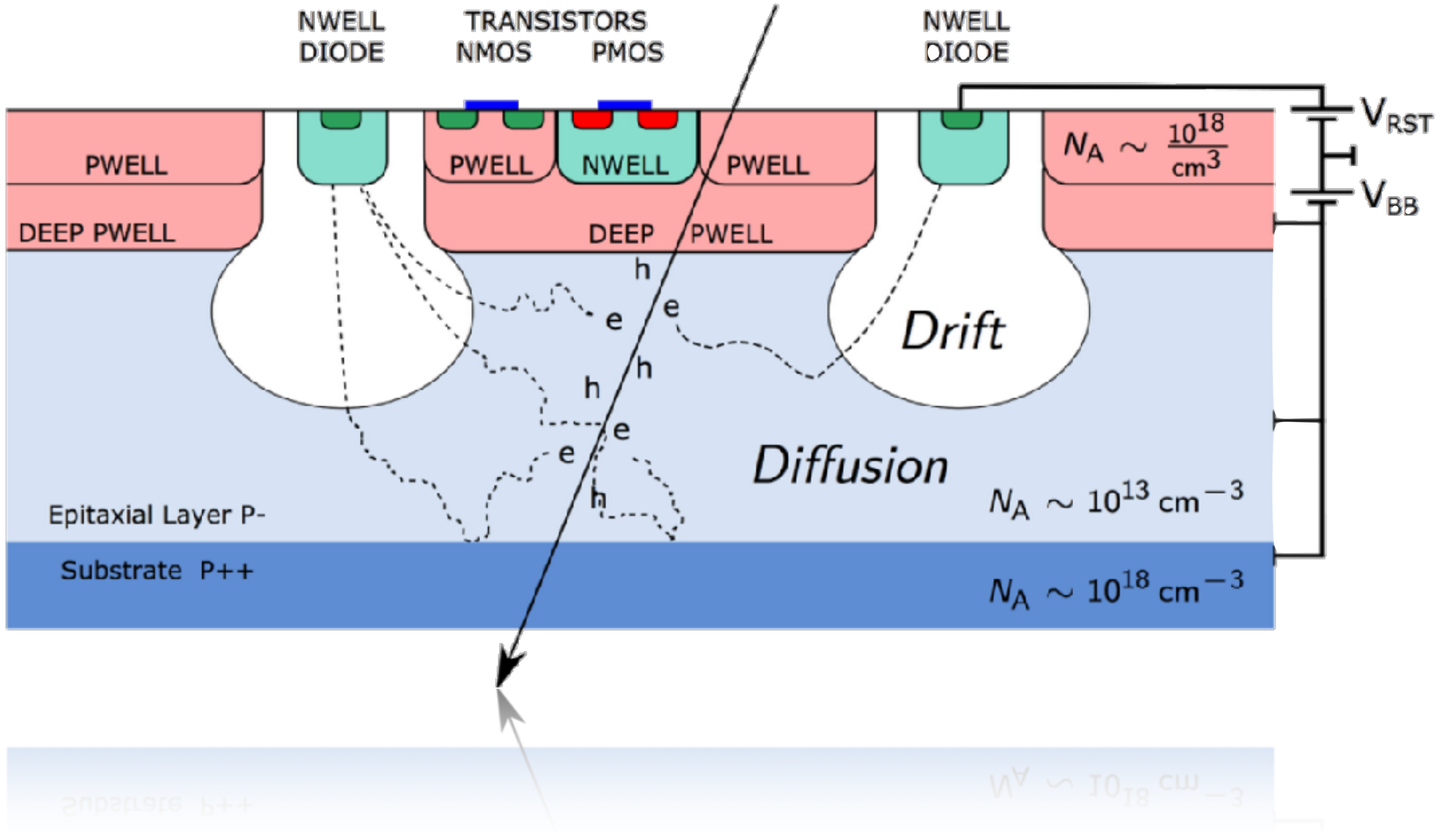
in TowerJazz 180 nm CIS

- MAPS (Monolithic Active Pixel Sensors) house on the same chip:
  - the sensitive volume, a high-resistive epitaxial layer
  - the analog front-end (amplifier, discriminator)
  - the readout electronics
- All of this fits into a device of 50 µm thickness



MAPS working principle (2)
in TowerJazz 180 nm CIS

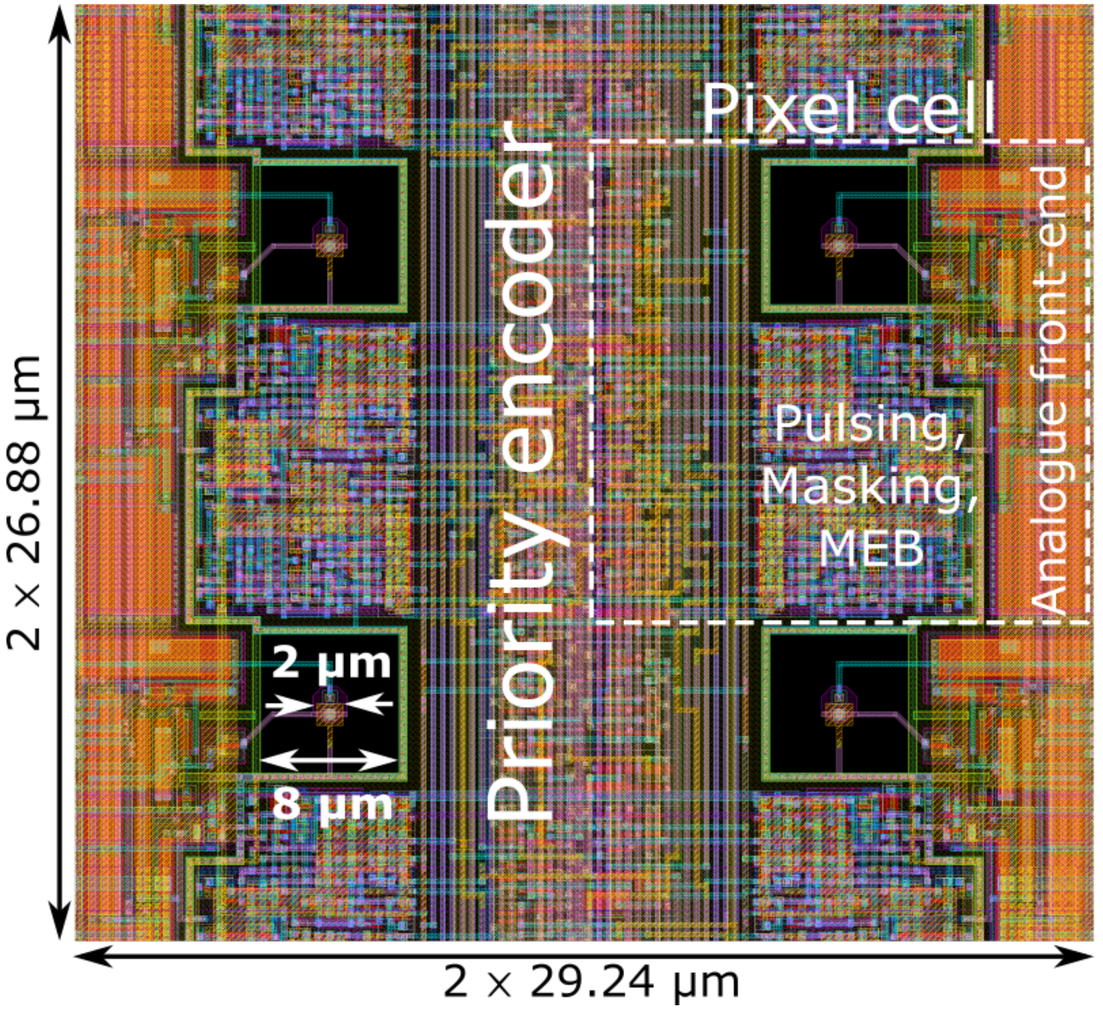
- The well structure isolates electronics from sensing volume
- Possibility to put complex logic over the active matrix
- Full benefit from high integration density offered by deep sub micron technologies
- Drift and diffusion volumes are “engineerable”
  - allows to optimise charge sharing (for position resolution, timing or radiation hardness)



MAPS working principle (3)

example: ALPIDE pixel

- **Front-end:**
  (9 transistors, full-custom)
  - continuously active
  - shaping time: < 10 µs
  - power consumption: 40 nW
- **Multiple-event memory:** 3 stages
  (62 transistors, full-custom)
- **Configuration:** pulsing & masking registers
  (31 transistors, full-custom)
- **Testing:** analogue and digital test pulse circuitry
  (17 transistors, full-custom)
- **Readout:** priority encoder, asynchronous, hit-driven



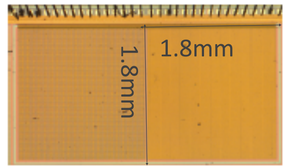
O(200) transistors / pixel

MAPS R&D within ALICE for ITS2

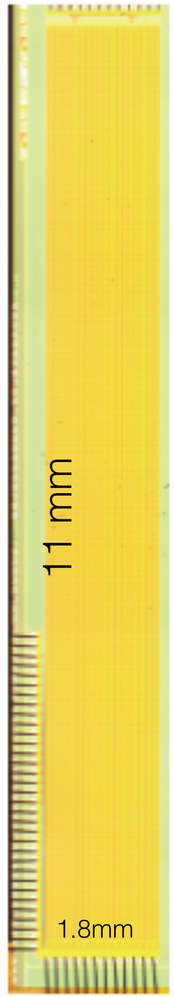
time line (simplified)

2012	Explorer	• study of technology • detection diode geometry • starting materials • radiation hardness
2013	pALPIDEss	• digital front-end • priority-encoder readout
May 2014	pALPIDE-1	• full-scale sensor • simplified interface
Apr 2015	pALPIDE-2	• chip-chip communication interface • module integration • *low-speed serial link*
Oct 2015	pALPIDE-3	• multiple-hit memory, final interfaces • last optimisation of pixel • *high-speed serial link (jitters)*
Aug 2016	**ALPIDE**	• final chip

Explorer



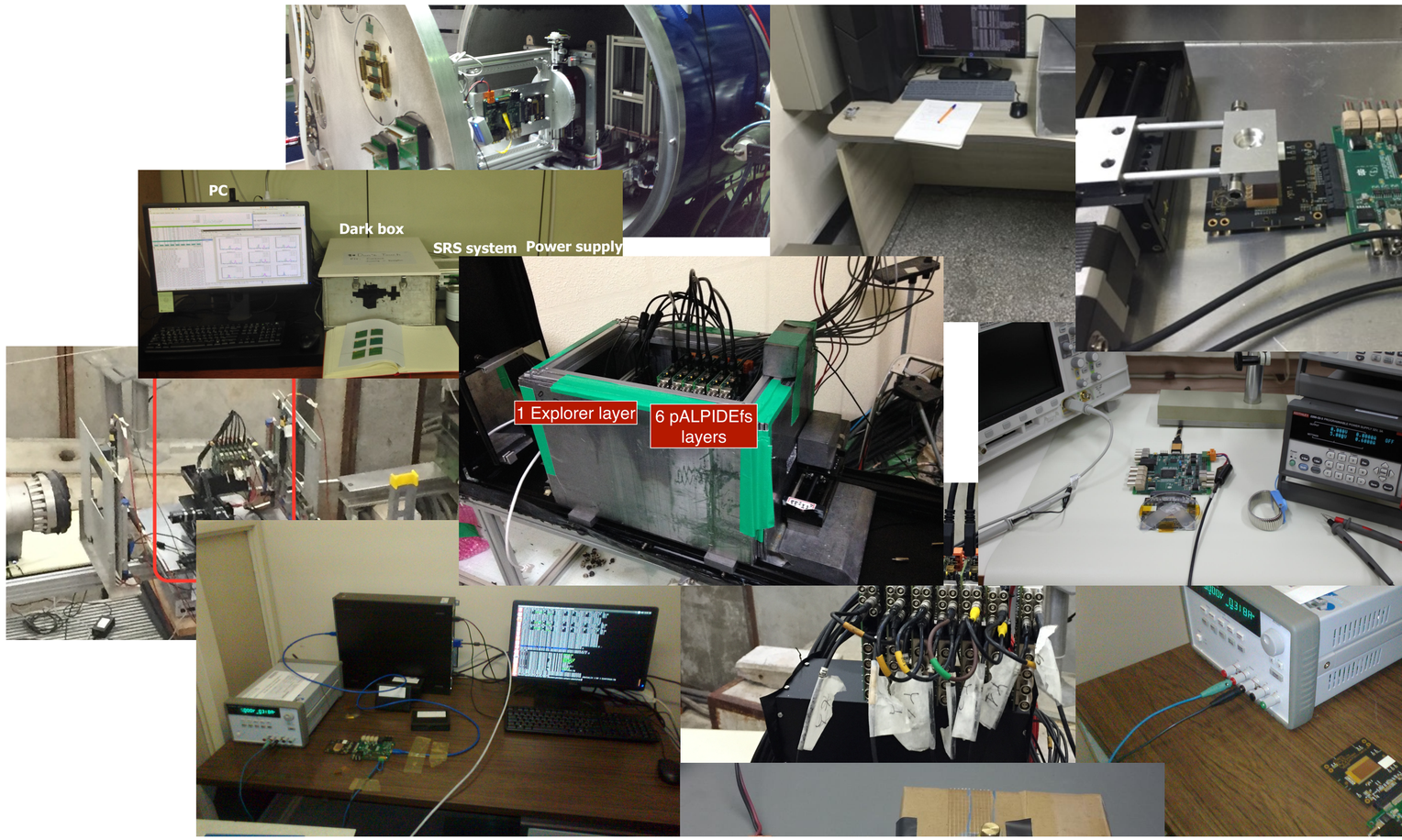
pALPIDEss



MAPS R&D within ALICE for ITS2

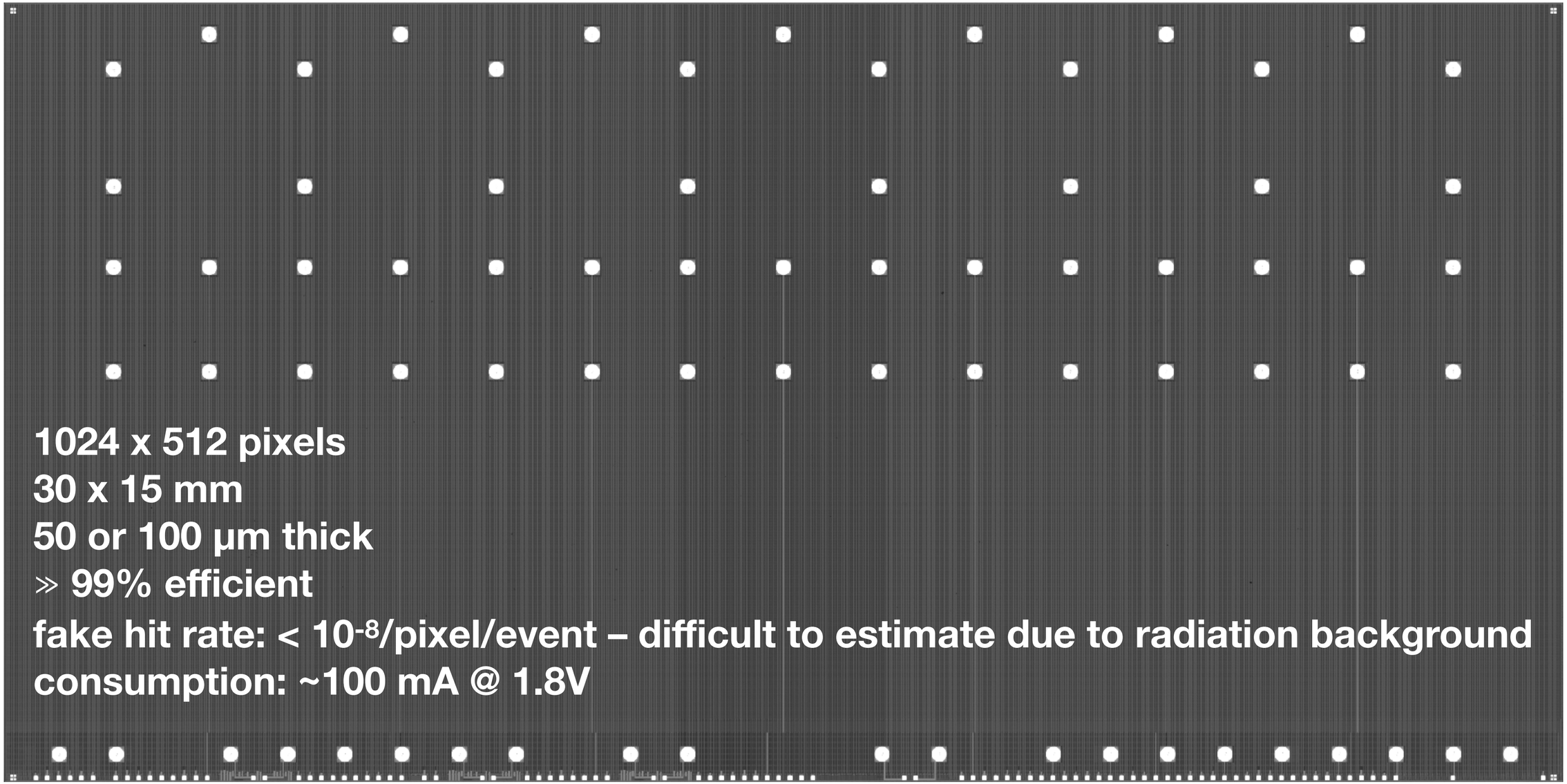
scope of R&D effort

- Many (>10) participating institutes
  → *biggest team within ITS project*
- Several test beam facilities (including newly established ones)
- A lot of expertise within the collaboration has been generated
- This pays off now for ITS3/65 nm



ALPIDE - the MAPS for ITS2

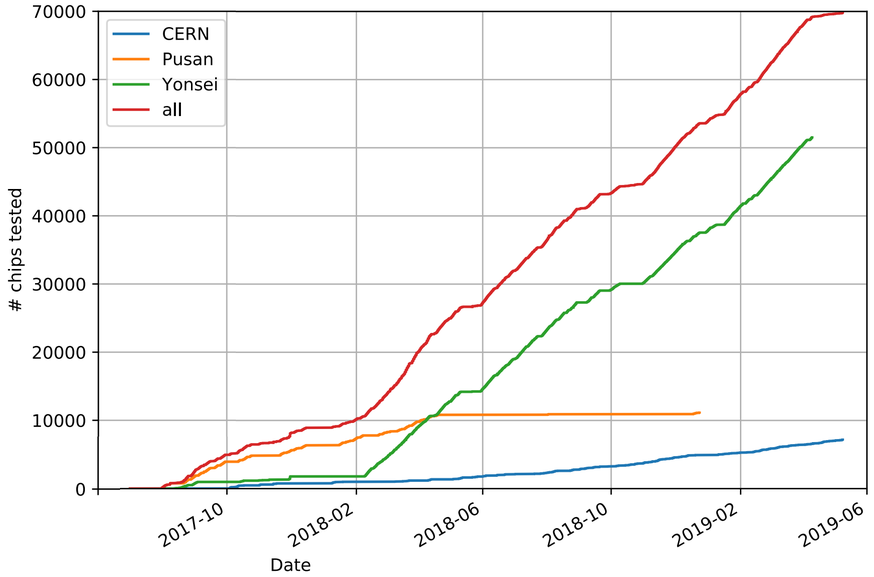
the current state of the art

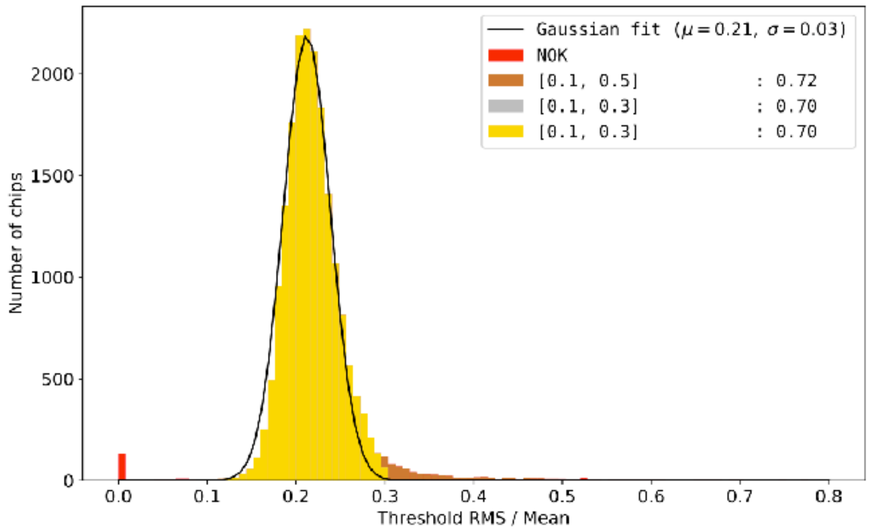


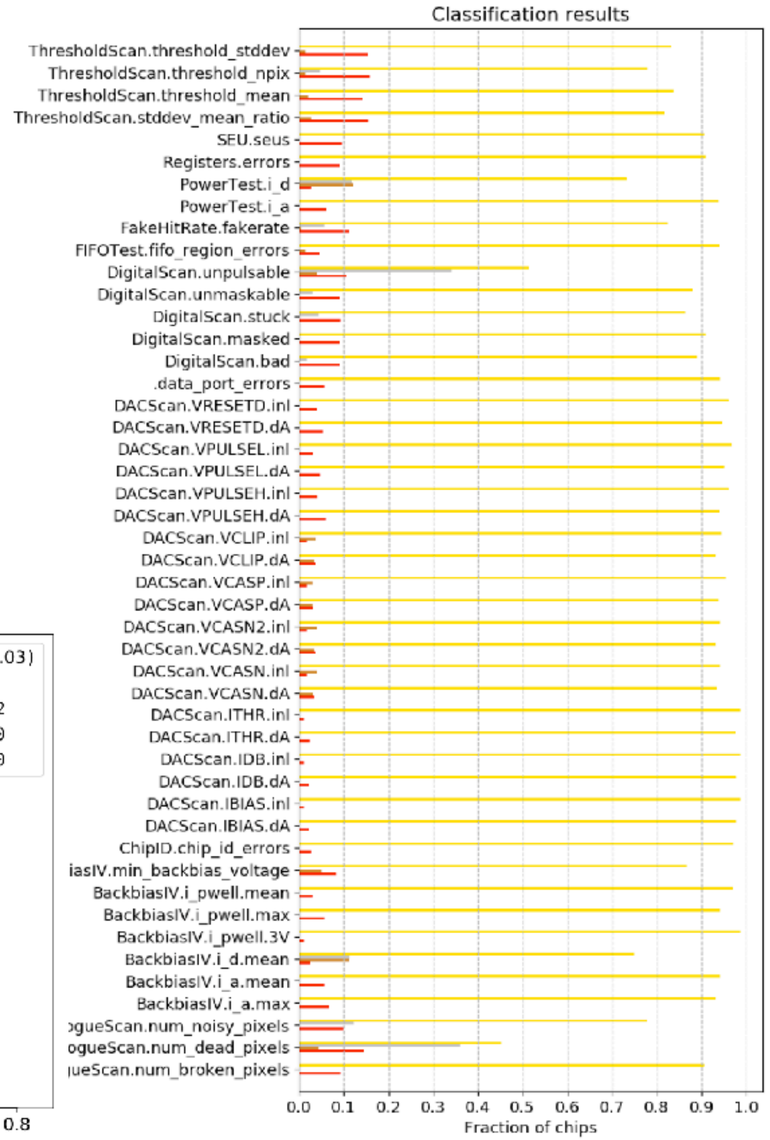
ALPIDE – mass production

results from 70,000 chips

- We are now in the position to quote performance figures and failure modes on large numbers
- This is an excellent starting point for scaling up
  - to larger chips
  - to higher volume



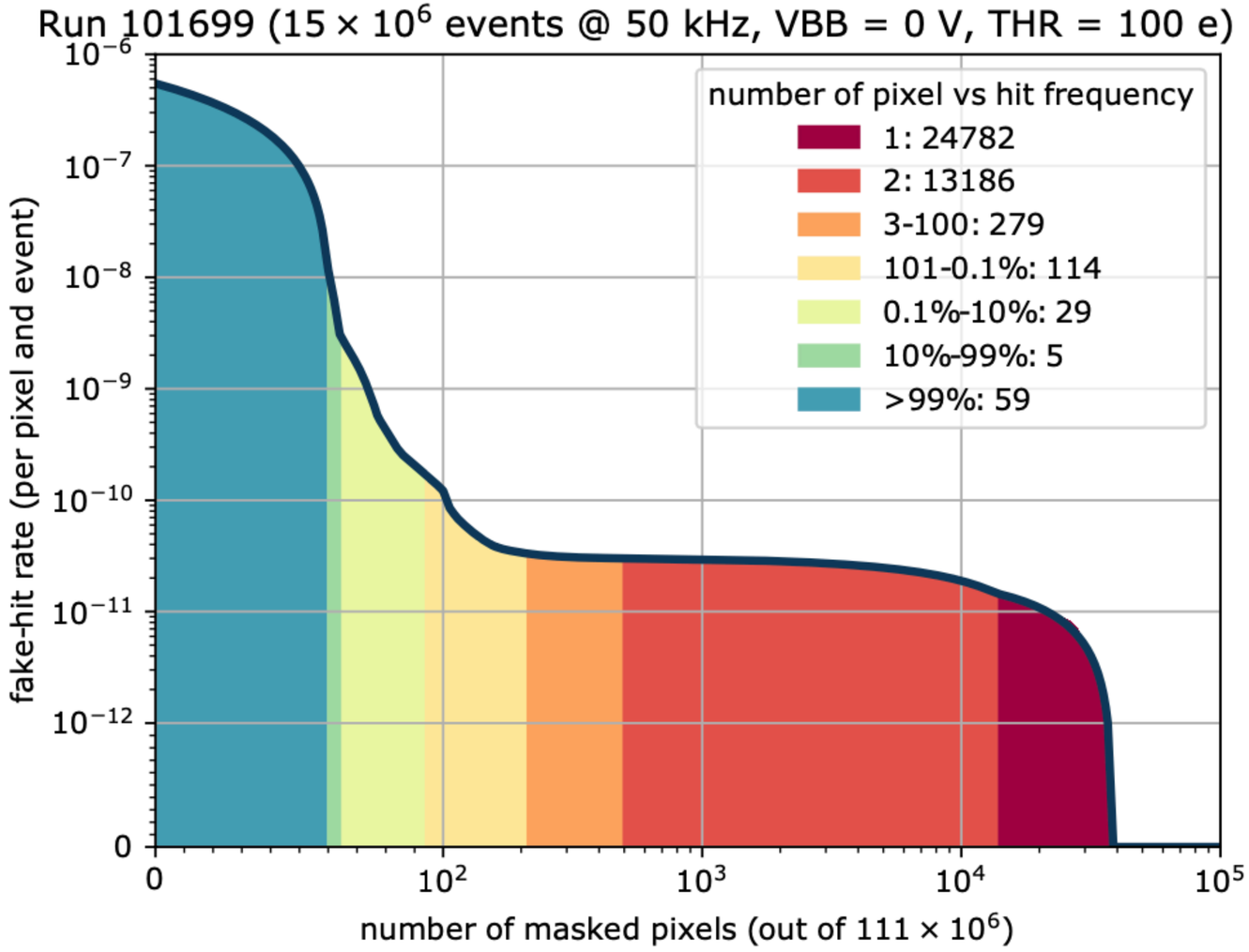




ALPIDE – integrated onto ITS2

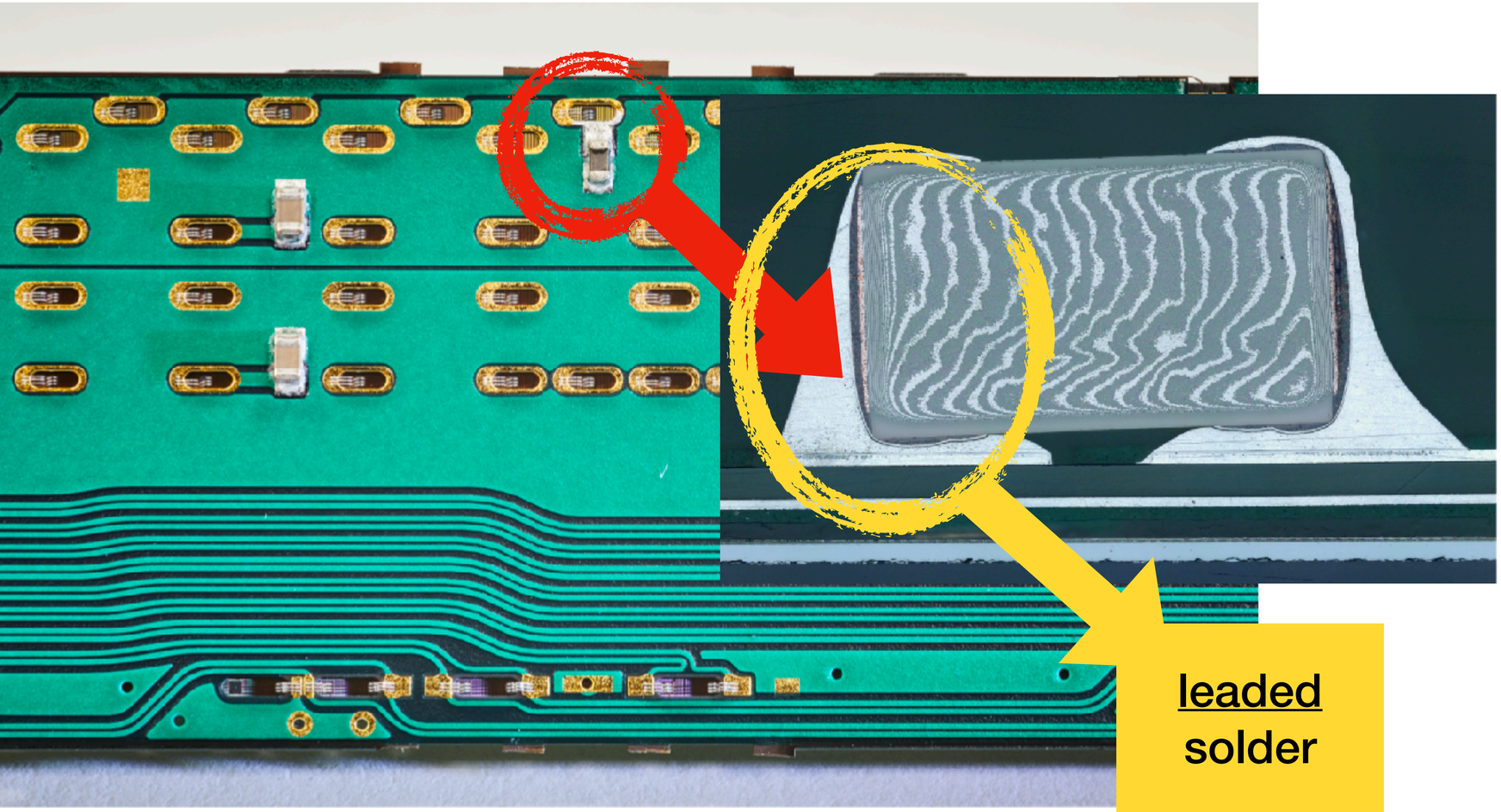
on-detector performance figures

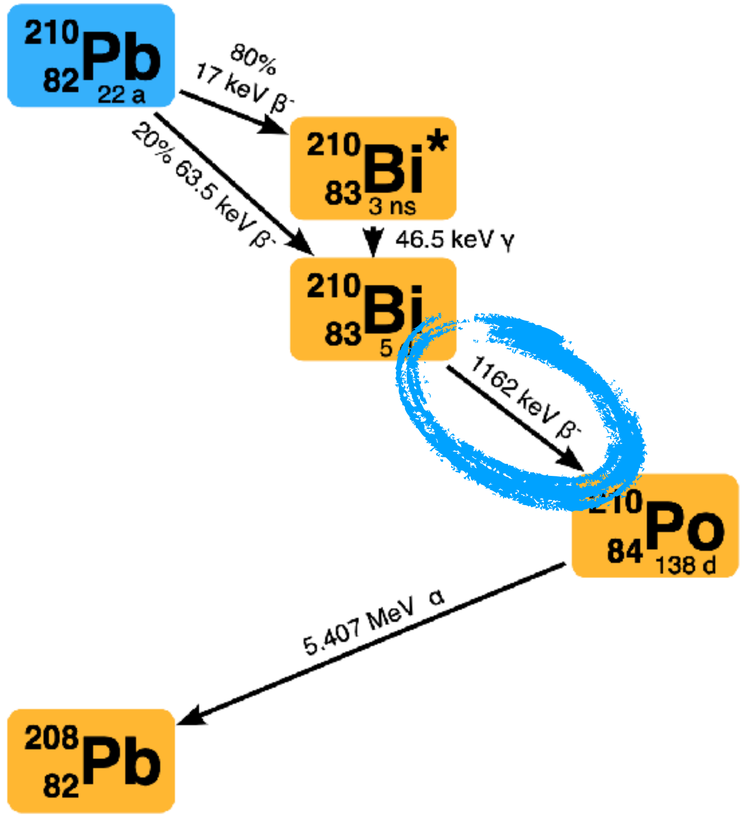
- Extremely low noise figures
  - known from bench tests
  - but now also observed in-situ on detector
- This is a real game changer in the application of CMOS sensors
  - it is orders of magnitude lower than previous generations of MAPS have achieved
  - essentially, a noise-free operation is now in reach



ALPIDE – integrated onto ITS2

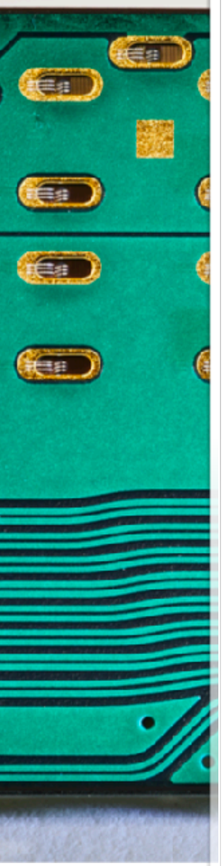
on-detector performance figures

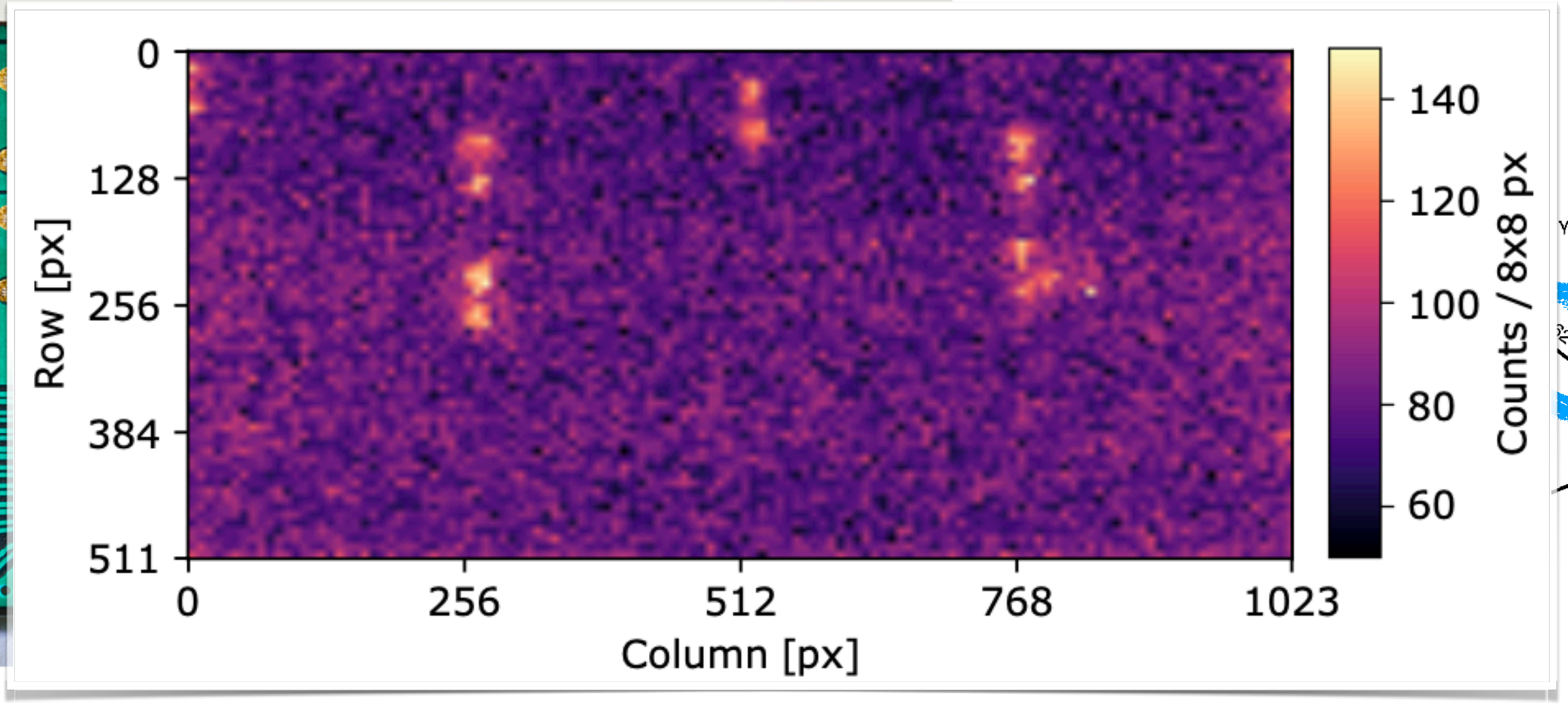




ALPIDE – integrated onto ITS2

on-detector performance figures

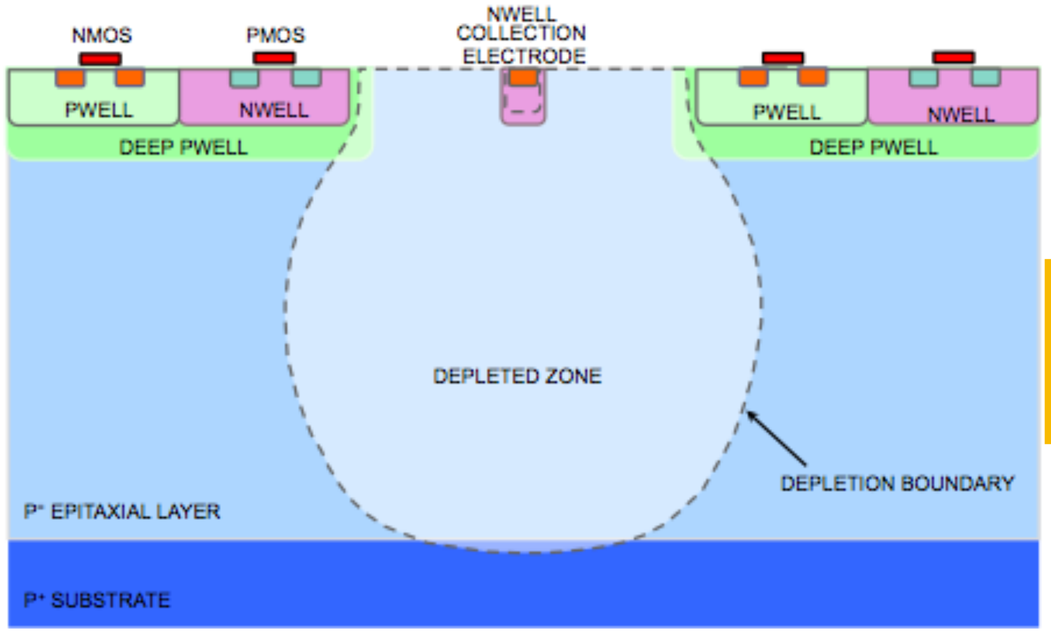




ALICE offspring

process modification for better timing and radiation hardness

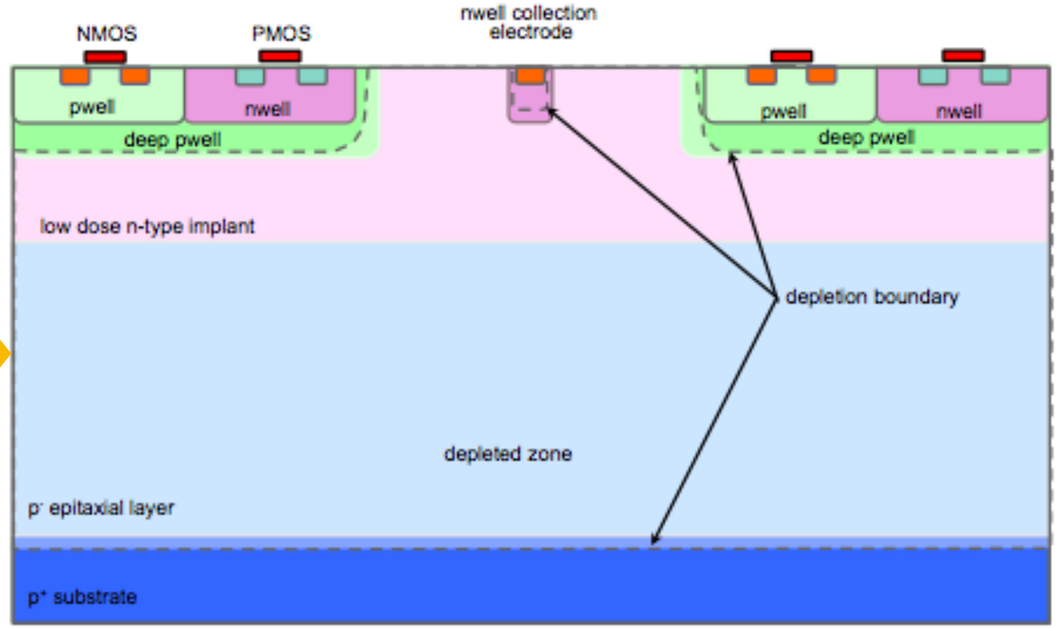
Foundry standard process



Partially depleted epitaxial layer
Charge collection time < 30 ns
Operational up to 10^{14} 1 MeV n_{eq}/cm^2

Developed and prototyped within ALPIDE R&D

Modified process CERN/Tower



Fully depleted epitaxial layer
Charge collection time < 1 ns
Operational up to 10^{15} 1 MeV n_{eq}/cm^2

Excellent co-operation with foundry!

Now being further pursued with MALTA, CLICpix, FastPix, …

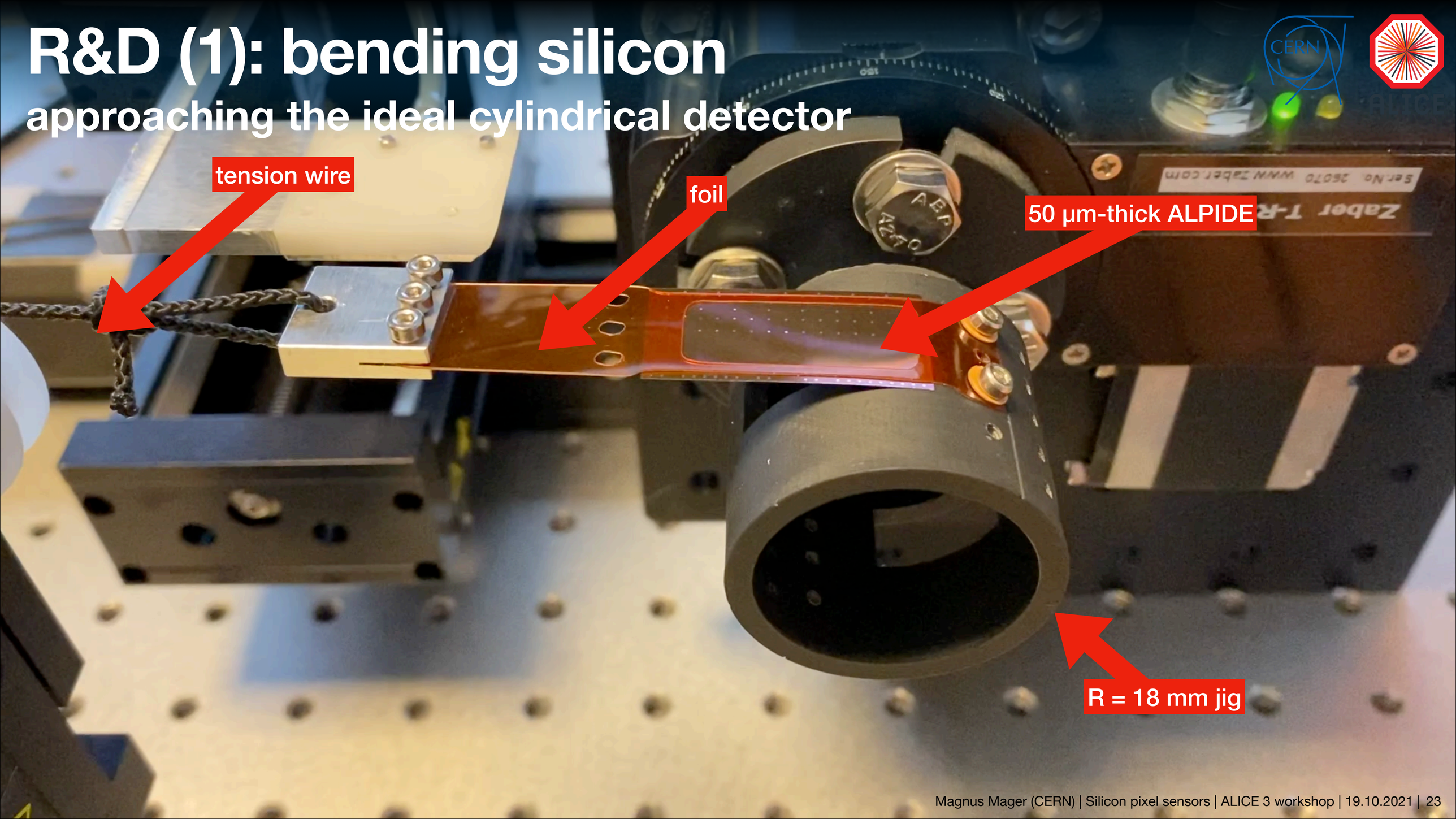
More details:
NIM **A871** (2017) 90-96
https://doi.org/10.1016/j.nima.2017.07.046

Now, it is an important asset for ALICE 3

R&D fronts (selection)

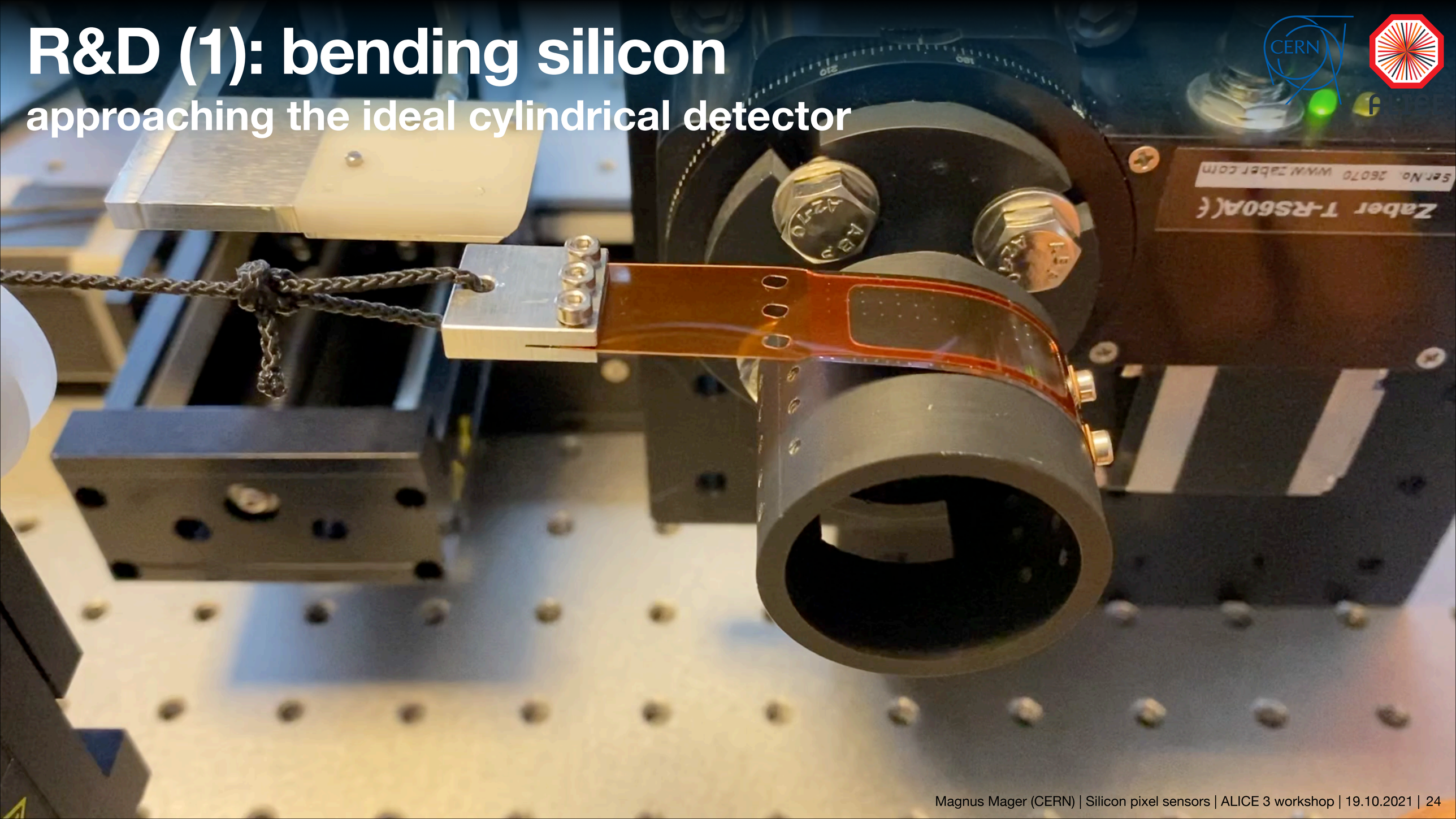
R&D (1): bending silicon

approaching the ideal cylindrical detector



R&D (1): bending silicon

approaching the ideal cylindrical detector



R&D (1): bending silicon

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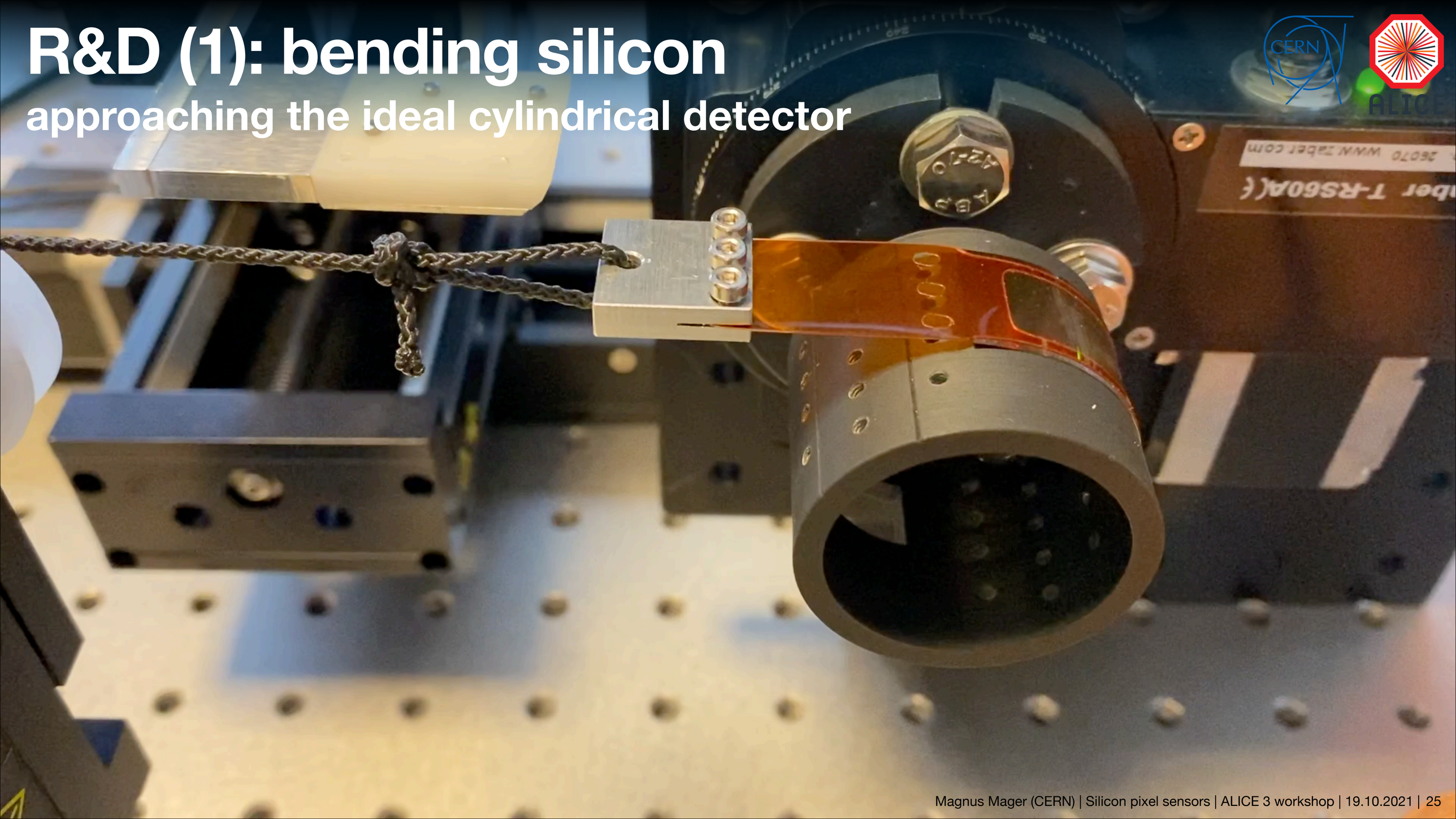
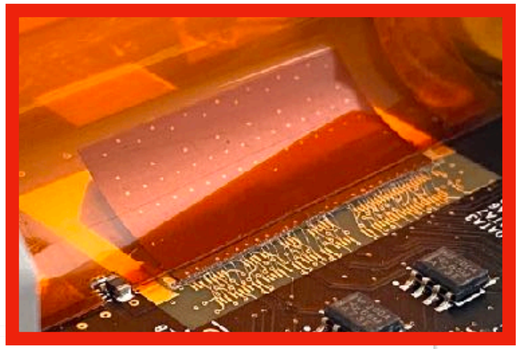


Test beam results (1)

1st paper: arxiv:2105.13000



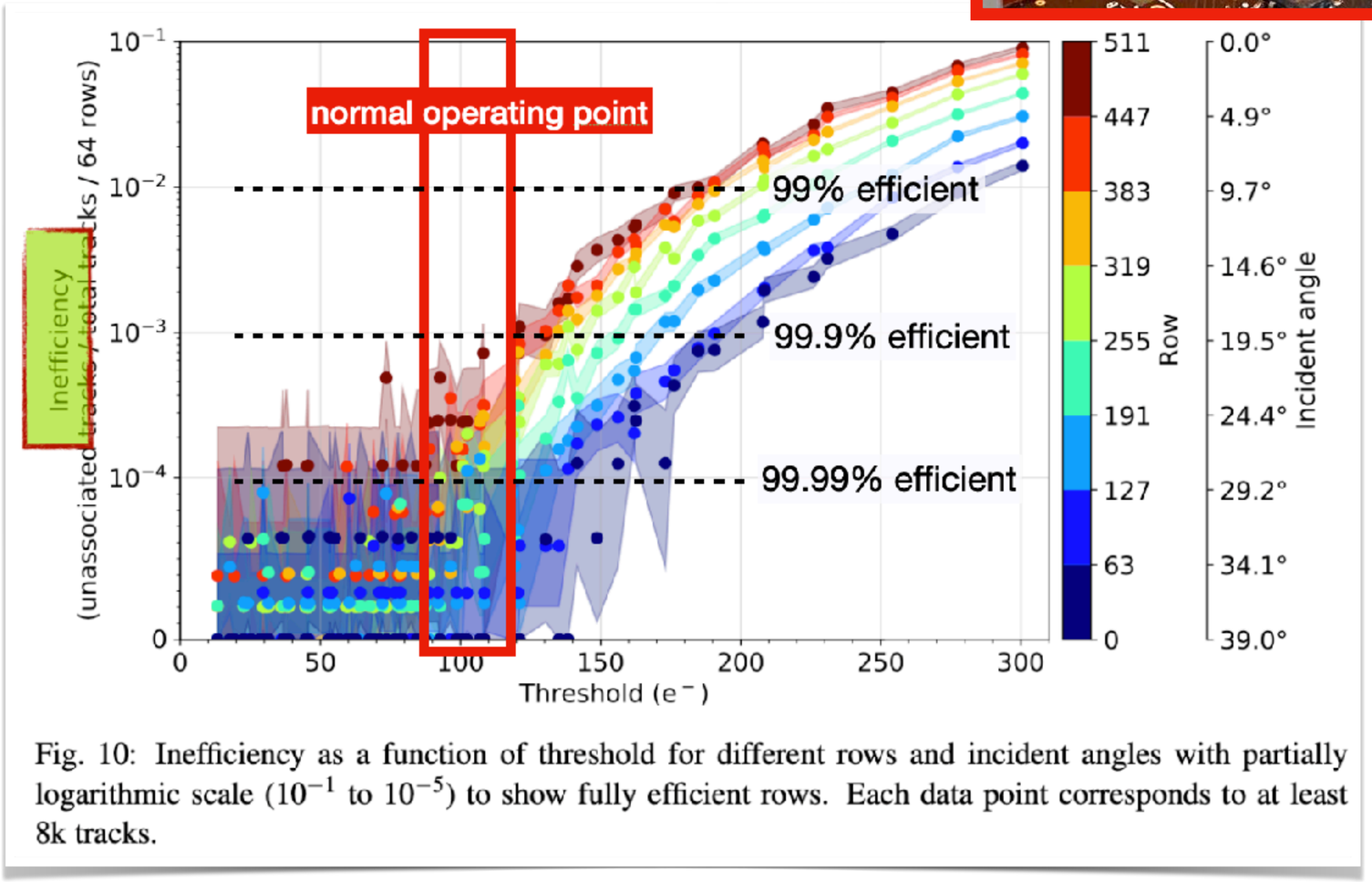


Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. Each data point corresponds to at least 8k tracks.

First demonstration of in-beam performance of bent Monolithic Active Pixel Sensors

ALICE ITS3

[a] European Organisation for Nuclear Research (CERN), Geneva, Switzerland
[b] GSI, Darmstadt, Germany
[c] Heidelberg University, Heidelberg, Germany
[d] INFN & University of Trieste, Trieste, Italy

Abstract

A novel approach for designing the next generation of vertex detectors foresees to employ wafer-scale sensors that can be bent to truly cylindrical geometries after thinning them to thicknesses of 20-40 µm. To solidify this concept, the feasibility of operating bent MAPS was demonstrated using 1.5 cm × 3 cm ALPIDE chips. Already with their thickness of 50 µm, they can be successfully bent to radii of about 2 cm without any signs of mechanical or electrical damage. During a subsequent characterisation using a 5.4 GeV electron beam, it was further confirmed that they preserve their full electrical functionality as well as particle detection performance.

In this article, the bending procedure and the setup used for characterisation are detailed. Furthermore, the analysis of the beam test, including the measurement of the detection efficiency as a function of beam position and local inclination angle, is discussed. The results show that the sensors maintain their excellent performance after bending to radii of 2 cm, with detection efficiencies above 99.9 % at typical operating conditions, paving the way towards a new class of detectors with unprecedented low material budget and ideal geometrical properties.

Keywords: Monolithic Active Pixel Sensors, Solid state detectors, Bent sensors

1. Introduction

The precision of barrel vertex detectors is mainly determined by three contributions: their radial distance to the interaction point, their material budget, and their intrinsic sensor resolution. In order to achieve hermiticity, they are typically built out of detector staves placed in layers around the beam pipe. This arrangement effectively sets a practical limit on the first two factors. ALICE,

*Corresponding author

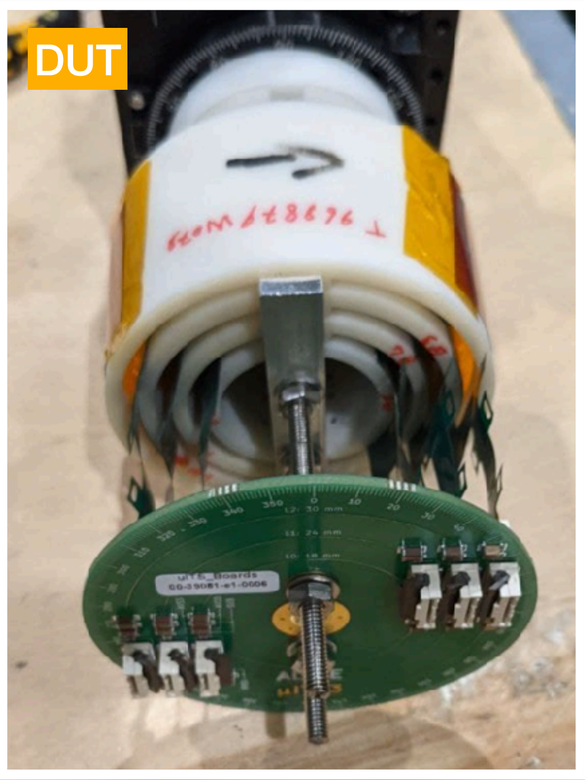
Preprint submitted to Nucl. Instrum. Methods Phys. Res. A *February 22, 2021*

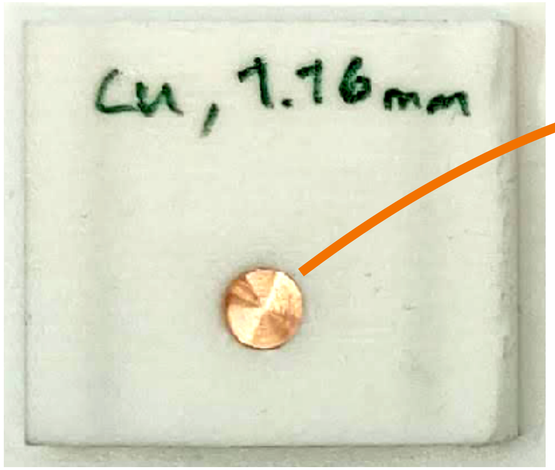
Clearly proving that bent MAPS are working!

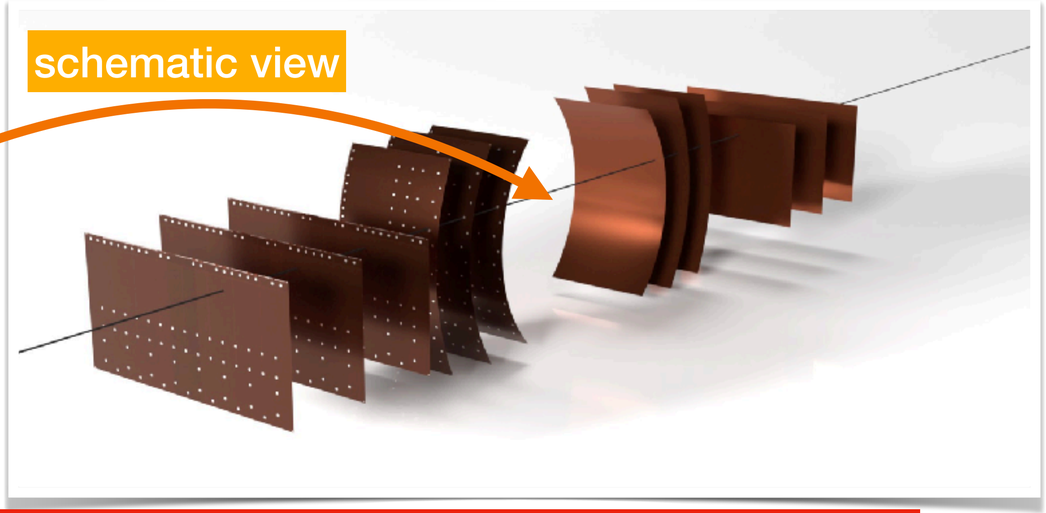
Test beam results (2)

µITS3

- µITS3, i.e. 6 ALPIDEs at ITS3 radii
  - two complete setups based on “gold” quality ALPIDE chips
  - one has a Cu target in the center: expect to see 120 GeV proton/pion–Cu collisions
- Several days of continuous data taking
  - detailed analysis ongoing







First “real” experiment, allows to study tracking/reconstruction

Test beam results (2)

µITS3

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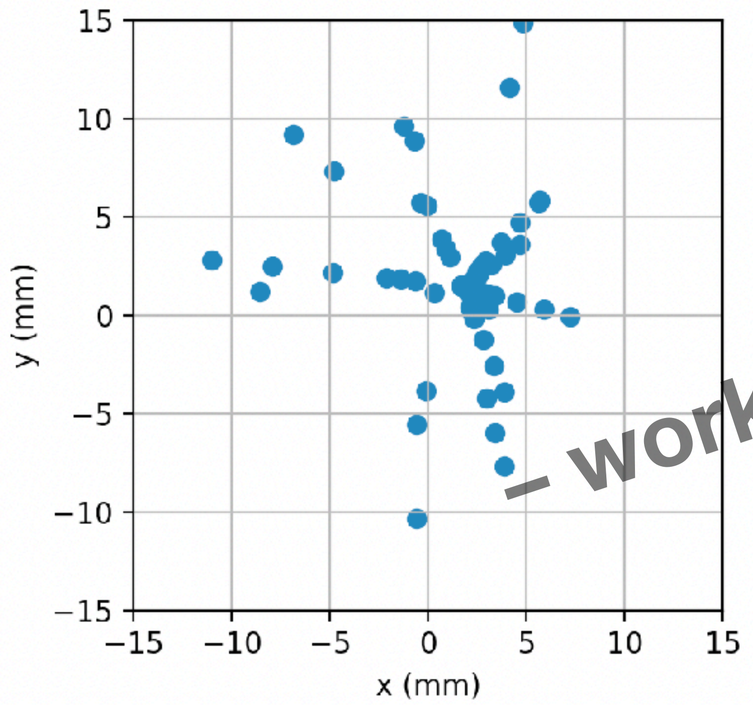
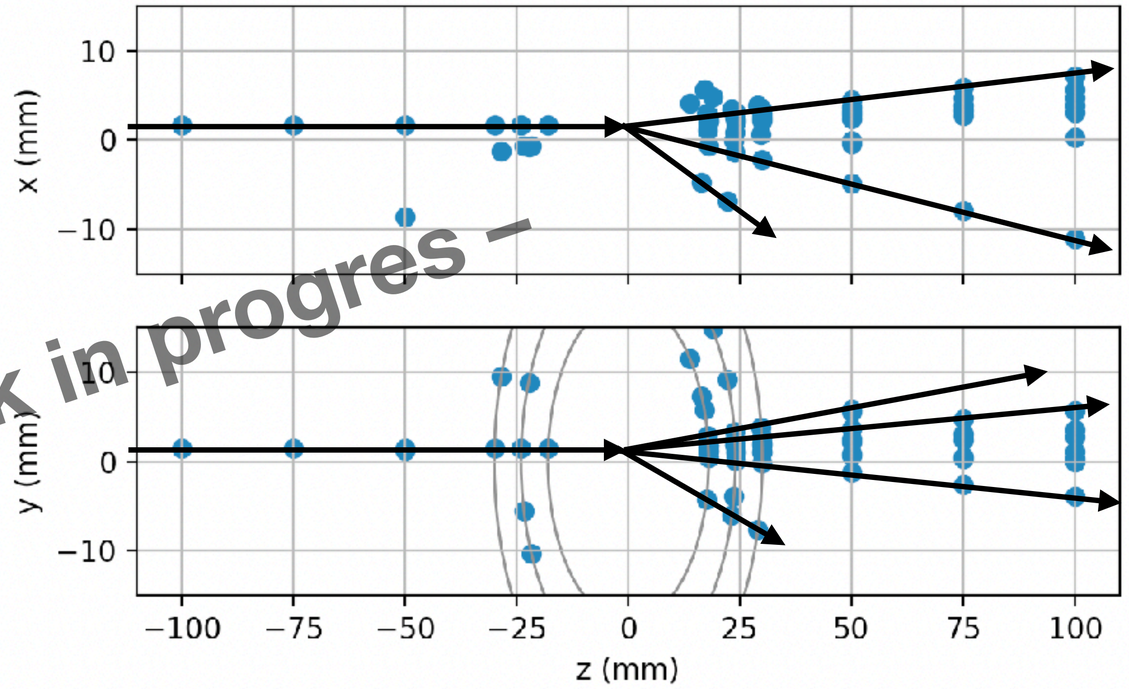
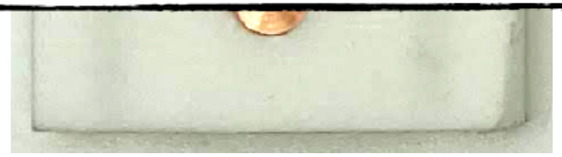
Example event

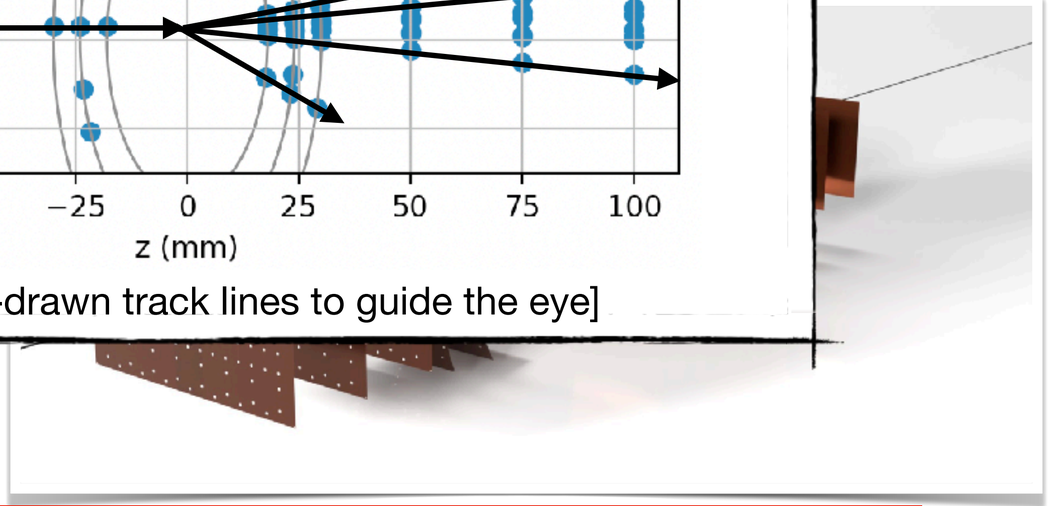




– work in progres –

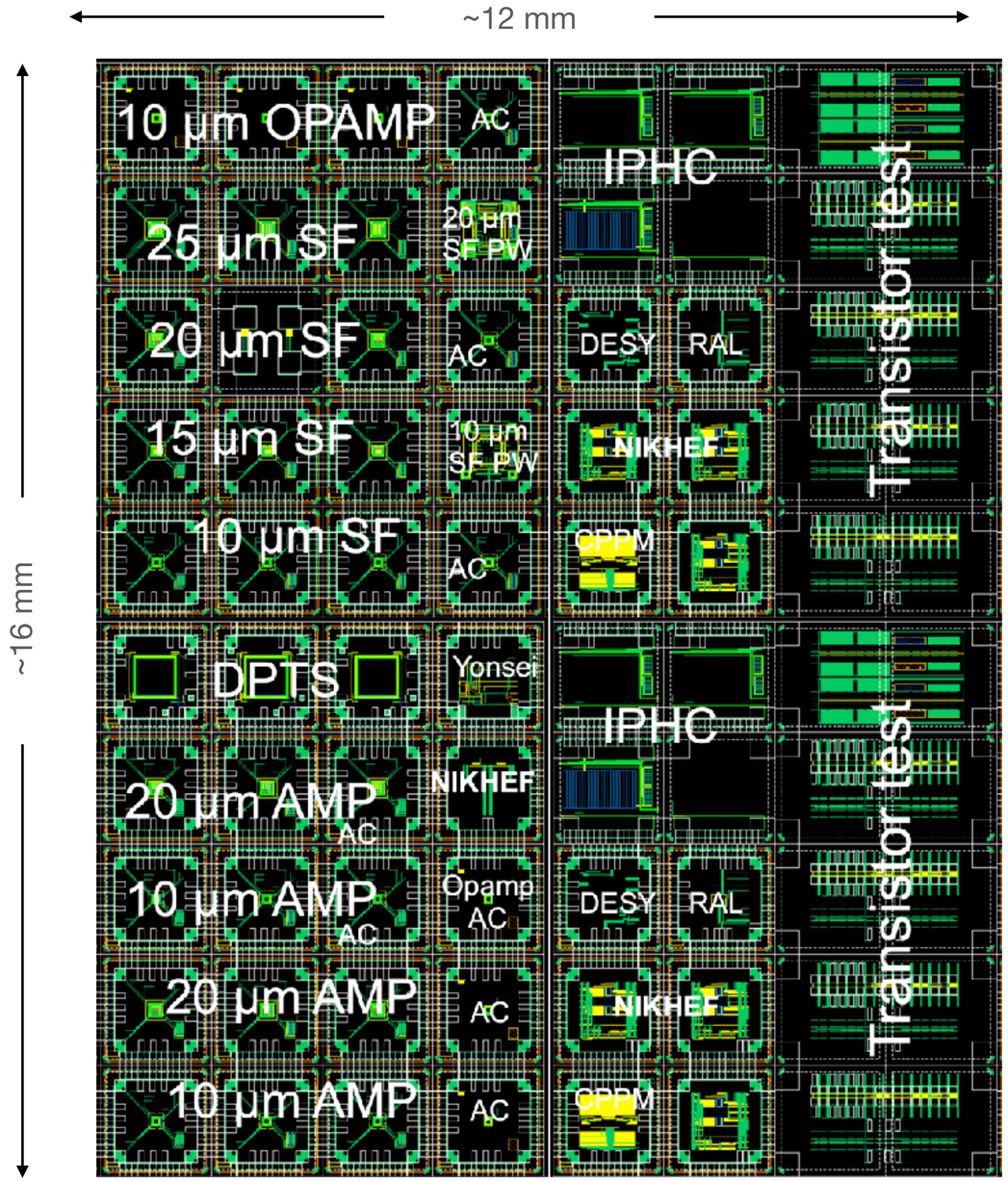
[few hand-drawn track lines to guide the eye]





First “real” experiment, allows to study tracking/reconstruction

R&D (2): 65 nm



- First submission in TowerJazz 65nm
  - scoped within CERN EP R&D WP1.2
  - significant drive from ITS3
  - + important contributions from outside (not ALICE) groups
- Contained several test chips
  - radiation test structures
  - pixel test structures
  - pixel matrices
  - analog building blocks (band gaps, LVDS drivers, etc)

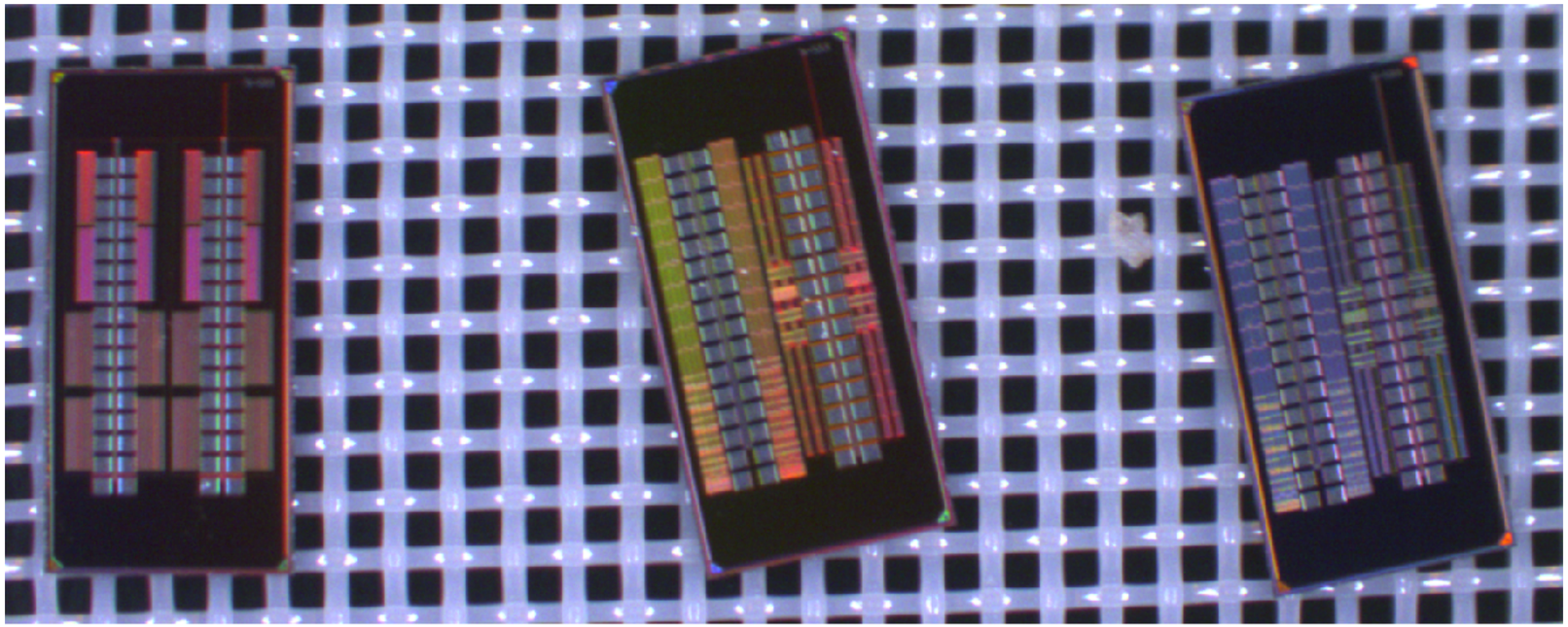
65 nm
first prototypes

- The first (and still small) prototypes have just arrived
- Intensive test campaign has started at several institutes

Transistor test structures

measuring radiation hardness

- Compatible with existing test system based on probe card
- Tests have already started
  - no apparent showstoppers so far
  - detailed analysis ongoing and in discussion with foundry

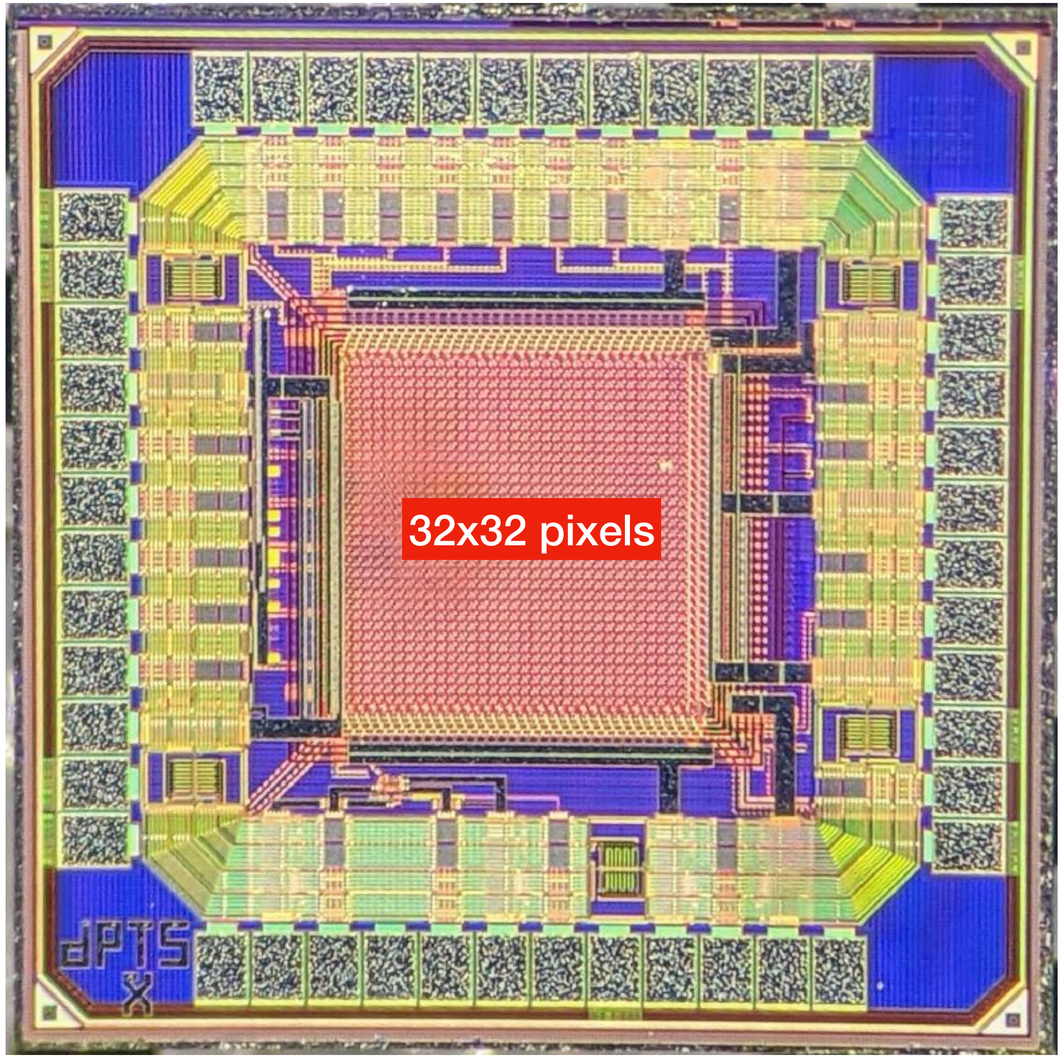


Very encouraging results, clears first milestone of 65 nm verification

Digital Pixel Test structure (DPTS)

measuring pixel performances

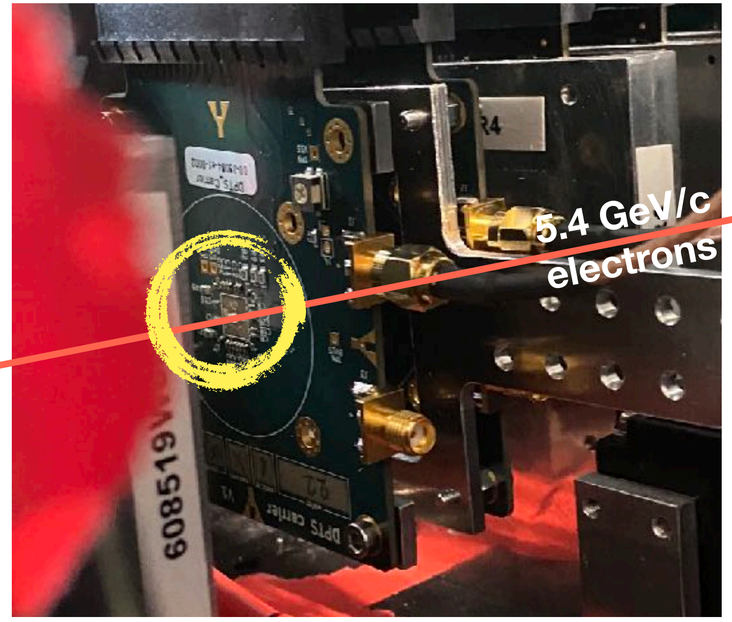
- Most “aggressive” chip in MLR1
- 32 × 32 pixels, 15 µm pitch
  - sizeable prototype, allows for “easy” test beam integration
- Asynchronous digital readout with ToT information
- Allows to verify:
  - sensor performance
  - front-end performance
  - basic digital building blocks
  - SEU cross-sections of registers

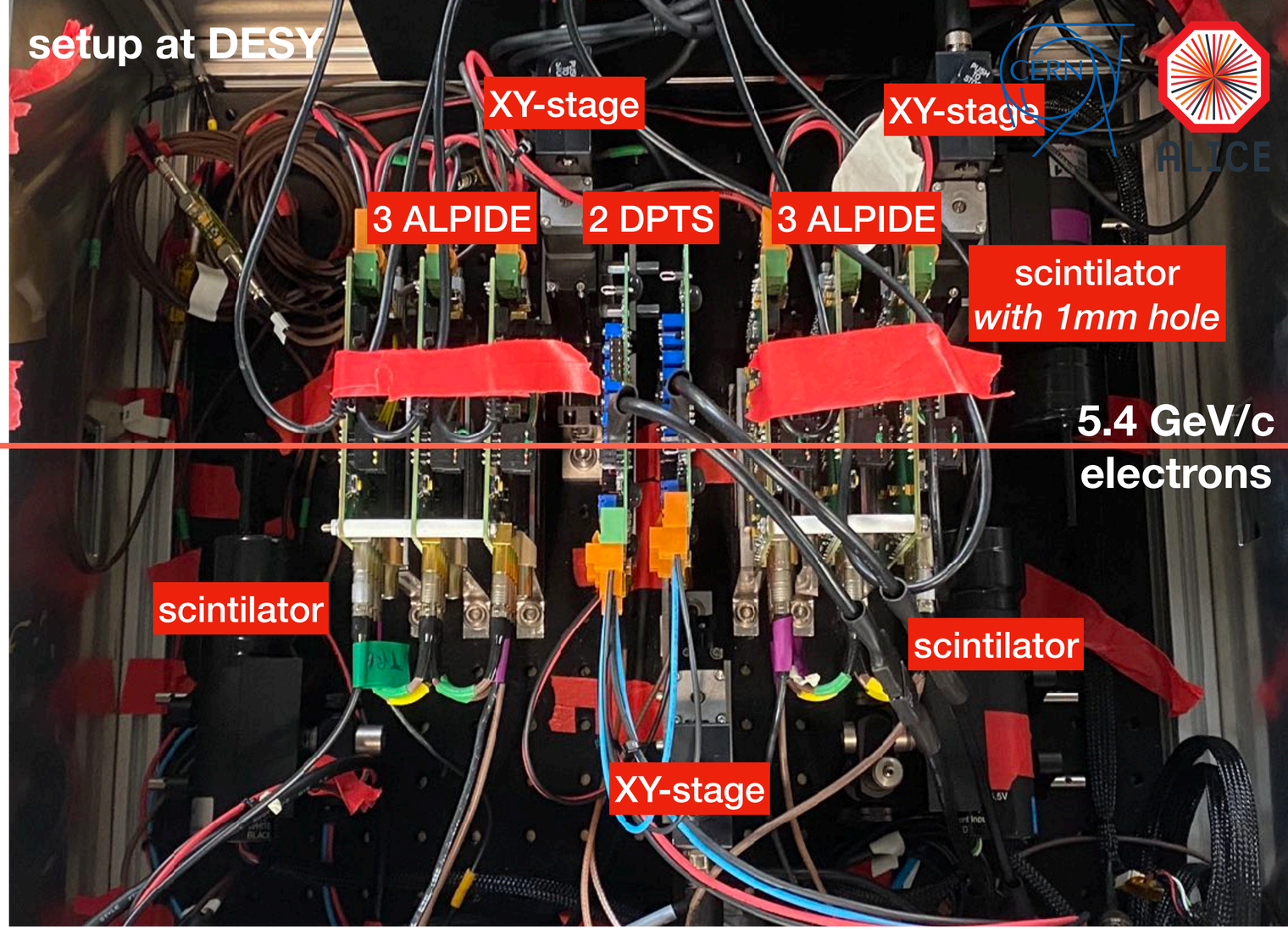


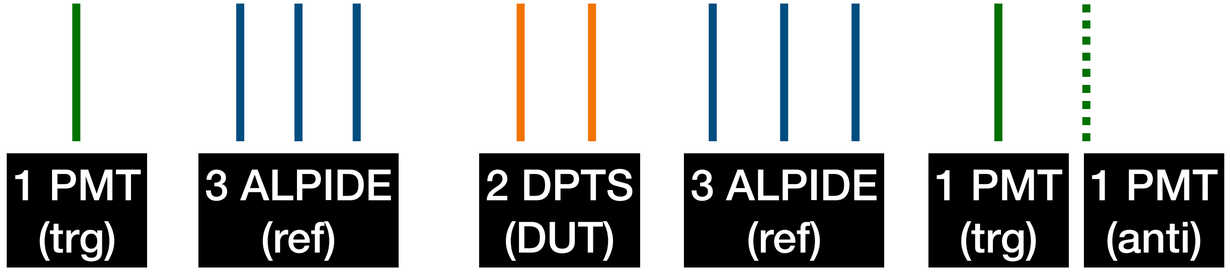
First beam test

Telescope with DPTS

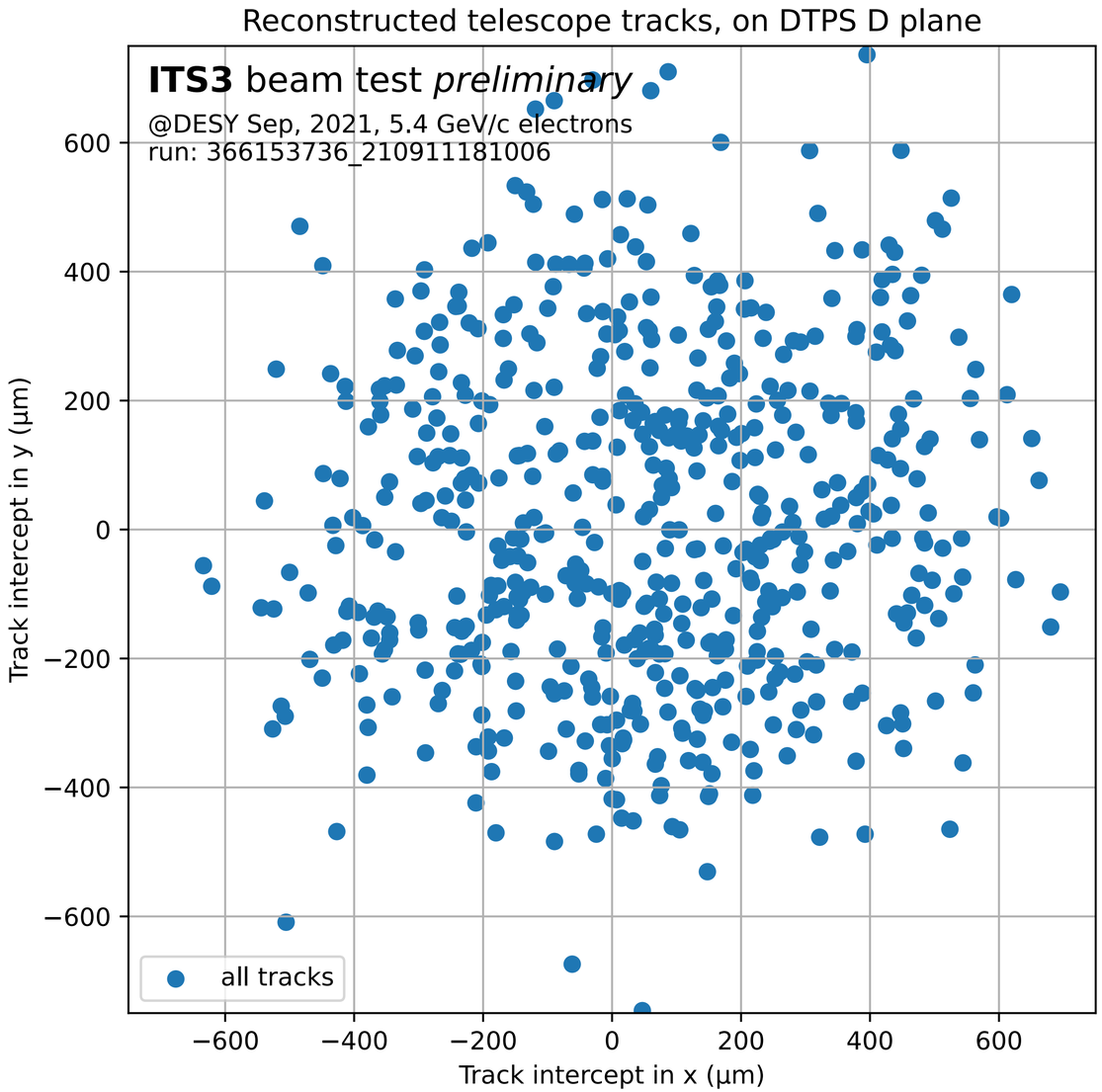
- Setup at DESY (Sep 2021)
- As we speak, another setup is running at the PS
- More beams at SPS and DESY planned for this year







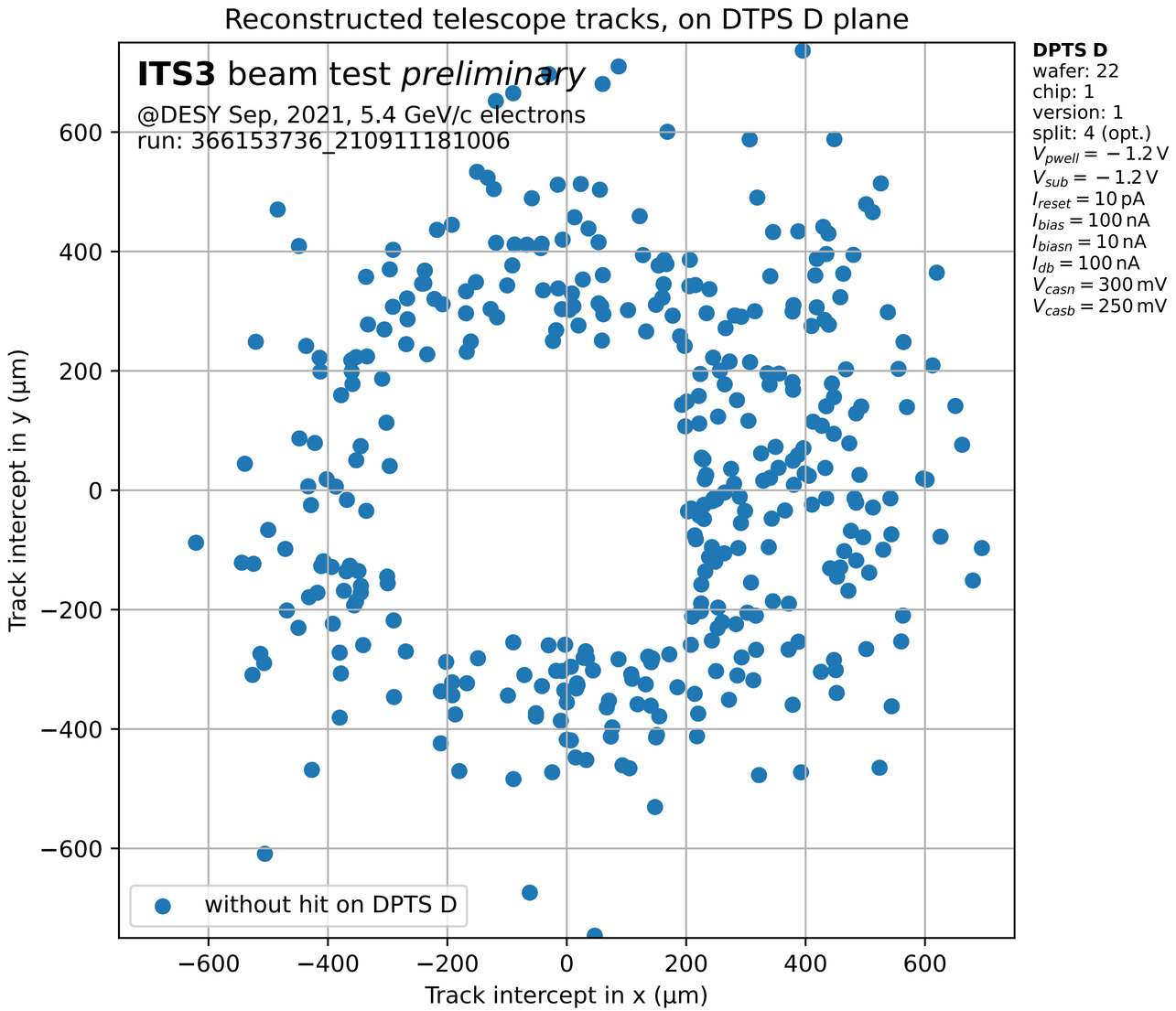
DPTS detection efficiency



- Beam spot and trigger tuned to illuminate a small area

first few % of total statistics analysed

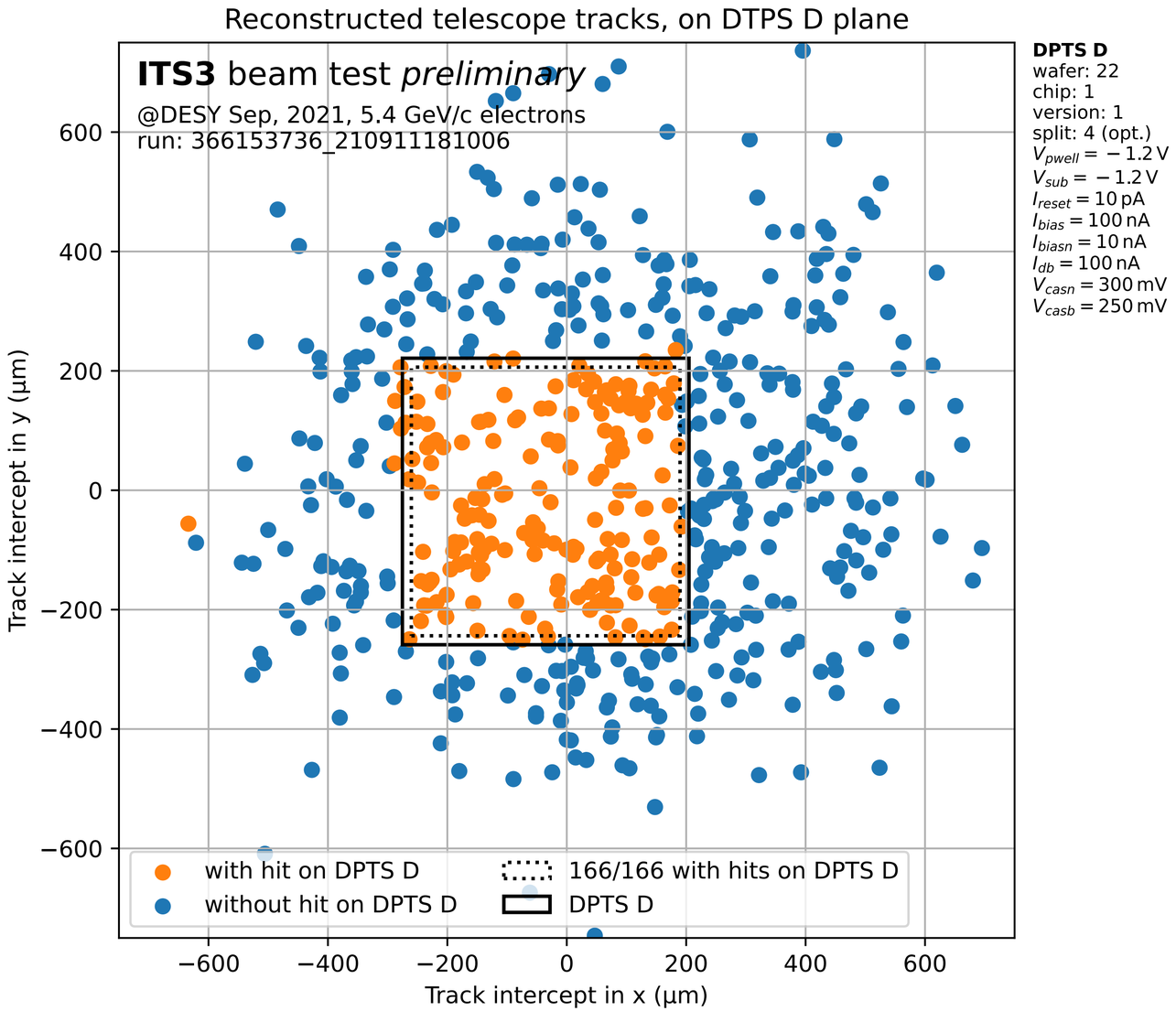
DPTS detection efficiency



- Beam spot and trigger tuned to illuminate a small area
- Looking at tracks without hit in the DPTS, a clear 100% shadow is seen

first few % of total statistics analysed

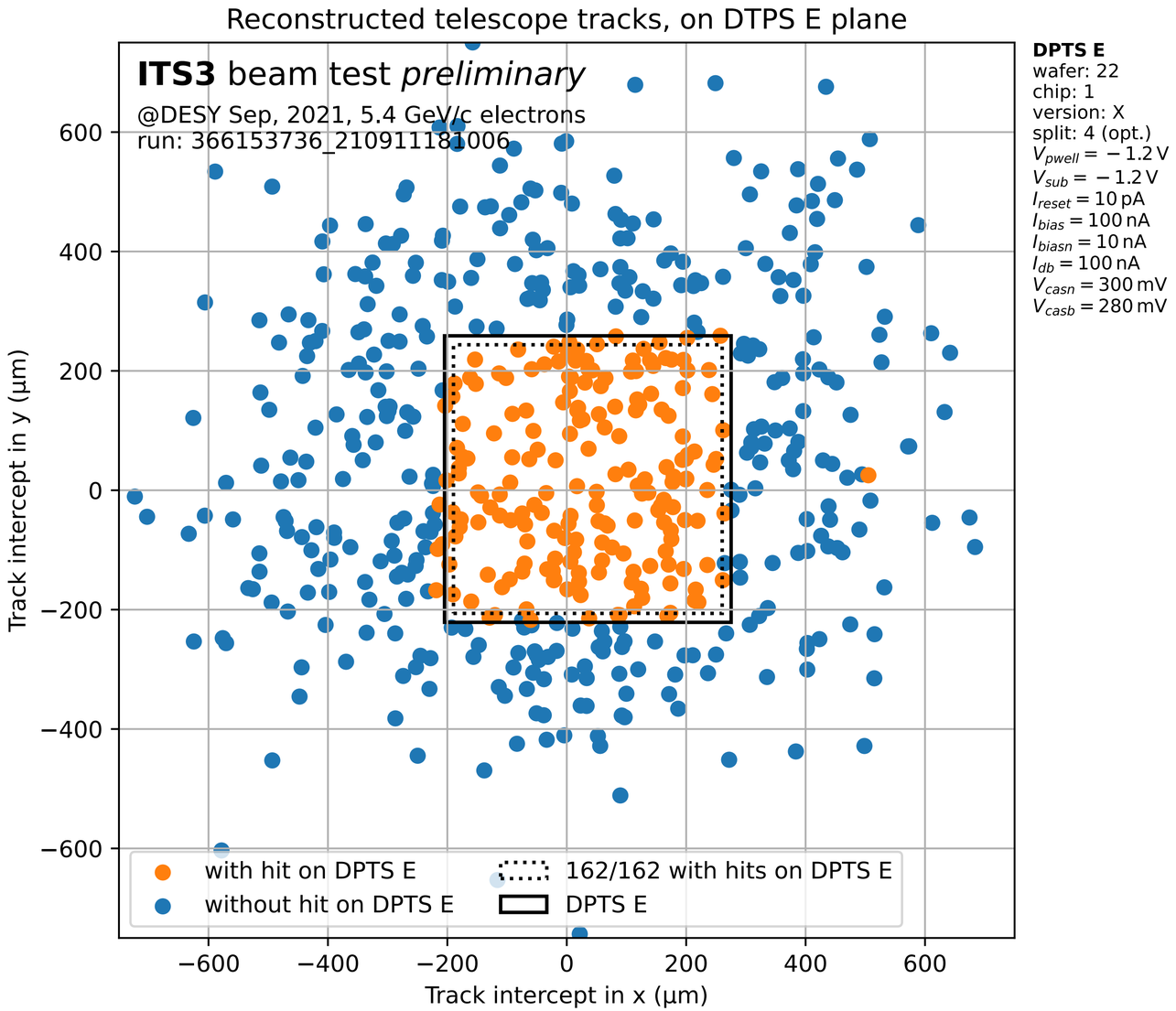
DPTS detection efficiency



- Beam spot and trigger tuned to illuminate a small area
- Looking at tracks without hit in the DPTS, a clear 100% shadow is seen
- The area matches precisely the DPTS
- **166/166** tracks in region of interest

first few % of total statistics analysed

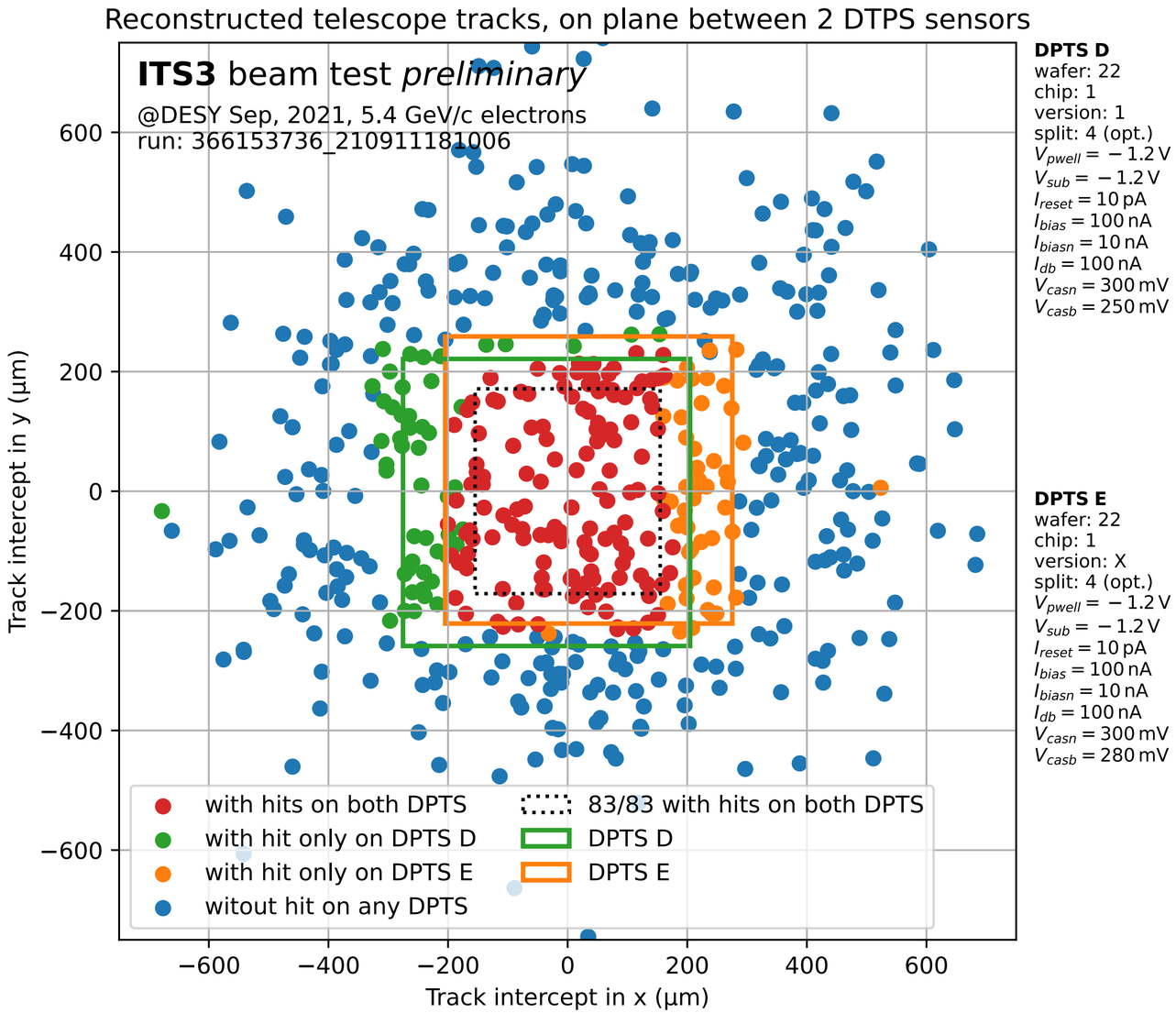
DPTS detection efficiency



- Beam spot and trigger tuned to illuminate a small area
- Looking at tracks without hit in the DPTS, a clear 100% shadow is seen
- The area matches precisely the DPTS
- **166/166** tracks in region of interest
  - similar for second chip **(162/162)**

first few % of total statistics analysed

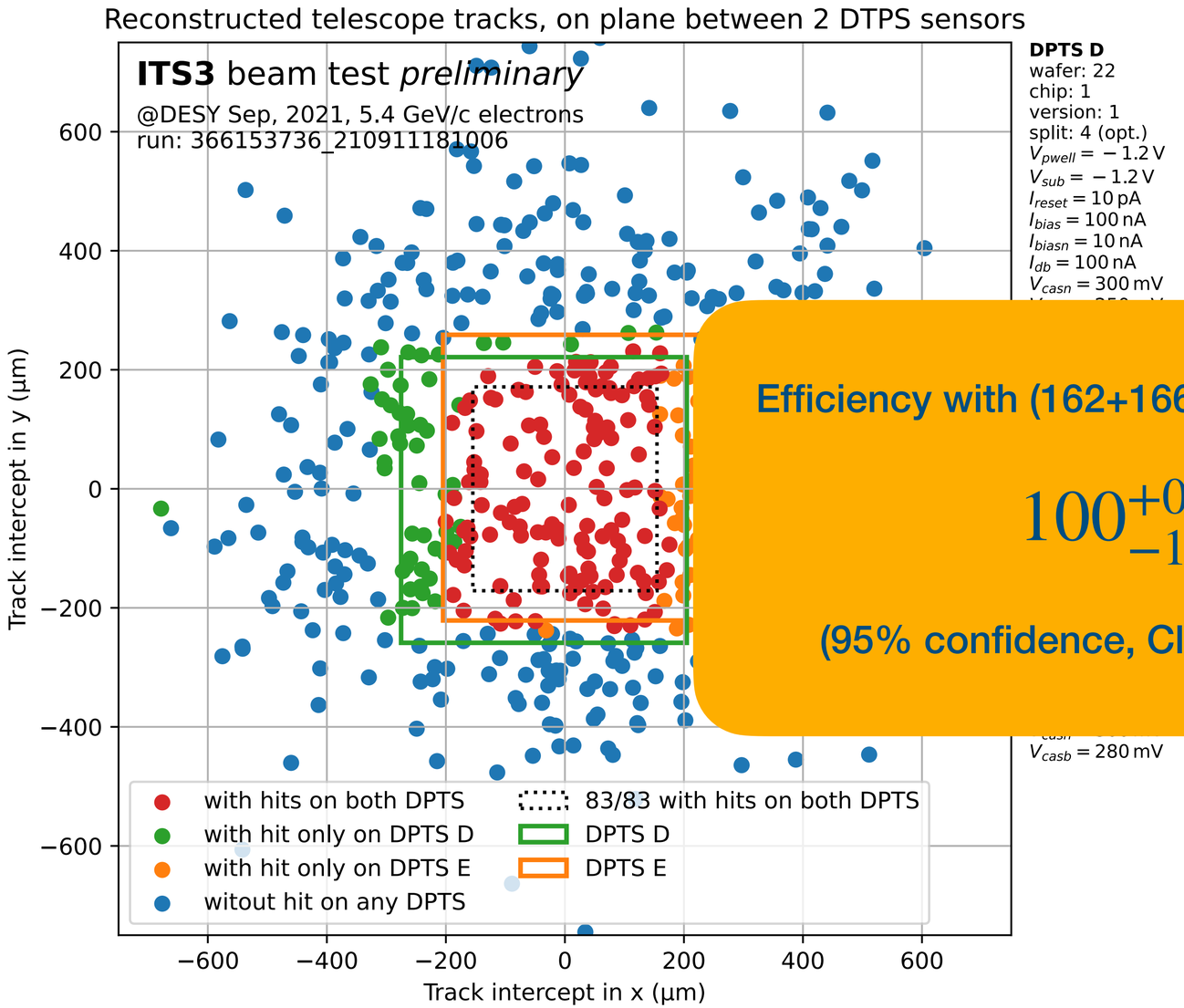
DPTS detection efficiency



first few % of total statistics analysed

- Beam spot and trigger tuned to illuminate a small area
- Looking at tracks without hit in the DPTS, a clear 100% shadow is seen
- The area matches precisely the DPTS
- **166/166** tracks in region of interest
  - similar for second chip **(162/162)**
  - and even for both in coincidence **(83/83)**

DPTS detection efficiency



Efficiency with (162+166)/(162+166) tracks:

$$100^{+0}_{-1}\ \%$$

(95% confidence, Clopper-Pearson)

- Beam spot and trigger tuned to illuminate a small area
- Looking at tracks without hit in the ar 100% shadow is seen
- atches precisely the
- cks in region of interest
  - similar for second chip **(162/162)**
  - and even for both in coincidence **(83/83)**

Excellent sensor *and* front-end performance already from *first* 65 nm prototype

Summary and outlook

- ITS3 and the ALICE 3 tracker are ***the* two concrete** undertakings that are and will advance MAPS technology
  - similar situation as ITS2, which marked a quantum step
- ALICE is at the forefront, introducing new technologies in HEP right now:
  - 65 nm MAPS
  - bent vertex detectors
- **ALICE 3** pushes this limits further
  - another order of magnitude higher in volume
  - higher demands in rates and radiation hardness
  - further commercialisation of components
- **Exciting times** and excellent future prospects

Thank you!