A. Alici, S. Bufalino, L. Pancheri, A. Rivetti

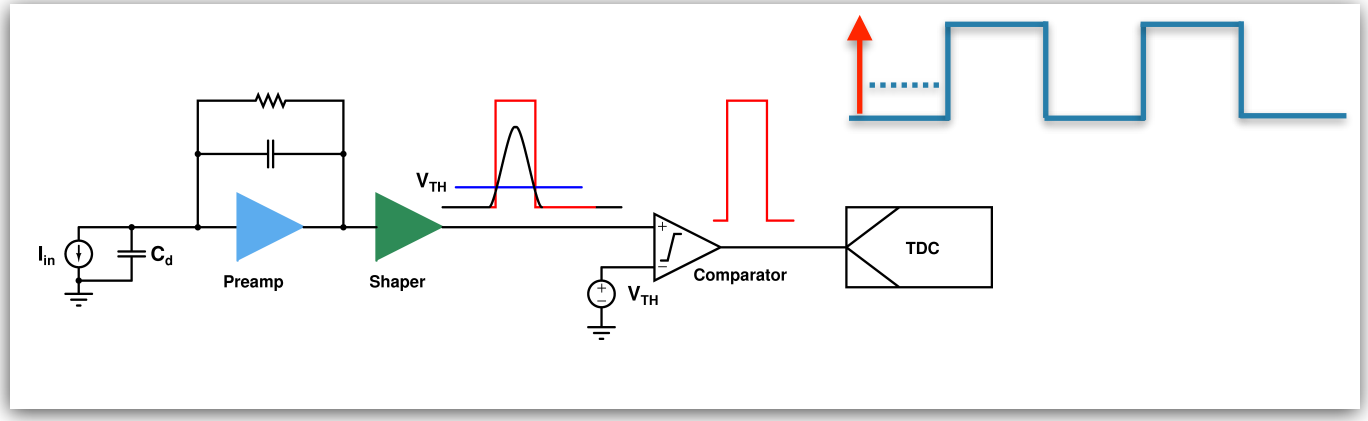
Silicon timing sensors

Setting the stage

	Inner TOF	Outer TOF	Forward TOF
Radius (m)	0.19	0.85	0.148 to 1.5
Length (m)	1.24	5.58	4.05
Surface (m^2)	1.48	29.8	14
Granularity (mm^2)	1×1	5×5	
Hit rate (kHz/cm^2)	74	4	122
NIEL (1 MeV n_{eq}/cm^2) / month	1.3×10^{11}	6.2×10^9	2.1×10^{11}
TID (rad) / month	4×10^3	2×10^2	6.6×10^3
Material budget ($\%X_0$)	1 to 3	1 to 3	1 to 3
Power density (mW/cm^2)	50	50	50
Time resolution (ps)	20	20	

- Cell size is coarse for the first layer and huge for the outer one
  - Large cell size imply large capacitance → issue for jitter
  - Actual cell size will be determined by timing performance
- Event rates and radiation levels are rather modest
- The readout architecture is mainly constrained by the data rate
- Same technology in both layers with minimal adaptation to optimise the NRE costs
- Most of the power will probably be burnt in the front-end

Key players in a timing detector



- Sensor
- Front-end amplifier
- Discriminator
- Time to Digital Converter
- Clock distribution network

Key players in defining the resolution

$$\sigma_t^2 = \sigma_J^2 + \sigma_L^2 + \sigma_D^2 + \sigma_{TDC}^2 + \sigma_{CDN}^2$$

- Noise in the front-end amplifier
- Landau fluctuation
- Field distortion
- TDC quantisation noise
- Jitter and skew in the clock distribution network

Key players: TDCs and CDNs

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 53, NO. 3, MARCH 2018

A 9-bit 215 MS/s Folding-Flash Time-to-Digital Converter Based on Redundant Remainder Number System in 45-nm CMOS

Bo Wu, *Member, IEEE*, Shuang Zhu, *Member, IEEE*, Yuan Zhou, *Member, IEEE*, and Yun Chiu, *Senior Member, IEEE*

	This work		JSSC '10 [7]	JSSC '14 [9]	JSSC '13 [10]	JSSC '13 [32]	ISSCC'15 [33]
Architecture	RNS		2D Vernier	Pipeline	Asyn. Pipeline	Two-Step	Flash
No. of bits	8.94	7.71	7	9	10	7	10
Resolution/ LSB size [ps]	9.4		4.8	1.12	1.76	3.75	1.17
Speed [MSPS]	215	500	50	250	300	200	100
DNL [LSB]	0.57	0.67	<1	0.6	0.6	0.9	0.8
INL [LSB]	1.1	1.8	3.3/1***	1.7	1.9	2.3	2.3
SSP [LSB]	0.74	0.84	N/A	0.69	0.7	N/A	N/A
N_{linear}*	7.86	6.23	4.90/6.00***	7.57	8.46	5.28	8.28
Power [mW]	24.2	27.3	1.7	15.4	115	3.6	0.78
FoM** [pJ/conv.-step]	0.48	0.73	1.14/0.53***	0.33	1.09	0.46	0.025
Area [mm^2]	0.08		0.02	0.14	0.88	0.02	0.036
Technology	45 nm		65 nm	65 nm	130 nm	65 nm	14 nm
Calibration	No		Background	No	Foreground	No	No

- **TDC bin 10 ps = 2.9 ps rms**

A 4GHz Clock Distribution Architecture using Subharmonically Injection-Locked Coupled Oscillators with Clock Skew Calibration in 16nm CMOS

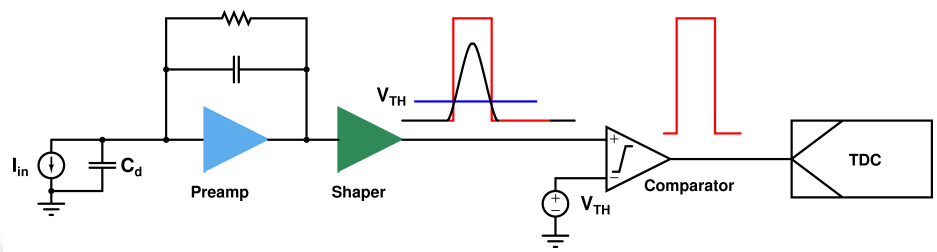
Lan-Chou Cho[1], Feng-Wei Kuo[1], Ron Chen[1], Jack Liu[1], Chewn-Pu Jou[1], Fu-Lung Hsueh[1], R. Bogdan Staszewski[2] [1]TSMC, Hsinchu, Taiwan, [2]University College Dublin, Ireland. email: lcchov@tsmc.com

	This work	[1]	[2]
Technique	SHILCO	Resonant	SHIL PLL
CMOS node	16 nm	180 nm	65 nm
Frequency (GHz)	4	1.5~2.1	2.4
Power (mW)	4.3	500	5.2
Integrated rms Jitter	87 fs	0.9 ps	188 fs
Skew(ps)	<0.8	2	N/A
FOM*	-258	N/A	-247

$* FOM = 20\log(\frac{\sigma_t}{1s}) + 10\log(\frac{P}{1mW})$, σ_t : rms jitter and P : power

Front-end error sources

Timing jitter



$$\sigma_t = \frac{C_d}{Q_{in}}\sqrt{\frac{2kTt_d}{g_m}}$$

$$g_m = \frac{2kTt_d}{\left(\frac{Q_{in}}{C_d}\sigma_t\right)^2}$$

Cd = 1 pF, Qin = 1 fC, td = 1 ns

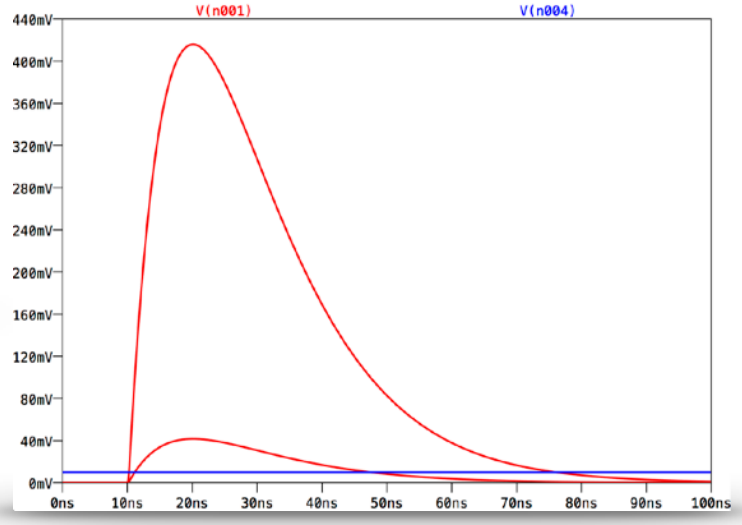
σt = 10 ps ⟶ gm = 3.3 mS, P > 4 mW

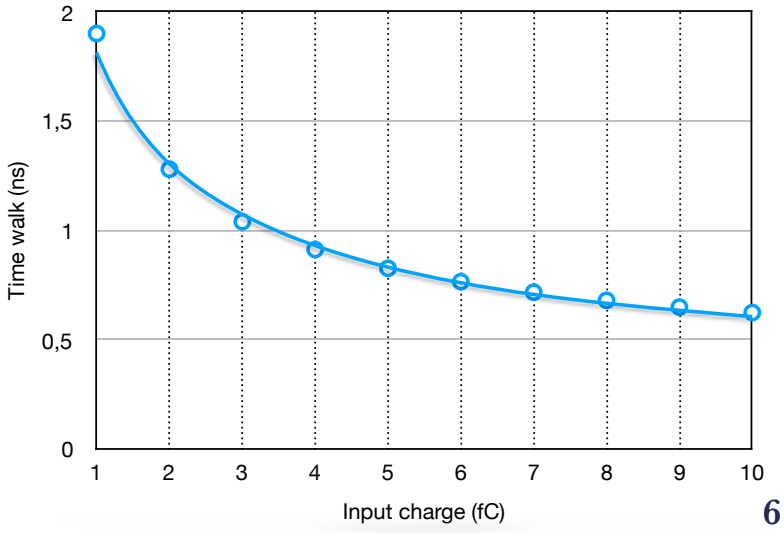
Cd = 100 fF, Qin = 1 fC, td = 1 ns

σt = 10 ps ⟶ gm= 800 µS, P > 40 µW

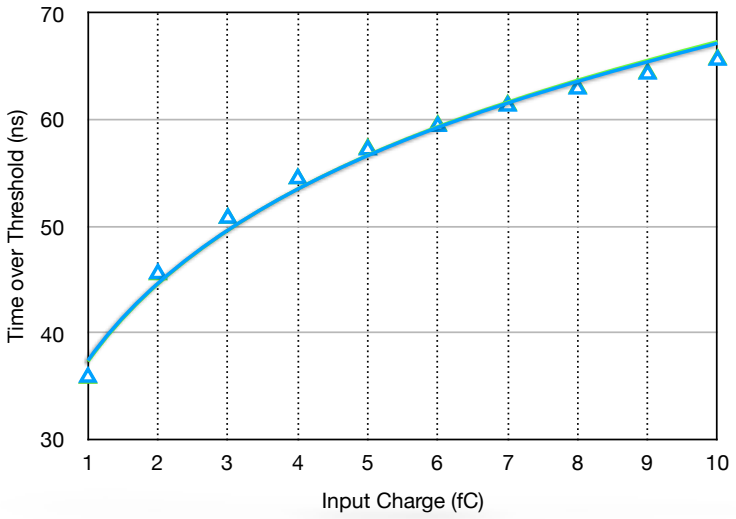
- **Q/C very important for good timing!**

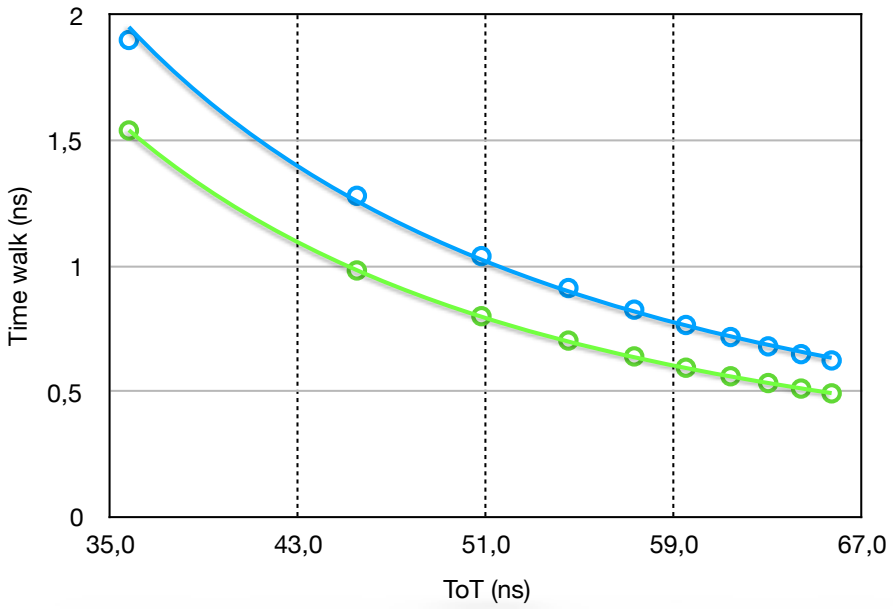
Time walk

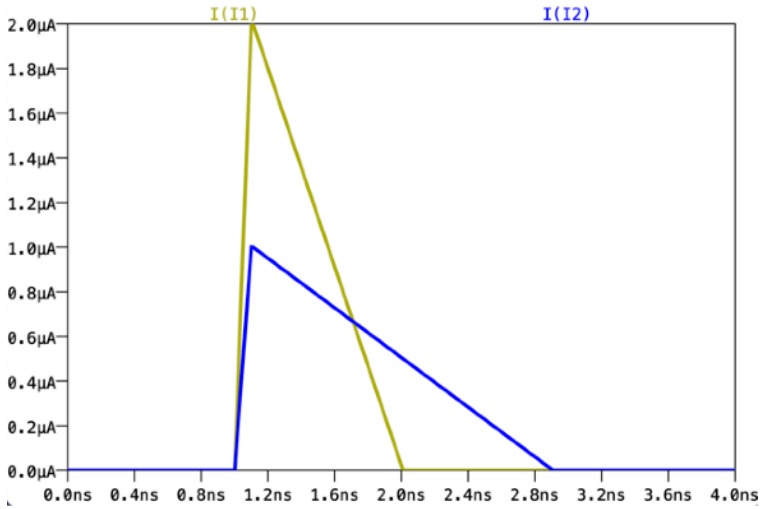




Signal shape and leading edge timing

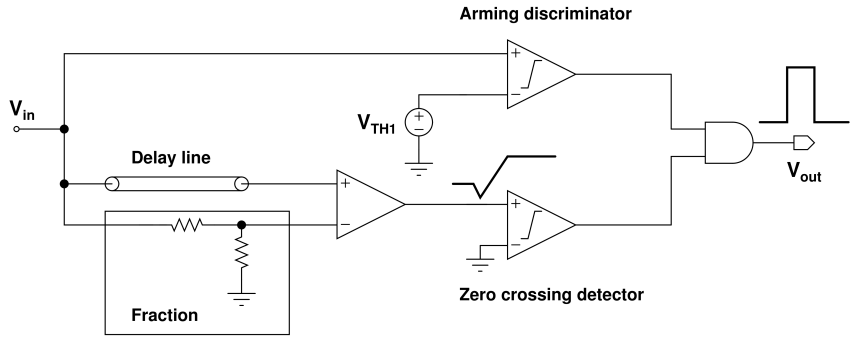






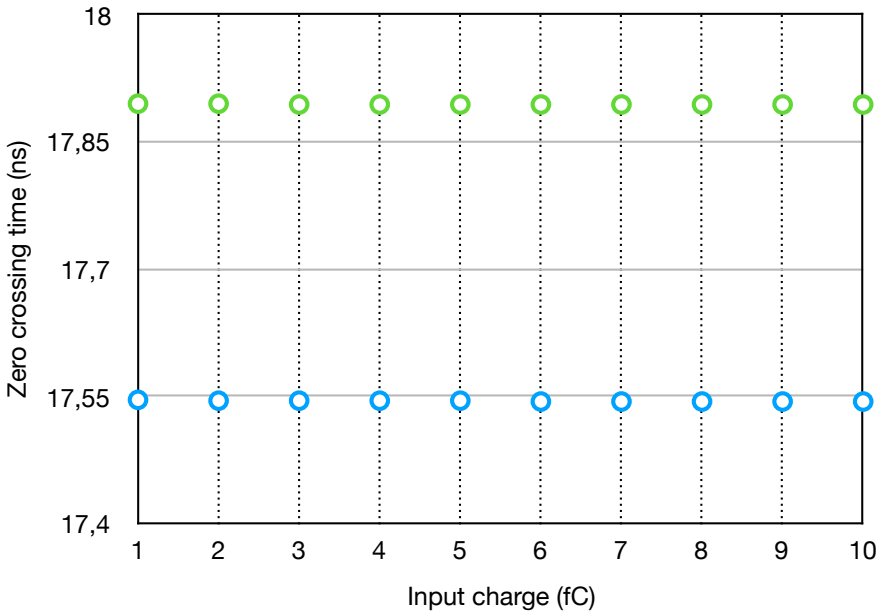
- **Pulse shape variations limit achievable timing resolution**
- **Detector and front-end co-design to predict reasonably timing performance**

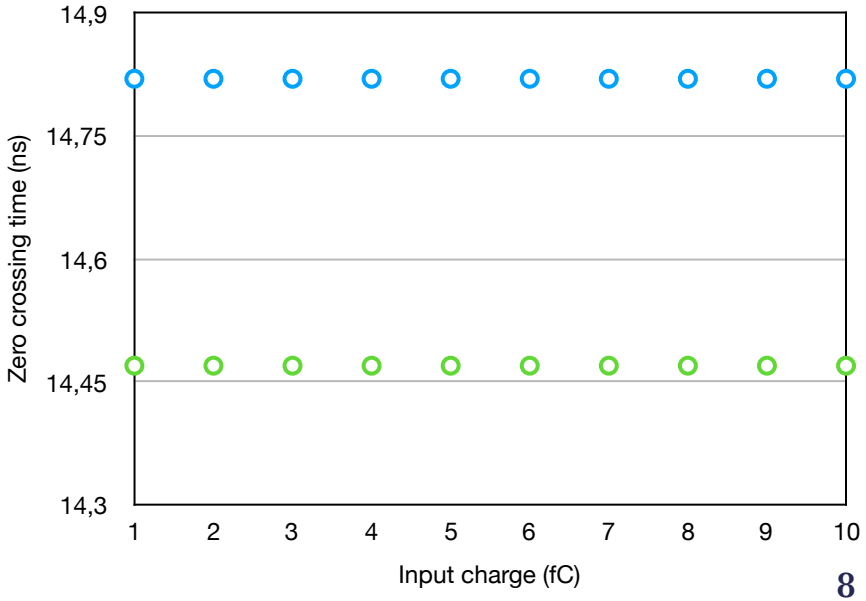
Signal shape and constant fraction timing



$$t_{zc} = \frac{t_d}{1-f}$$

$$t_{zc} = \frac{t_d e^{\frac{t_d}{\tau}}}{e^{\frac{t_d}{\tau}} - f}$$



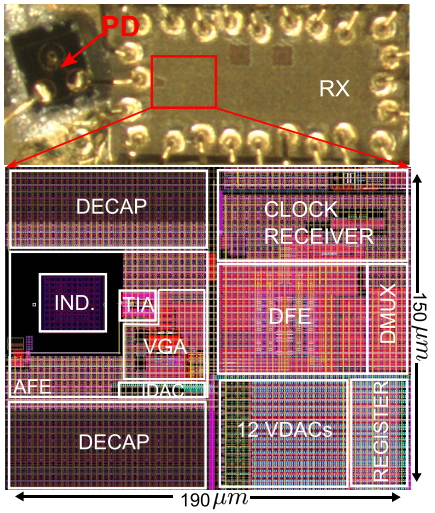


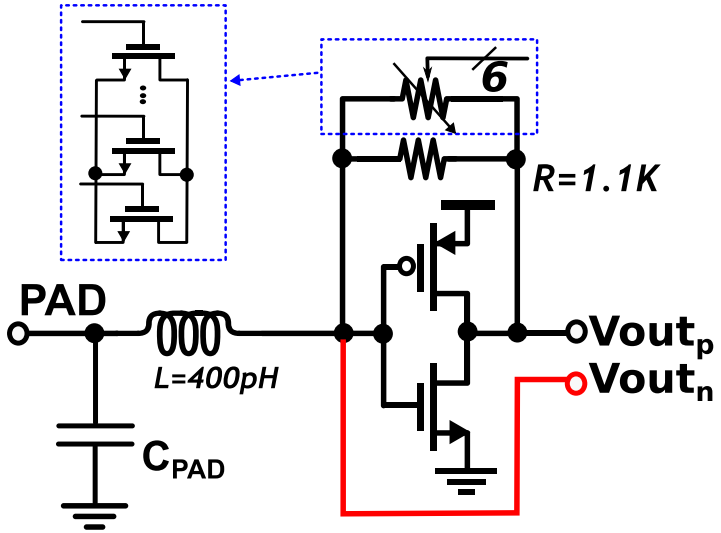
Can we exploit the signal rise time?

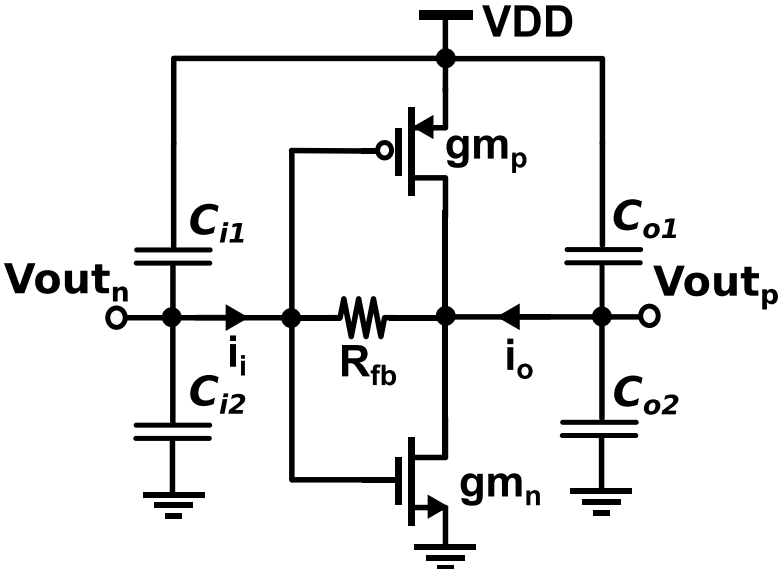
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 52, NO. 12, DECEMBER 2017

A 64-Gb/s 1.4-pJ/b NRZ Optical Receiver Data-Path in 14-nm CMOS FinFET

Ilter Ozkaya, *Student Member, IEEE*, Alessandro Cevrero, *Member, IEEE*, Pier Andrea Francese, *Senior Member, IEEE*, Christian Menolfi, *Member, IEEE*, Thomas Morf, *Senior Member, IEEE*, Matthias Brändli, Daniel M. Kuchta, *Senior Member, IEEE*, Lukas Kull, *Senior Member, IEEE*, Christian W. Baks, Jonathan E. Proesel, *Senior Member, IEEE*, Marcel Kossel, *Senior Member, IEEE*, Danny Luu, *Student Member, IEEE*, Benjamin G. Lee, *Senior Member, IEEE*, Fuad E. Doany, Mounir Meghelli, *Member, IEEE*, Yusuf Leblebici, *Fellow, IEEE*, and Thomas Toifl, *Senior Member, IEEE*



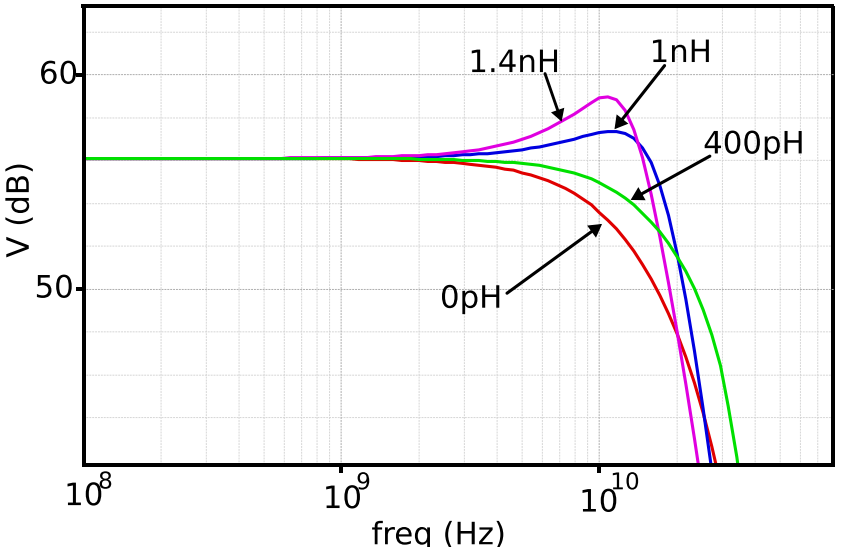


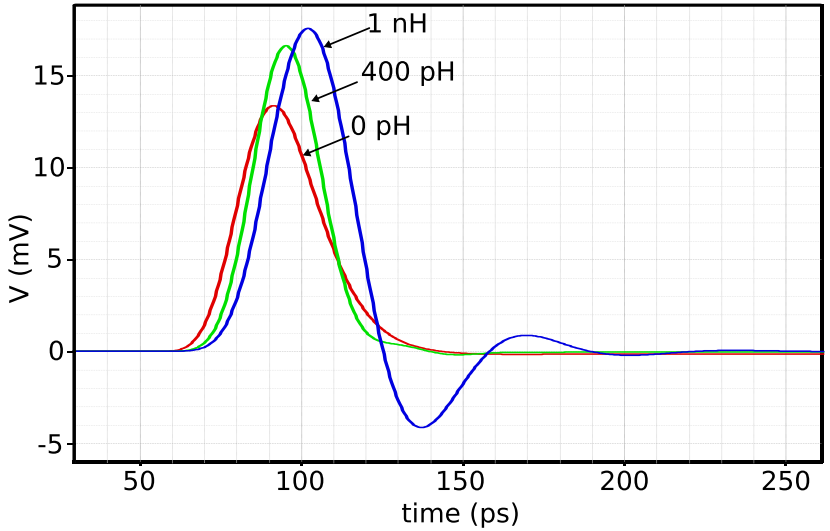


Front-end with 25 ps peaking time!?

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 52, NO. 12, DECEMBER 2017

A 64-Gb/s 1.4-pJ/b NRZ Optical Receiver Data-Path in 14-nm CMOS FinFET

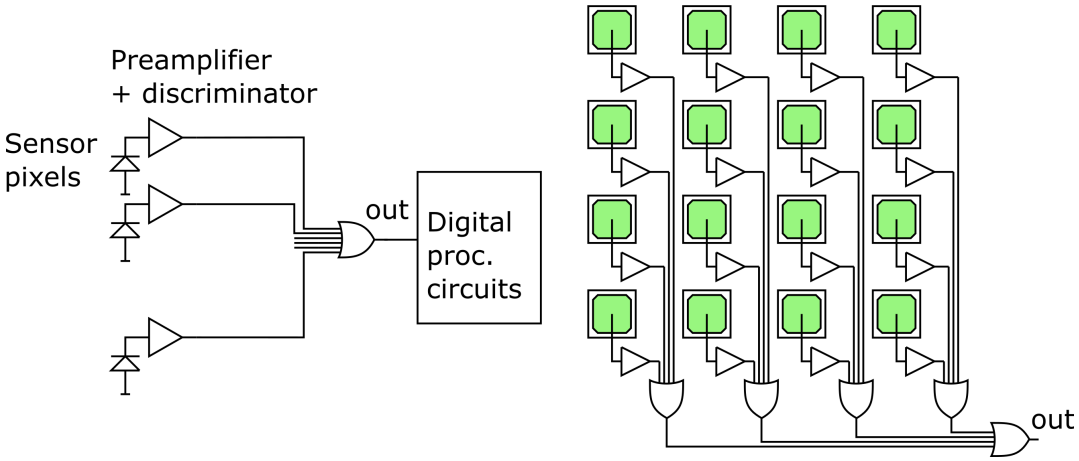




- **Power O(10 mW) for 100 fF input capacitance**
- **Power density: 25 W/cm^2**
- **Sensor performance are very important!**

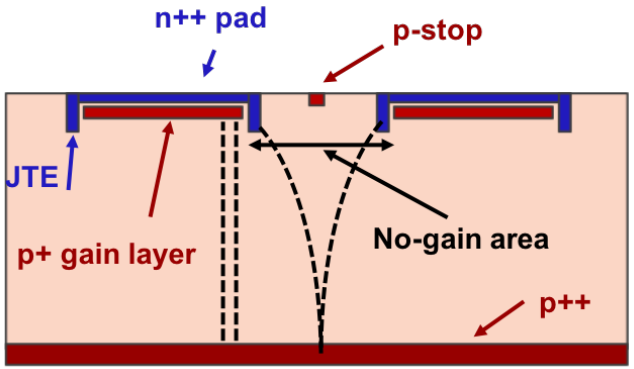
First thoughts

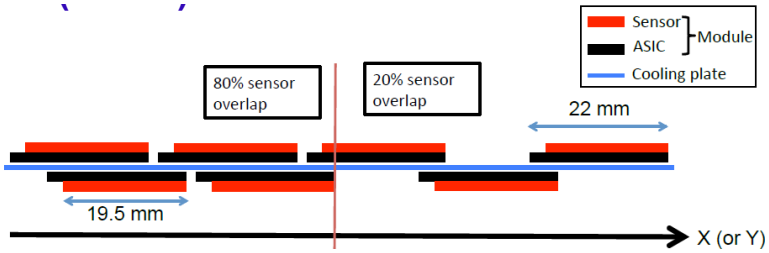
- Design of critical IPs with TOF-grade performance is matter of good (excellent!) engineering.
- Read-out architecture (almost) invariant
- Moderate data rate allows sharing of resources
- Key challenges at the sensor and sensor to front-end interface
- To make realistic assessments and appropriate choices, careful sensor simulations are needed



Sensor options: LGAD

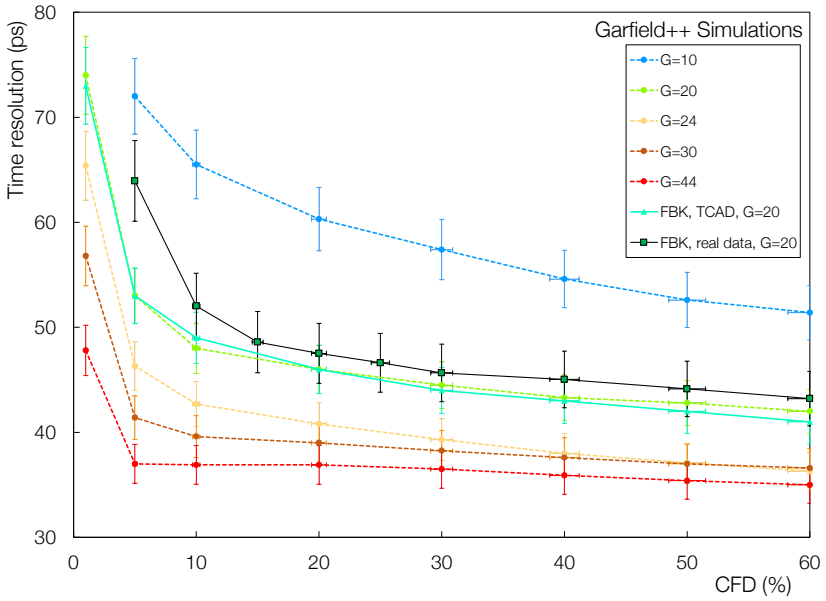
- The choice of CMS and ATLAS for the timing layers
- State of the art LGAD do not allow for very small pixels, but this is not an issue for the TOF
  Several approaches being investigated to improve the fill factor
- Radiation hardness is up to 10^{15}, so much higher than what needed in the TOF
- CMS and ATLAS approach: 1.3 mm x 1. 3 mm pads.
- Sensor is 2 cm x 4 cm connected to a 2 cm x 2 cm front-end chip via bump bonding
- Front-end is 65 nm for CMS and 130 nm for ATLAS

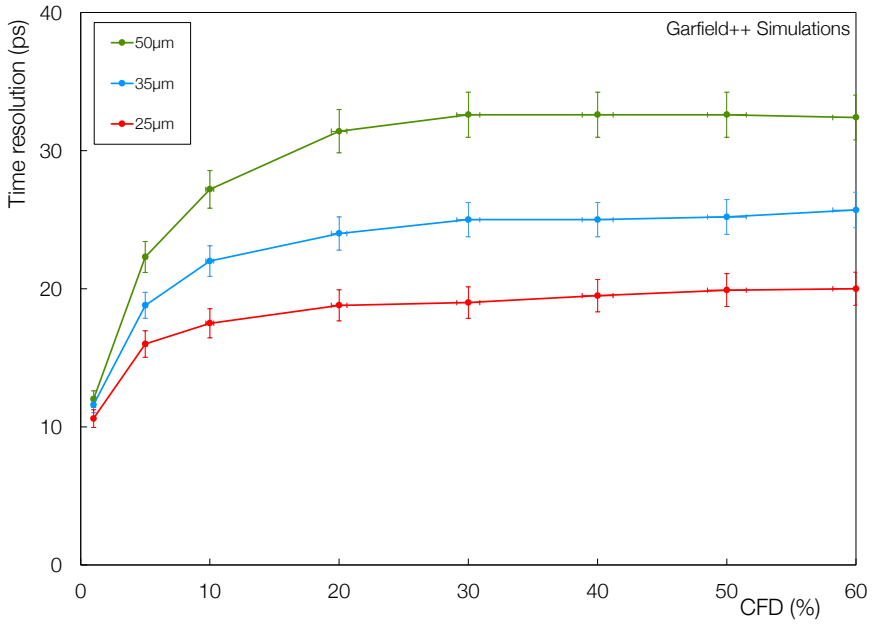




- 50 µm active thickness
- Gain > 20: resolution dominated by sensor
- 35 ps rms

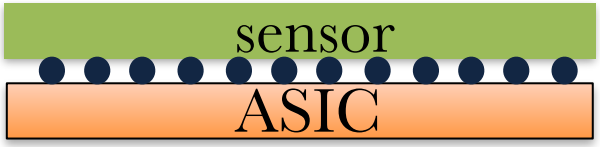
LGAD simulated performance



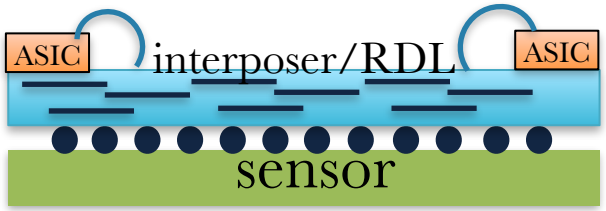


- **LGAD with gain of 20 and 25 µm thickness can achieve TOF-grade performance**

LGAD module concepts for TOF

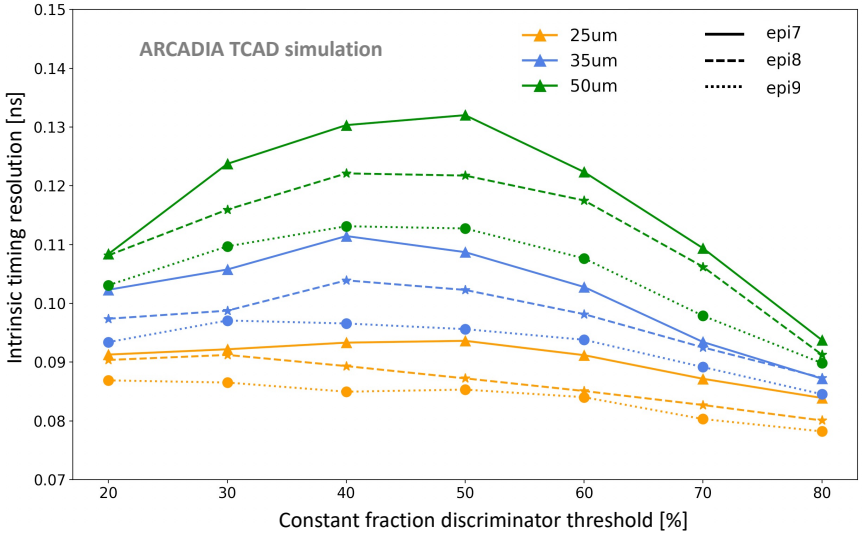


- ASIC and sensor area comparable
- Direct bump bonding
- Shorter connections
- ASIC prototyping requires going to engineering run in an early stage
- Watch high-frequency feed-through

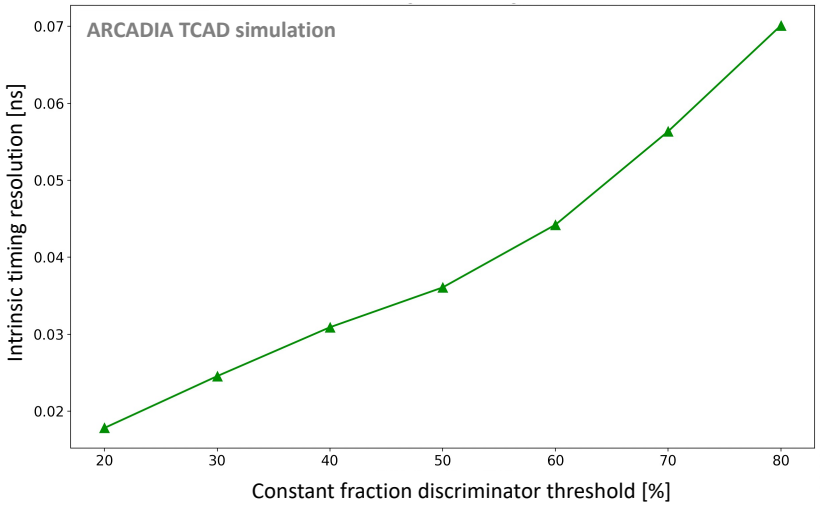


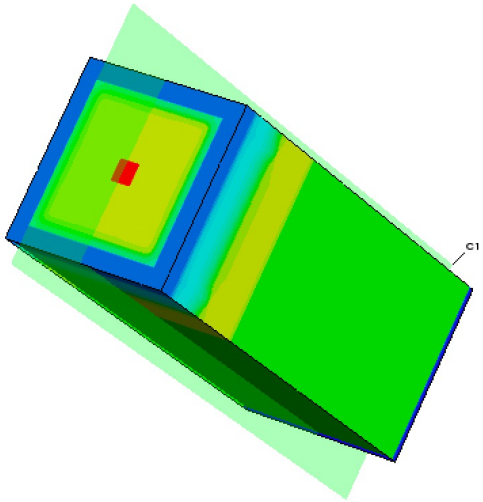
- ASIC can be much smaller
- ASIC prototyping in MPW
- Very advanced node possible
- Longer connection…
- …but best results still obtained with wire bonding!
- Less high-frequency feed-through

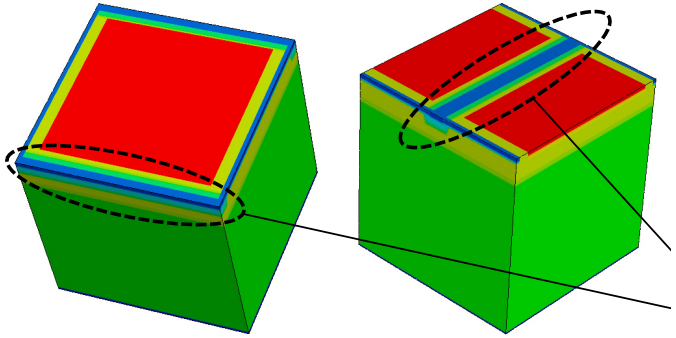
What about CMOS sensors?



Large collection electrode



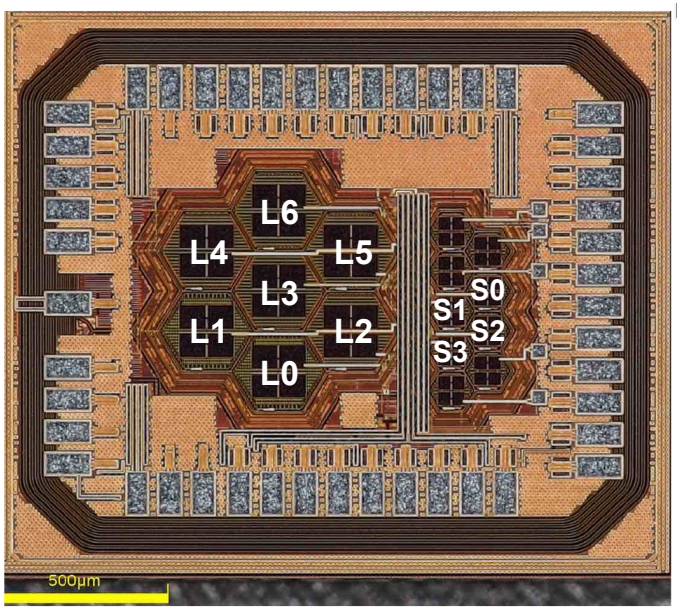


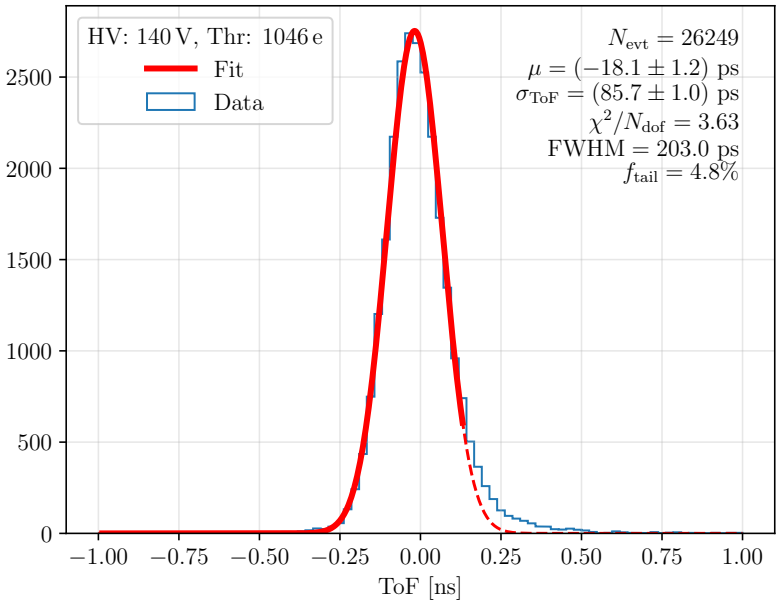


BiCMOS sensors in SiGe technology

Time resolution and power consumption of a monolithic silicon pixel prototype in SiGe BiCMOS technology

L. Paolozzi,[a,1] R. Cardarelli,[b] S. Débieux,[a] Y. Favre,[a] D. Ferrère,[a] S. Gonzalez-Sevilla,[a] G. Iacobucci,[a] M. Kaynak,[c] F. Martinelli,[d,e] M. Nessi,[d] H. Rücker,[c] I. Sanna,[f,2] D.M.S. Sultan,[a] P. Valerio[a] and E. Zaffaroni[a,3]





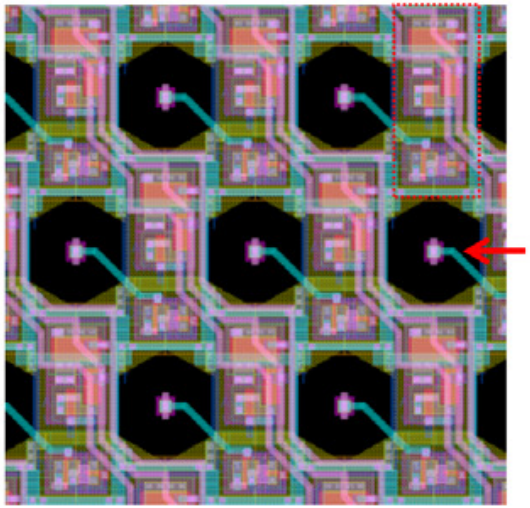
ATTRACT FastPix

Monolithic CMOS sensors for sub-nanosecond timing

Thanushan Kugathasan [a,*], Taeko Ando [b], Dominik Dannheim [a], Takeharu Goji Etoh [b], Magdalena Munker [a], Heinz Pernegger [a], Angelo Rivetti [c], Kazuhiro Shimonomura [b], Walter Snoeys [a]

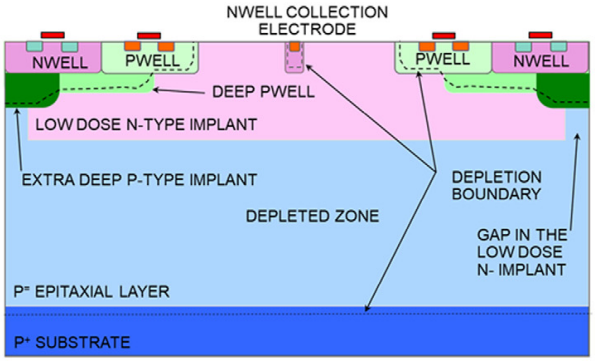
[a] *CERN, Geneva, Switzerland*
[b] *Ritsumeikan University, Kyoto, Japan*
[c] *INFN, Torino, Italy*

Pixel in the matrix



5 PMOS per pixel

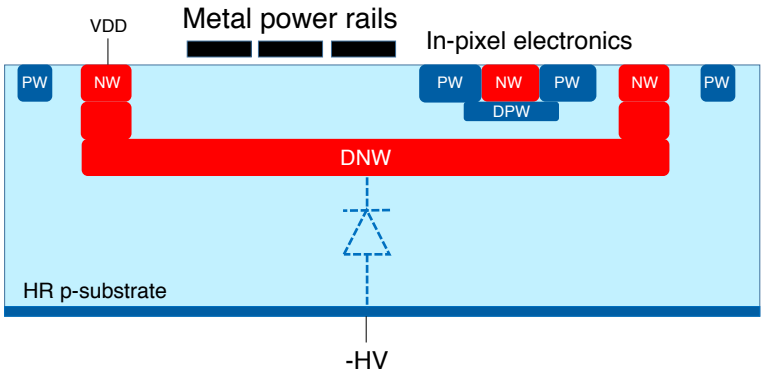
n-well electrode

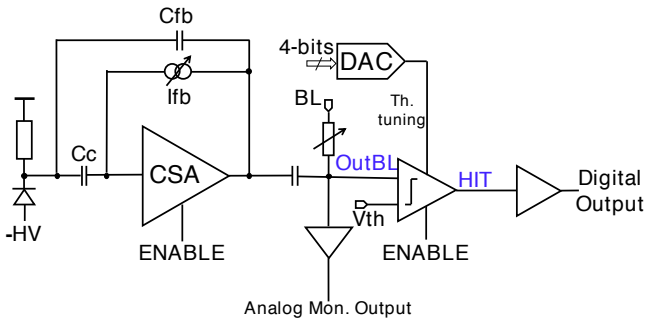


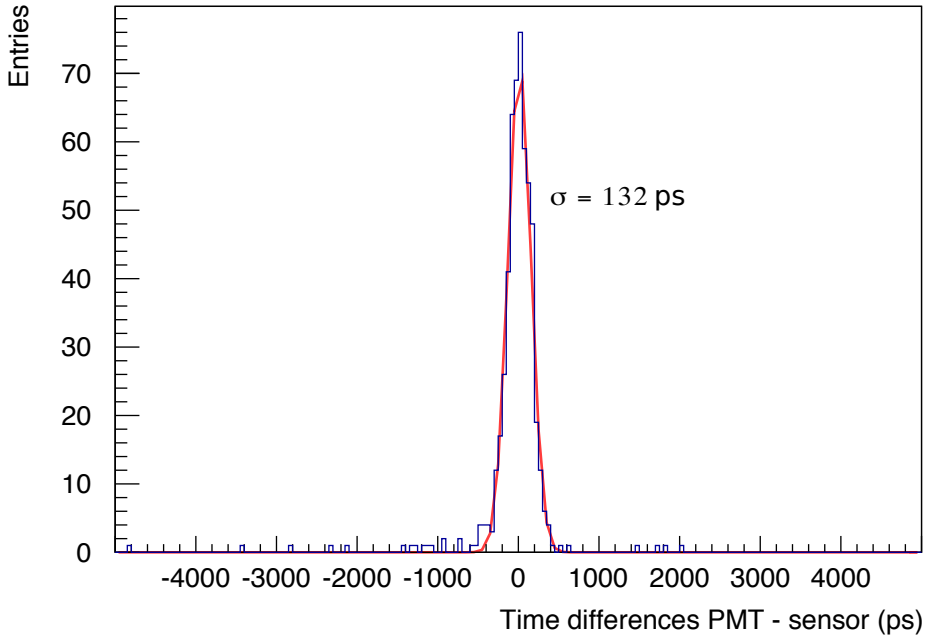
Fully depleted CMOS

CACTUS: A depleted monolithic active timing sensor using a CMOS radiation hard technology

Y. Degerli[a,1] , F. Guilloux[a] , C. Guyot[a] , JP. Meyer[a] , A. Ouraou[a] , P. Schwemling[a] , A. Apresyan[b] , R. Heller[b] , M. Mohd[b] , C. Pena[b] , S. Xie[c] , T. Hemperek[d]

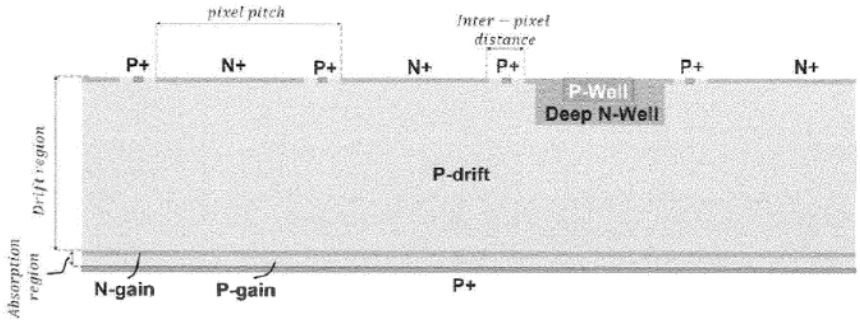




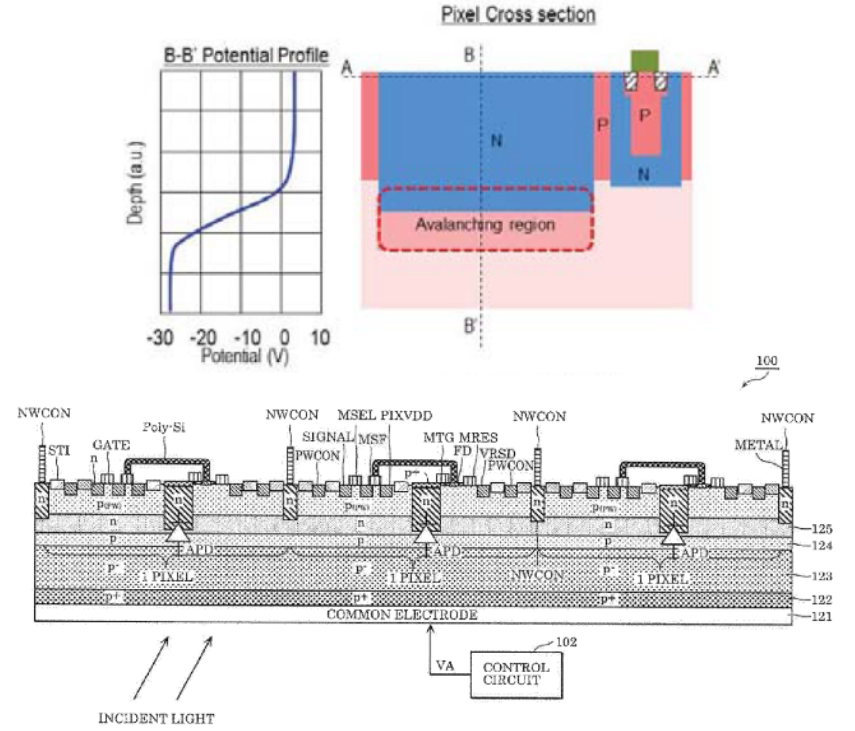


Adding gain to CMOS sensors

- G. Iacobucci et al. UniGe
- Patent EP 3 654 376 A1
- Gain in layer in the back
- No HV in the front-side
- Target 1 ps resolution



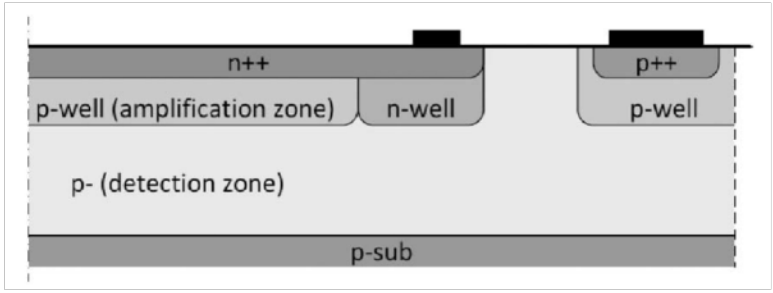
- Avalanche pixel with 6 um pitch
- No HV in the front-side
- Y. Hirose et al. IEEE ISSCC 2019
- PANASONIC patent EP 3 448 018 A1



Adding gain to CMOS sensors

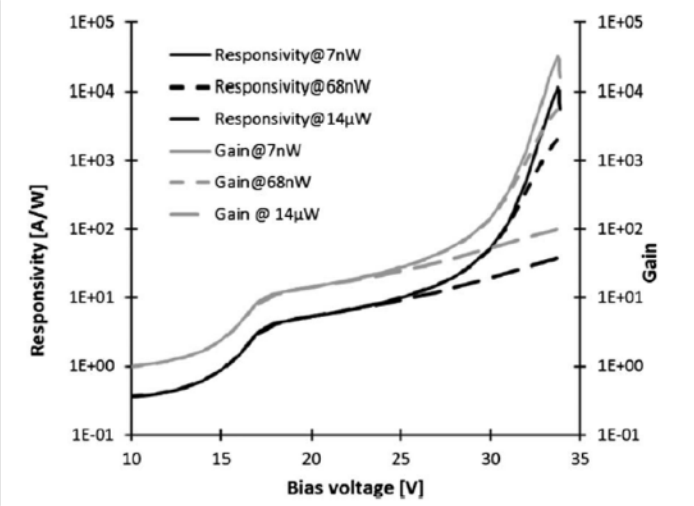
University of Wien: APD for optical detection applic.

Process: CMOS 0.35um
Active area: n++/pwell/p-
Active thickness: 12um
P- doping: 2e13 cm^{-3}



Advantages:
- Easily compatible with most fabrication processes (requires custom implantations)

Disadvantages:
- Sensors should be biased at high voltage: AC coupling
- Bias structures needed.

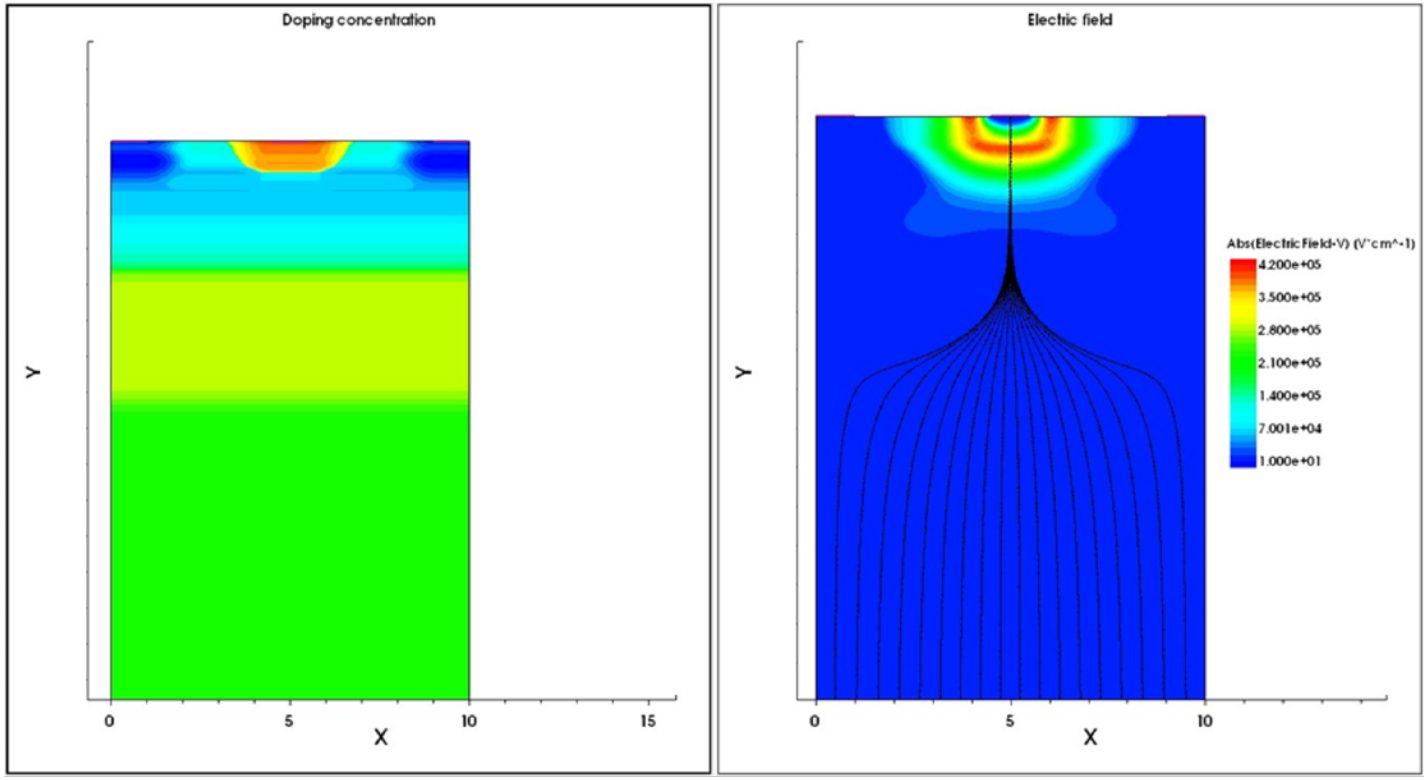


W. Gaberl et al., IEEE EDL 2014

2

Adding gain to CMOS sensors

- Preliminary simulations with the 110 nm process used by ARCADIA

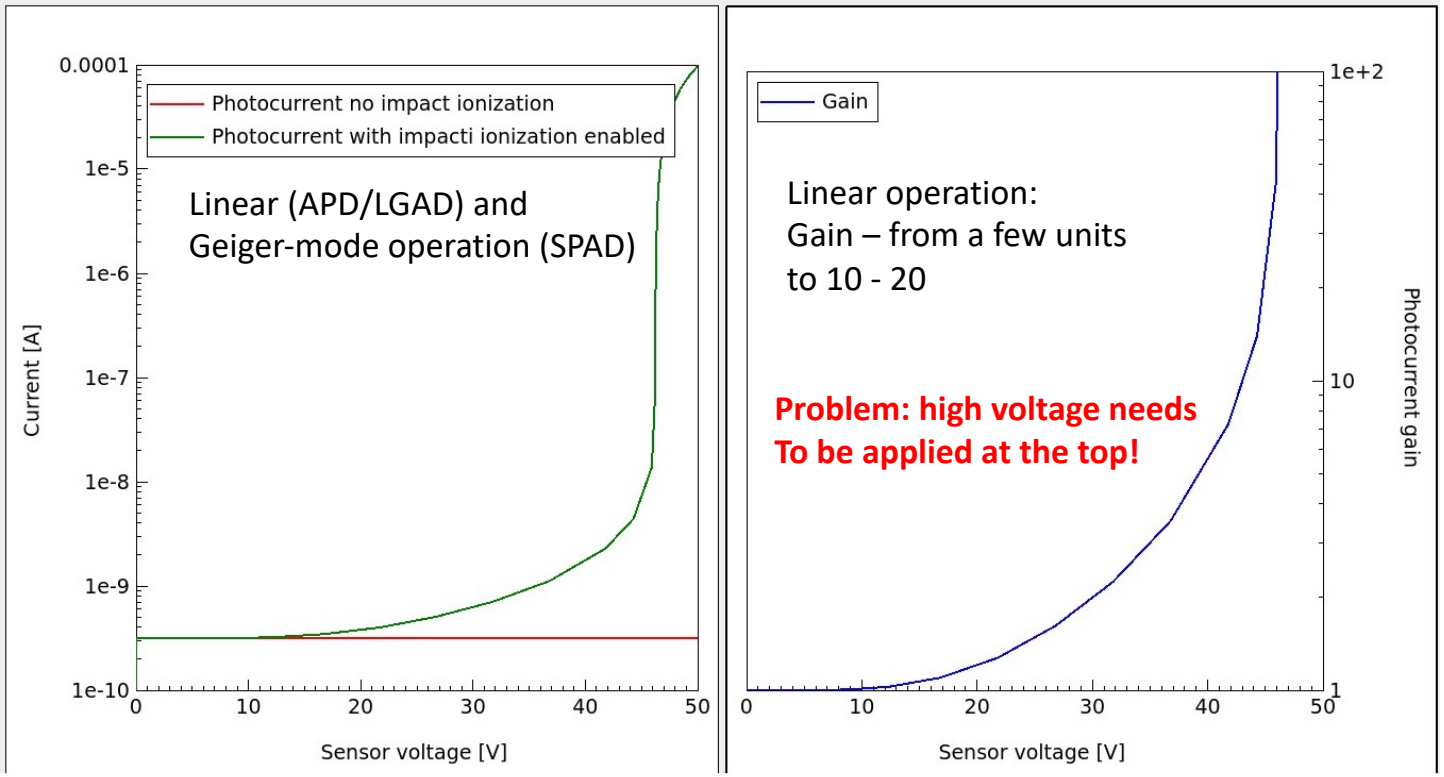


- High (negative) backside voltage for charge collection
- High positive sensor voltage for avalanche
- Monolithic electronics is possible only with AC coupling
- Concept can be used both for thick (100s micron) and thin (10s micron) sensors: gain and charge collection are decoupled

Adding gain to CMOS sensors

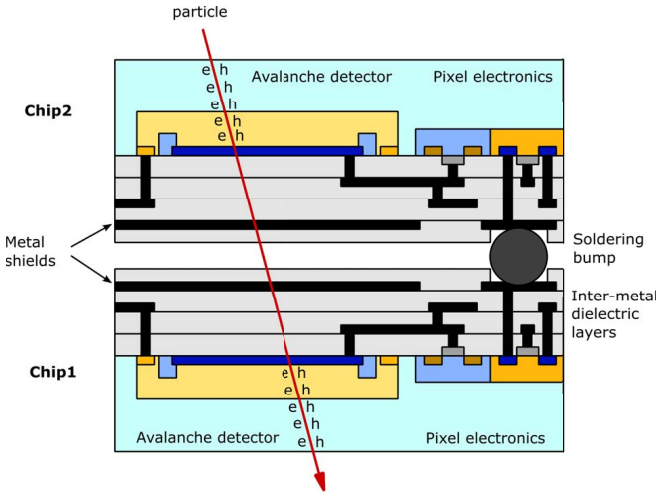
IV curves and quasi-stationary gain

Substrate thickness: 50um – Backside voltage: -15V



SPADs

- Three kind of SPAD-based sensors
  - Analog SiPM: most mature and widely available. Time resolution of 20 ps FWHM for 1 mm x 1 mm SiPM (about 40 pF capacitance)
  - 2D digital SiPM: fill factor, technology optimization - best CMOS SPAD 12.1 ps FWHM, 180 nm, DCR 20MHz/cm^2 at room T, 160 kHz at - 65 C.
  - Time resolution: 12.1 ps (25 um), 16 ps (50 um), 27 ps (100 um) FWHM.
  - 3D digital SiPM: 2 tier approach
  - …but it is not necessary to readout every single SPAD!
  - SPAD-based sensors used to detect charge particles only in limited number of R&D
  - For charge particles, efficiency expected to be larger than fill factor
  - Performance should be comparable



Conclusions

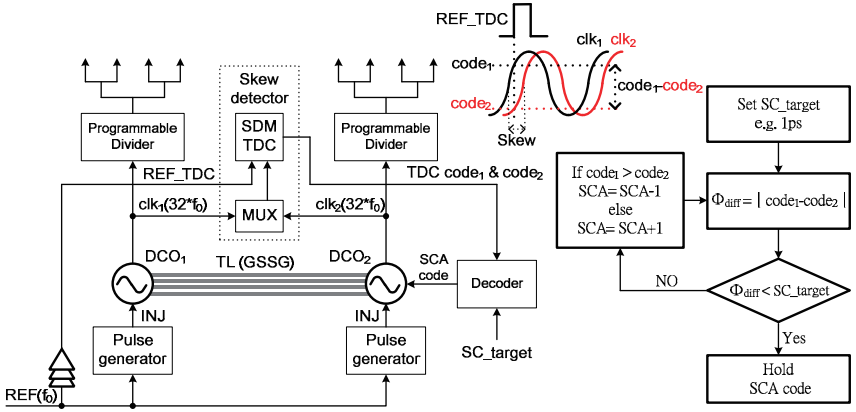
- CMOS sensors are an attractive solution for the TOF
- Timing potential of CMOS sensors not yet fully exploited
- 20 ps or better resolution can be envisaged and worth of further R&D
- Adding gain to CMOS can be the game changer
- SPAD interesting if TOF-RICH readout are combined
- LGAD provides a solid fall-back solution

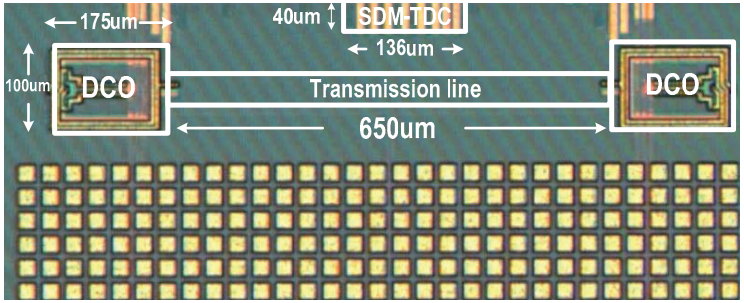
Back-up

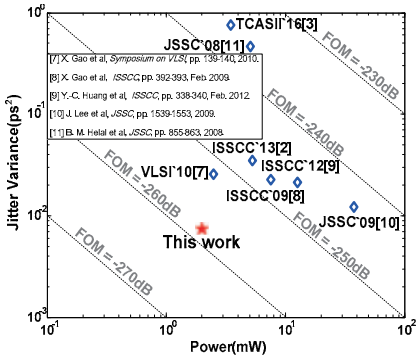
Key players: CDNs

A 4GHz Clock Distribution Architecture using Subharmonically Injection-Locked Coupled Oscillators with Clock Skew Calibration in 16nm CMOS

Lan-Chou Cho[1], Feng-Wei Kuo[1], Ron Chen[1], Jack Liu[1], Chewn-Pu Jou[1], Fu-Lung Hsueh[1],
R. Bogdan Staszewski[2] [1]TSMC, Hsinchu, Taiwan, [2]University College Dublin, Ireland. email: lcchov@tsmc.com

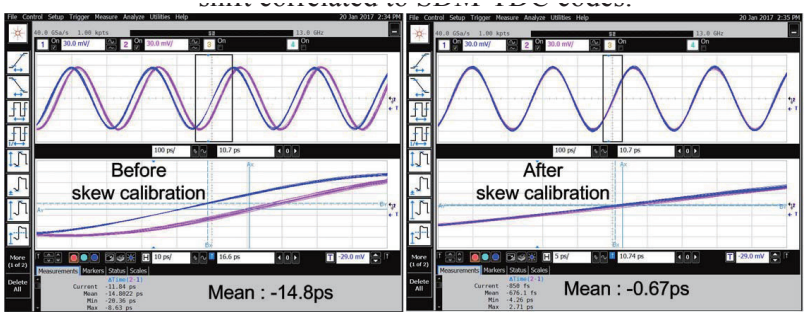






	This work	[1]	[2]
Technique	SHILCO	Resonant	SHIL PLL
CMOS node	16 nm	180 nm	65 nm
Frequency (GHz)	4	1.5~2.1	2.4
Power (mW)	4.3	500	5.2
Integrated rms Jitter	87 fs	0.9 ps	188 fs
Skew(ps)	<0.8	2	N/A
FOM*	-258	N/A	-247

$*FOM = 20\log(\frac{\sigma_t}{1s}) + 10\log(\frac{P}{1mW})$, σ_t : rms jitter and P : power



Key players: CDNs

20-ps Resolution Clock Distribution Network for a Fast-Timing Single-Photon Detector

N. Egidos, R. Ballabriga, F. Bandi, M. Campbell, D. Gascón, S. Gómez, J. M. Fernández-Tenllado, X. Llopart, R. Manera, J. Mauricio, D. Sánchez, A. Sanmukh, and E. Santin

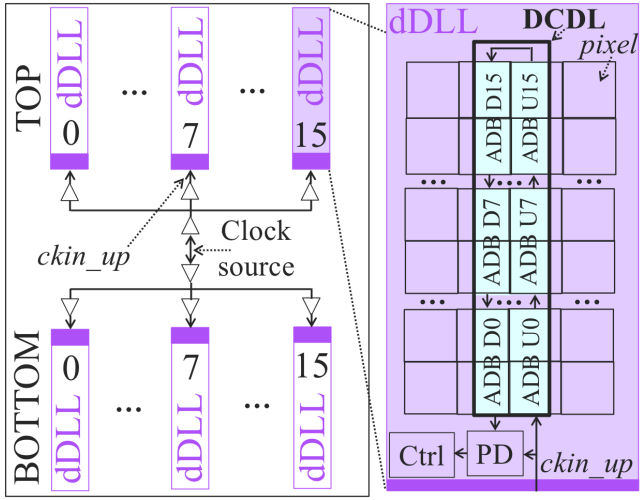


TABLE II

GUIDELINES TO SCALE THE CDN WITH THE CHIP AREA

Chip area (cm^2)	Number of pixels (pixel pitch = 376 µm)	Number of DCDL stages	Master clock frequency (MHz)	Number of dDLLs in the CDN
0.3x0.3	8x8	8 [a]	80 [c]	2
0.6x0.6	16x16	16 [a]	75	4
0.9x0.9	24x24	24 [a]	50	6
1.2x1.2	32x32	32 [a]	40	8
1.5x1.5	40x40	20 [b]	60	20
1.8x1.8	48x48	24 [b]	50	24
2.1x2.1	56x56	28 [b]	45	28
2.4x2.4	64x64	32 [b]	40	32

TABLE VI

TIME PERFORMANCE OF THE CDN

Corner	ADB LSB (ps)	Min. delay line (ns)	Max. delay line (ns)	Number of clock cycles required to lock for various values of the standard deviation of jitter, σ_j (ps)			
				1	2	3	4
Fast	4	11.14	26.24	6481	8389	10297	5512
Typ	5	16.21	41.04	11386	15113	17697	7105
Slow	7	24.64	67.57	14088	14182	14712	15144

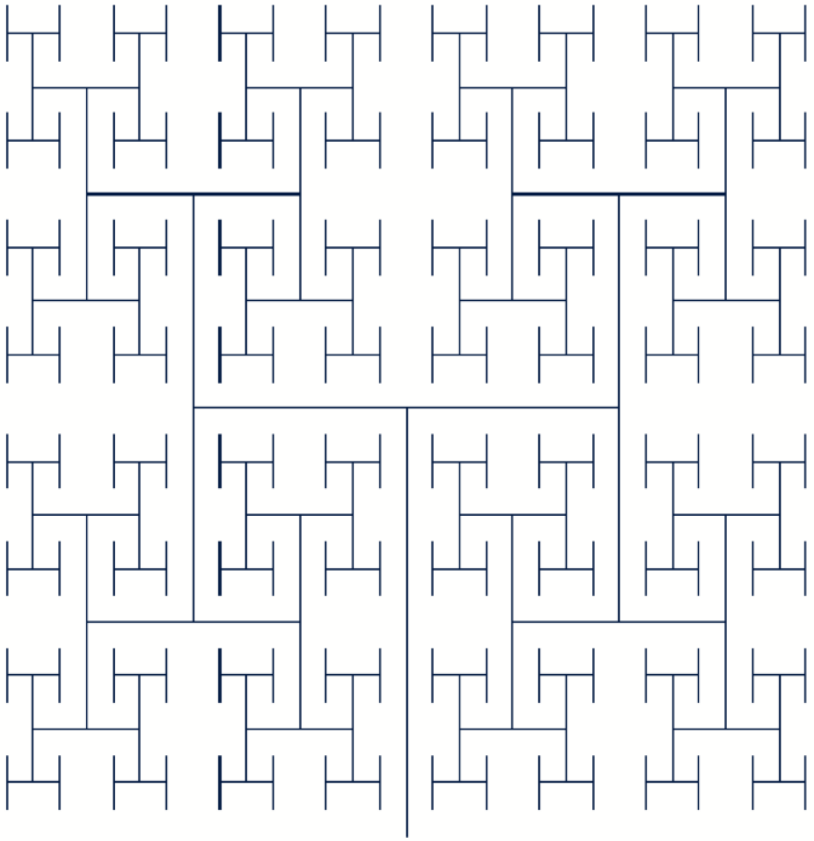
TABLE VIII

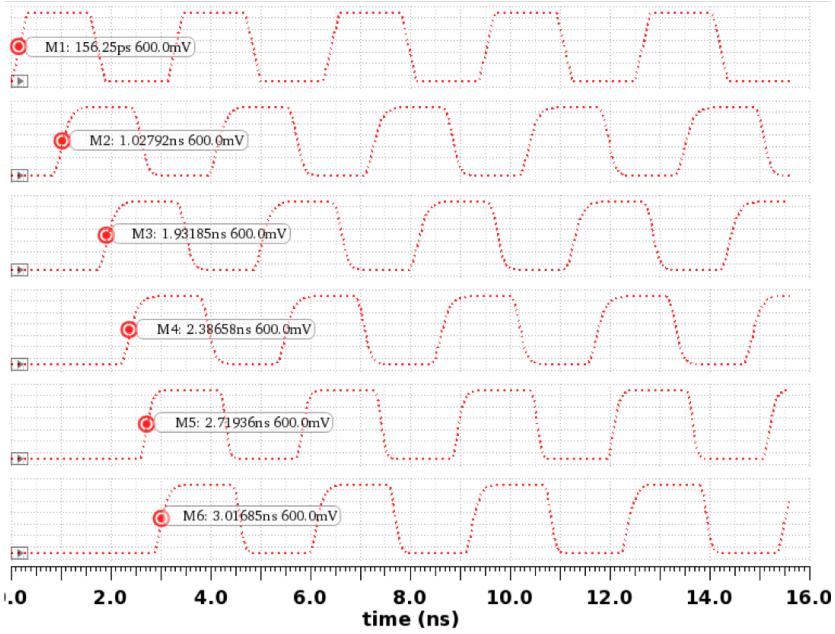
ESTIMATED POWER CONSUMPTION OF THE CDN AT THE CHIP LEVEL

Chip area (cm^2)	0.3 x 0.3	0.6 x 0.6	0.9 x 0.9	1.2 x 1.2	1.5 x 1.5	1.8 x 1.8	2.1 x 2.1	2.4 x 2.4
P_{CDN} (mW)	0.6	1.7	3.7	6.4	10.3	14.6	19.7	25.5

Key players: CDNs

- From CMS MIP Timing detector TDR





- 320 MHz clock
- Distributed to the full matrix
- 17 ps skew
- 21 mW power