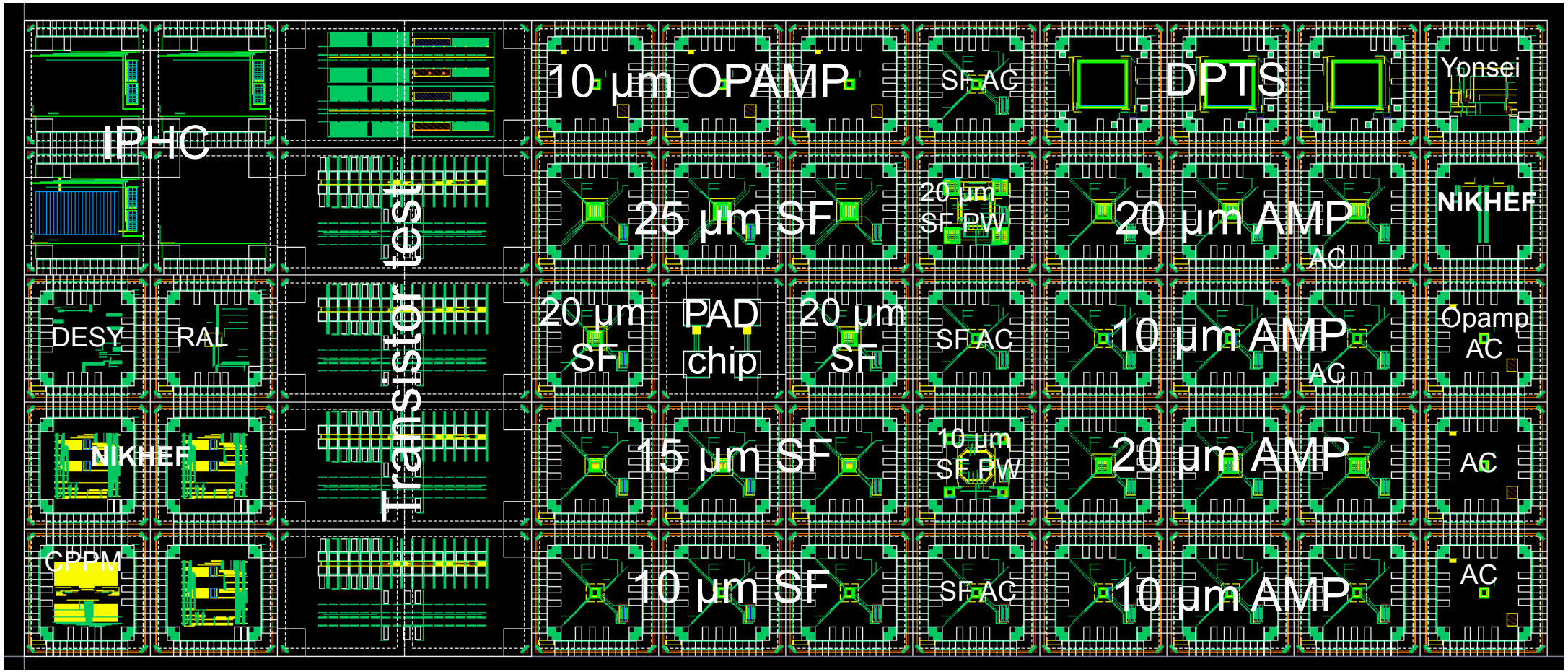
WP1.2 Status report

11/11/2021 G. Aglieri Rinella, M. Campbell and W. Snoeys for the whole team

TPSCo 65nm ISC CMOS imaging technology



EP R&D

GDS2	GDS1
GDS3	GDS1

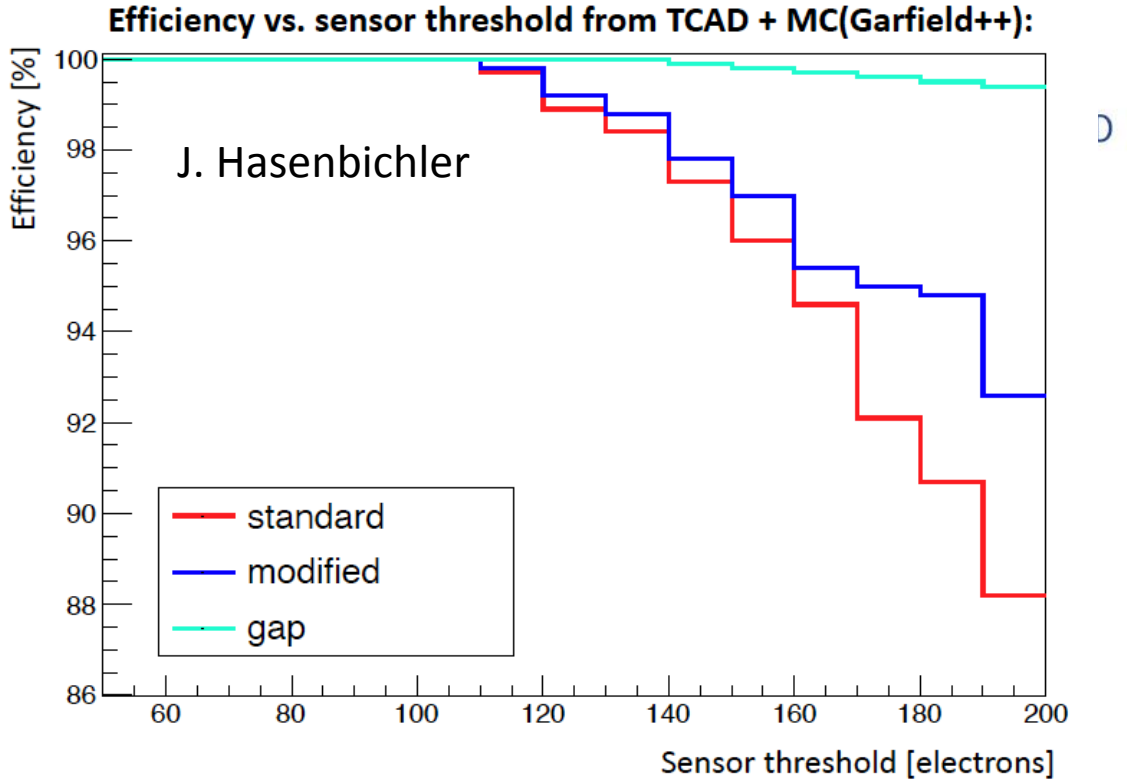
- IPHC: rolling shutter larger matrices, DESY: pixel test structure (using charge amplifier with Krummenacher feedback, RAL: LVDS/CML receiver/driver, NIKHEF: bandgap, T-sensor, VCO, CPPM: ring-oscillators, Yonsei: amplifier structures
- Transistor test structures, analog pixel (4x4 matrix) test matrices in several versions (in collaboration with IPHC with special amplifier), digital pixel test matrix (DPTS) (32x32), pad structure for assembly testing.
- After final GDS placement, GDS1 is instantiated twice.
- Converged with 4 splits of 3 wafers

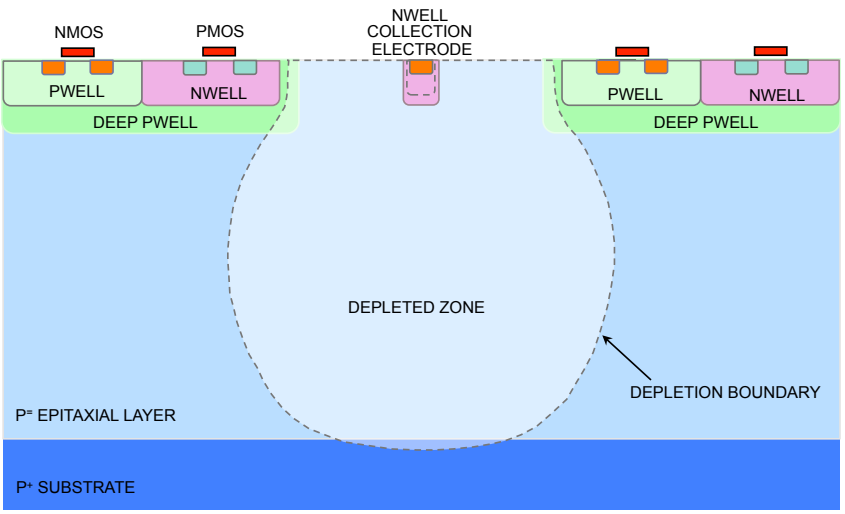
SPLITS

- 4 process splits, 3 wafers each
  - **Split 1: default process**
  - Split 2: first intermediate process
  - Split 3: second intermediate process
  - **Split 4: optimized process**

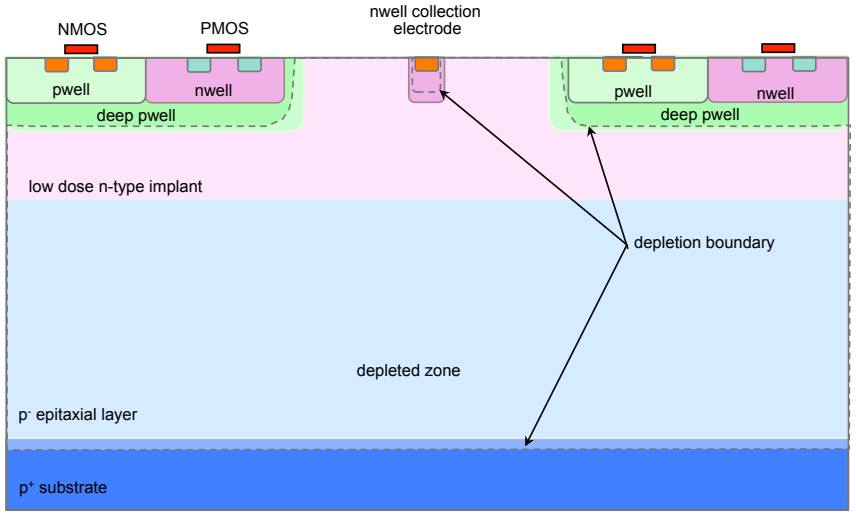
- 3 main pixel designs
  - Standard
  - Modified
  - Gap

If successful, similar situation as in 180nm, but modifications more needed in 65 nm for good charge collection.

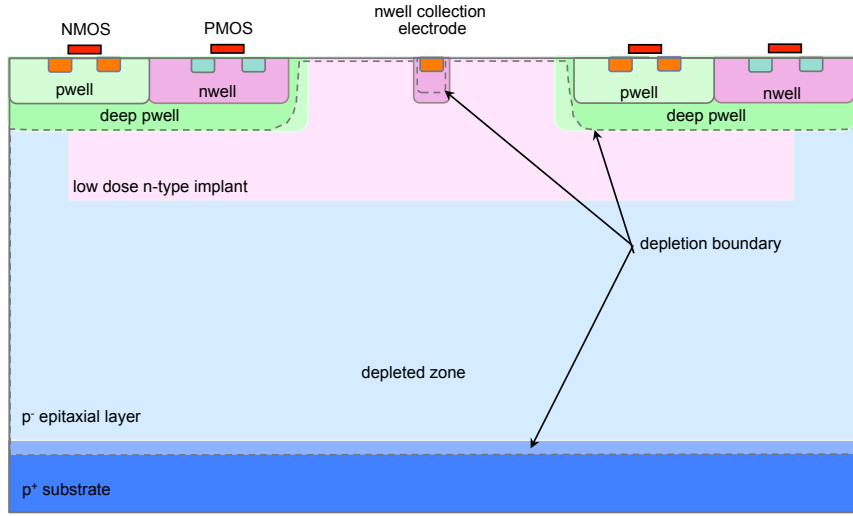




Standard



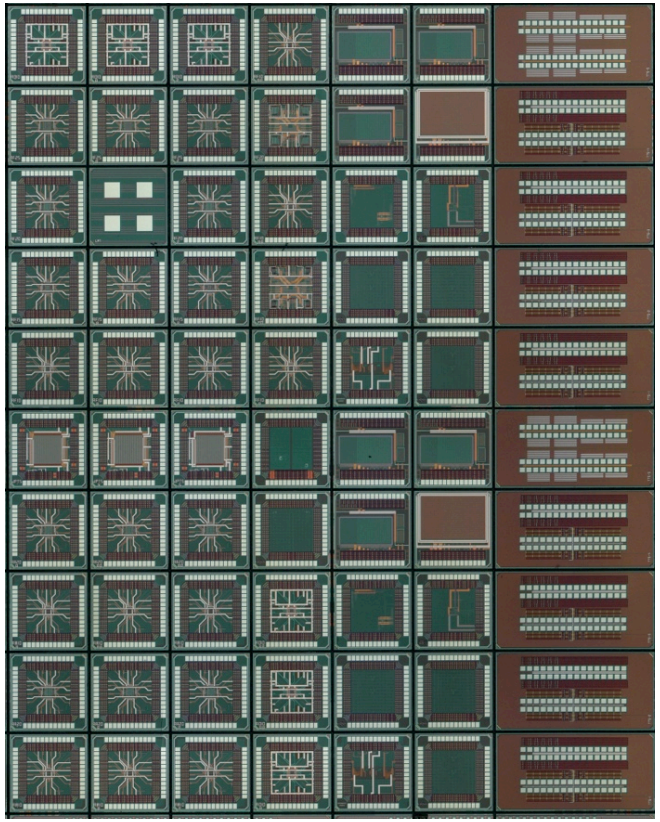
Modified

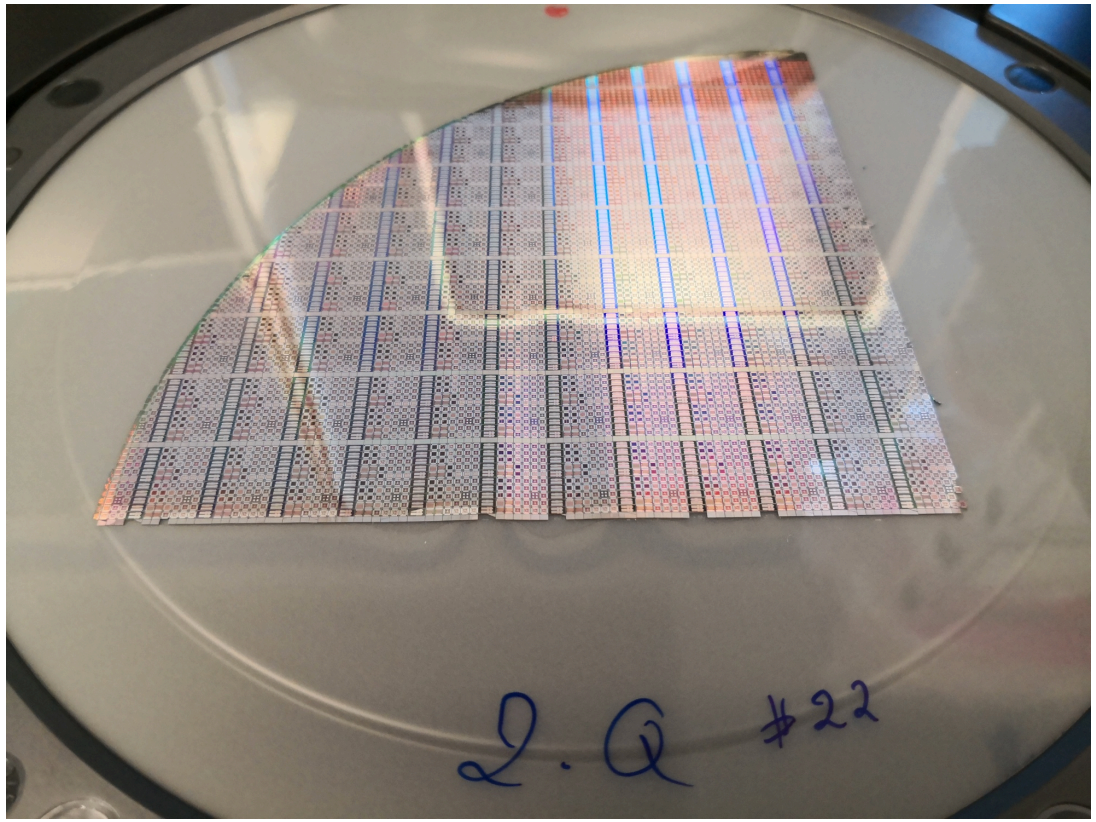


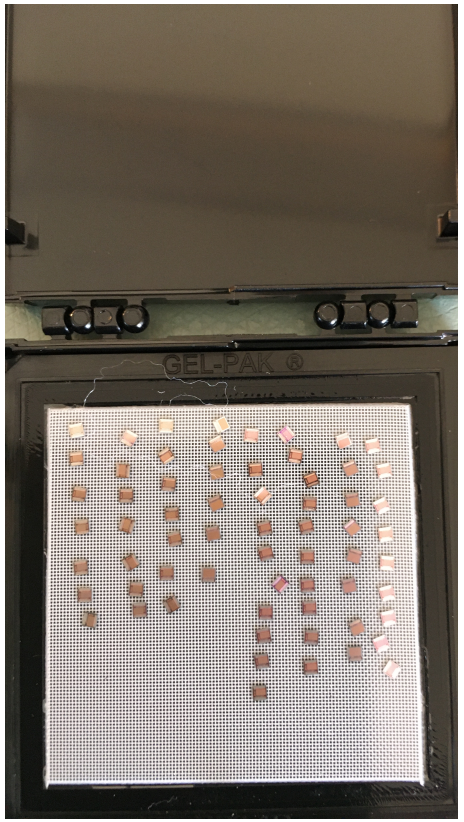
Gap

MLR1 Production:

- Received further diced chips (25/box, 2 boxes per chip), for both splits: dicing: significant follow-up effort (Magnus)
  - Distributed chips to groups -> done
  - Prepare dicing for other splits, just in case, to be done







MEASUREMENTS

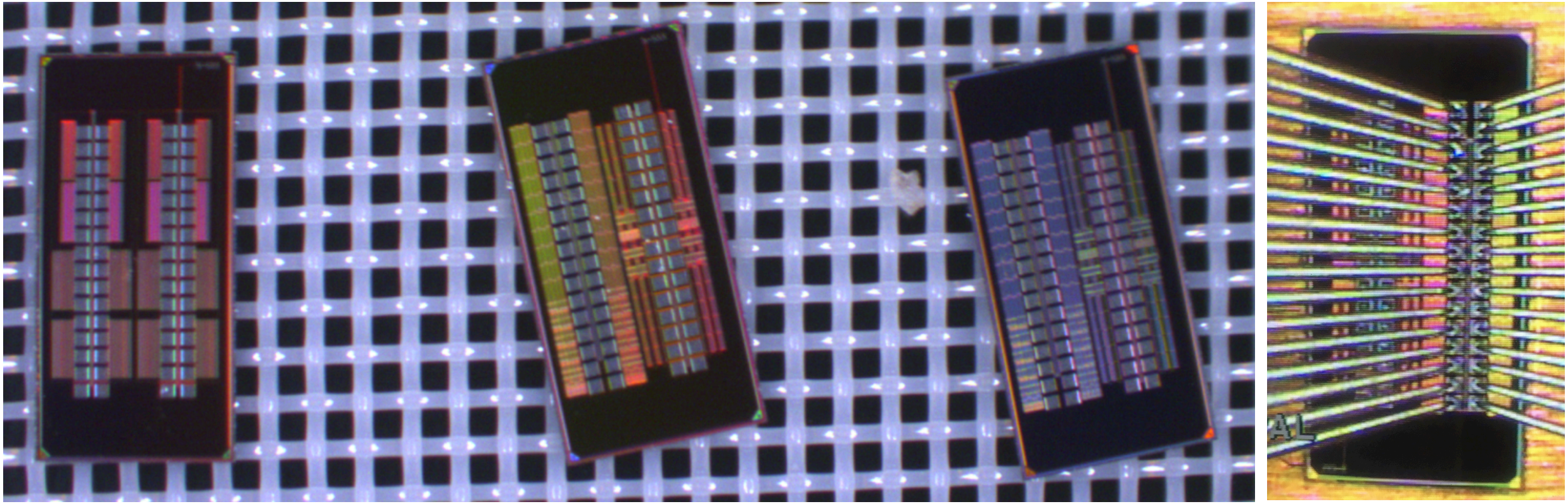
- Transistors -> no show stoppers, working on report

- Pixel prototypes
  - DPTS efficient operation, proves both front end and process, and basic digital functionality, investigation of operating margins, used as baseline (with some modifications) for the stitched matrices (see also Magnus Mager's Detector Seminar)
  - APTS functional but noise issue in measurement setup, first Landau distributions becoming available. APTS is vehicle for comparison against TCAD/Monte Carlo simulations
  - CE65 (IPHC), and also DESY test chip: first life in in test beam

- Biasing blocks: DAC, Bandgap, T-sensor, VCO (aim towards proven blocks for stitched sensors in ER1)
  - Functional
  - NIEL (neutrons) (Hartmut): first batch irradiated, next batch being prepared, no results yet
  - X-ray: encouraging results on IPHC DAC, and on bandgap, VCO in the pipeline
  - SEE (Protons Prague): from DPTS, cross-section as expected (NIEL up to 1E13 so far)

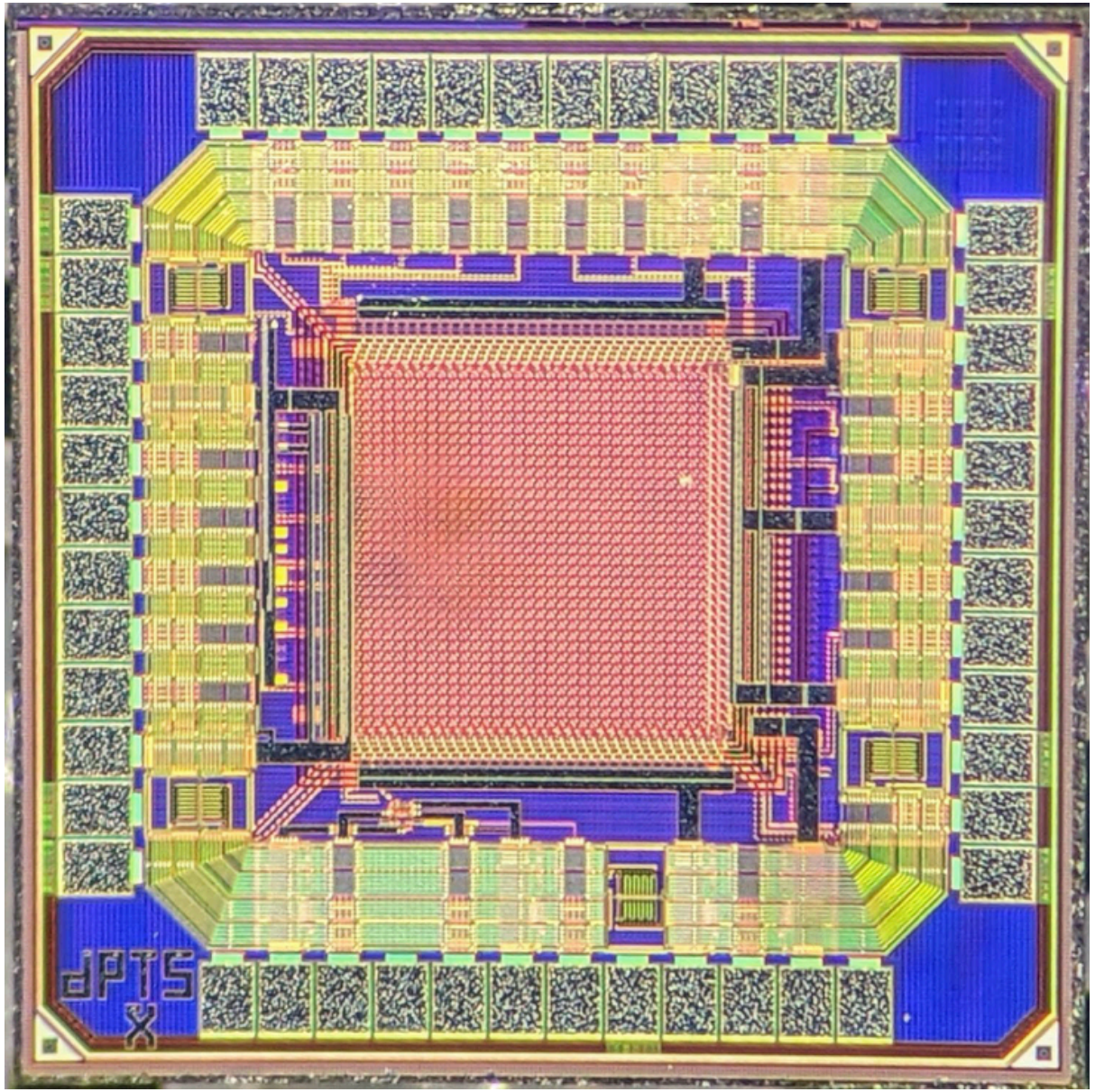
- Ring oscillators: good correspondence with measurements, no irradiations yet.

65 nm transistor prototypes



- Compatible with existing test system based on probe card.
- Tests have started
  - No apparent show stoppers, very encouraging results
  - Detailed analysis ongoing and in discussion with the foundry

Digital Pixel Test Structure (DPTS)

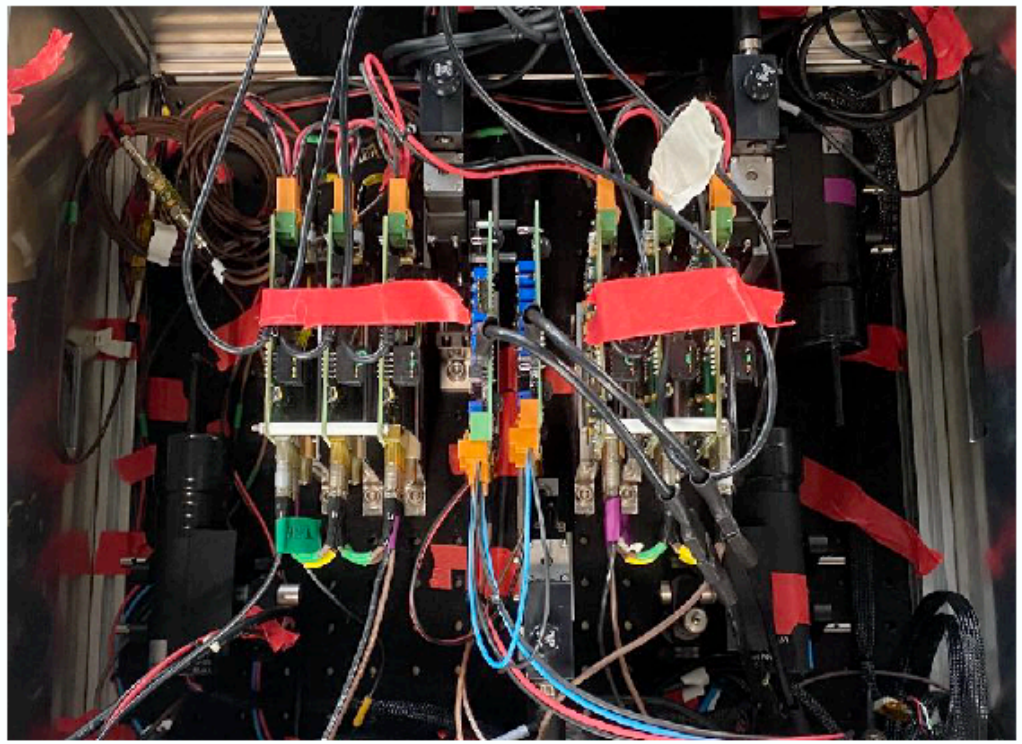


- Most “aggressive” chip in MLR1
- 1.5 mm x 1.5 mm test chip
- 32 x 32 pixels 15 µm pitch
- Asynchronous digital readout with Time-over-Threshold (TOT) information
- Allows verification of
  - Sensor *and* Front-end performance
  - Basic digital building blocks
  - SEU cross-sections of registers

Beam test campaigns

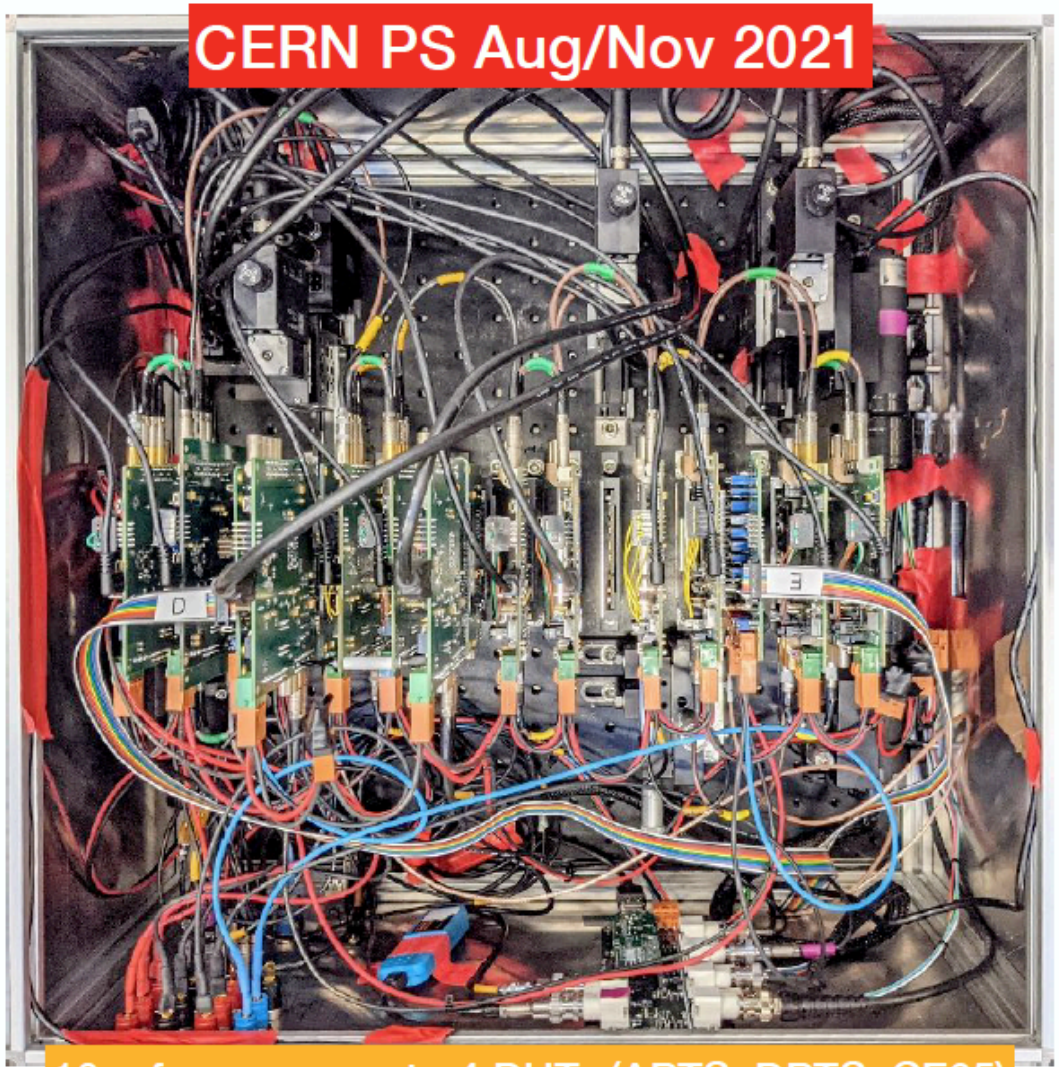
Using the flexible ITS3 ALPIDE telescopes

DESY Sep 2021



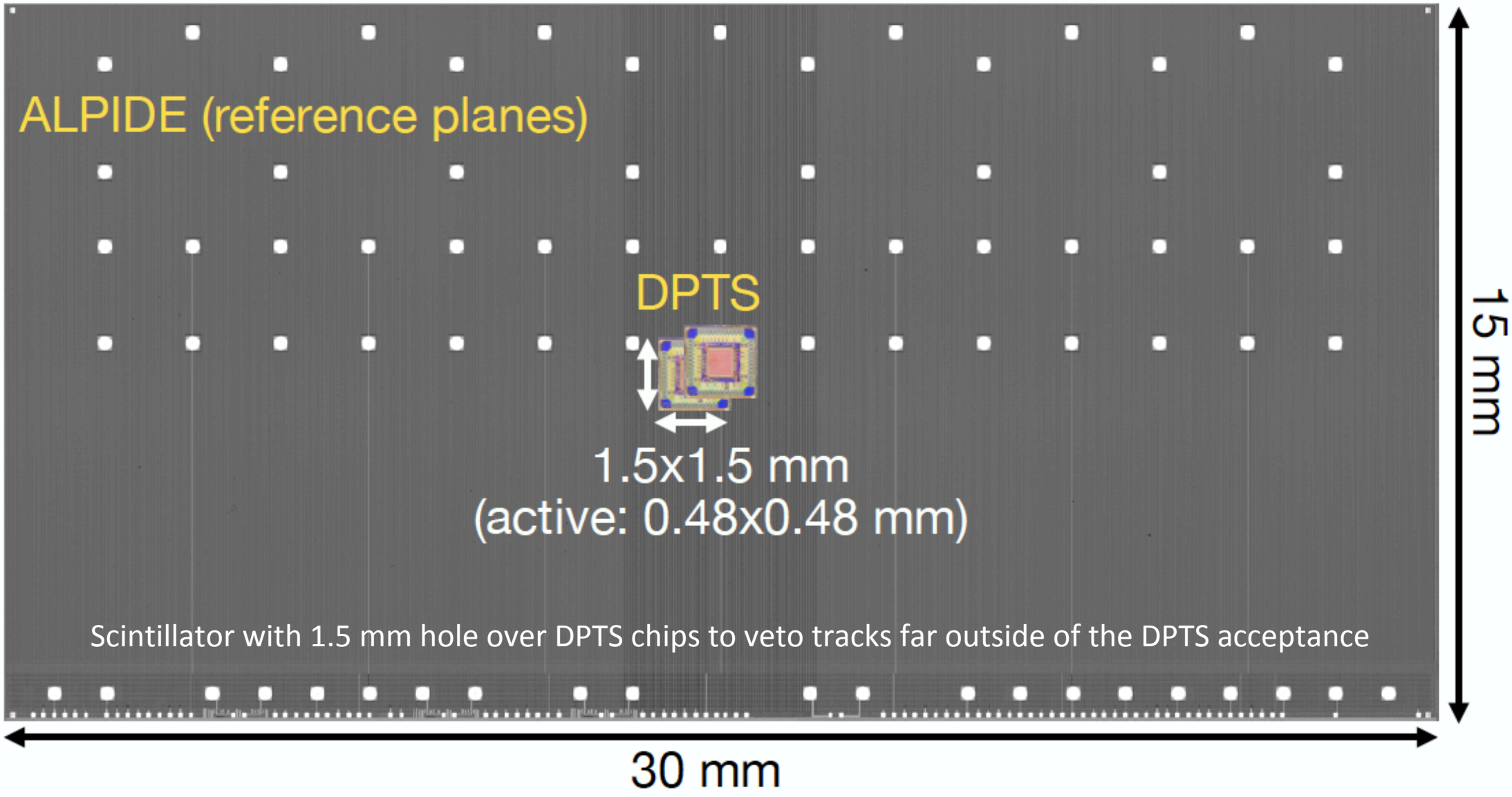
6 references, 2 DPTS DUTs

CERN PS Aug/Nov 2021



10 references, up to 4 DUTs (APTS, DPTS, CE65)

DPTS beam test results (by ALICE measurement team)



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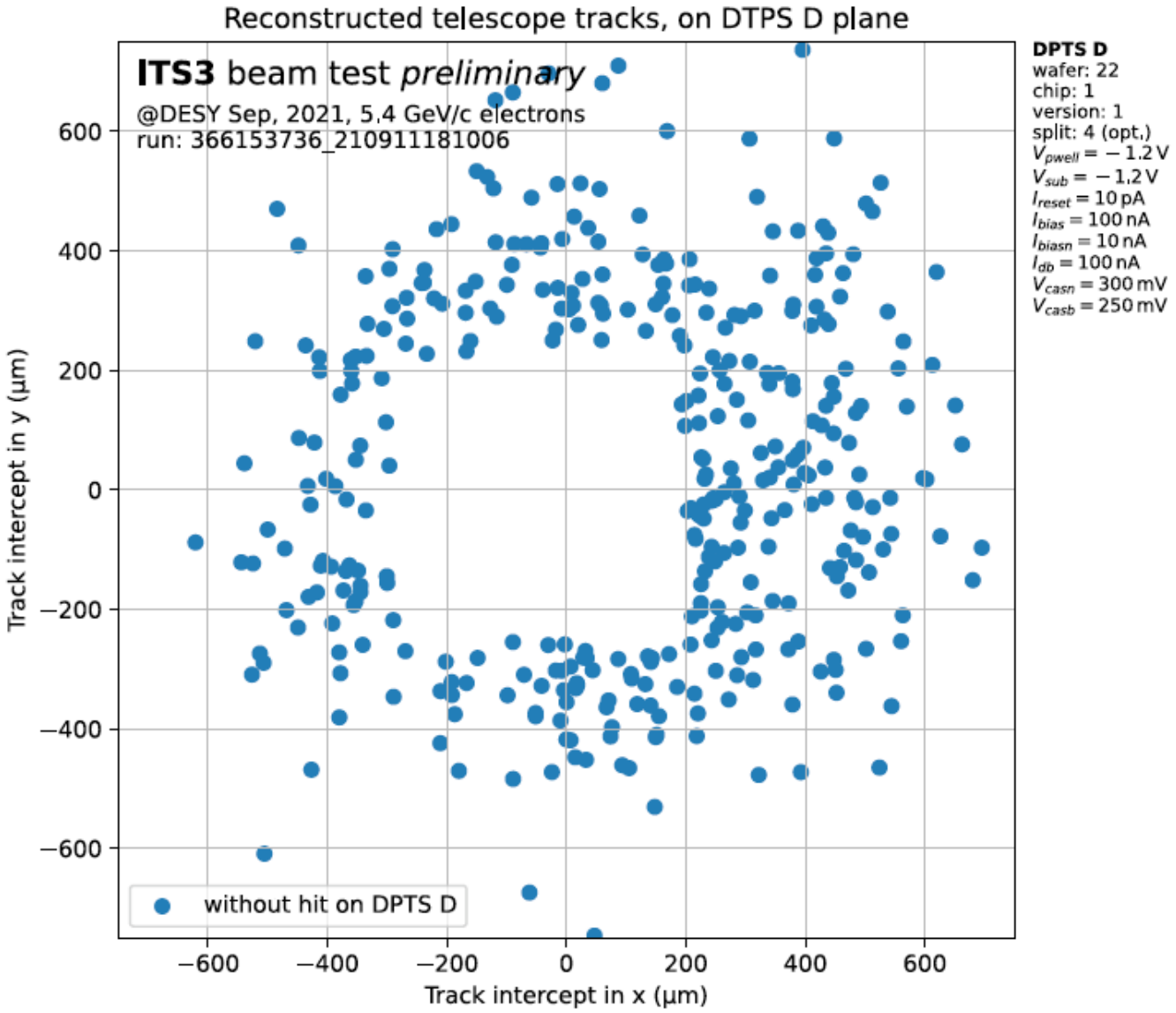
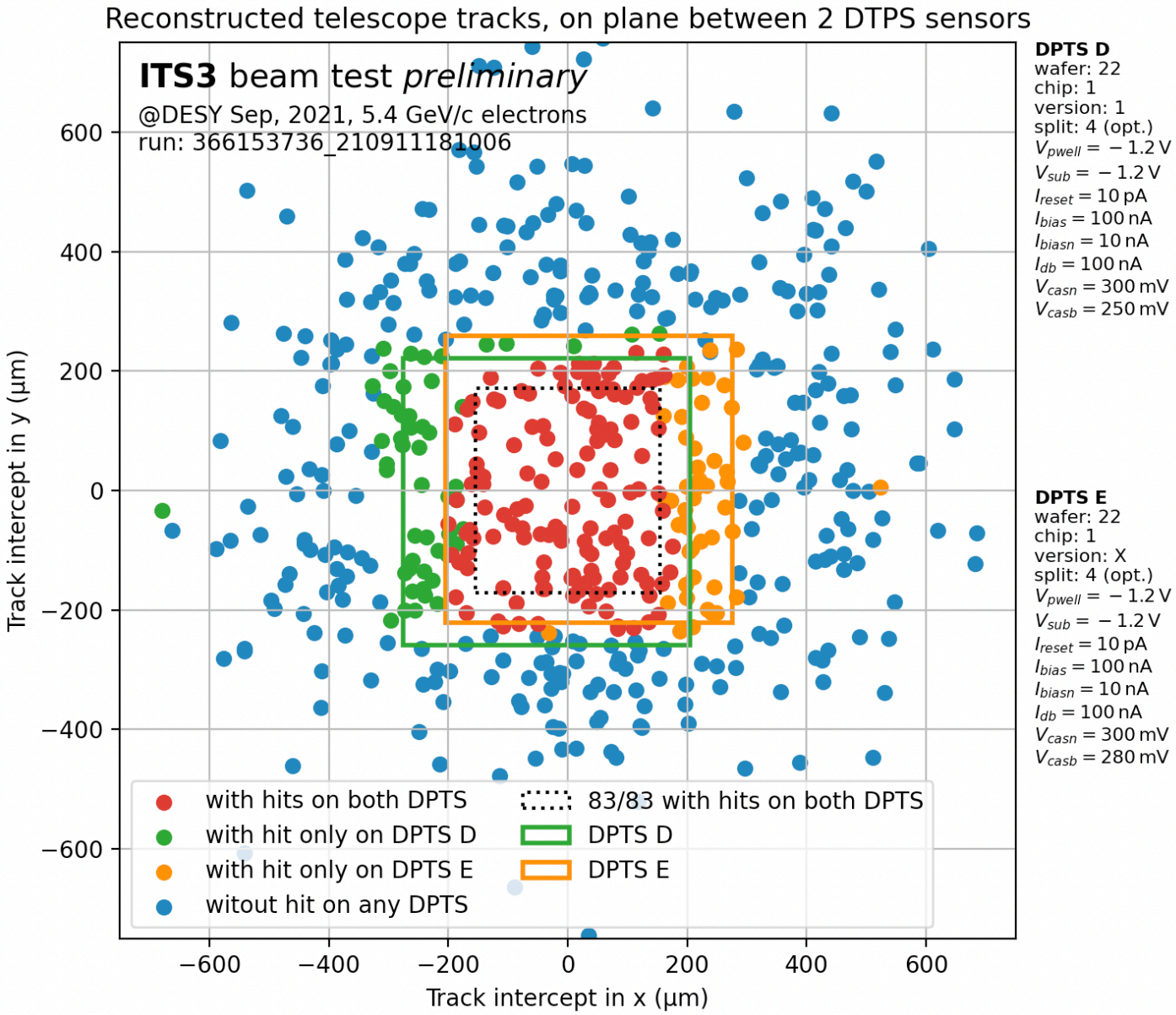


- Particle tracks not detected by the DPTS illustrate a clear 100 % shadow corresponding to the sensitive area of DPTS

DPTS beam test results (by ALICE measurement team)



- NO blue dots within sensitive area of the two chips, they see all tracks passing through
  - 166 for the first chip (green + red dots)
  - 162 for the second chip (orange + red dots)
  - 83 tracks in common (red dots)

  (only a few % of the data analyzed)

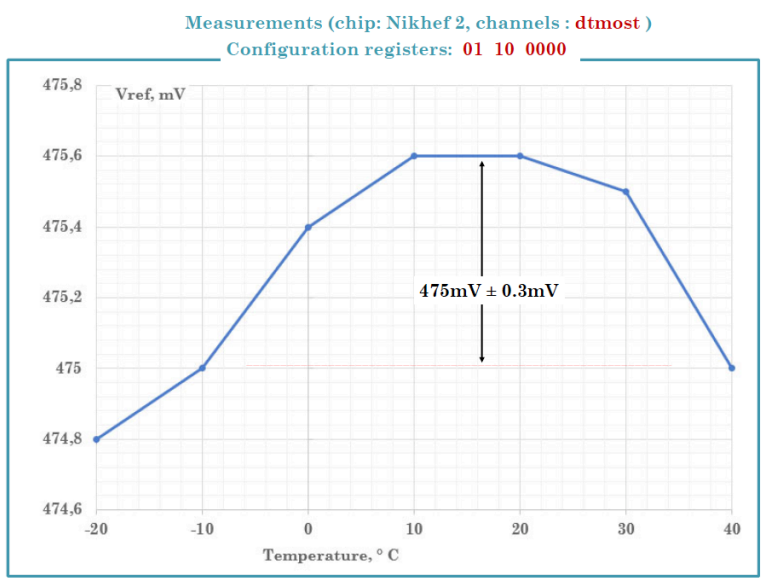
- Efficiency with (162+166)/(162+166) tracks:

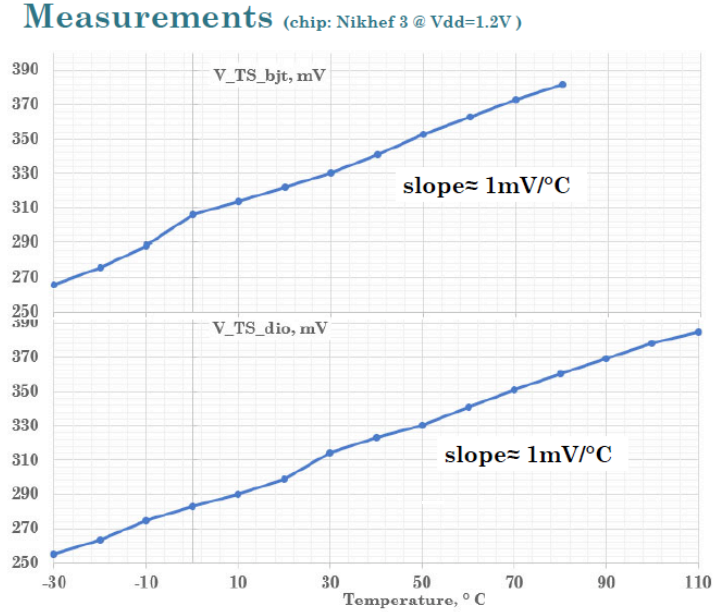
  $100\ \%\ ^{+0\%}_{-1\%}$

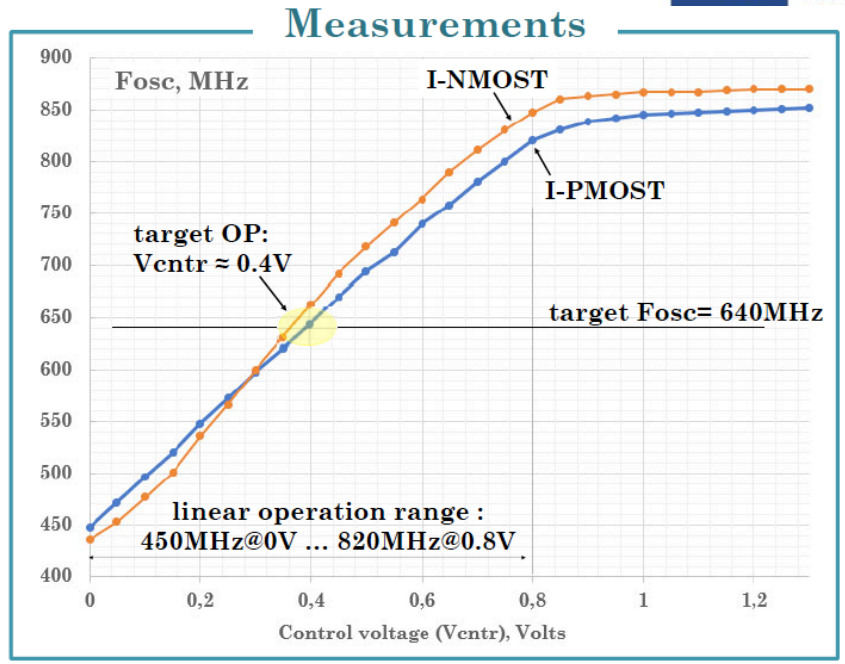
  (95% confidence, Clopper-Pearson)

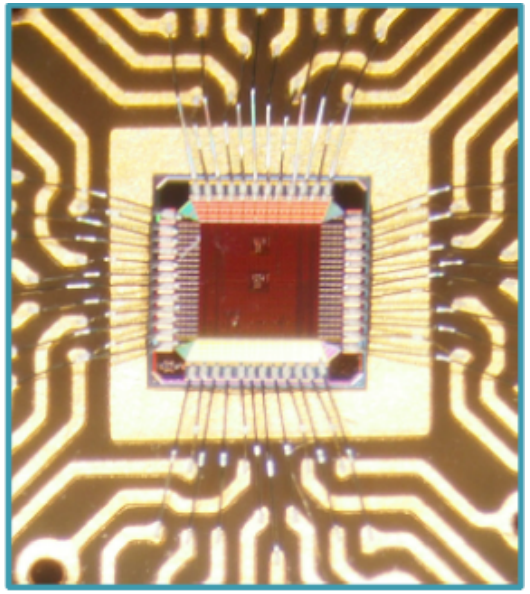
- Excellent sensor *and* front-end performance already from first 65 nm prototype

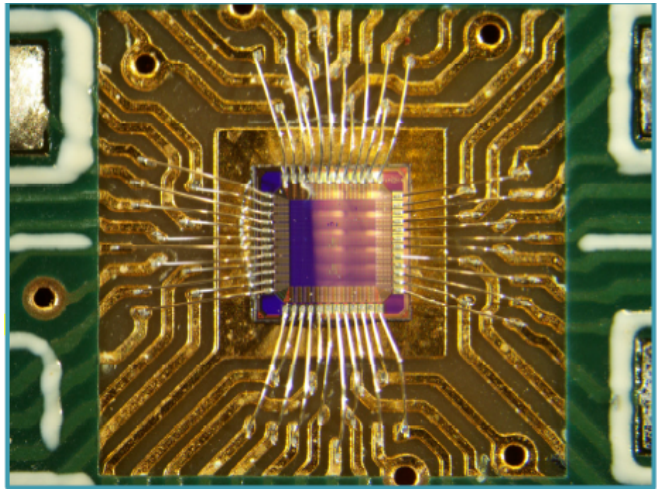
MEASUREMENTS NIKHEF

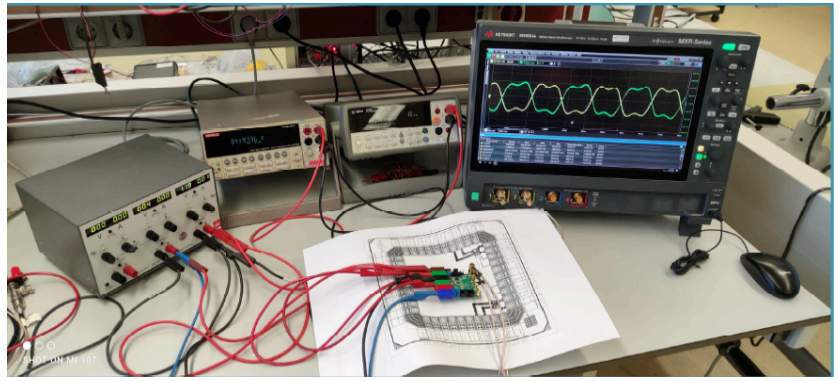






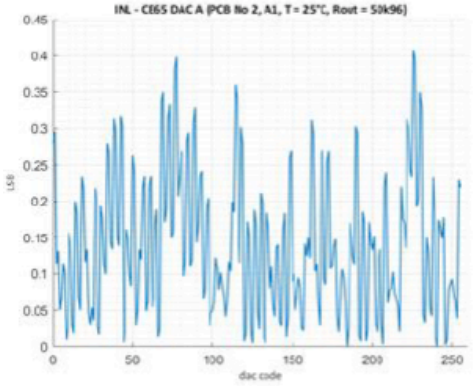


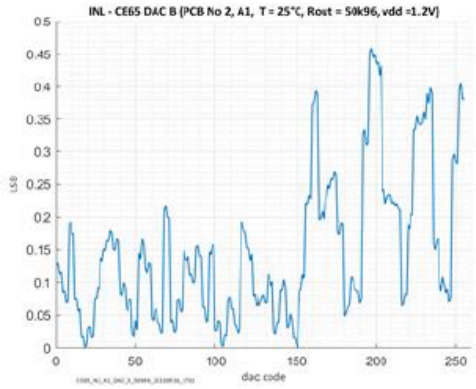


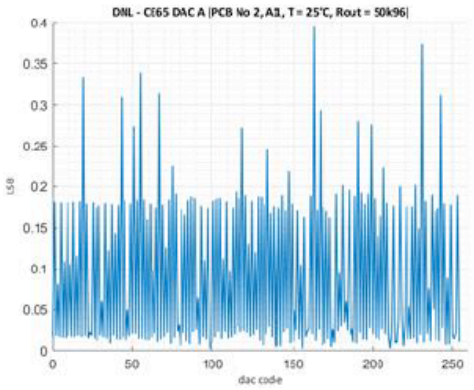


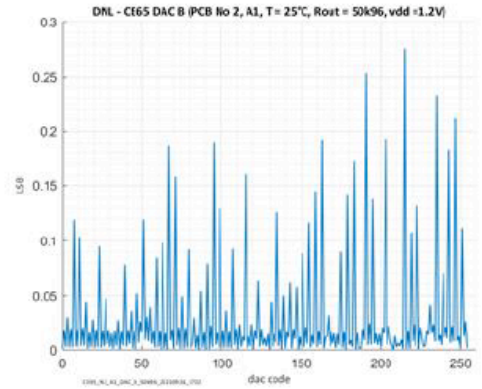
- 4 flavors of bandgap and Temp-sense, and VCO
- All functional, X-ray irradiations ongoing

MEASUREMENTS CE65 current DACs fully operational

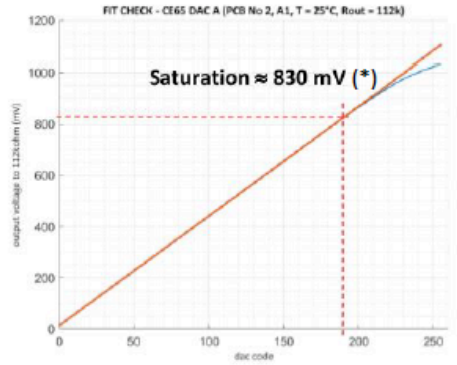




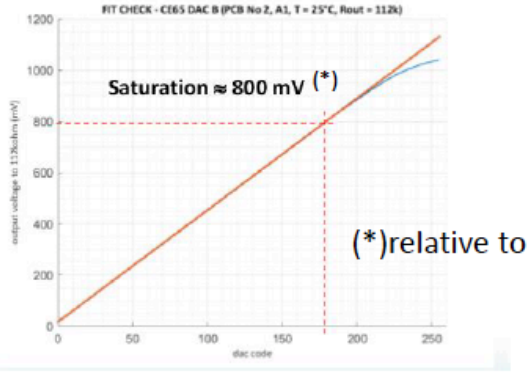




DAC A



DAC B

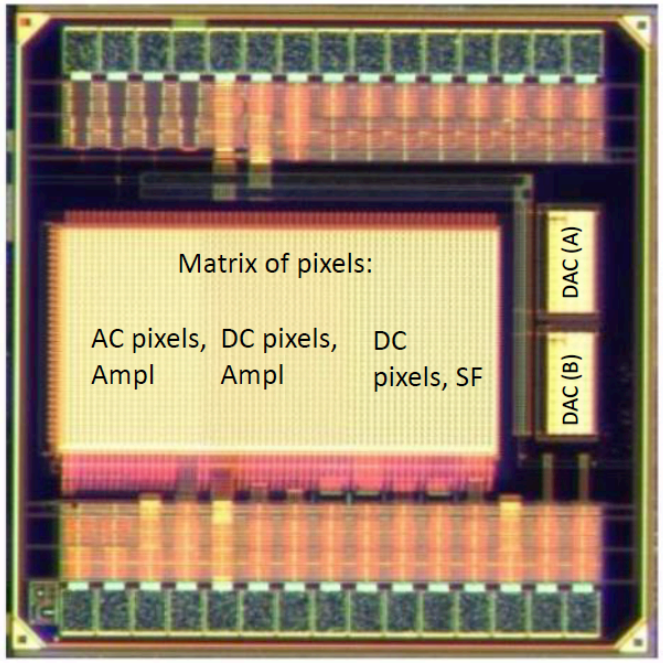


(*)relative to vdda=1.2V

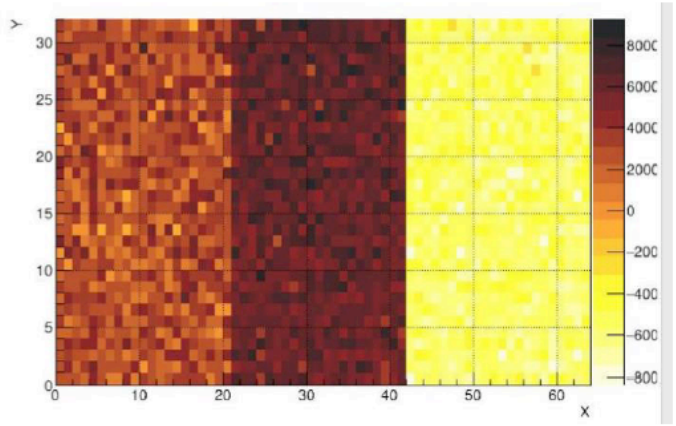
1) INL,DNL <0.5LSB
2) operating output voltage range [1.2V – 0.4 V]

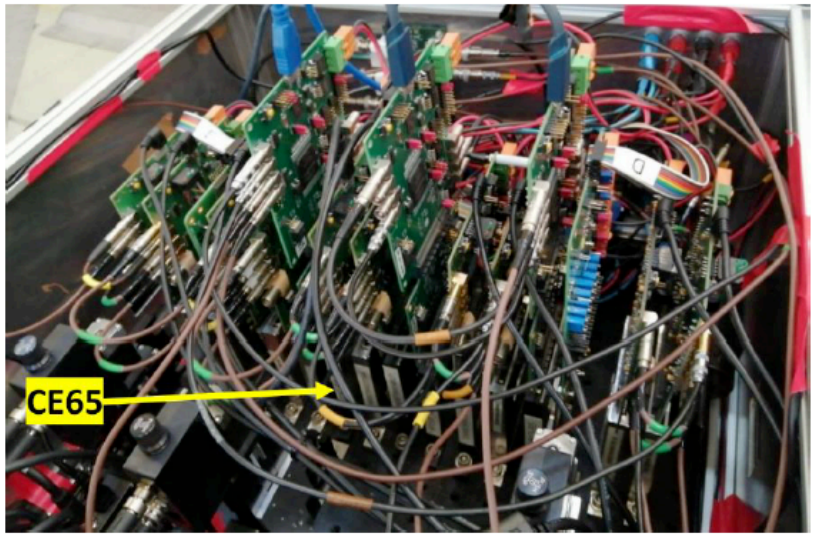
- 2 flavors functional in good agreement with simulations
- No showstoppers

MEASUREMENTS first life in CE65

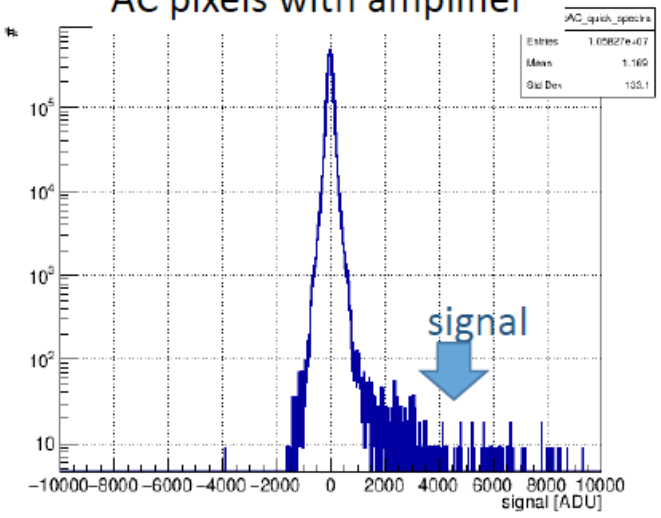


Online image of raw data from pixel matrix, clearly showing expected behavior/difference of 3 types of pixels

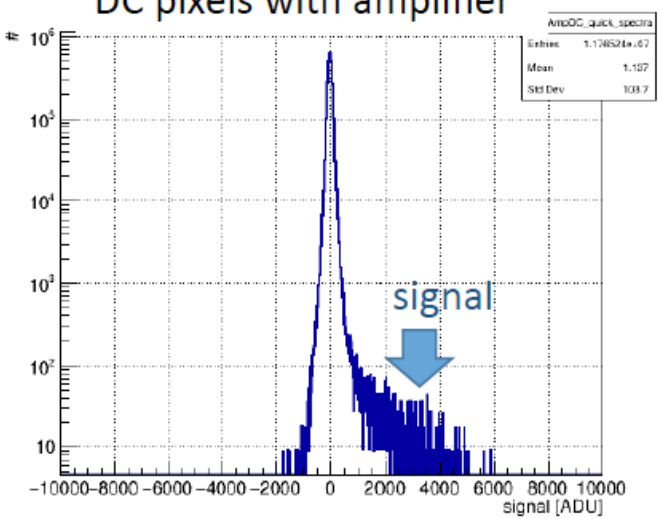




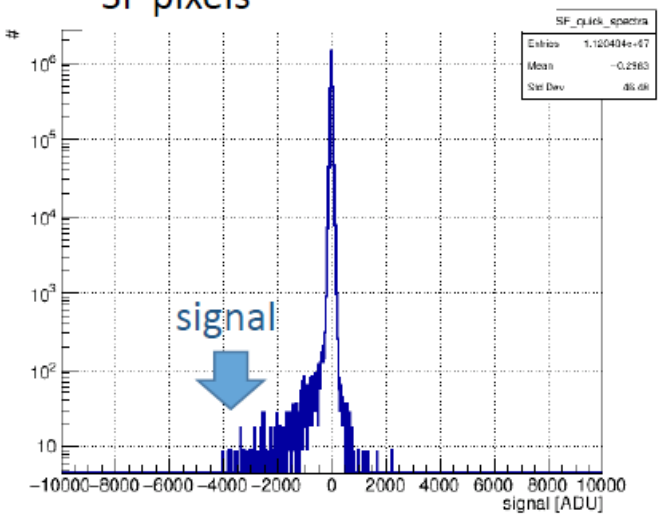
AC pixels with amplifier



DC pixels with amplifier

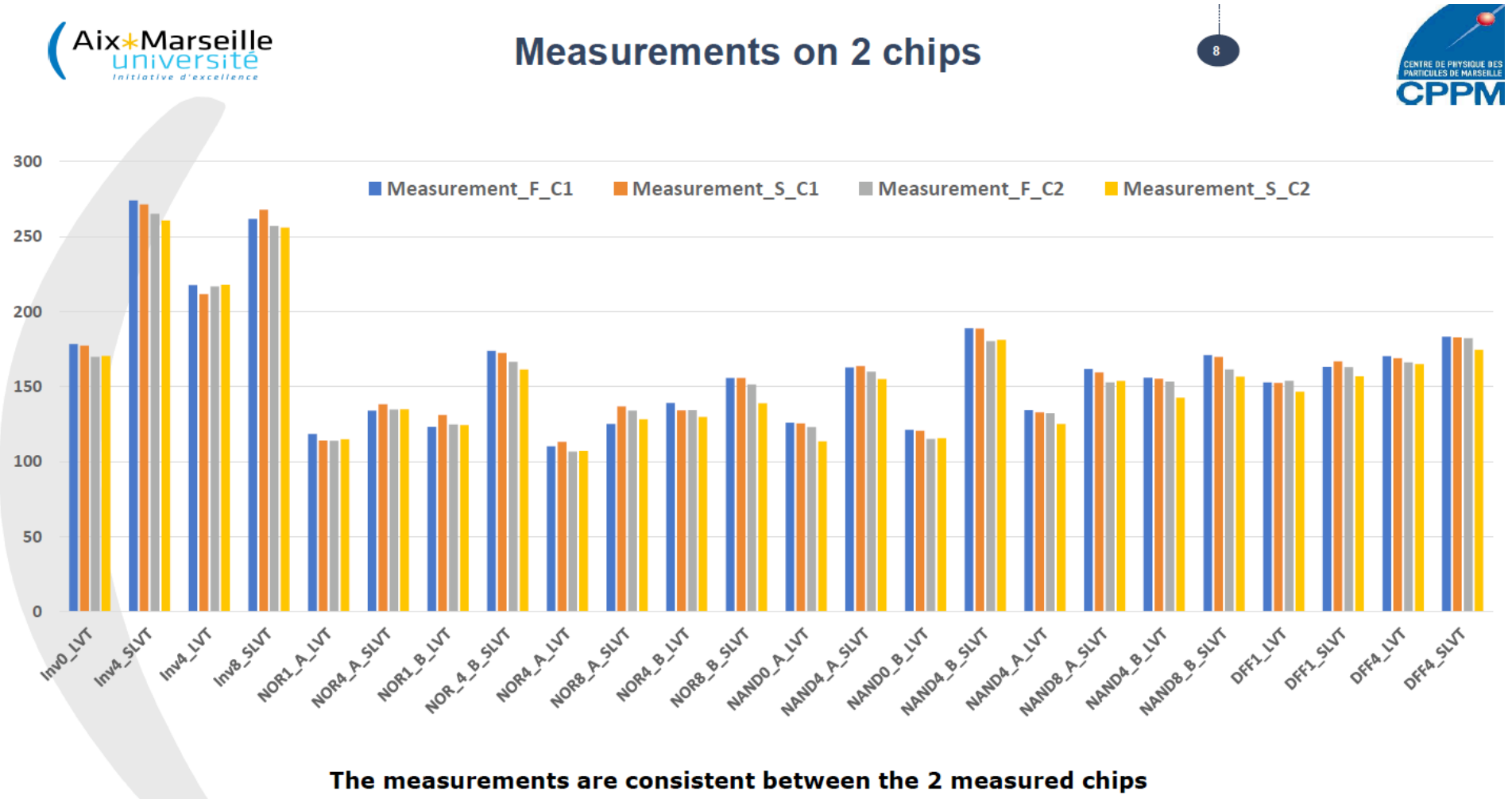


SF pixels



MEASUREMENTS RINGOSCILLATORS

- 24 flavors oscillating in good agreement with simulations
- No irradiation results yet



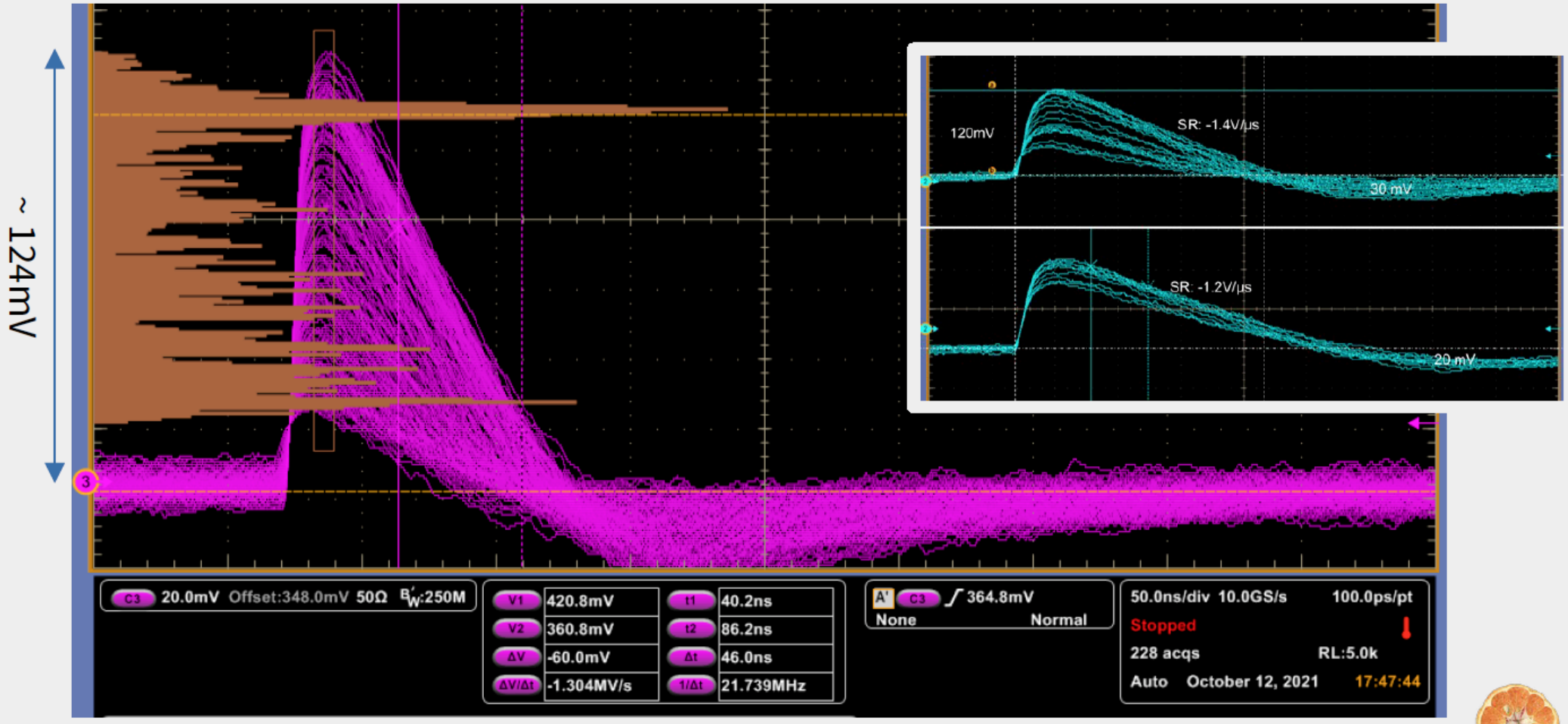
The measurements are consistent between the 2 measured chips

MEASUREMENTS DESY

Also first pulses from electron beam at DESY !

EP R&D

Measurements of Pixel Matrix with Fe55 Source



11 S. Spannagel - EP R&D WP 1.2 - Tangerine / Measurements 03/11/2021

MEASUREMENTS RAL

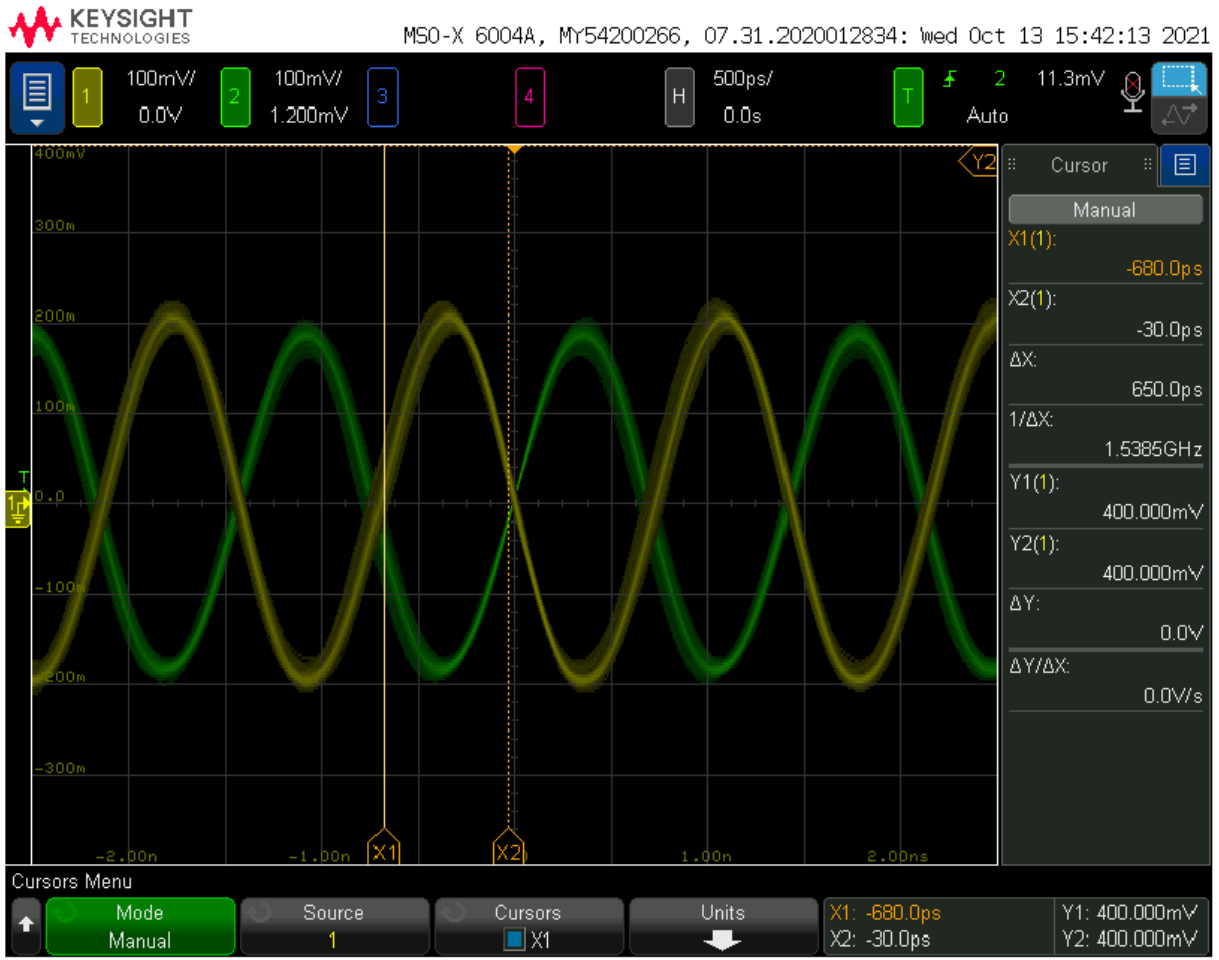
CML driver and receiver functional

EP R&D

MLR1 Testing

Testing

- Working to at least 700MHz (1.4Gbit/s)
- 800mV differential signal at that speed
- 49.3% duty cycle
- Jitter not measurably worse than input
- Better test set up needed to fully characterise



Science and Technology Facilities Council

TOWARDS STITCHED ENGINEERING RUN 1 (ER1)

- Main aim after results from MLR1: prove stitching (also for ALICE ITS3 TDR !)

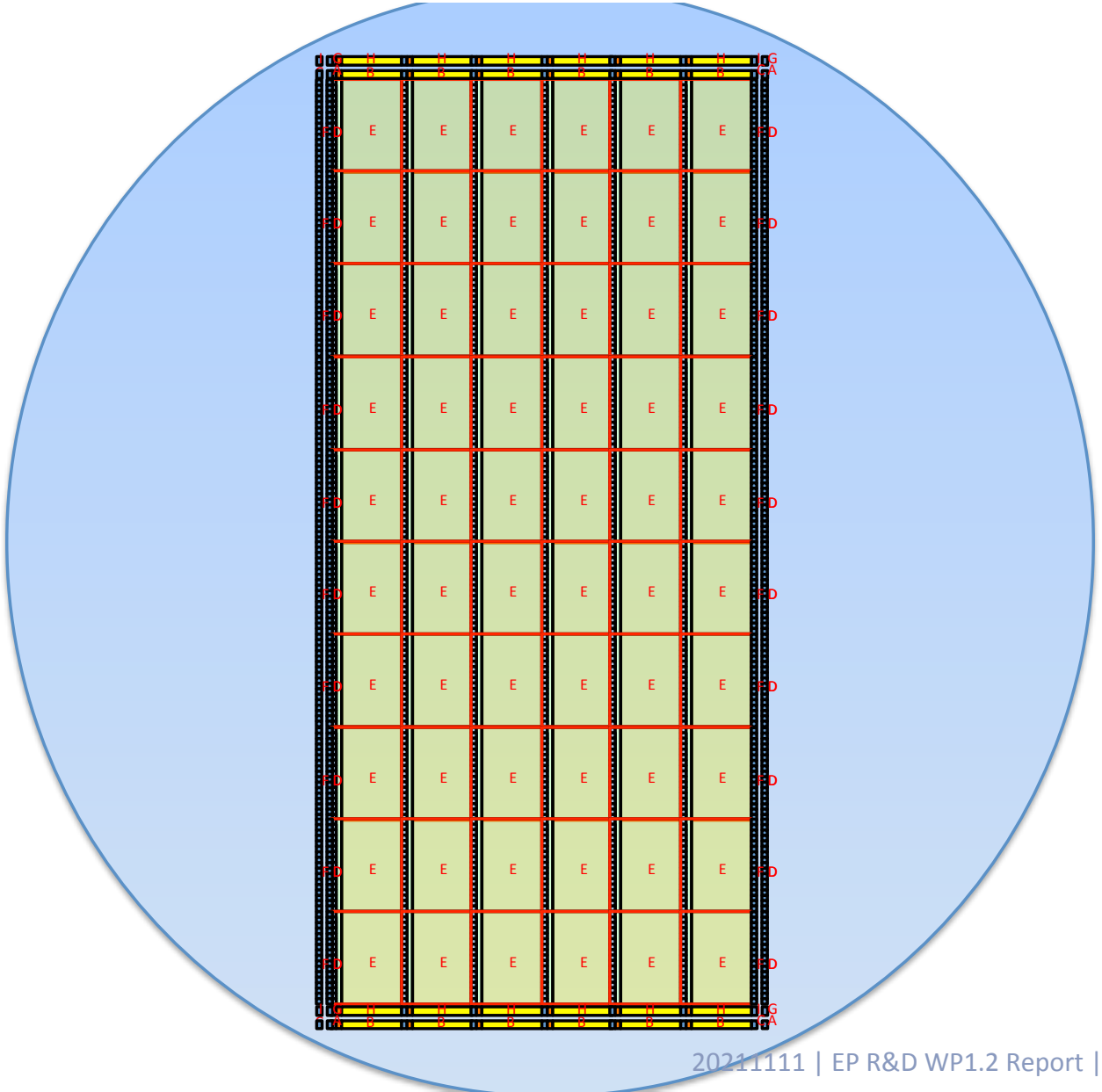
- Preparation with purchasing of ER1 (and later stitched engineering runs for ITS3 – WP1.2):
  - Input for Finance Committee prepared
  - Offer received
  - Discussion with groups on contribution

- Stitching plan approved, can go ahead, need cross-check with dicing companies

- Received proposal for new metal stack
  - Last thick metal replaced by two others with better design rules
  - Good opportunity, already for stitched engineering run ER1, but will need some time to adapt
  - Cadence digital design kit (DDK) and remainder of PDK to be available end of November, pads still to be investigated

- Challenges in design activities:
  - Balance between measurement and design activity, significant learning from both
  - Adaptation to new metal stack and constraints from stitching

Reticle and Design Concepts



Submitted GDS for wafer and reticle approval
Approved by Foundry !!

NEED CROSS-CHECK with dicing company
(GDS prepared with last metal and pad opening only)

6 x 10 central fields:
MOSS and MOST chips
+ 17 test sites 1.5 mm x 1.5 mm (60 x per wafer)

6 top and 6 bottom fields
Endcaps MOSS and MOST chips

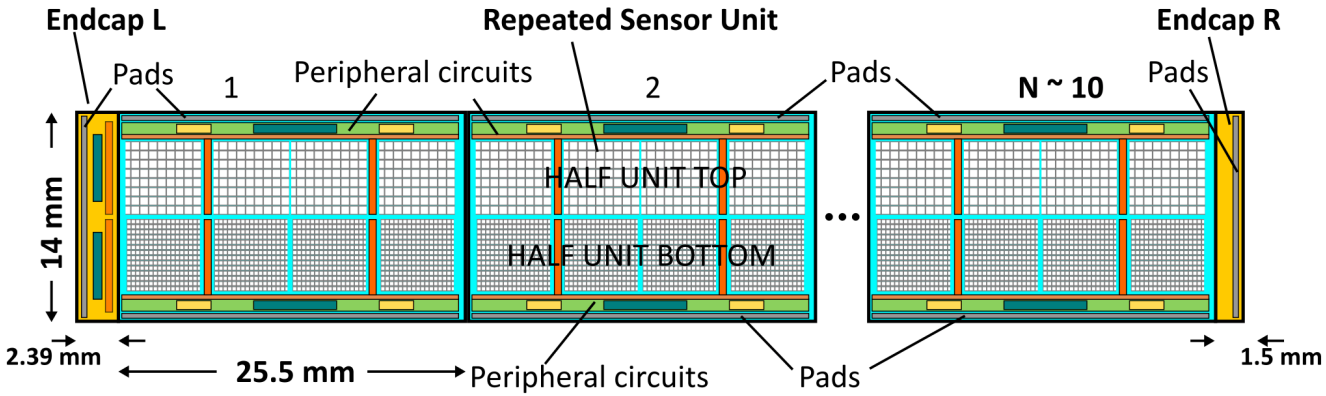
10 left and 10 right fields
~ 40 test sites 1.5 mm x 1.5 mm (20 x per wafer)

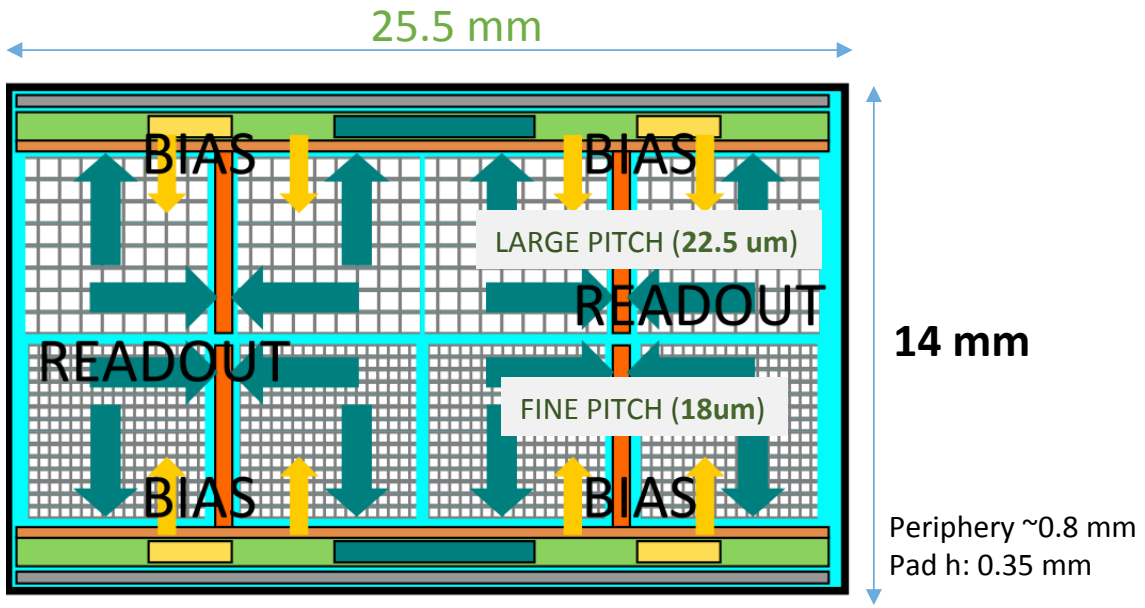
Chips for ER1: to be updated and mapped into floorplan

EP R&D

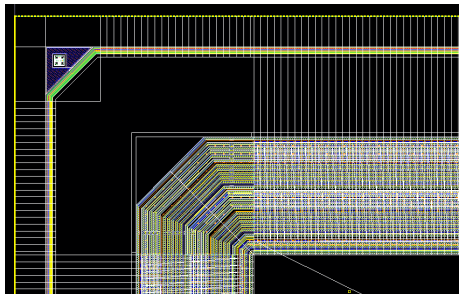
Design	Purpose	Institute	# of test sites	Comments
MOSS	stitched sensor prototype develop stitching know-how, more conservative Focus on technology options, power distribution, signal routing, yield	INFN, IPHC, NIKHEF, CERN	-	1D stitching Matrix as simple as possible
MOST	Stitched sensor prototype, develop stitching know-how, more aggressive Study yield with high density layout parts and fine power segmentaton Low power and transmission of timing information over long distance	NIKHEF, IPHC, Heidelberg, CERN, INFN	-	Many parts in common with MOSS
H2M	Hybrid to Monolithic Investigate MAPS and architectures in non-stitched sensor	DESY and CERN	2	
CE65++	Pixel optimization vehicle Focus on optimizing pixels and front-end	IPHC	tbd	
SEU chips	Prototype with memories and flops Measure SEE cross-sections (SEL, SEU)	INFN Bari	2	
PLL NIKHEF	First step in high speed transmitter	NIKHEF	1	High speed transmission
PLL+buffer	First step in high speed transmitter	RAL	1	High speed transmission
Pixel test DESY	Pixel sensor and front end prototype	DESY	1	
Pixel test SLAC	Pixel matrix prototype	SLAC	1	
APTS	Analog pixel test structure	IPHC and CERN	tbd	
DPTS	Digital pixel test structure	CERN	tbd	
TTS1-5	Transistor test structures	CERN	10	
ADC prototype	Desired function	not covered		generated from DAC ?
Supply regulation	Desired function	not covered		Interest from several corners

MOSS Monolithic Stitch Sensor Prototype Concept

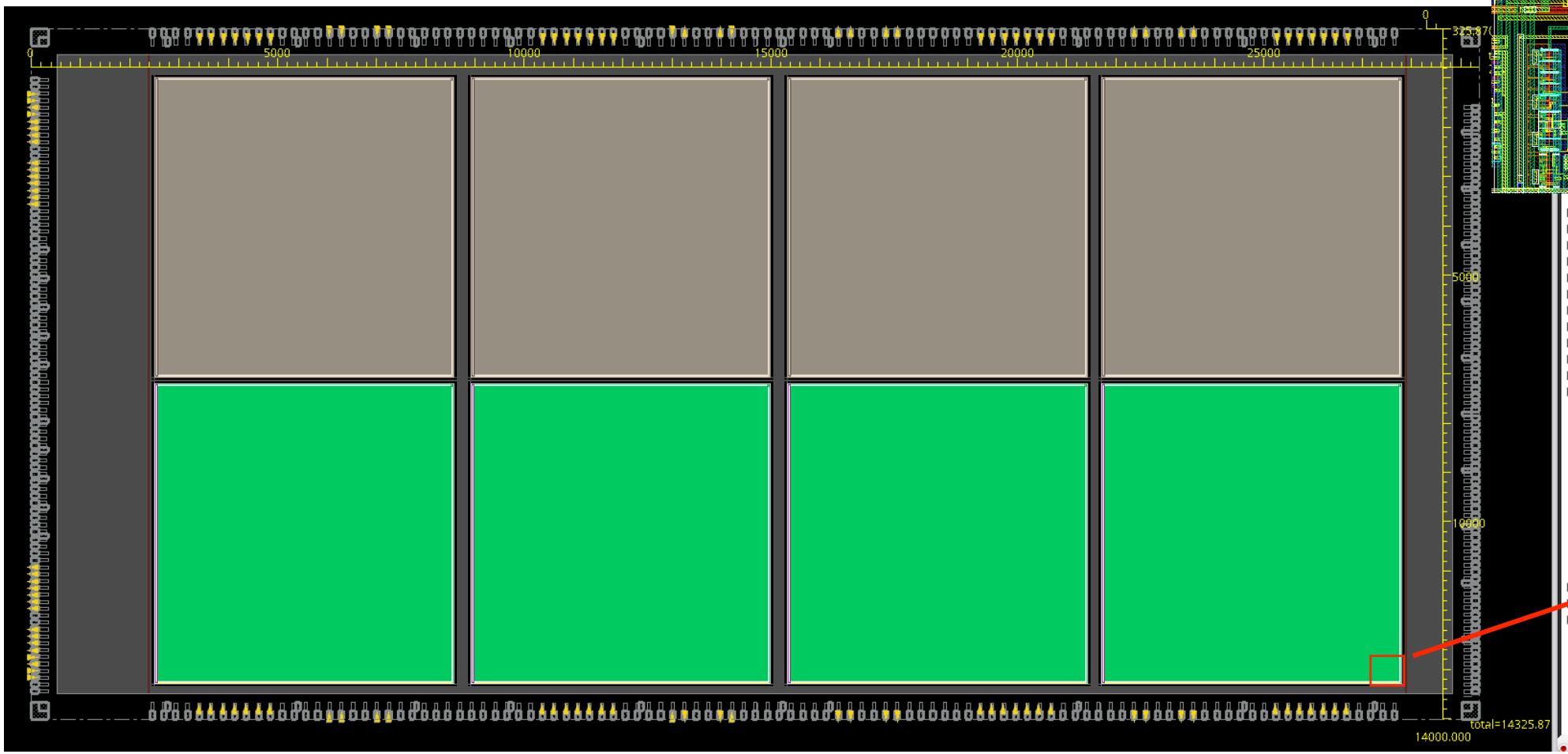


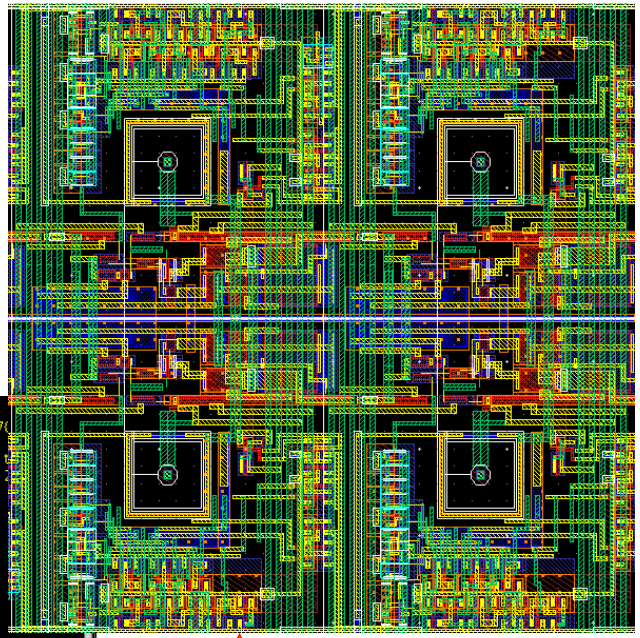


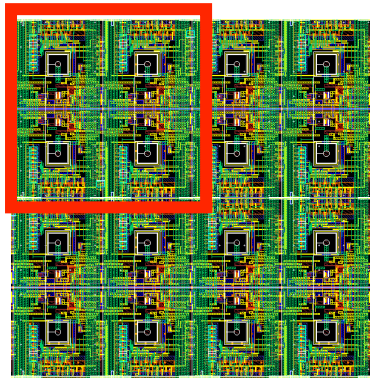
- Implement a large sensor abutting identical but functionally independent sub-units
  - Repeated Sensor Unit, Endcap Left, Endcap Right
  - Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**



MOSS - Progress on fine pitch matrix



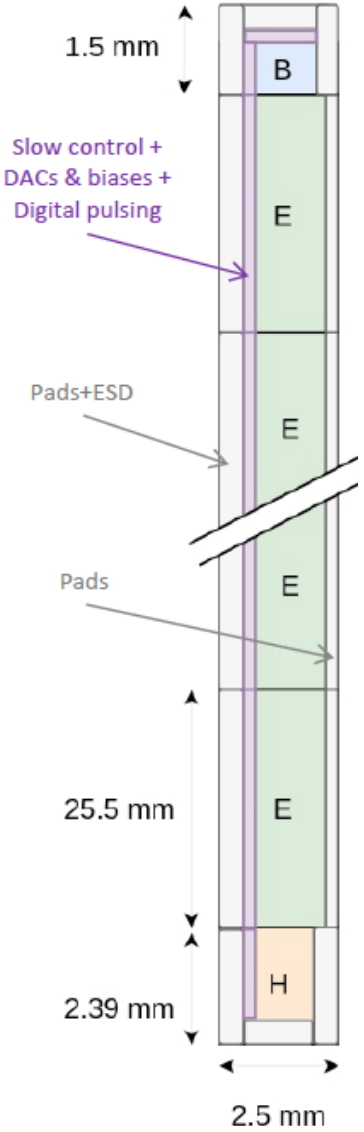




Summary - MOSS

- MOSS Stitched Sensor Prototype Progress on:
  - Fine Pitch Pixels, Fine pitch Matrix
  - Specifications, Geometry, PAD ring, Top Level Implementation Flow
  - Readout Modules RTL entry, verification testbenches
- Next
  - DACs and Biasing
  - Large Pitch Pixels and Large Pitch Pixel Matrix
  - Stitched Communication Backbone Busses
  - Top Level PnR and Verification
- Challenges
  - Port designs and flow to new metal stack once Design Kits become available
  - Design Custom PAD cells (with new metals) and update pad ring

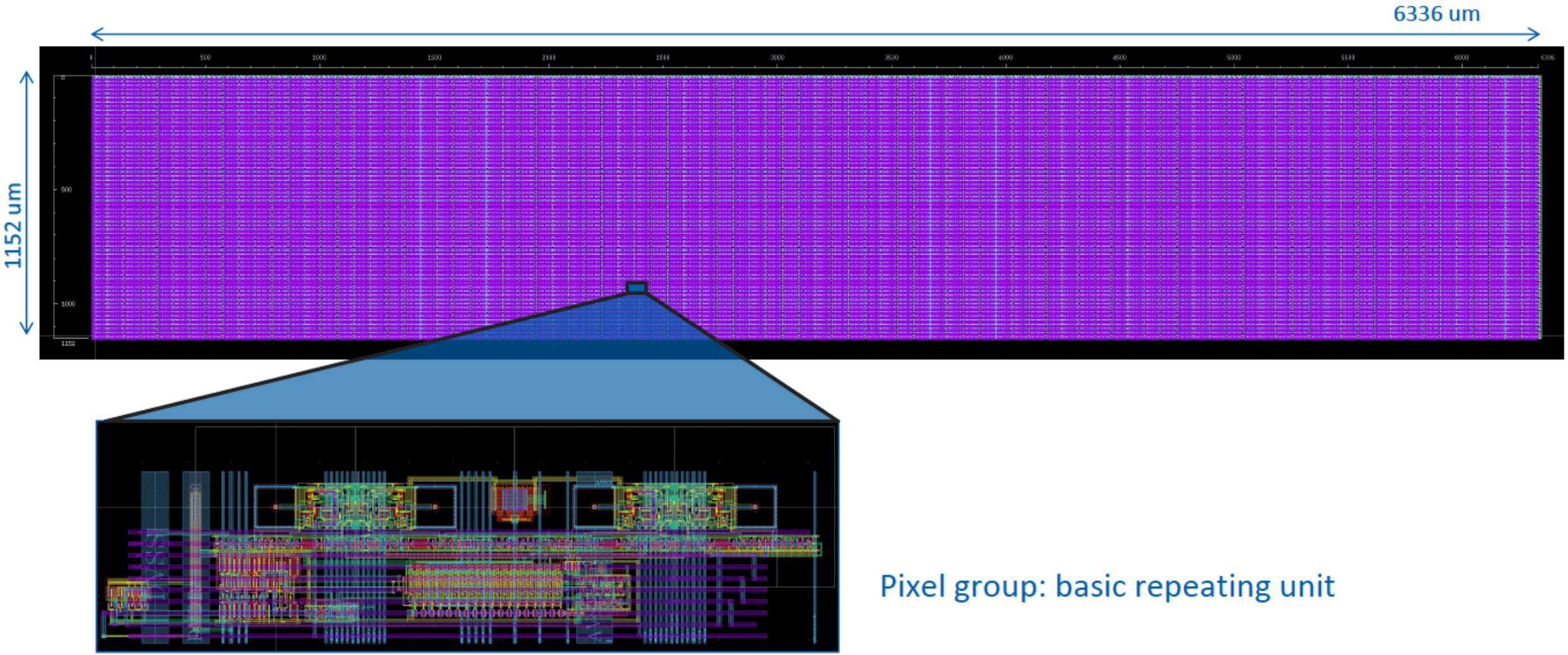
Summary - MOST Stitched Sensor



- Aim of MOST:
  - Investigating yield preserving local density
  - Explore low power asynchronous serial readout solutions with long distance data and timing transmission
- Progress and target:
  - Pixel matrix well advanced, good progress on bottom periphery
  - Slow control, biases, padring very similar to MOSS
  - Target to match MOSS project timeline and first draft of chip by end of November
- Next
  - Digital modeling and verification of peripheral circuits (bottom periphery, digital pulsing…) together with pixel matrix
  - Implementation of remaining macro cells and digital blocks (biases, slow control, pulsing)
  - Top Level PnR and Verification
- Challenges
  - Port designs and flow to new metal stack once DKs become available
  - Design Custom PAD cells (with new metals) and update pad ring

MOST pixel matrix

Pixel submatrix layout: 4 of these cells make the pixel matrix for one stitch



Pixel group: basic repeating unit

H2M (hybrid to monolithic) DESY& CERN

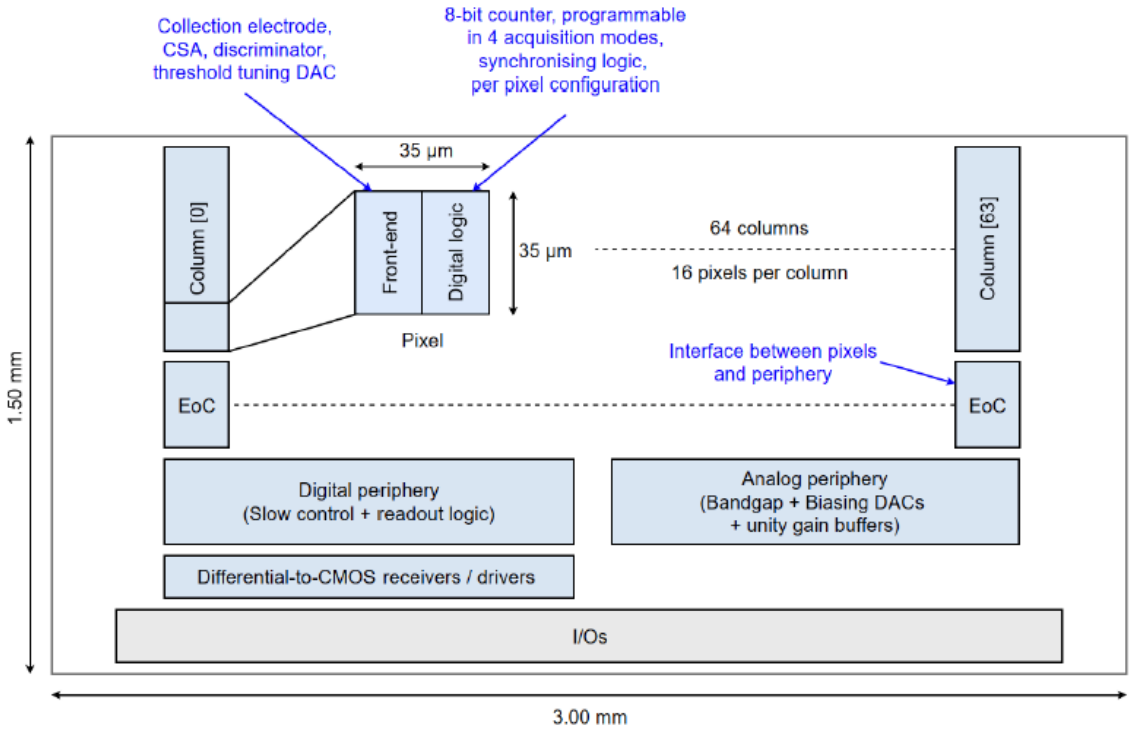
EP R&D

- Development aims:
  - Digital-on-top design flow and methodology
  - Porting a hybrid pixel architecture into a monolithic process
  - Design and testing of a compact digital cell library
  - Compare the system level behaviour with the hybrid embodiment
  - Optimising interconnect and mechanical schemes to minimise the cost per unit area

Analog Front end DESY (C. Reckleben, K. Hansen)
Biasing & Digital CERN (A. Dorda & I. Kremastiotis)
Bandgap NIKHEF (V.Gromov)

Design in progress, verification effort started (A. Pulli), slow control based on Medipix4/Timepix4

- The H2M chip:
  - 3 x 1.5 mm^2 chip
  - 64 x 16 square pixels
  - 35 µm pitch
  - 8-bit counter per pixel
  - 4 acquisition modes:
    - Time of Arrival (ToA)
    - Time over Threshold (ToT)
    - Photon counting
    - Triggered binary readout, with configurable strip length

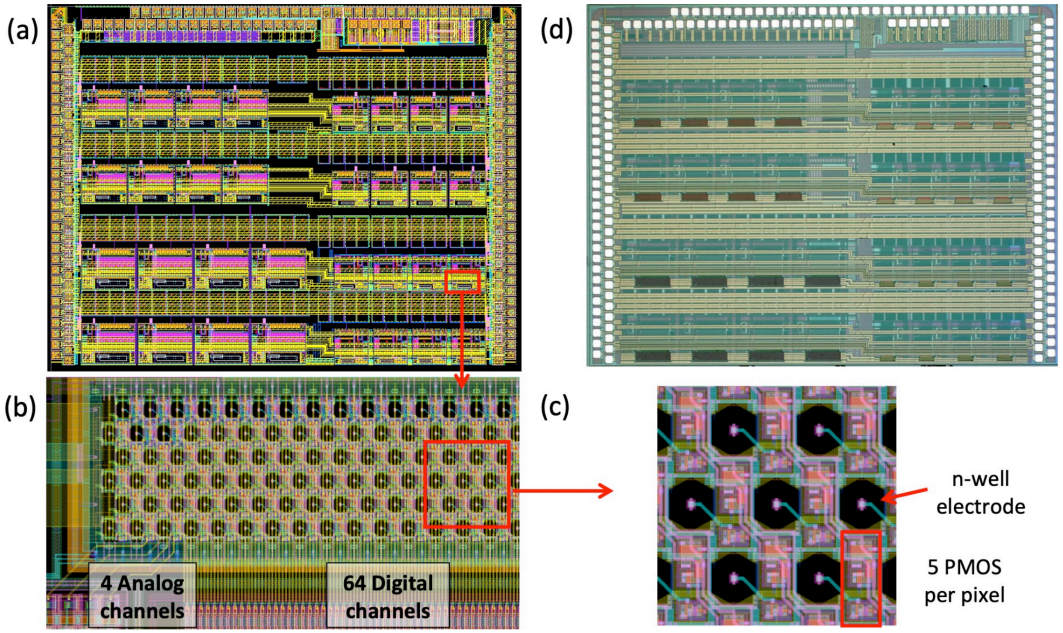


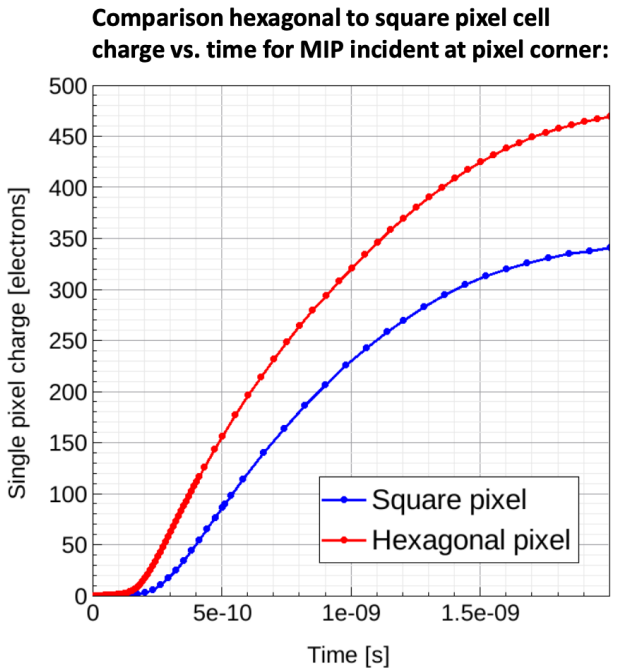
TIMELINE UPDATE

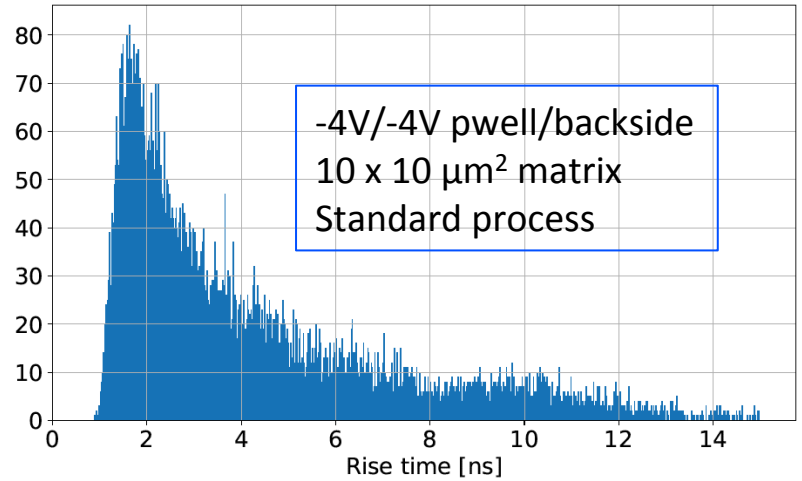
- Representative mock submission with new metal stack not within reach for end of November due to:
  - change of metal stack
  - PDK, DDK only available at that date
  - Progress on the design
  - Challenge to balance design and measurement effort, still significant learning from both

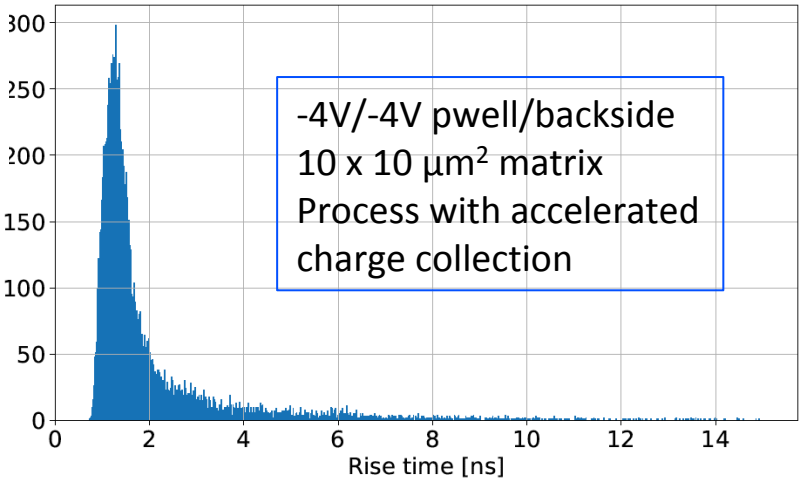
- Proposal for updated schedule
  - First draft version of stitched chips by end of November with old metal stack, some work already ongoing for port to new stack
  - Mock submission end of February (maybe still some type of mock submission before Christmas)
  - Real submission end of April

FASTPIX ATTRACT project: ^{90}Sr Risetime distributions









T. Kugathasan et al., https://doi.org/10.1016/j.nima.2020.164461 (ATTRACT: INFN, Ritsumeikan University and CERN)

Direct relation between charge collection and process variant (TowerJazz 180nm)

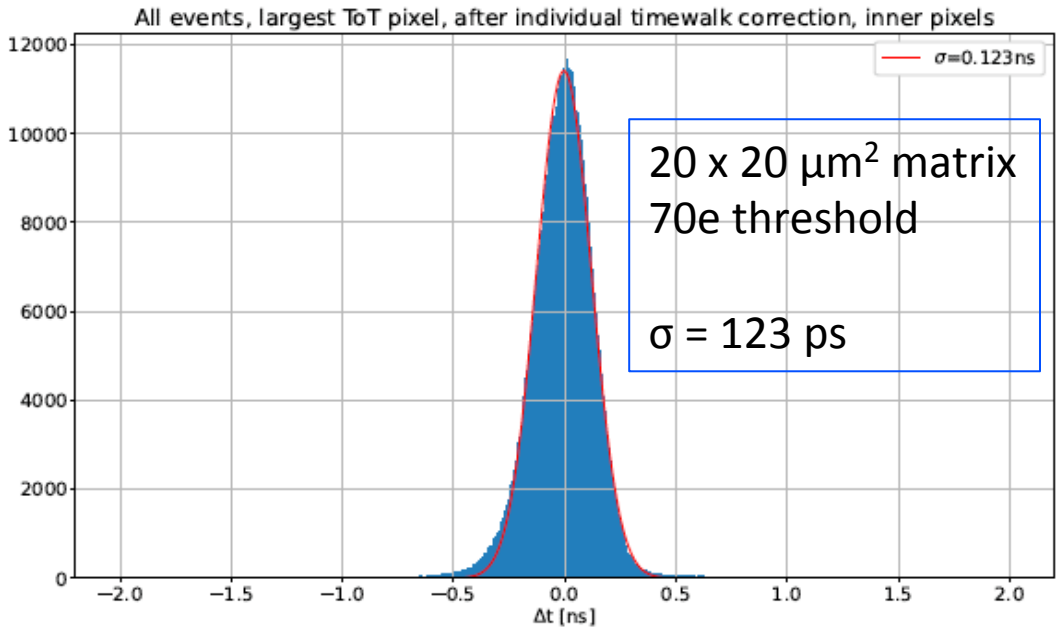
Significant impact even at very small pixel pitch

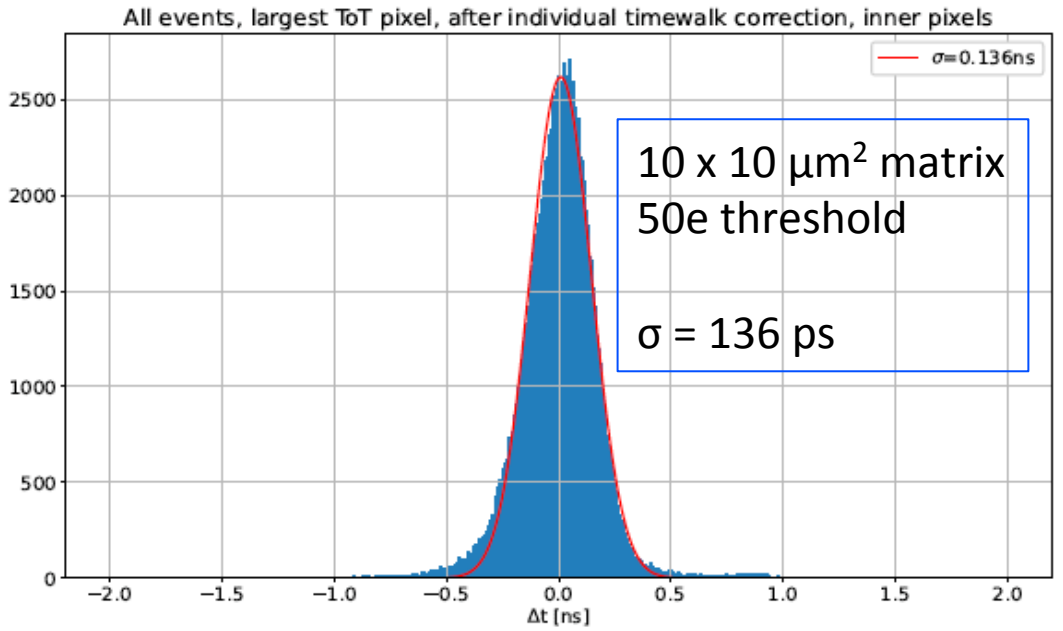
Hexagonal pixels (pitch 8.66, 10, 15 and 20 µm)

- better approximation of a circle
- charge sharing in the corners between 3 pixels instead of 4 -> more margin
- collection electrodes on hexagonal grid, circuit to remain on Manhattan layout

E. Buschmann, D. Dannheim, K. Dort, M. Muenker, J. Braach

FASTPIX ATTRACT project: test beam





Wafer 18
-6V/-6V pwell/ backside

20x20 µm² matrix (left)
70e threshold

10x10 µm² matrix (right)
50e threshold

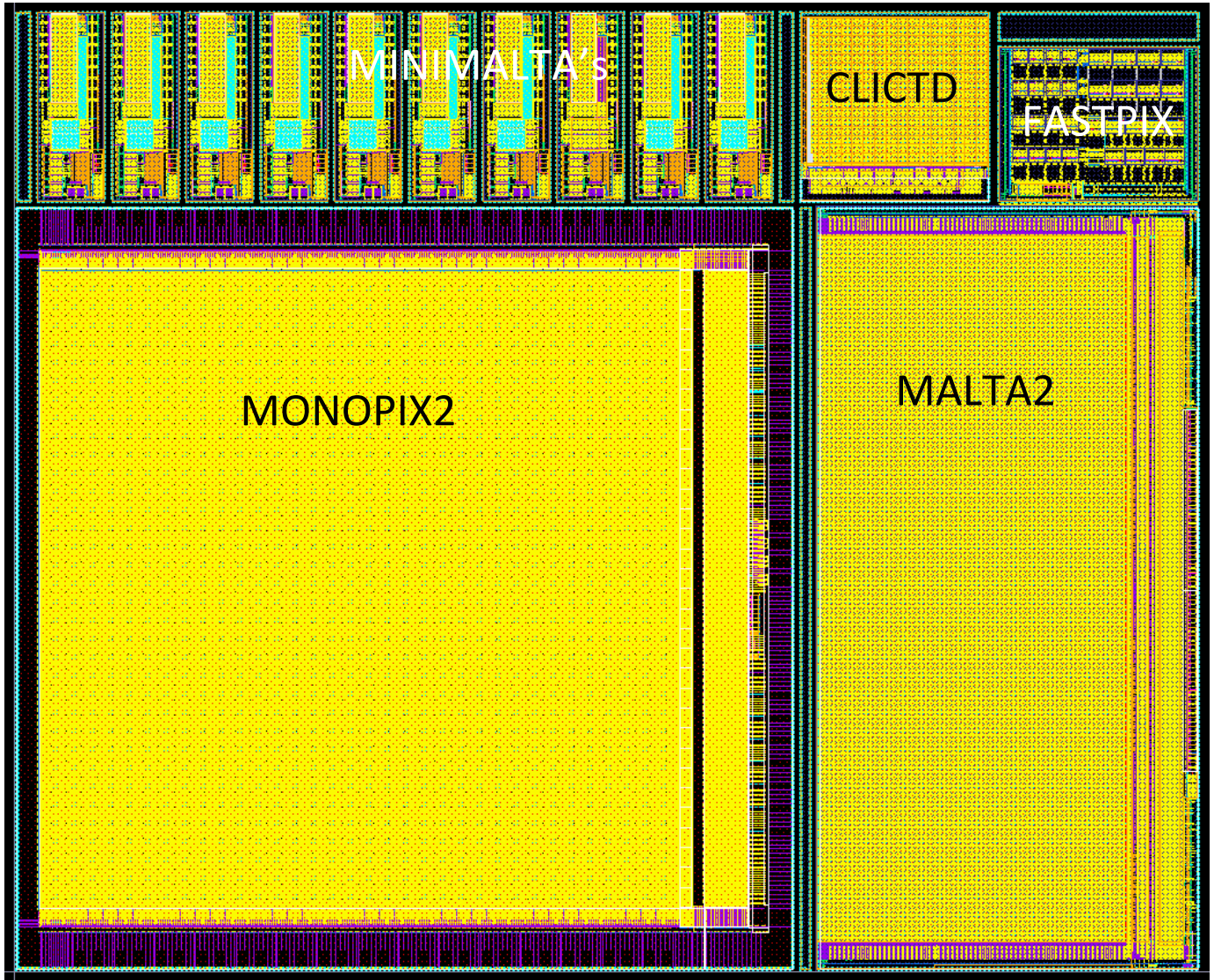
- Timing after timewalk correction on 20µm (left) and 10µm (right) matrix
- Pixel-by-pixel correction for best results, reaching below 200ps resolution
- 10µm matrix is operated at lower threshold with a few Hz noise rate
- Larger cluster sizes for 10µm leads to lower average seed charge and thereby more time walk and makes decoding more difficult

See Eric Buschmann et al. 12th Workshop on Picosecond Timing Detectors for Physics, work in progress !!

STREAM2 run (TJ 180 nm)

Includes monopix2, malta2, minimaltas, CLICTD, and Fastpix test chips

- Bonn, CPPM, IRFU and CERN (monopix/malta/ minimalta)
- CLICTD & FASTPIX
- Process modifications for sensor radiation tolerance and fast charge collection
- After measurements on recent Minimalta included with FASTPIX run, increased size and cascoded M3 transistor for further RTS noise reduction and improved threshold uniformity
- **Tests ongoing** (IRFU, CPPM and Bonn also received LF submission back)



Summary:

- TPSCo 65 nm: Significant learning from both measurement and design effort
  - Measurements:
    - Process (importance of TCAD & Monte Carlo !!) and front end proven
    - No showstopper on the transistors
    - Many chips and blocks from MLR functional
    - Silicon proven elements for stitched sensor
  - Design:
    - Matrices for stitched devices well advanced, some test chips close to completion with old metal stack, more work on others
    - Revision of time line necessary: new metal stack, balance between design and measurement effort
  - Paperwork for NDA (Michael & co), preparation for Finance Committee (Francois et al), offer etc
- TJ 180nm:
  - FASTPIX: timing below 150 ps
  - STREAM2 & CLICTD: encouraging measurements also on Cz

THANK YOU TO ALL CONTRIBUTING PEOPLE, GROUPS AND INSITUTES

SPARE

Progress Since Mid-September

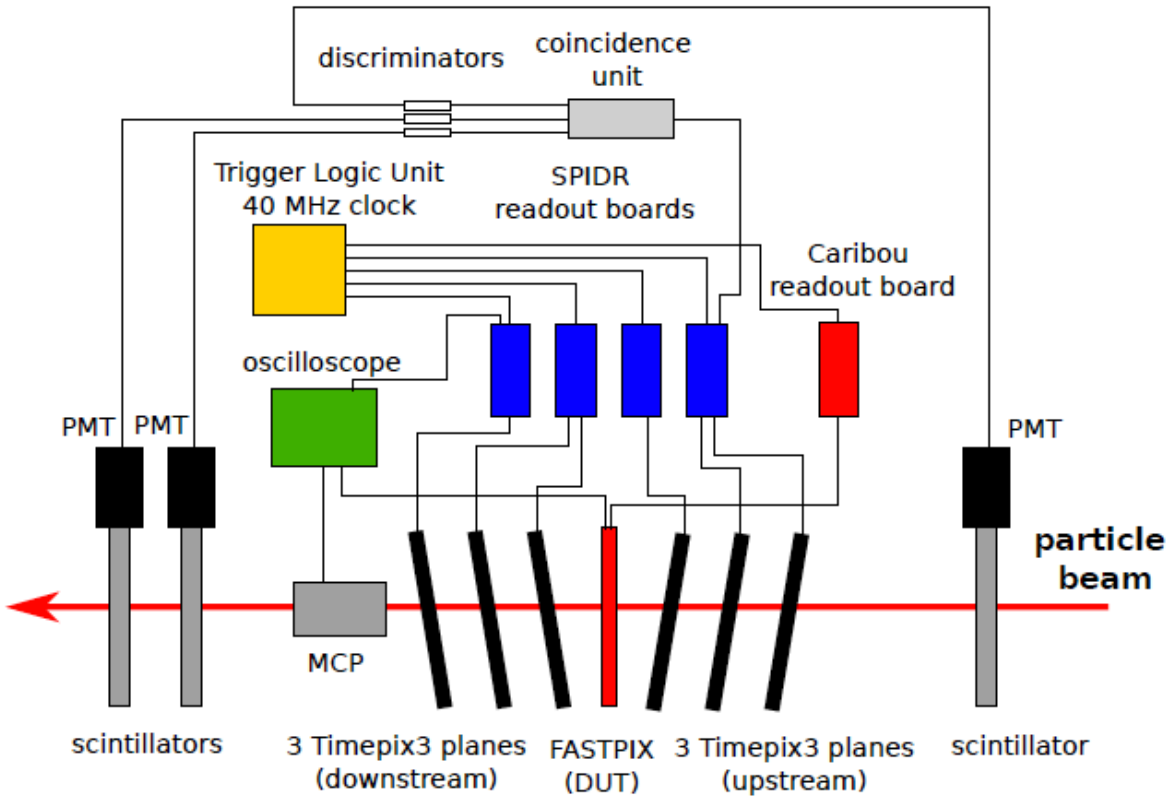
- Stitching Plan Approved
- Specifications
  - Power Domains, Pads and I/Os, DACs, Stitched Communication Backbone
- Pixel (Analog and Digital) and *Fine* Pitch Pixel Matrix
  - Choice of pixel front-end, introduction of reverse biasing, digital pixel, integration of matrix
- DACs, Biasing and Monitoring
  - Effort now available and work ongoing
- Control and Readout modules, RTL entry
- Verification by simulation
  - Directed simulation testbenches and UVM framework components
- Top Level Digital-on-top Implementation flow
  - Placement of pad ring

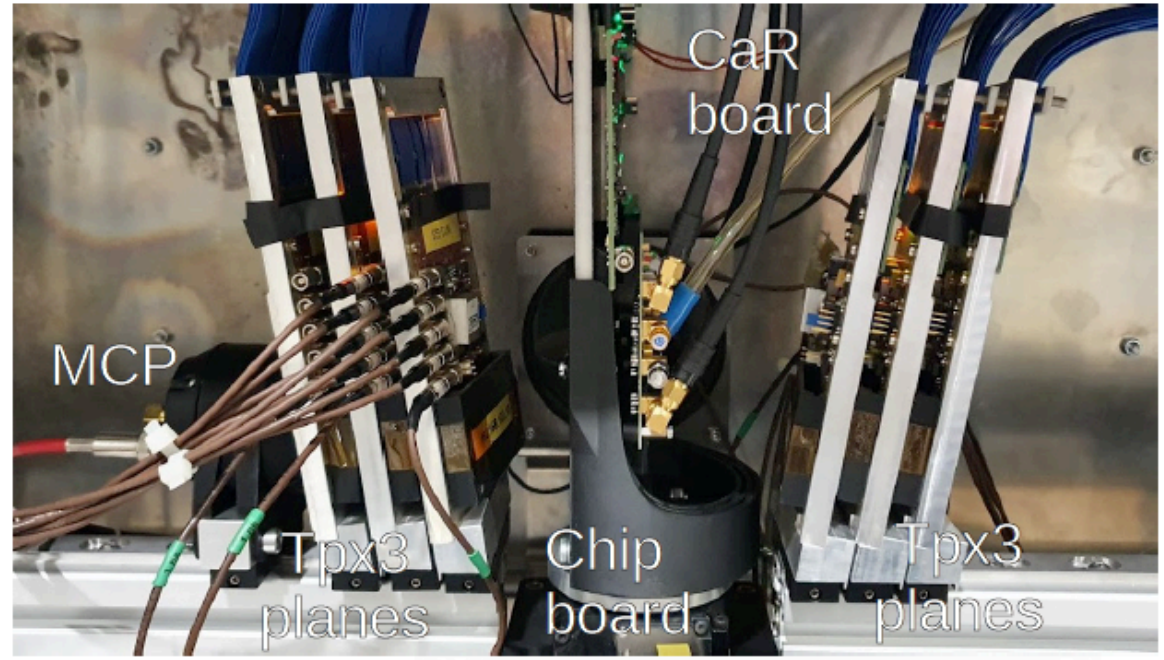
Items and Challenges Ahead

- Design of *Large Pitch* Pixel and Pixel Array
- Port blocks and design to new metal stack
  - Available End of November
- Stitched Communication Backbone
  - Effort currently unavailable
- Design of *custom pad cells* and pad ring
  - Effort currently unavailable and need of design kit for the new metal stack
- Isolation of independent power domains
  - Need design and connection of many physical cells
- Yield maximisation
  - Missing quantitative information and criteria
- Verification Plan and Verification Tests

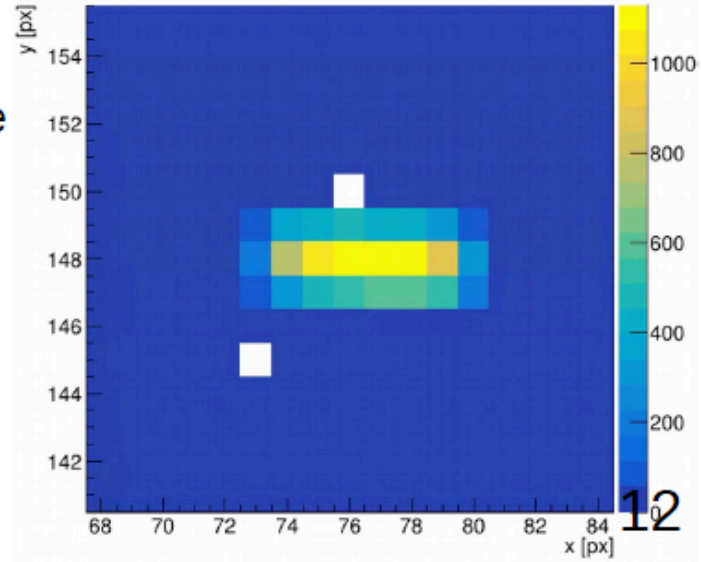
Test-beam Measurements - Setup

- Test-beam at SPS in August and September in Timepix3 telescope
- Micro-channel plate as fast time reference (expected resolution below 10ps, see: J. Bortfeldt et al.)
- New improved chip board for FASTPIX





Hitmap of TPX3 plane showing events with associated FASTPIX triggers (55x55um² pixels on TPX3)



- Readout of FASTPIX and MCP with oscilloscope
- Synchronisation of oscilloscope triggers to telescope DAQ
- **Test-beam still ongoing: only preliminary results**