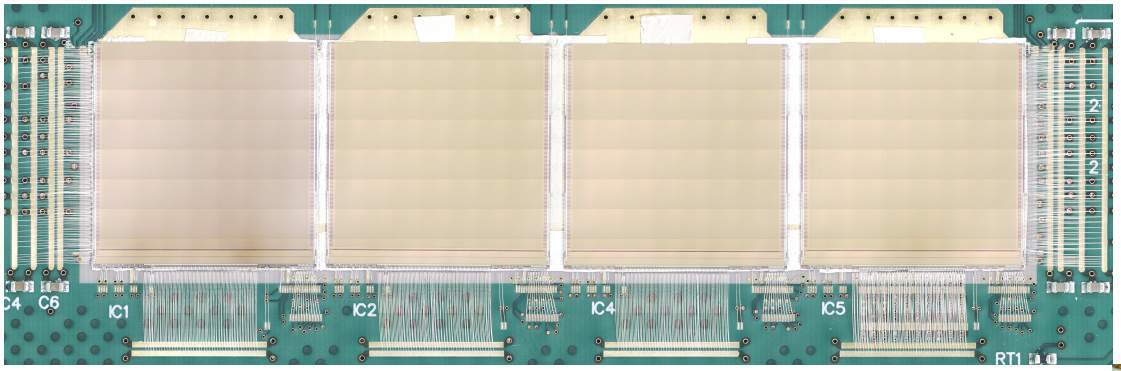
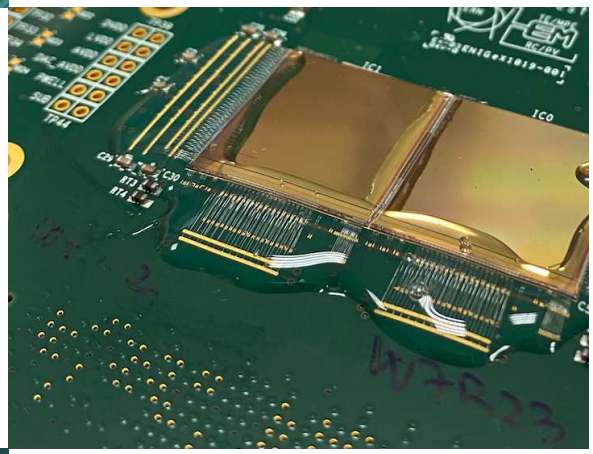


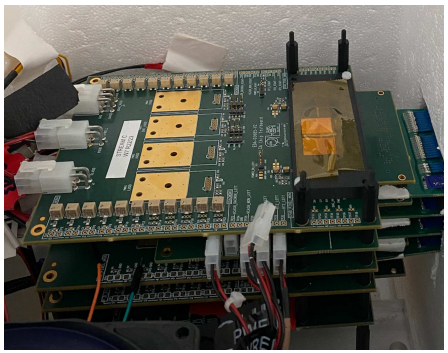
EP-DT
Detector Technologies
EP R&D

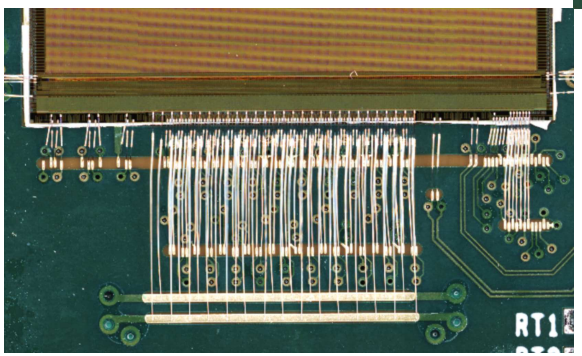
Work Package 1.3

Multi-chip module studies using the MALTA monolithic pixel chip

Florian Dachs

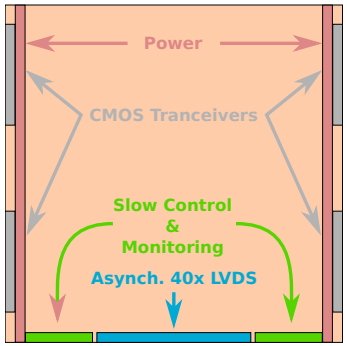




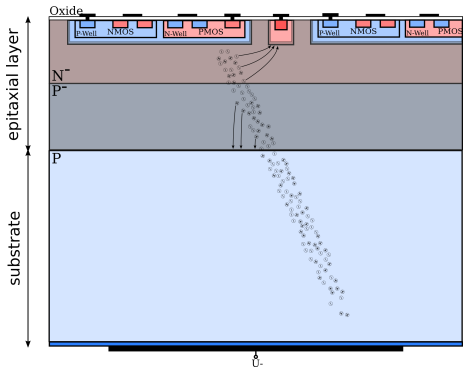


MALTA

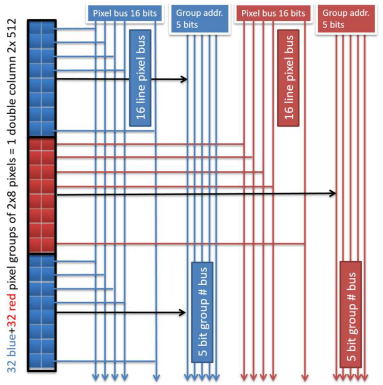
- monolithic silicon pixel chip
- produced in a 180 nm process by TowerJazz
- default laser dicing with 15 µm distance to sensitive region
- default thinning to 100 µm
- built-in functionality for large area pixel modules (chip-to-chip transfer)
- see: Measurement results of the MALTA monolithic pixel detector



- $\sim 2 \times 2\,\mathrm{cm}^2$ area, 750 contact pads sized $88 \times 88\,\mu\mathrm{m}^2$
- redundant chip-to-chip data and 40x parallel output for main readout
- 512×512 pixel matrix



- $36.4 \times 36.4\,\mu\mathrm{m}^2$ pixels with small collection diode
- 25 or 30 µm high-resistivity epitaxial silicon or Cz silicon

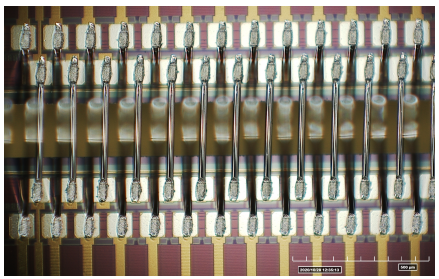


- asynchronous front end and readout
- asynchronous oversampling for DAQ

Studied interconnection techniques

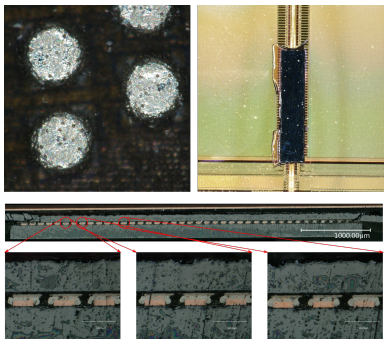
- several interconnection techniques are studied for chip-to-chip and module level connections to build large area and light-weight modules
- chip-to-chip connections with direct connections as well as using a Si-bridge

wire bonding



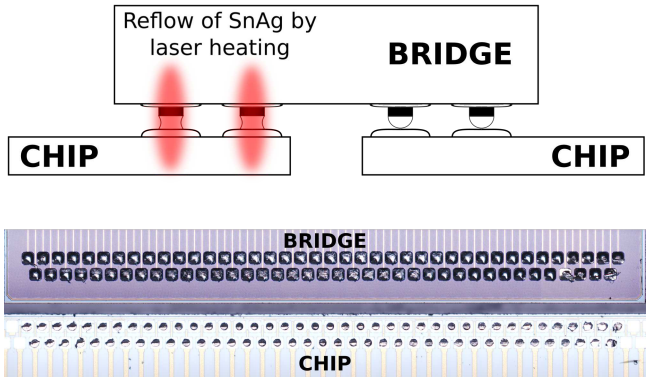
- working assemblies produced
- failures can be repaired
- needs mechanical protection
- min. bond length dictates gap between chips

ACF



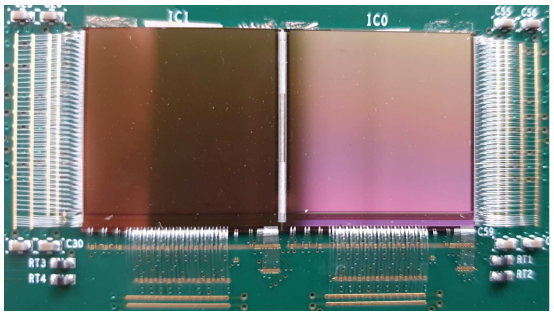
- potential for fast interconnection process
- connection could also provide mechanical stability
- assembly process optimization ongoing

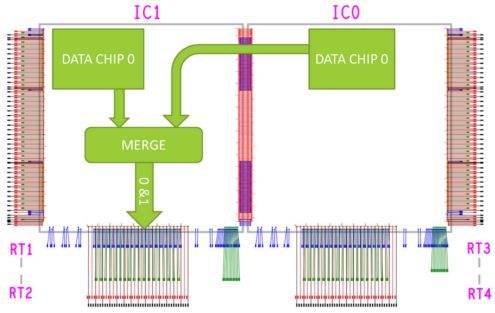
reflow

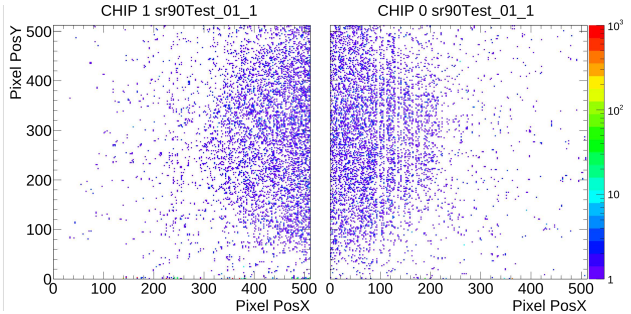


- electrical and mechanical connection using local laser heating
- mechanical stability limited by pad size connection area
- test assemblies received, evaluation ongoing

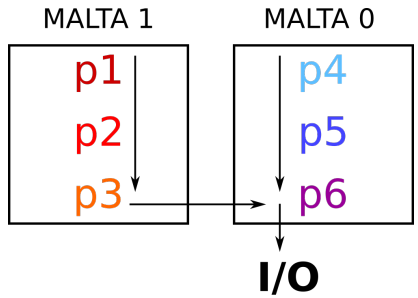
MALTA 2-chip: data transmission

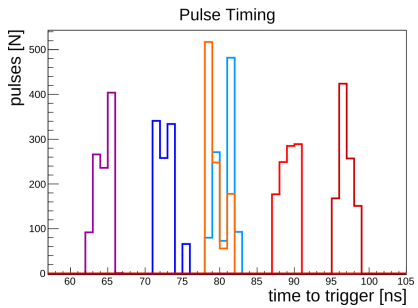




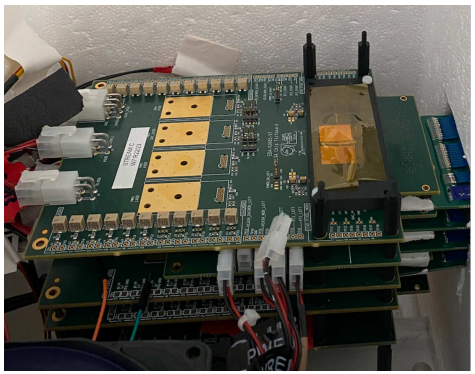


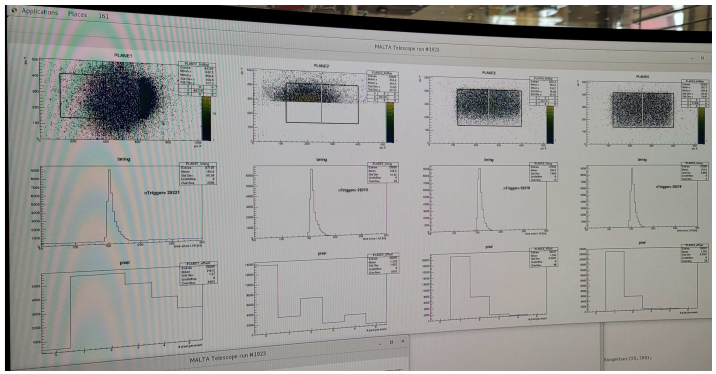
- two 2-chip modules assembled and confirmed working
- data from the secondary chip is forwarded to the primary via CMOS transceivers
- both chips can be configured as primary to test connection both ways
- data transmission tested via source scans and time of arrival of pulsed signals

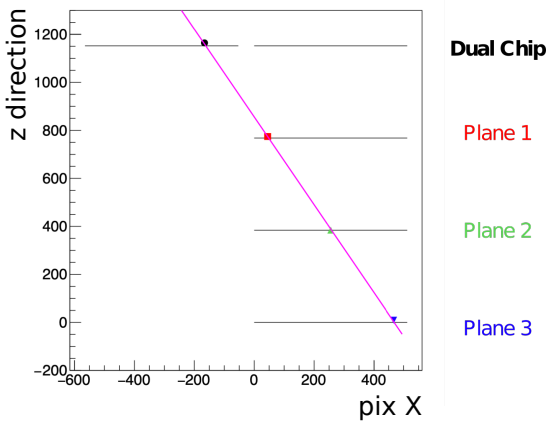




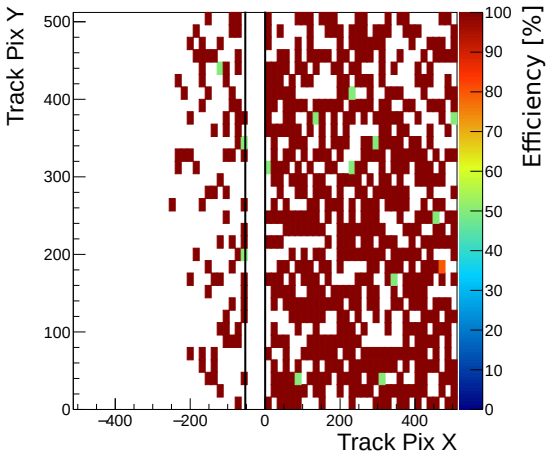
MALTA 2-chip: cosmics tracking



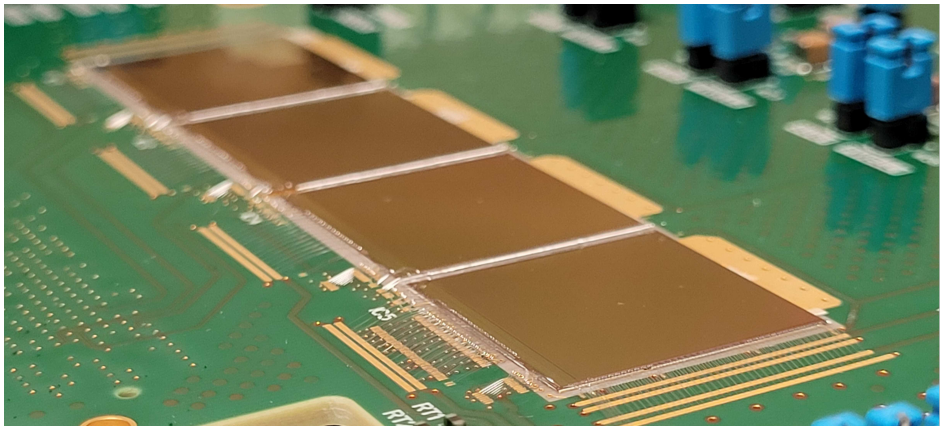


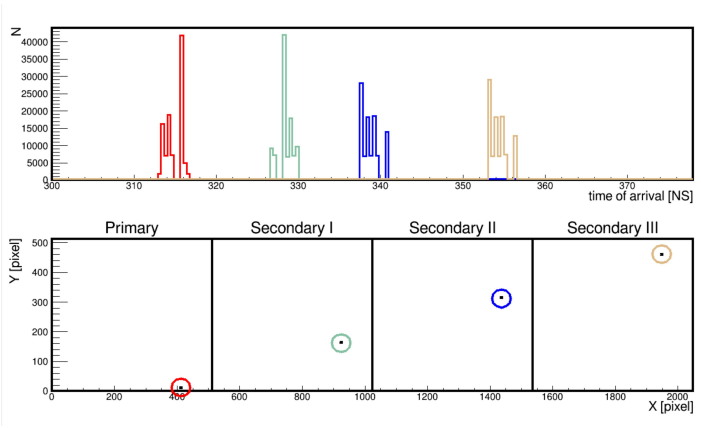


- modules successfully encapsulated with Sylgard and integrated in 4-plane telescope
- cosmic data taken and processed with the MALTA cosmic telescope (A. Gabrielli and V. Dao)
- 1940 µm gap between active areas on 2-chip module defined by wire bond requirement, gap can be reduced using other interconnection techniques



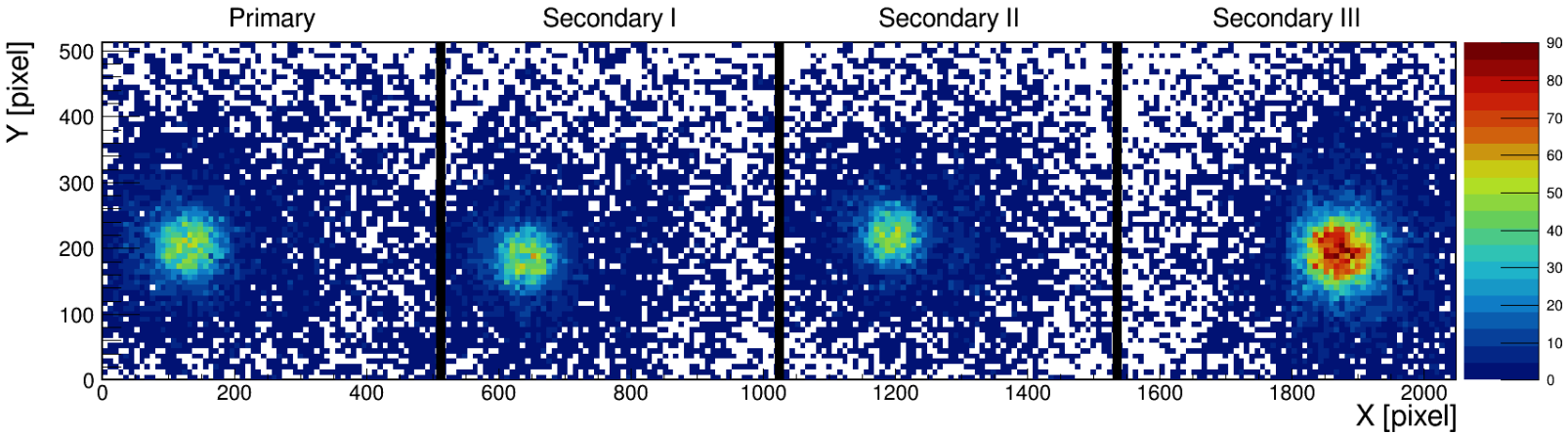
MALTA 4-chip: data transmission





- first working 4-chip module assembled
- full dimension of module is $\sim 8 \times 2\,\mathrm{cm}^2$
- chips tested individually to sort out failures before full interconnections are done
- initial pulse timing tests with limited number of pixels successfully performed
- validation in beam tests tentatively planned for next year

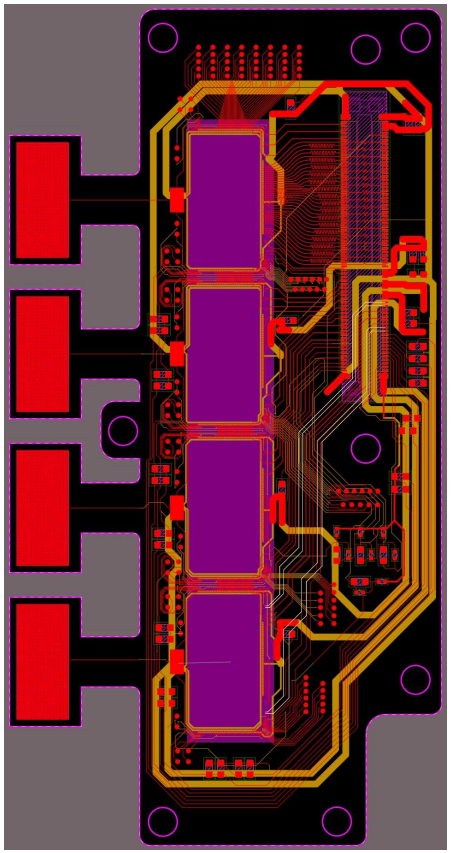
MALTA 4-chip: data transmission



- successful source scan done on all chips in a single readout cycle where the source was moved from chip to chip
- full software and firmware implementation ongoing
- further tests to optimize powering and readout ongoing

MALTA flex carrier

- design based on findings with 4-chip module
- light-weight, 2-metal-layer flex with $\sim 45\,\mu m$ thickness
- implemented for MALTA2 chips
- flex production process permits $80 \times 80\,\mu m^2$ pads on carrier for direct pad-to-pad connections with chips
- face down bonding for minimal gaps between chips
- several bonding techniques being investigated
  - solder reflow
  - gold-stud / conductive glue bonding
  - ACF



Conclusions

- development of large scale and light weight modules with monolithic MALTA pixel detectors
- 2-chip and 4-chip assemblies have been successfully produced with wire bond interconnections to test data and power transmission
- further interconnection techniques are investigated to further reduce the material budget and dead area between chips
- design of a light-weight flex carrier for 4 chips (8 cm long) completed
- reliability tests (thermal cycling) and irradiation studies of the interconnection after initial characterization