EP R&D WP5
Status & Plans

CERN EP R&D Day 2021

11 Nov. 2021

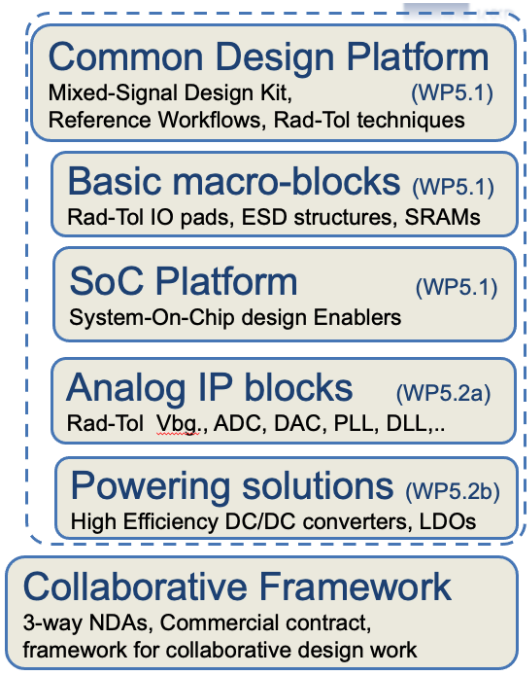
Kostas Kloukinas
Davide Ceresa
Stefano Michelis

WP5 Activities

WP 5 R&D

Leader: Kostas Kloukinas
Deputy: Davide Ceresa

- Activity 5.1: CMOS Technologies
  - Technology survey and evaluation
  - Radiation Effect studies
  - Common Design Platform
  - Collaborative Framework



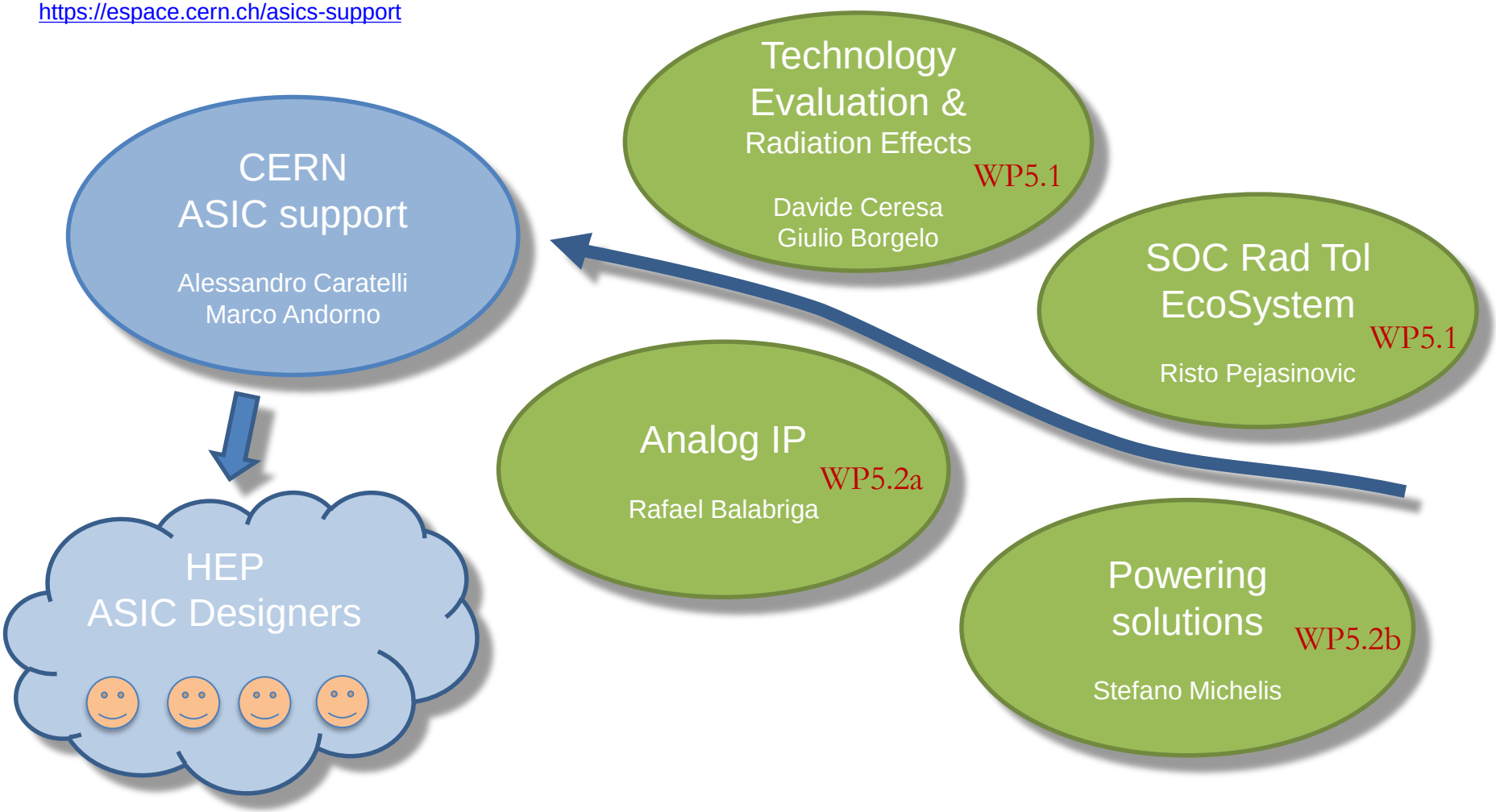
- Activity 5.2: Design & IPs
  - 5.2a: Analog IP blocks
    - Hard IP block development
  - 5.2b: Powering Solutions
    - High Efficiency DC/DC converters and power management

Resources 2020-21

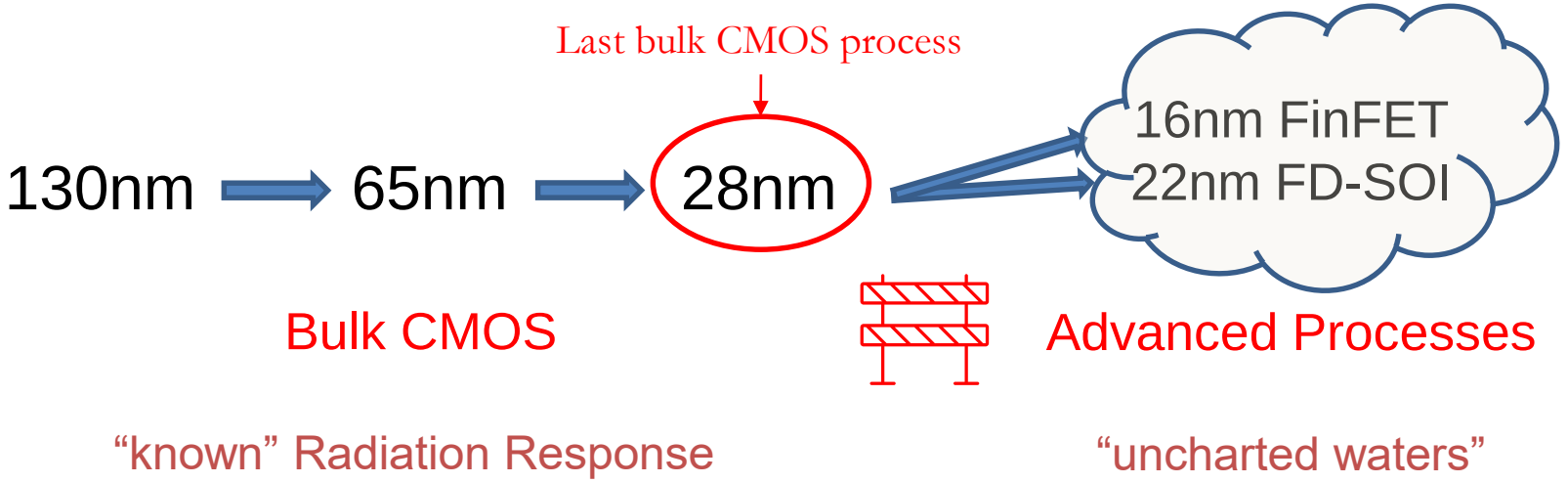
- WP5.1
  - Kostas Kloukinas *(Staff)*
  - Davide Ceresa *(Staff)*
  - *Giulio Borghello (Staff)*
  - Risto Pejasinovic *(Fellow)*
  - Georgios Athanasoulas *(Tech. Student)*
- WP5.2a
  - Rafael Ballabriga *(Staff)*
  - *Jan Kaplon (Staff)*
  - Markus Piller (*Doct. Student*)
  - Franco Bandi *(Fellow)*
- WP5.2b
  - Stefano Michelis *(Staff)*
  - *Giacomo Ripamonti (Fellow, non-WP funding)*
  - Pablo Antoszczuk *(Fellow)*
  - Mattia Balutto *(Tech. Student)*
- CERN ASIC Support
  - *Alessandro Caratelli (Staff)*
  - *Marco Andorno (Fellow, non-WP funding)*

WP5 "workgroups"

Synergy with CERN ASIC support & foundry services
https://espace.cern.ch/asics-support

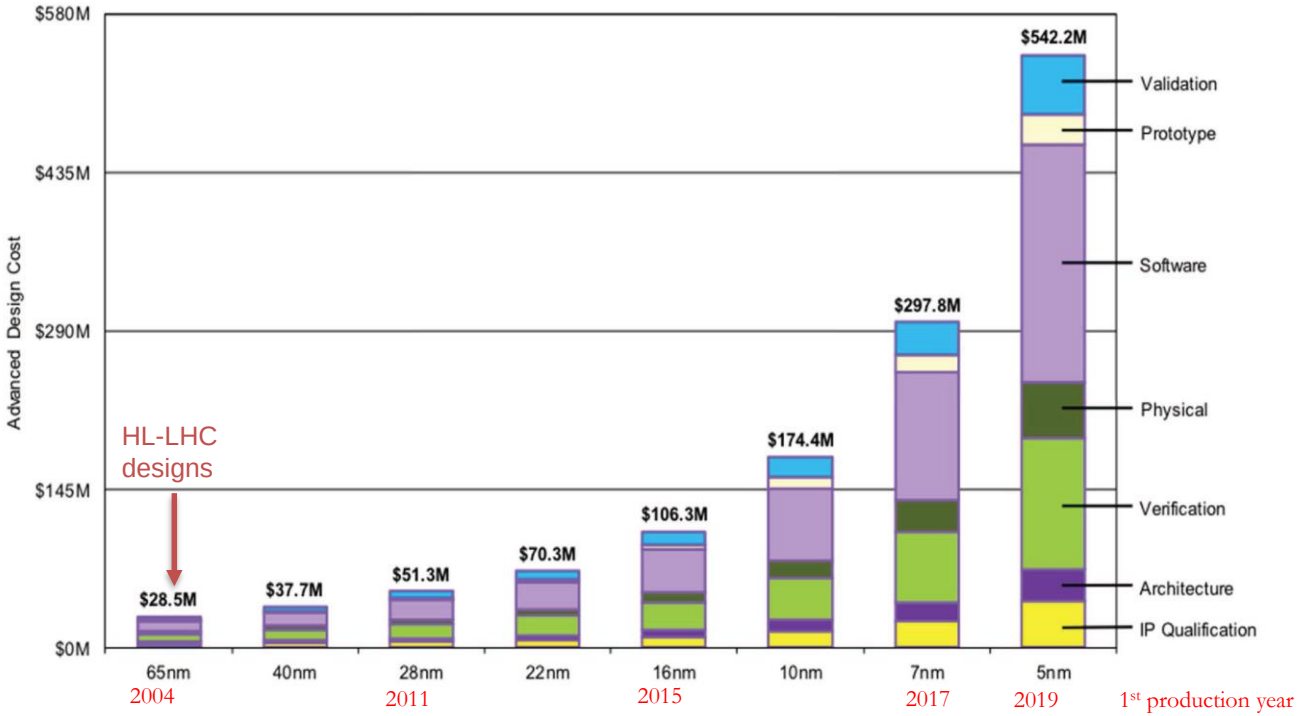


WP5.1 Technology Survey



- Survey criteria
  - Radiation performance — High TID (~1GRad)
  - Accessibility (availability of frequent MPW runs)
  - Long-term availability
  - Technical support
  - Cost

ASIC development costs



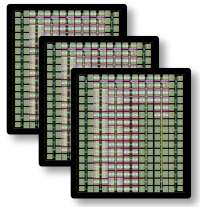
Chip Design and Manufacturing Cost under Different Process Nodes: Data Source from IBS*

- Escalating design development costs
- Techno-economic constraints associated with the use of Ultra Deep Submicron technologies

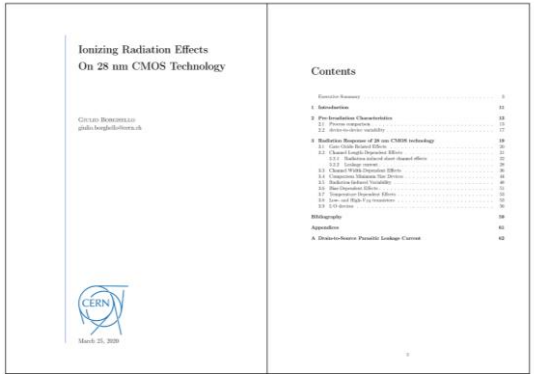
WP5.1 Technology Survey

- Three processes evaluated for TID radiation tolerance
  - 28nm bulk CMOS processes
    - Foundry A (one variant, Low Power)
    - Foundry B (two variants, High Performance, Low Power)
  - 22nm CMOS FD-SOI process
    - Foundry A

Prototyped & irradiated test chips



- Selected a 28nm bulk CMOS technology as the mainstream process for future Rad-Tol designs
  - High-k gate oxide is not a problem
  - Lower degradation than 65nm
  - Short transistors are more radiation hard

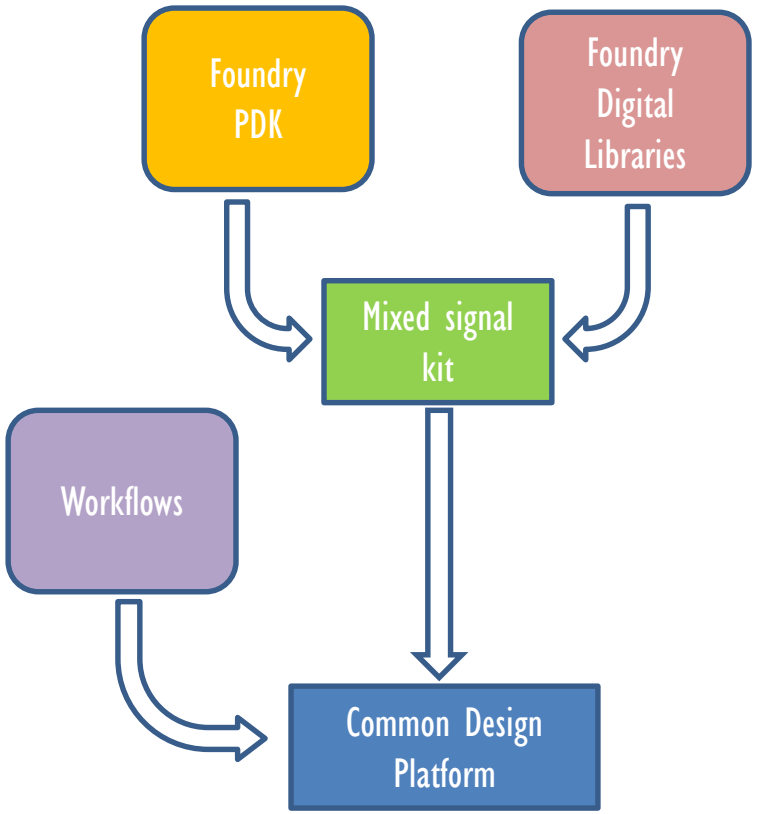

Ionizing Radiation Effects
On 28 nm CMOS Technology

Contents

  - Test results by Giulio Borghello on https://indico.cern.ch/event/973925/
  - TID Studies on Advanced Technologies (FinFET) will continue

28nm Common Design Platform

- Common Design Platform:
  - Support collaborative work of distributed design teams
  - Optimize efforts to integrate a “design environment”
  - Avoid incompatibilities
- 28nm Mixed Signal Kit:
  - Foundry PDK
  - Digital libraries with physical views
- Design Workflows
  - Analog, Digital and Mixed-Signal designs
  - Validated workflows
  - EDA Platform: Cadence Virtuoso/Genus/Innovus
- Developed by
  - CERN ASIC Support Team
    in collaboration with Cadence VCAD Design Services



CERN ASIC support Team
Alessandro Caratelli
Marco Andorno

SOC design Platform

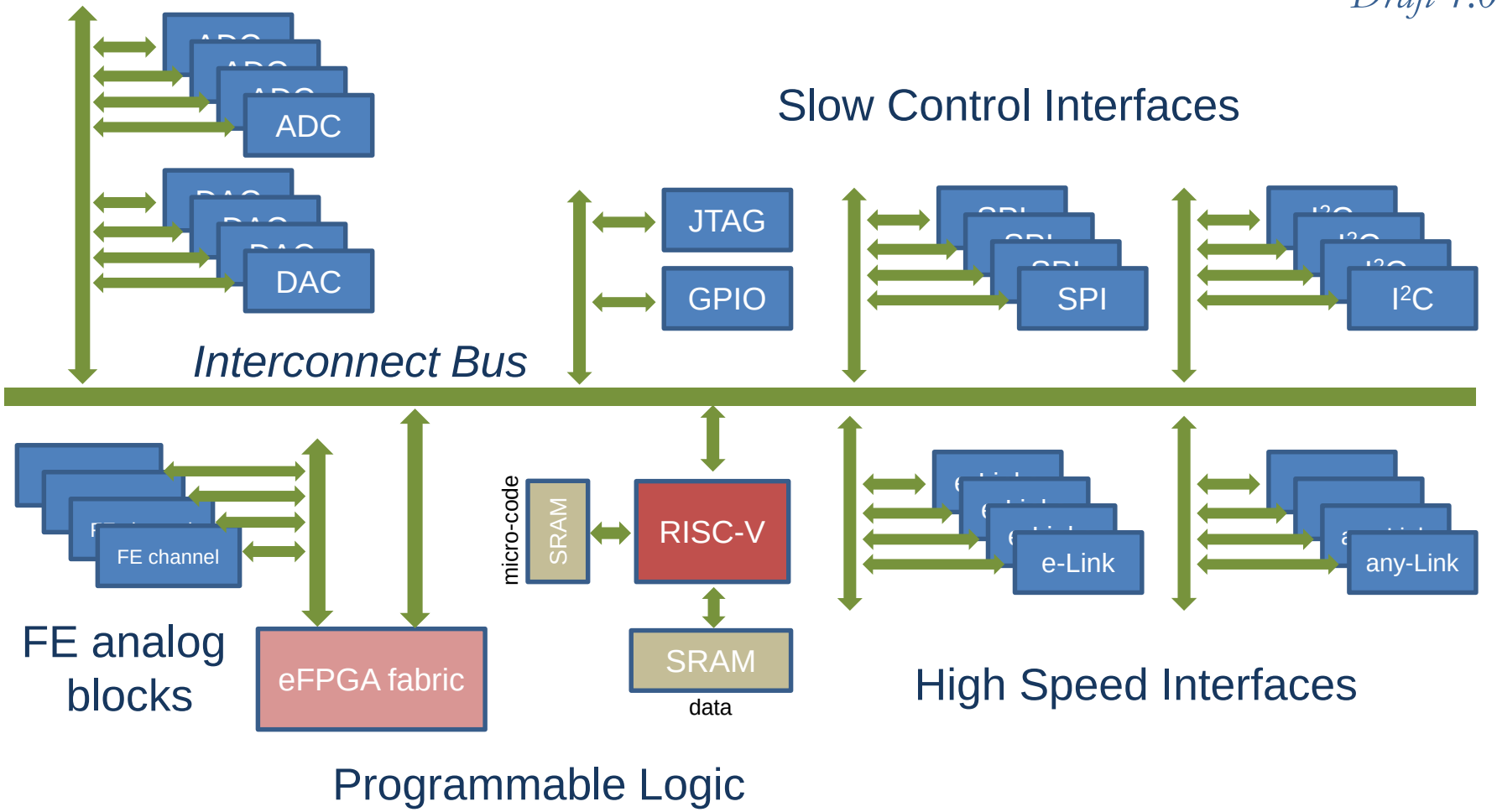
- Motivation
  - Meet the challenges of future FE ASIC designs
  - Introduce a more abstract design methodology
  - Reduce Design and Verification phases

- Proposed solution
  - Complement the Common Design Platform with an SoC Design Platform
  - Define standardized interconnects for IP blocks
    - Develop IP blocks that adhere to a standard
    - Facilitate Hierarchical digital Implementation and Verification
    - IP blocks accompanied by Verification IP code
  - Programmable, flexible logic (core processor, eFPGA)
  - Employ Radiation Tolerant design techniques

SoC Radiation Tolerant Ecosystem

Conceptual Scheme

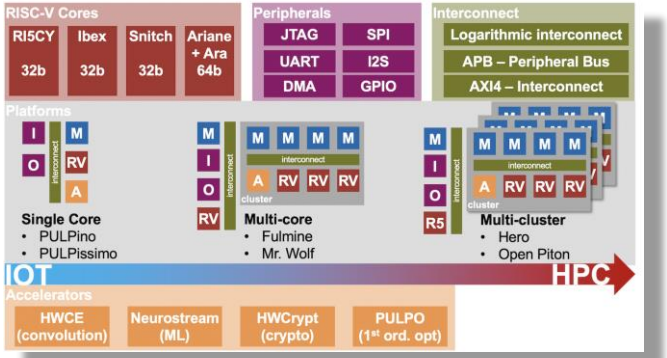
Draft 1.0



SoC partners

- Surveyed *open source hardware RISC-V*
  - Selected the PULP Platform

- ETH-Zurich
  - Parallel Ultra Low Power (PULP) Platform
  - Open-source RISC-V architecture
  - PULP team ….https://pulp-platform.org/team.html
  - Regular meetings and technical support



- KU Leuven University (Belgium)
  - High-Performance fault-tolerant RISC-V microprocessors for harsh environments
  - Fault tolerance systolic array Deep Neural Network (DNN) accelerator
  - Established bi-weekly meetings

KU LEUVEN

Team leader: Prof. Jeffrey Prinzie (jeffrey.prinzie@kuleuven.be)
Principal researchers: Karel Appels, Mohamed Mounir, and Naïn Jonckers

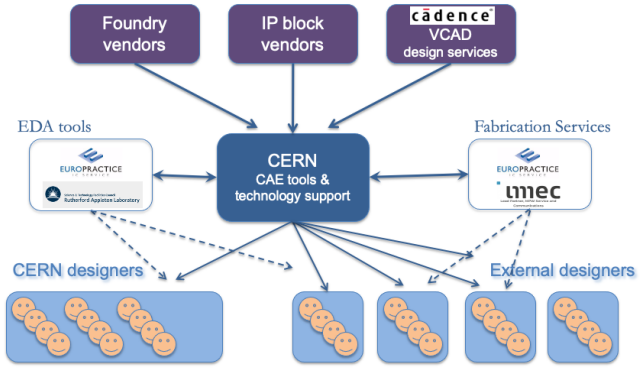
Collaborative Framework

- Commercial frame contract
  - CERN has a frame contract that allows small-scale prototyping (MPWs)
  - It will be extended to cover full maskset engineering and production works
  - The frame contract is accessible by HEP Institutes and Universities, via CERN

- NDAs
  - Special 3-way NDA that permit collaborative work
    - Permit the exchange of designs and technical data among collaborators
    - Europractice IC services (IMEC) helped greatly the negotiations with the Foundry
    - CERN has recently signed the 3-way NDA
    - Institutes will soon be invited to sign the 3-way NDA and access the Common Design Platform
  - Compliance with EDA tool vendors design sharing agreements
    - In coordination with Europractice EDA tools service

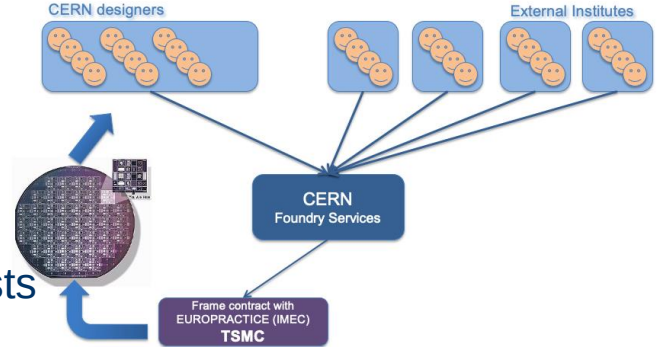
Collaborative Framework

- CERN aims to provide to the HEP community
  - ASIC design support Services
    - Common Design Platform
    - Rad-Tol IP blocks & SoC EcoSystem
    - Maintenance
    - Technical support
    - Training



asic.support@cern.ch

  - Foundry access services
    - Via IMEC-Europractice service
    - Prototyping on scheduled MPWs runs
    - Dedicated Engineering and production runs
    - Cost effective solution by sharing prototyping costs and benefiting preferential budgeted prices



foundry.services@cern.ch

The "28nm Forum"

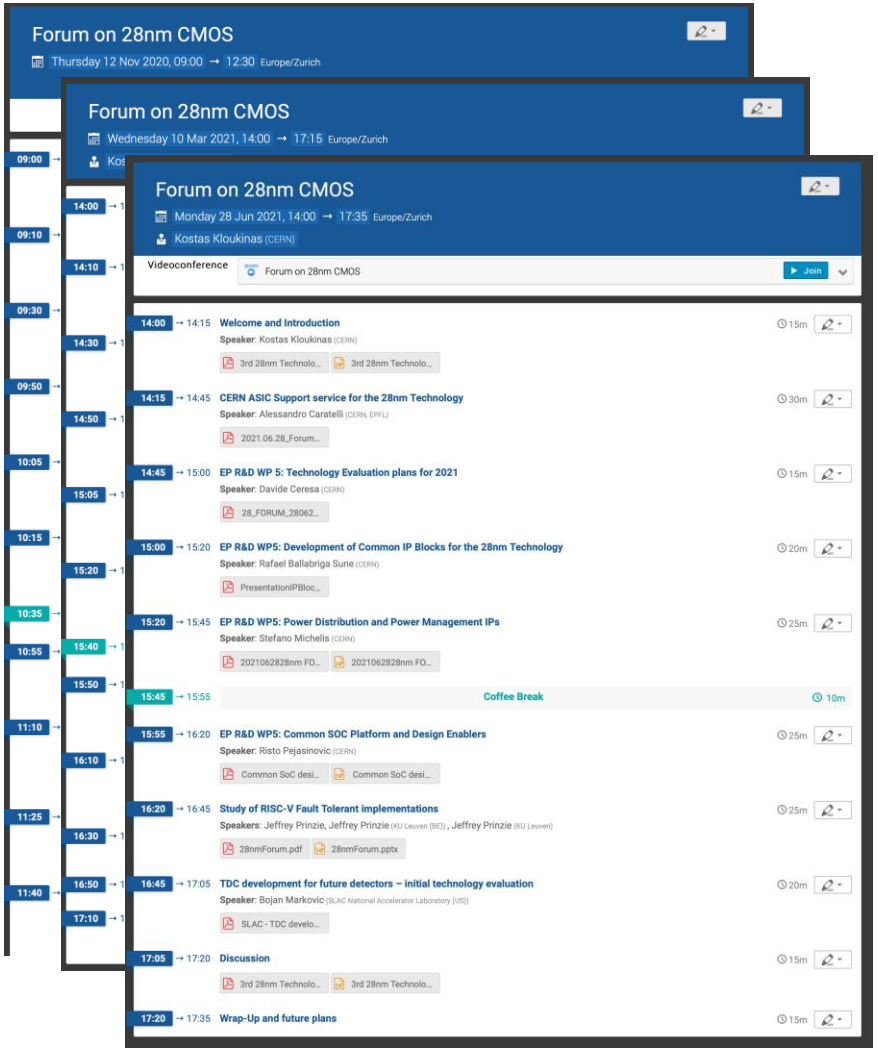
- Purpose of the 28nm Forum
  - CERN to communicate the EP R&D WP5 activities
  - Institutes to present their developments and future plans
  - Identify synergies
  - Establish collaborations

28nm Technology Forum Sessions

1st session (Nov. 12, 2020) https://indico.cern.ch/event/970389/
2nd session (Mar. 10, 2021) https://indico.cern.ch/event/1009040/
3rd session (July 28, 2021) https://indico.cern.ch/event/1042567/
4th session proposed for **Q1 2022**

established periodicity: 3 times per Year

- Restricted access; requires registration
- Self-inscribed CERN e-group: **28nm-Forum@cern.ch**



WP5.1: TECHNOLOGY EVALUATION

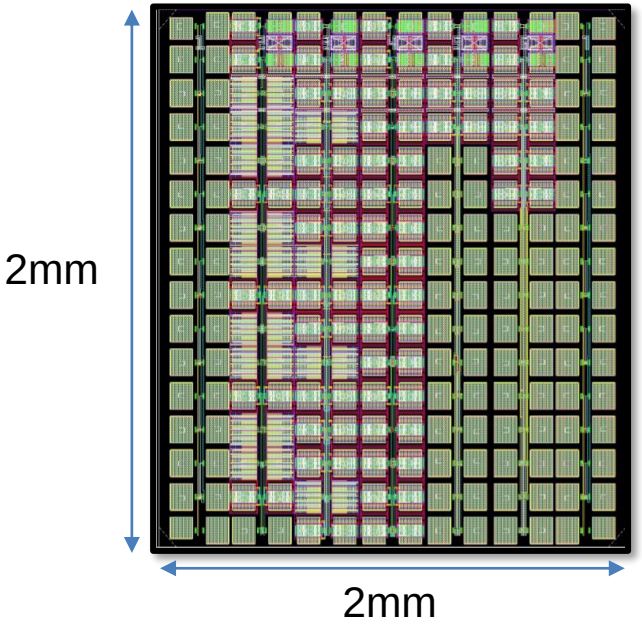
Davide Ceresa

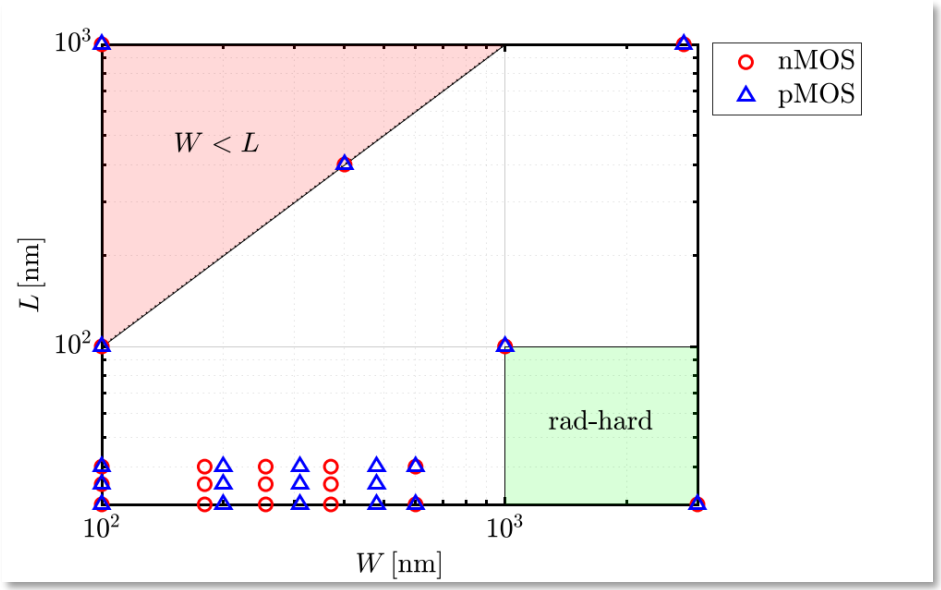
WP5.2A: ANALOG IP BLOCKS

Davide Ceresa on behalf of Rafael Balabriga

TID chip in HPC+

- TID (Total Ionizing Dose) chip
  - Study cumulative radiation effect on single transistors
  - Design ported from HPC version
  - Submission done on mini-@sic run of June 23rd

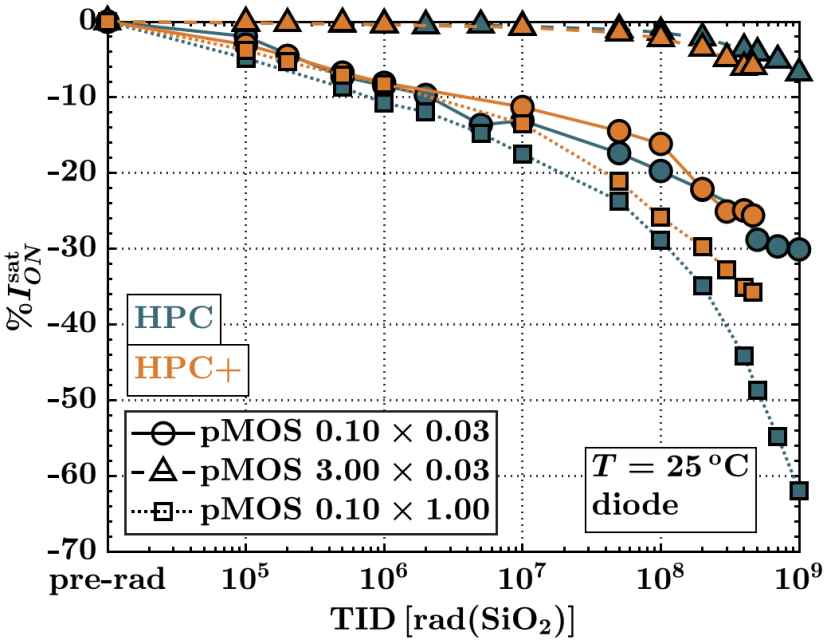




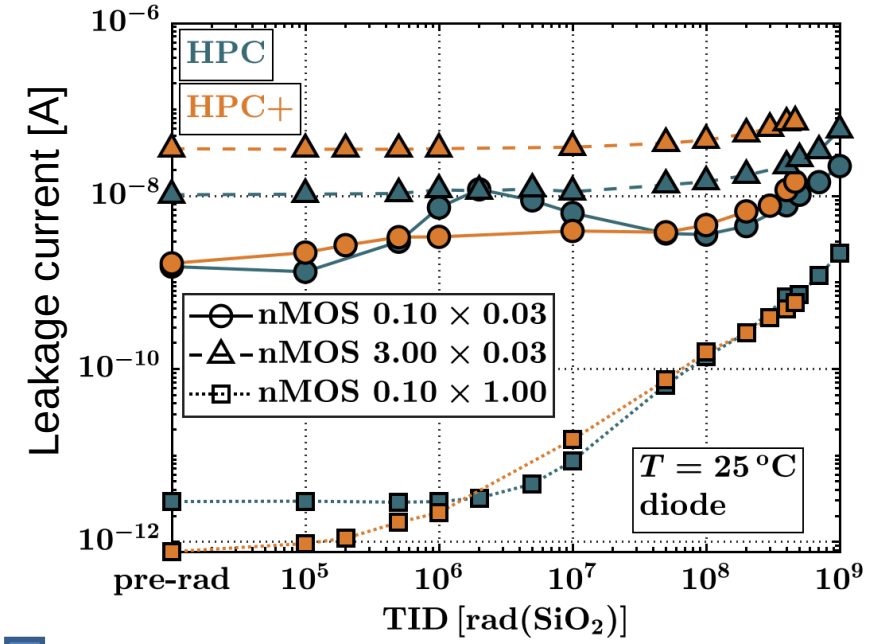
TID chip preliminary results

WP 5 EP R&D

Saturation current in PMOS transistor



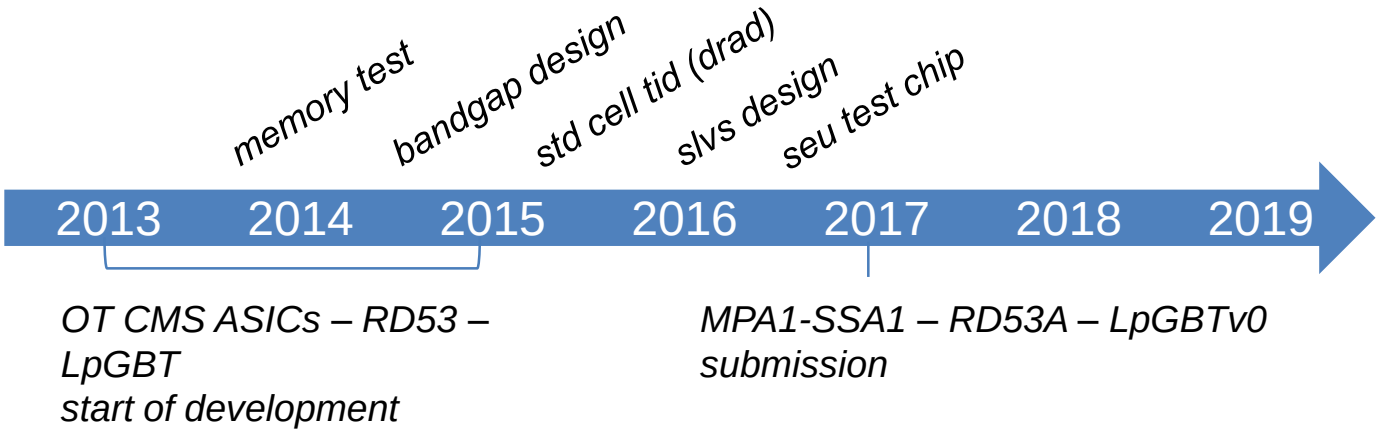
Leakage current in NMOS transistor



Preliminary results very similar to HPC flavor

Next activities: EXP28

65 nm tech. Evaluation and macro block was done during large chip design:

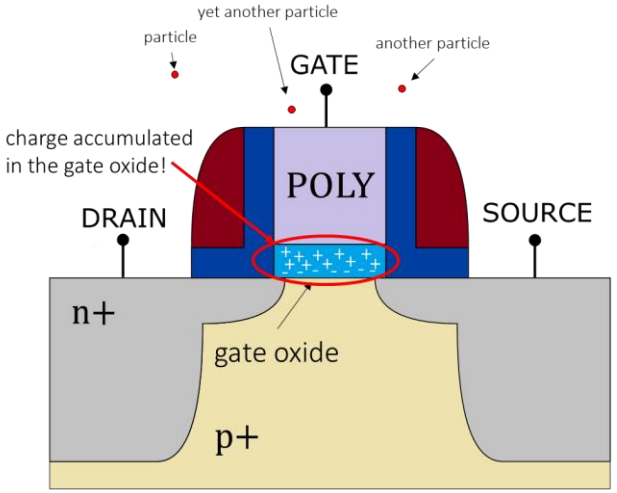


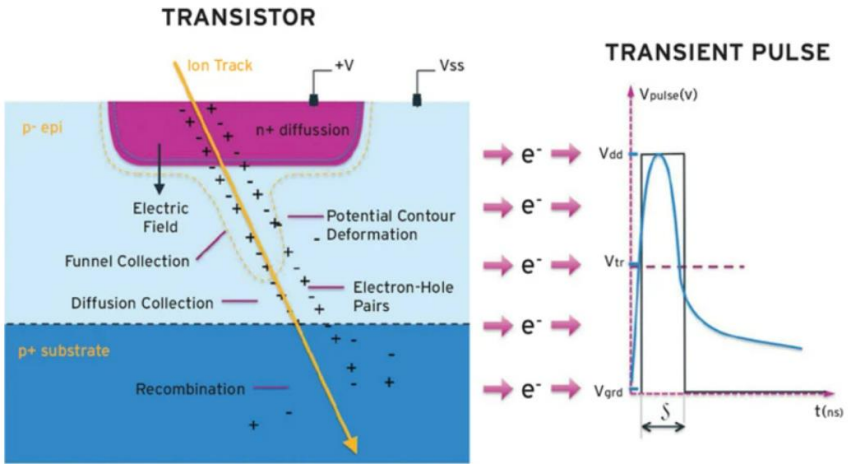
Develop a test chip family to explore and experience with the 28 nm technology

- Completed before large project starts
- Fulfil needs of the different applications
- Be reusable

EXP28 TEST CHIP FAMILY

Next activities: EXP28





Total ionizing dose (TID) and single event effect (SEE) on different circuitries:

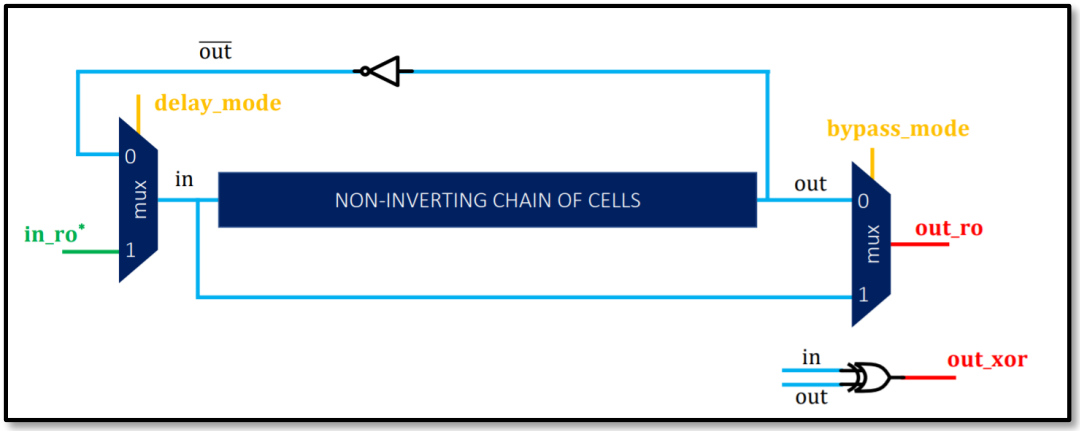
- Foundry Standard cell libraries
- Foundry memory compiler
- IP blocks
- Rad-Tol ESD protection
- Rad-Tol I/O pads

Outsourced to SOFICS

Provide basic building block and design guidelines for 28nm design

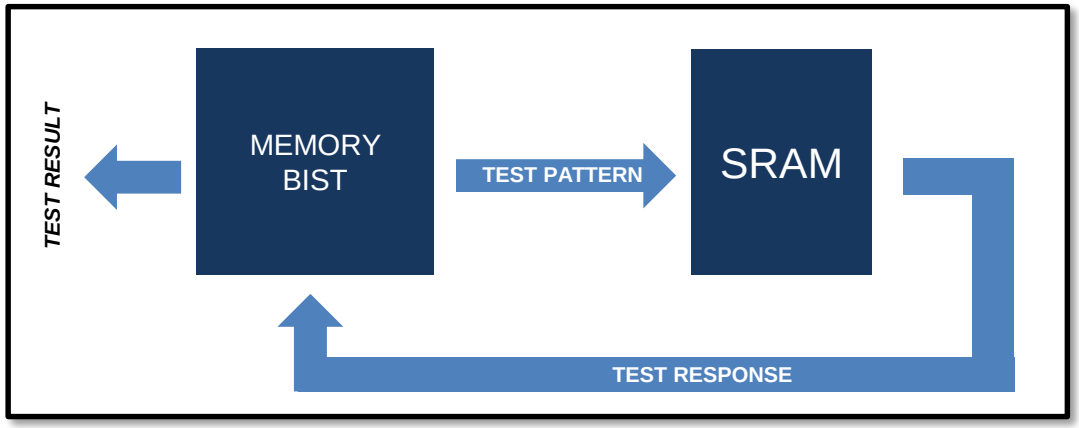
TID effect on digital logic

RING OSCILLATOR FOR STANDARD CELL TID DEGRADATION



- Degradation measured as variation of frequency in a ring-oscillator
- Un-balancing between rise and falling time measuread with a delay chain

BUILT-IN-SELF-TEST (BIST) FOR SRAM TID DEGRADATION



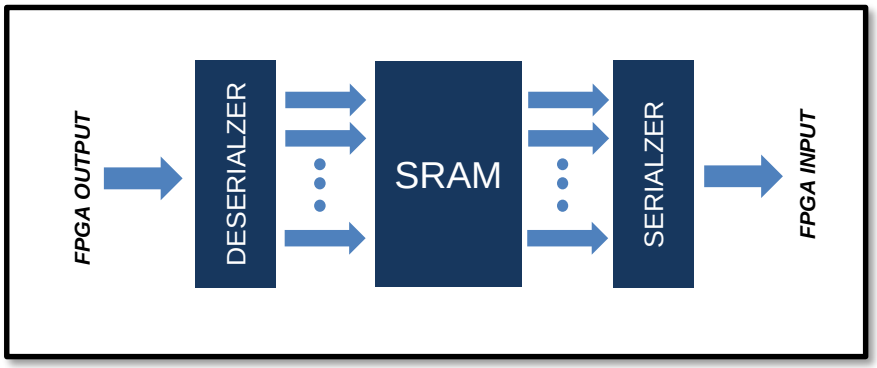
- BIST required to cope with high speed memory (access time ~ few ns)
- Foundry memory includes sub-minimum transistor size
- Different type of memory tested (single/dual port, standard/ultra-high density)

SEE effect on digital logic

SIHIFT REGISTER FOR STANDARD CELL SEU STUDY

- Cross-section of single and multi-bit upset
- Minimum distance for avoiding multi-bit upset
- Different type of standard cells

SER/DES FOR SRAM SEU STUDY



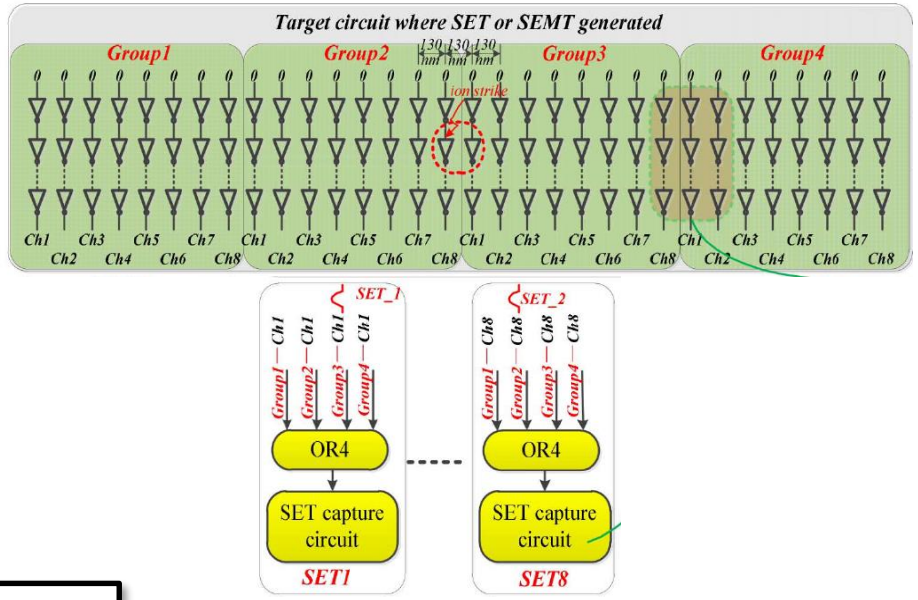
- Direct access to the memory for functional and SEU testing.
- Limited number of pads: Ser/Des logic
- Maximize sensitive area: multiple instantiation

SEE effect on digital logic

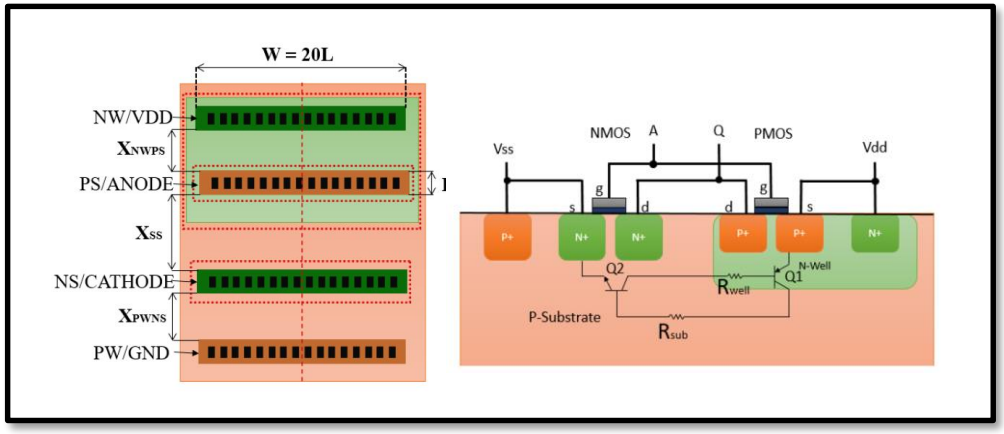
WP 5 R&D

SET DETECTOR FOR STANDARD CELL SET STUDY

- Cross-section for single and multiple transient
- Transient length vs LET particle
- Fully digital implementation
- Based on Vernier detector



PNPN TEST STRUCTUR FOR SEL STUDY



- Evaluate minimum distance between substrate contact
- Requires per cell power measurement
- With and without deep n-well

EXP28 test-chips submission

- TID CHIP
  - RING OSCILLATOR – *main designer G. Borghello*
  - SRAM BIST – *RTL designer G. Bergamin*
- SEE CHIP
  - SRAM SER/DES - *RTL designer G. Bergamin*
  - SEU SHIFT REGISTER
- MIX CHIP
  - SET VERNIER DETECTOR
  - SEL TEST STRUCTURE
  - IP BLOCKS

28 NM MPW SUBMISSION

RESERVED FOR THE

16th OF DECEMBER

Objectives IP Blocks Activity

- Build experience in the selected technology by designing and characterizing IP blocks that will be used in more complex HEP chips

- Disseminating results and provide guidelines to designers. Actions:
  - Write documentation with available components in the technology (MOS transistors, capacitors, resistors, characteristics of the metal stack) and design guidelines (F. Bandi, M. Piller)
  - Create a tool for assisting analog designers on transistor sizing in a systematic way using the gm/id methodology (F. Bandi, M. Piller)
  - Create technical meetings to share information between designers (start in 2022)

- A part from the shared IP blocks, other circuits will be designed in 28nm CMOS in collaboration with other projects or Work Packages (proprietary blocks)

Design of IP (shared) blocks

ON CHIP REFERENCES	
Bandgap voltage reference, Temperature monitor	Collaboration with Bergamo, Submission December 2021
CONVERTERS	
Digital to Analog Converter for biasing	M. Piller (DOCT), Submission December 2021
Analog to Digital Converter for monitoring	Design start Q1 2022*
OPERATIONAL AMPLIFIERS	
Rail to Rail Operational Amplifier (fast)	J. Kaplon (STAFF), Submission 2022
Rail to Rail Operational Amplifier (slow (e.g. monitoring in unity gain configuration))	M. Piller (DOCT), Submission December 2021
DATA TRANSMISSION	
Differential line drivers/receivers	F. Bandi (FELL), Submission December 2021
PLL	
Analog	F. Bandi (FELL), Design start January 2021
Digital	Design start Q2-Q3 2022*

*Second Fellow on IP blocks starts Q1 2022

Design of proprietary blocks

- Front-end circuits
  - Amplification, filtering and discrimination (A/D conversion) for 2-D readout circuits. (Charge sensitive amplifier, shaper and comparator for sensors with input capacitance <100fF and leakage current per pixel <20nA)
  - Collaboration with WP1.1 Hybrid Pixel Detectors (V. Sriskaran (Fellow)) in view of precise timing front ends

- Input stage and discrimination for the readout of detectors with intrinsic amplification for timing layers (SiPMs, MCPs) (M. Piller's PhD. thesis)

- The lessons learnt will be shared with the HEP community through the documentation or through other IP blocks generated (e.g. DACs, OpAmps, etc)

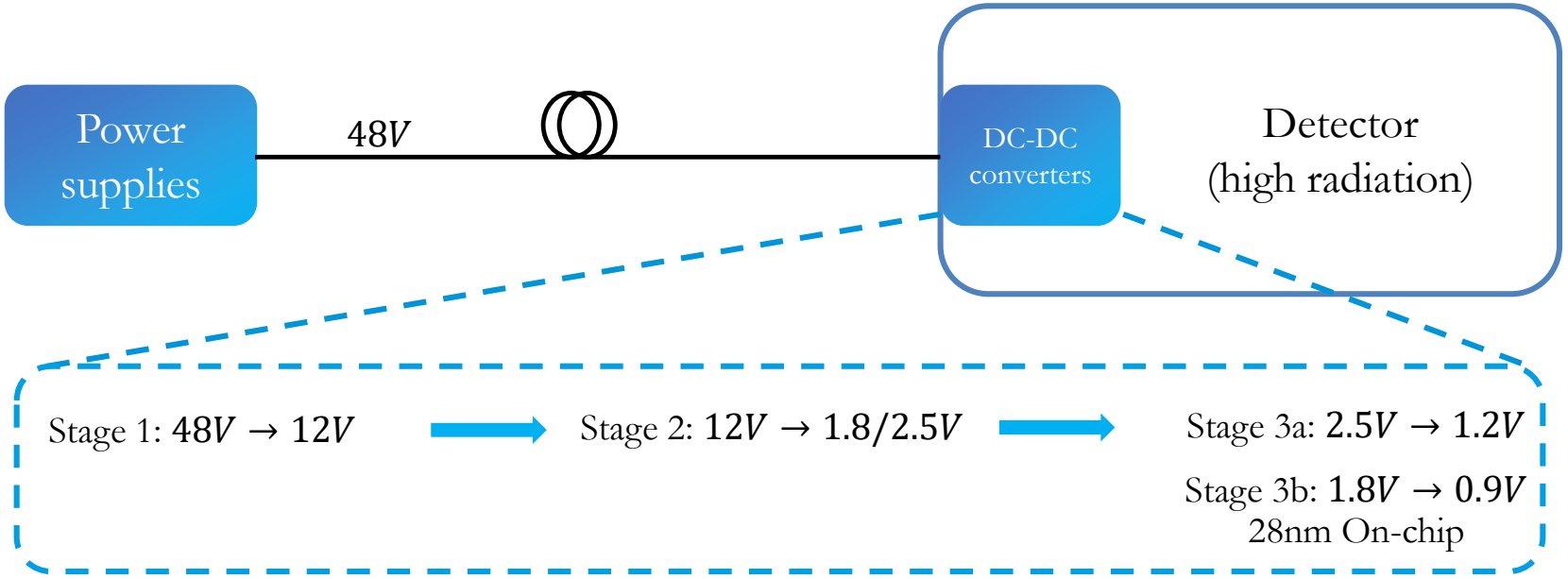
W5.2B: POWERING SOLUTIONS

Stefano Michelis

Power distribution in the HL-LHC experiments

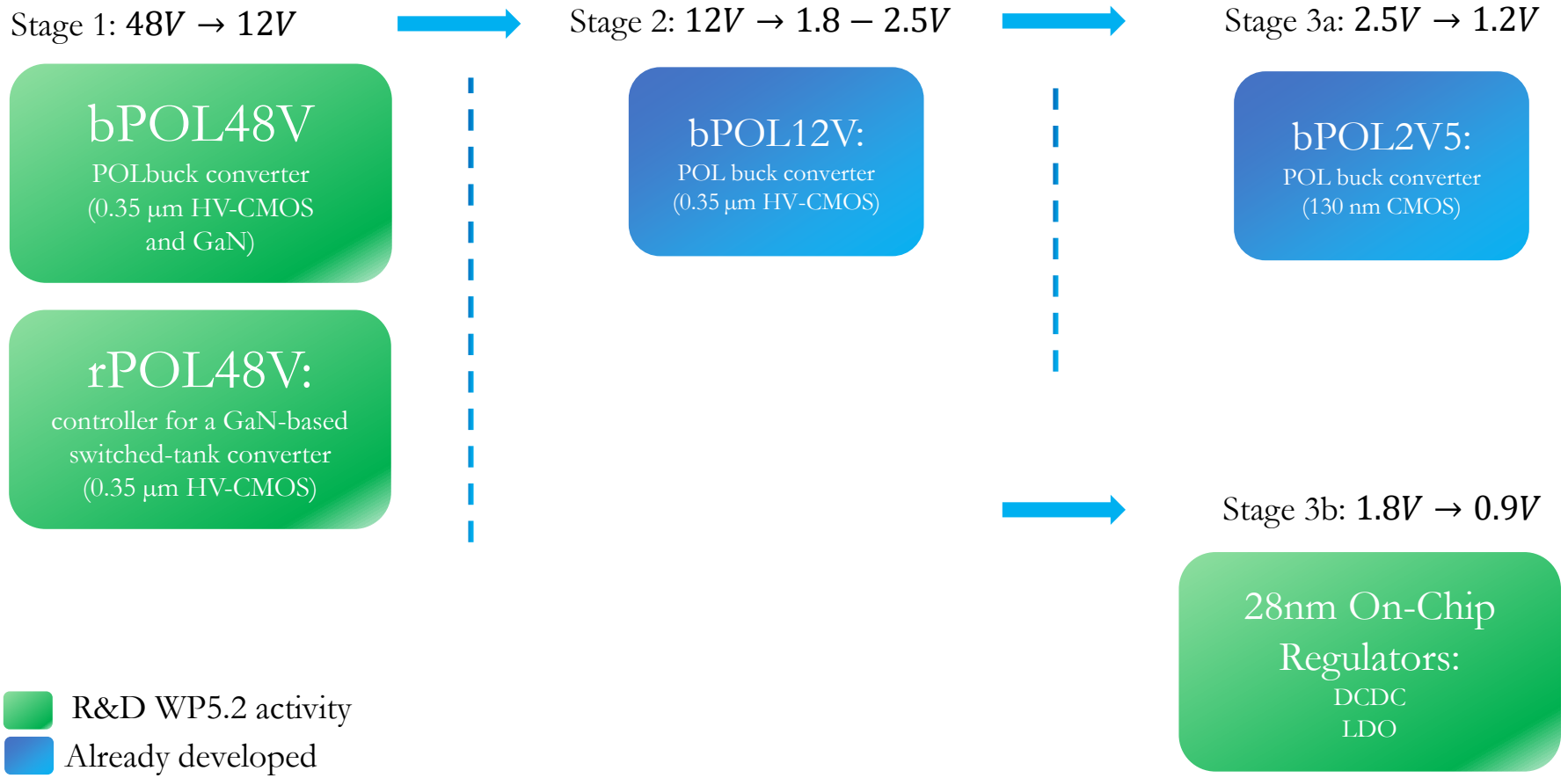
Radiation-tolerant DC-DC converters must be used to power the on-detector electronics in HEP experiments, in order to comply with the power consumption and material minimization requirements.

A power distribution system based on three stages of DC-to-DC conversion is proposed.



Power management ASICs: projects

WP 5 EP R&D

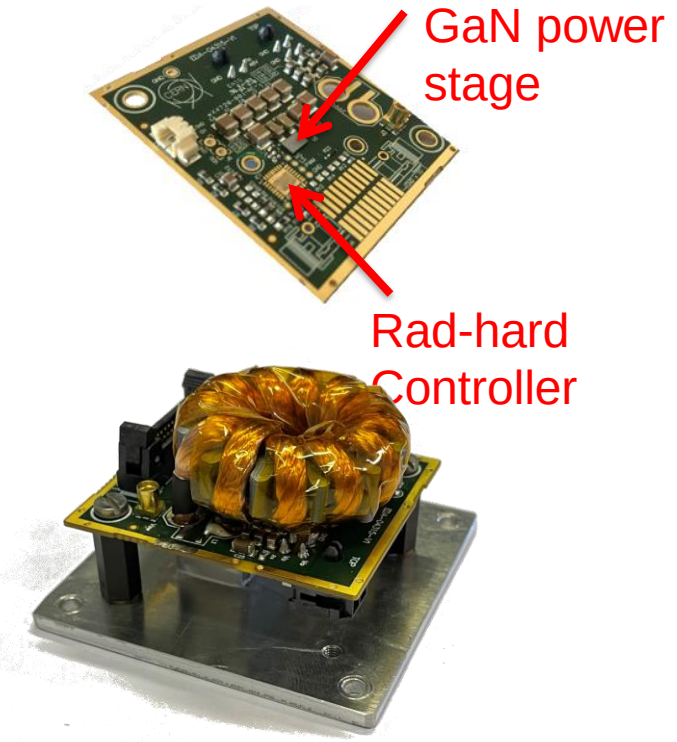


Stage1 R&D WP5.2
bPOL48V: 48V-input buck DC-DC converter

WP 5 EP R&D

bPOL48V is composed by a rad-hard controller designed by CERN and a Gallium Nitride (GaN) power stage, developed under WP5.2 R&D program.
The GaN ASIC is the EPC2152, a collaboration with EPC has been established for space applications

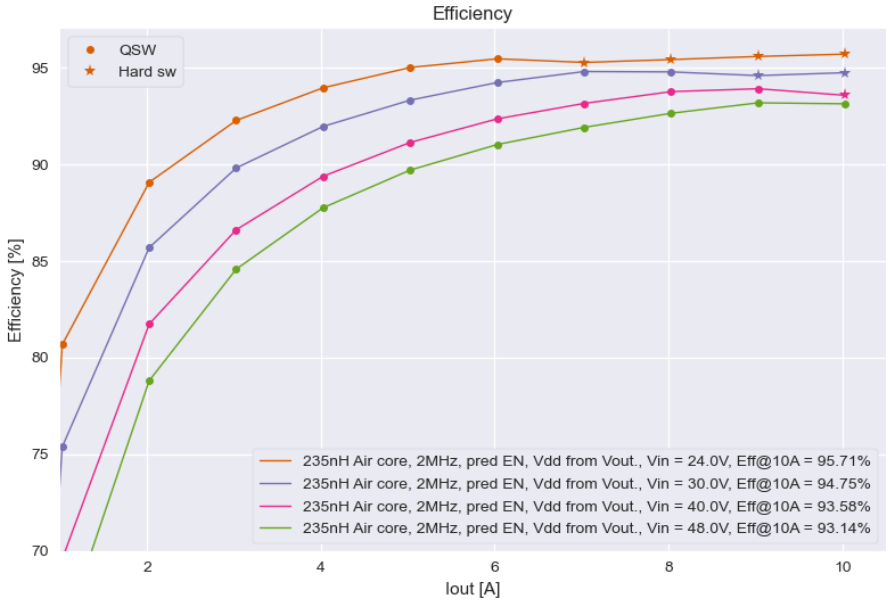
specs	Vin max	48V
	Typ Vout	12V
	Iout max	12A
Rad specs	TID max	50 Mrad
	SEE max	46 MeV/(mg/cm²)
	DD max	4e14 n/cm2 2.23e14 p/cm2(30MeV)
reliability	To be tested, Rack in construction	
Production	26000 dies in 2022	

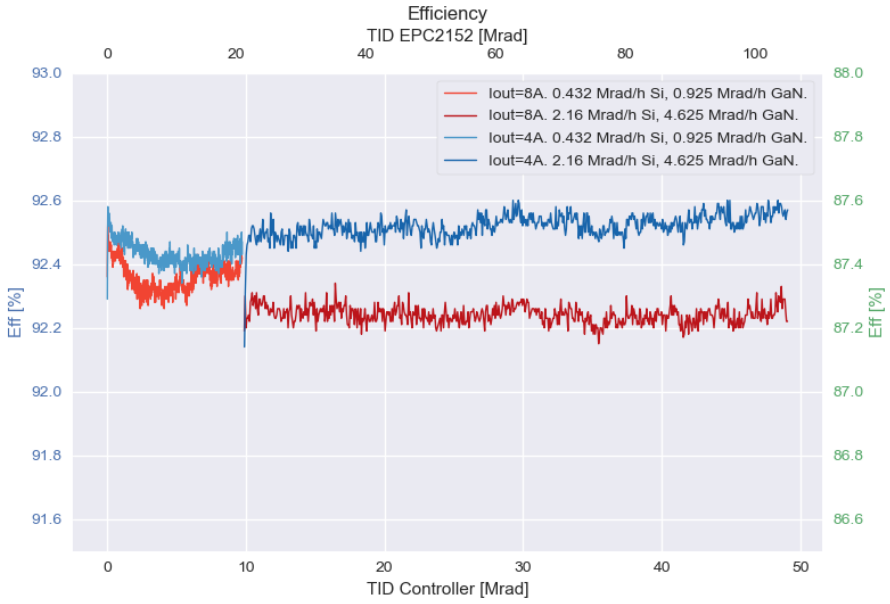


NB
TID=Total Ionizing Dose
SEE= Single Event Effect
DD= Displacment Damage

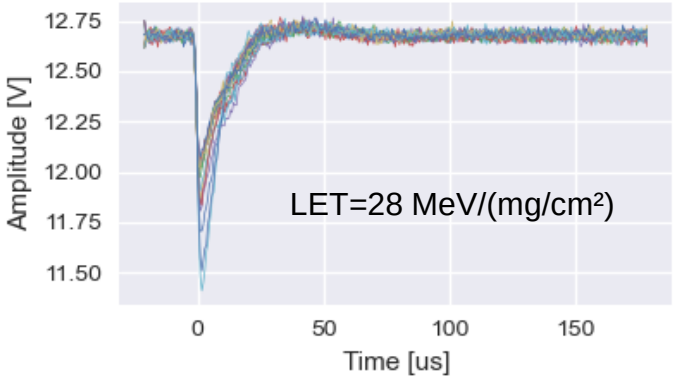
Design by S. Michelis, P. Antoszczuk (WP5.2 fellow)

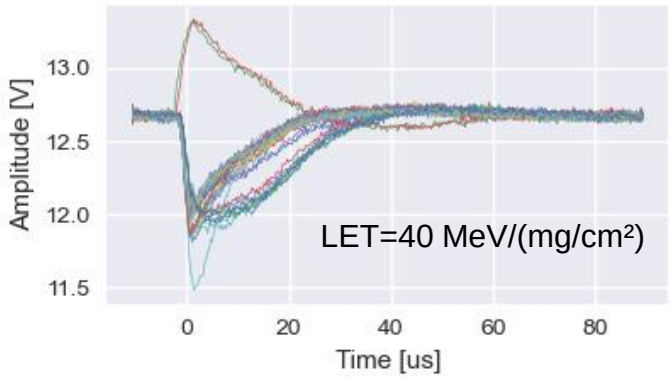
Stage1
bPOL48V: radiation testing





With V1, we went up to LET=40 MeV/(mg/cm²), only around 10% transients, Vin=48V



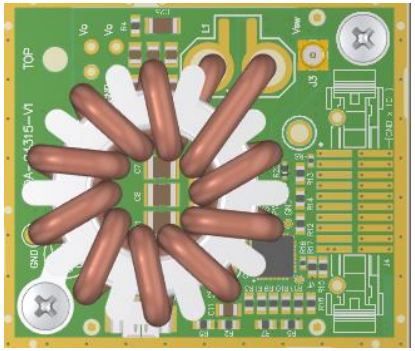


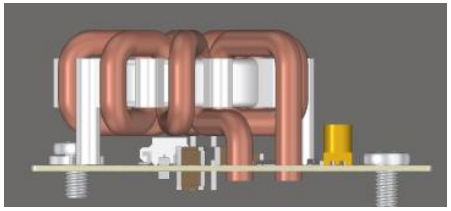
V2 is a slighty modified version to be able to go to LET=80 MeV/(mg/cm²) for space applications

Stage1 R&D WP5.2
rPOL12V: 48V-input Switched Tank Converter (STC)

rPOL48V is a WP5.2/KT-fund development in collaboration with University of Udine, aiming to a 30A very compact and efficient DCDC converter, fixed ratio 4.

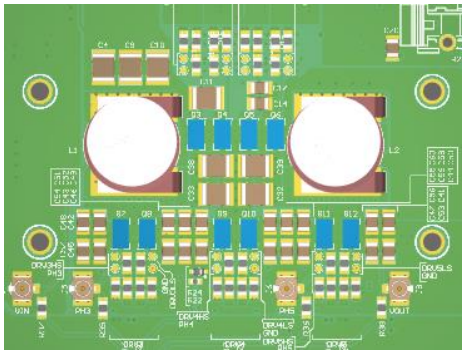
bPOL48V (buck)
production grade

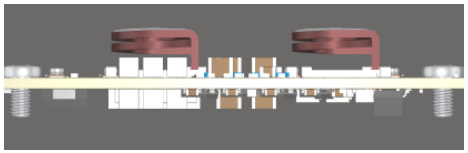




vs.

rPOL48V (resonant)





Design by Udine, G. Ripamonti and P. Antoszczuk (WP5.2 fellow)

Stage1and 2 R&D WP5.2 Technology characterization

Today the designs are in the following technologies

Stage1: 80V CMOS 0.35um (OnSemi I3T80)

Stage2: 25V CMOS 0.35um (OnSemi I3T25)

Stage3: 2.5V CMOS 0.13um

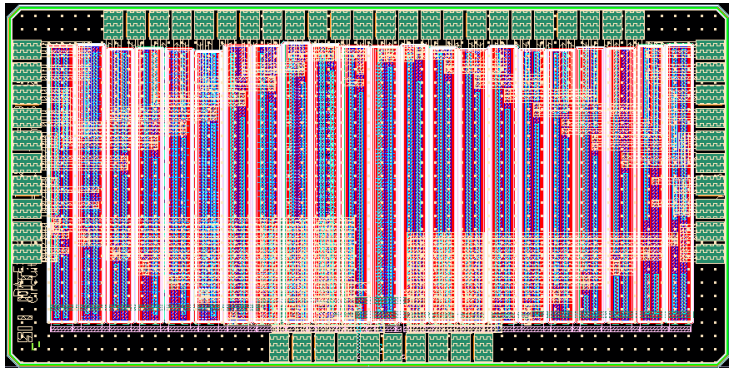
We are looking to possible substitute technlogies, in particular for the high voltage stages (1 & 2).

3 test chips have been submitted in May 2021 in the 0.18um I4T Onsemi technology (with 15V, 30V, 45V and 70V devices)

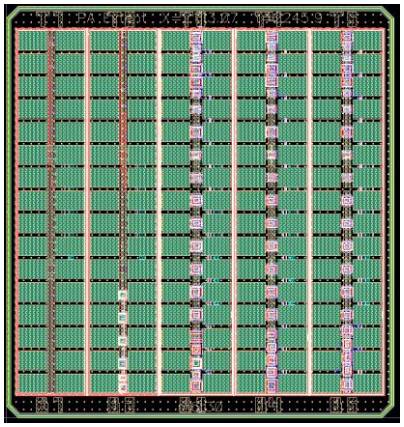
The testchips will be at CERN in Dec 2021 and caracterization will start (TID, DD and SEE).

In parallel, caracterization for other GaN technolgies is on-going.

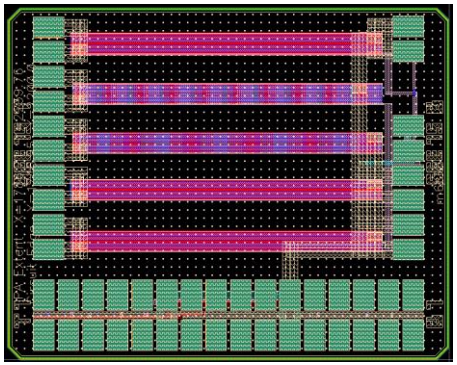
30V-45V-70V device SEE testchip



30V-45V-70V device TID testchip

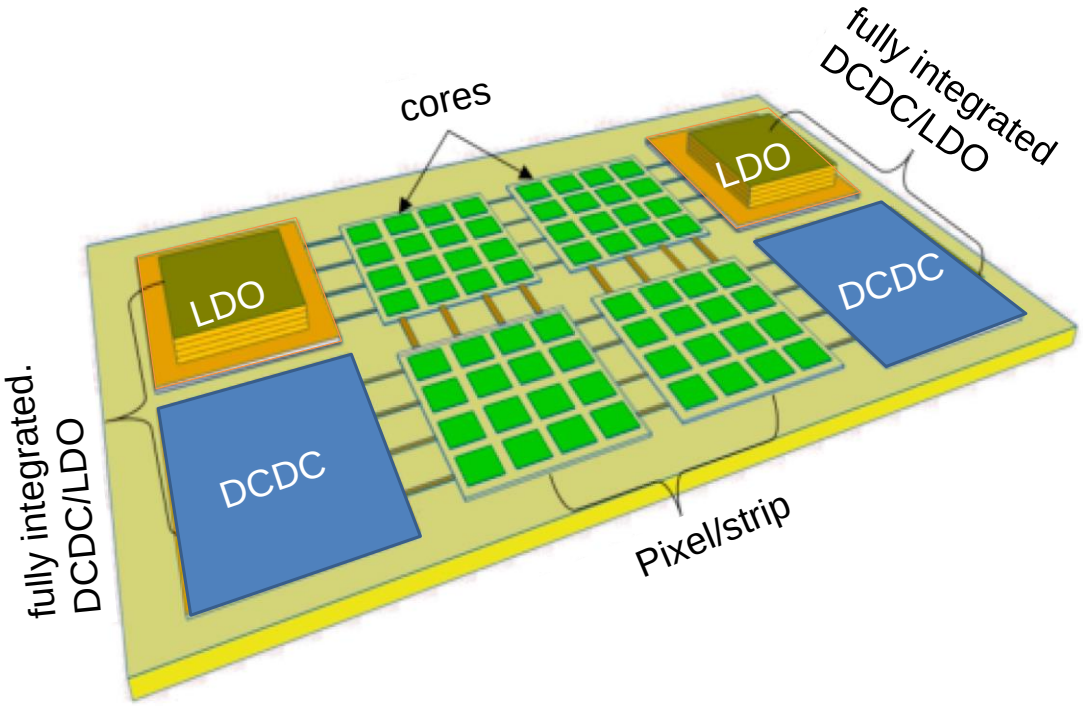


15V device TID&SEE testchip



Stage3b R&D WP5.2
28nm On-chip power management & voltage ref

We are looking at the possibility to design fully integrated Point of Load converter/regulator Macro-blocks to allow a localised power conversion and regulation. This will allow a more efficient power distribution and optimization of the voltage for each part of the circuit



Stage3b R&D WP5.2
28nm On-chip power management & voltage ref

In the R&D WP5.2 two collaborations with external institutes have been promoted for the design of Macro block in 28nm technology:

- University of Bergamo for the design of a rad-hard bandgap reference circuit (G. Traversi, L. Gaioni). First submission foreseen for December 2021

- Graz University of technology (TU Graz) for the design of rad-hard linear regulators and LDO in 28nm (A. Michalowska, Z. Dominik, N. Czepl).The goal is having a family of linear regulators with different Iout capability, Power on-off, programmable Vout.

CERN development:

- Since the R&D of the bPOL48V has been faster than foreseen, we are looking also in the design of fully integrated DCDC converter, ratio 2


Thank You