WP6: High Speed Links

CERN EP Department

R&D on experimental technologies

EP R&D Day 2021

11 – 12 November 2021

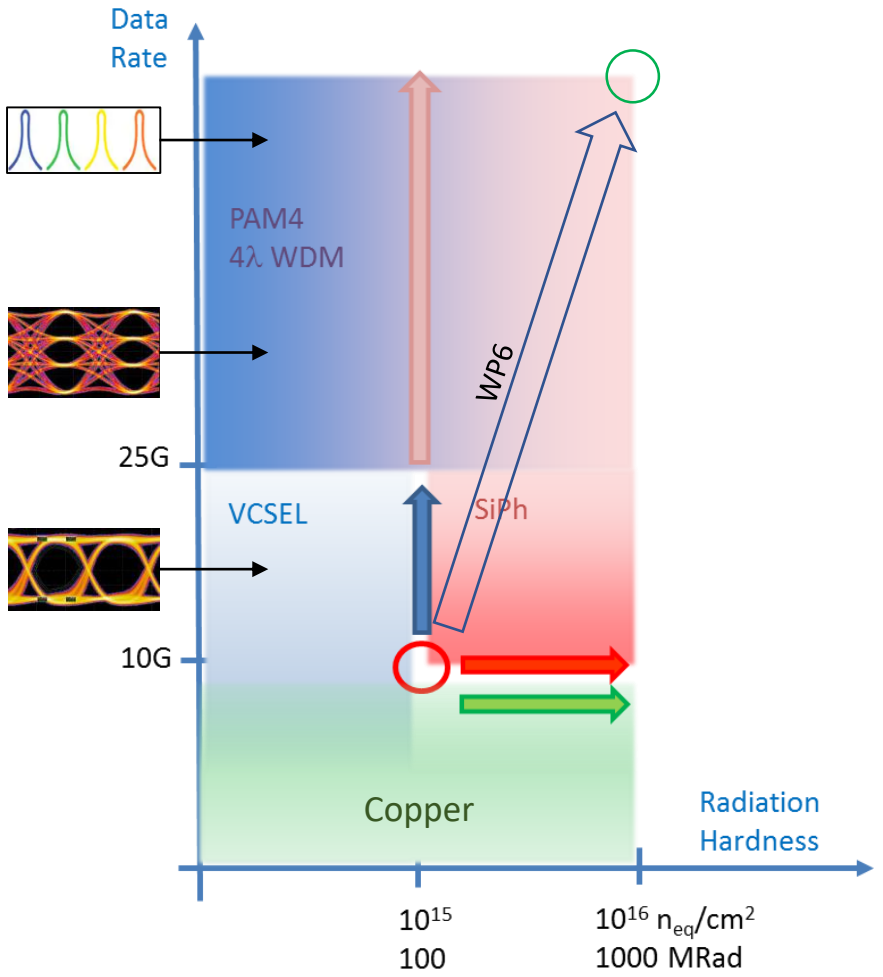
P. Moreira & C. Scarcella on behalf of the WP6 team

CERN
EP-ESE
Electronic Systems for Experiments

EP R&D

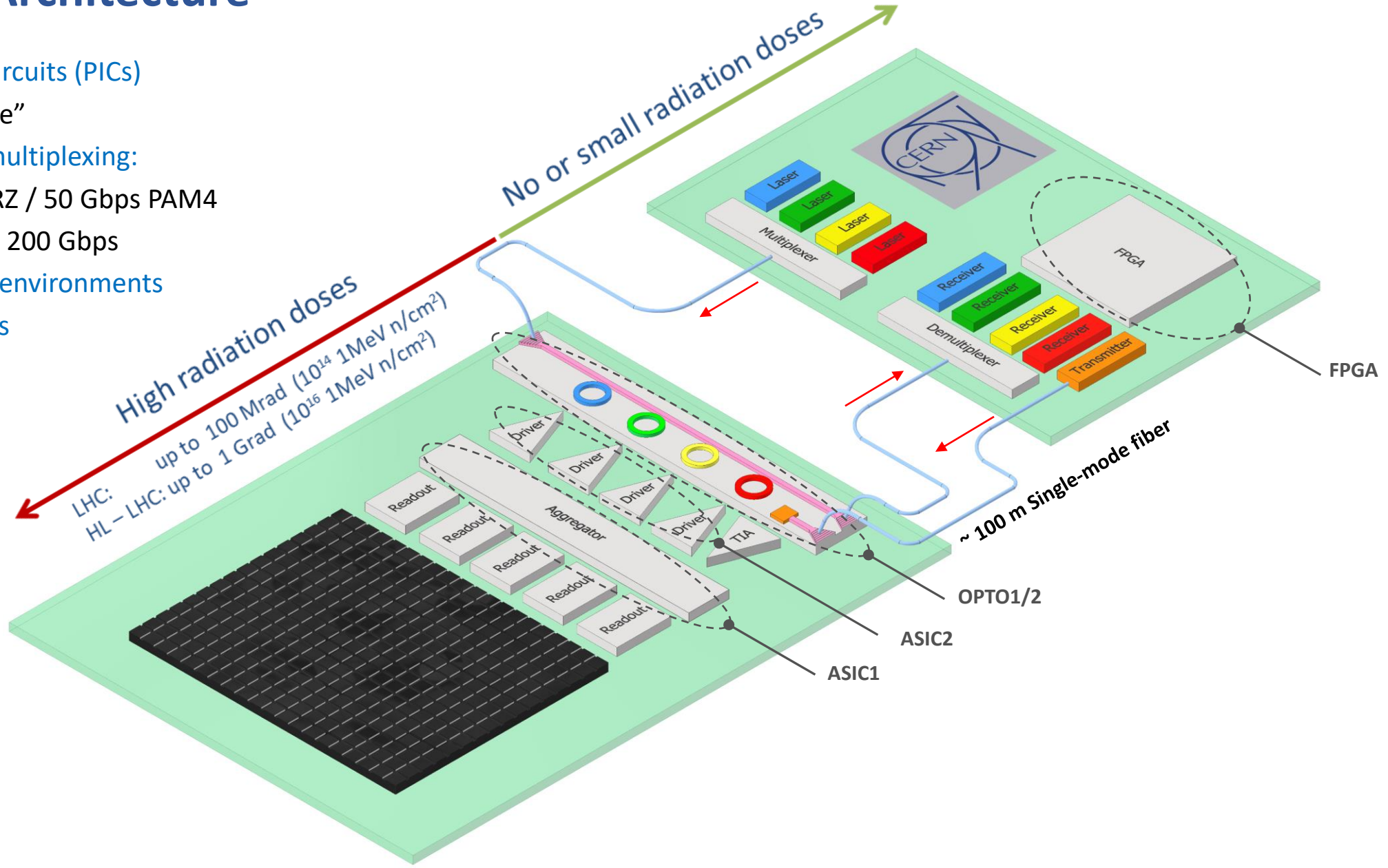
WP6 Goal

- **Provide the future HEP systems with:**
  - High bandwidths: ~50 Gbps / lane
  - High radiation tolerance
  - Low power
- **FPGAs**
  - Compatible with the state-of-the-art
- **ASICS**
  - Advanced technologies 28nm CMOS
  - High order modulation formats (PAM4)
  - Drivers for SiPh optoelectronics
- **Optoelectronics**
  - Silicon Photonics (SiPh)
  - External Modulators
    - Ring & MZ
  - Wavelength Division Multiplexing (WDM)

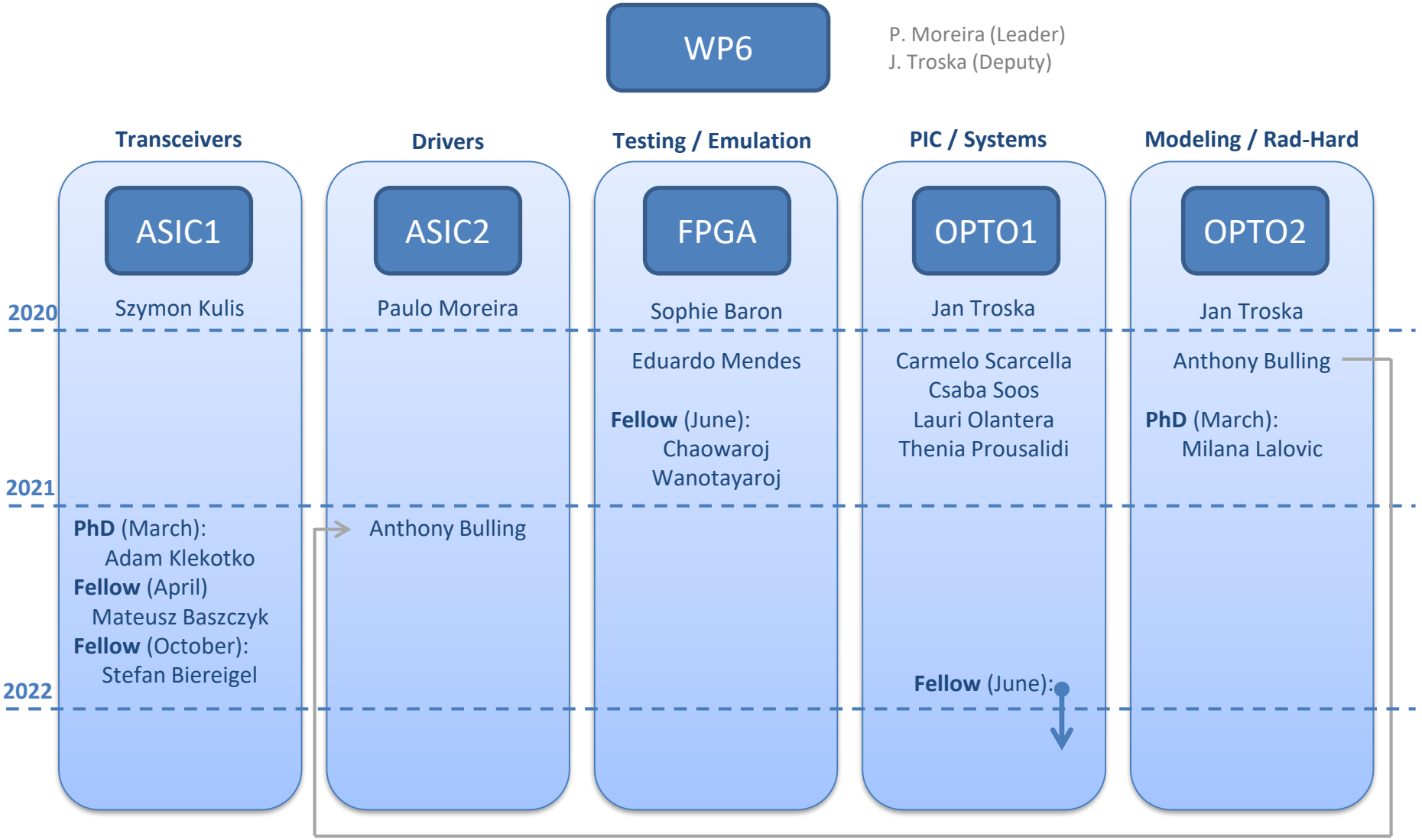


Future HEP Link Architecture

- Photonic Integrated Circuits (PICs)
  - RadHard “promise”
- Wavelength division multiplexing:
  - Lane: 25 Gbps NRZ / 50 Gbps PAM4
  - Fibre: 100 Gbps / 200 Gbps
- Laser out of radiation environments
- Low power / Low mass



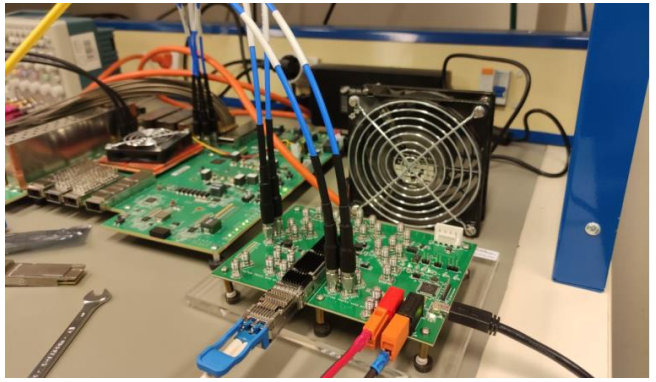
WP6 Life


WP6
P. Moreira (Leader)
J. Troska (Deputy)
Transceivers
Drivers
Testing / Emulation
PIC / Systems
Modeling / Rad-Hard
ASIC1
ASIC2
FPGA
OPTO1
OPTO2
2020
Szymon Kulis
Paulo Moreira
Sophie Baron
Eduardo Mendes
Fellow (June):
Chaowaroj Wanotayaroj
Jan Troska
Carmelo Scarcella
Csaba Soos
Lauri Olantera
Thenia Prousalidi
Jan Troska
Anthony Bulling
PhD (March):
Milana Lalovic
2021
PhD (March):
Adam Klekotko
Fellow (April)
Mateusz Baszczyk
Fellow (October):
Stefan Biereigel
Anthony Bulling
2022
Fellow (June):

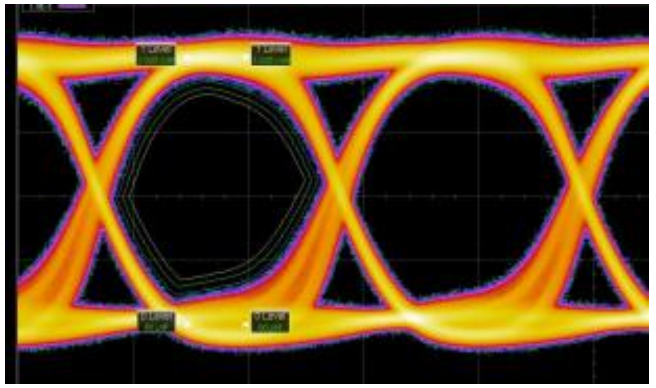
FPGA

- Technology survey
  - FPGAs
  - Optoelectronics COTS
  - Emerging standards
- Laboratory demonstrations
  - With state-of-the art
    - FPGA (Vertex – UltraScale+)
    - QSFP-DD optoelectronics devices
    - FEC coding: KP4-RS10 (544, 514)
  - 28 Gbps NRZ
  - 56 Gbps (PAM4 – 28 GBd)
    - PAM4 essential for > 25 Gbps/lane

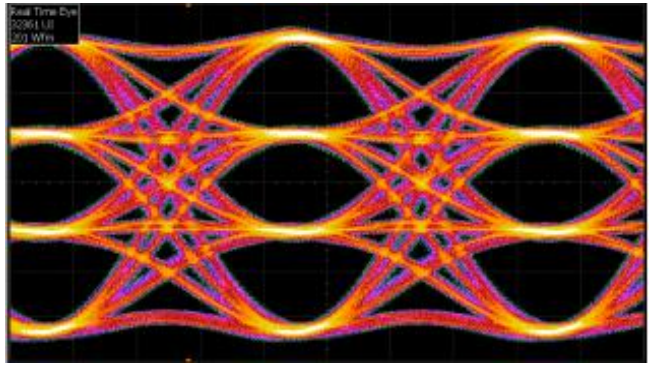
FPGA based demonstrator



NRZ 28 Gbps Electrical



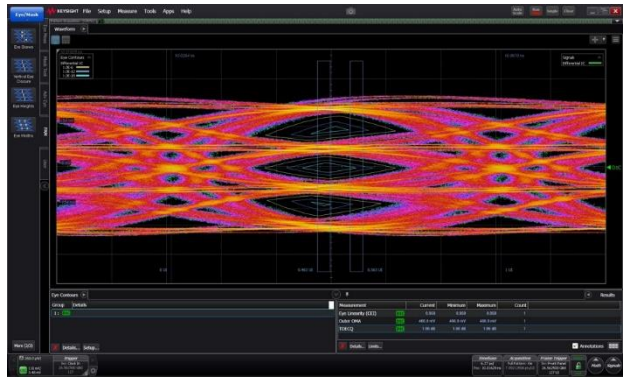
PAM4 56 Gbps Electrical



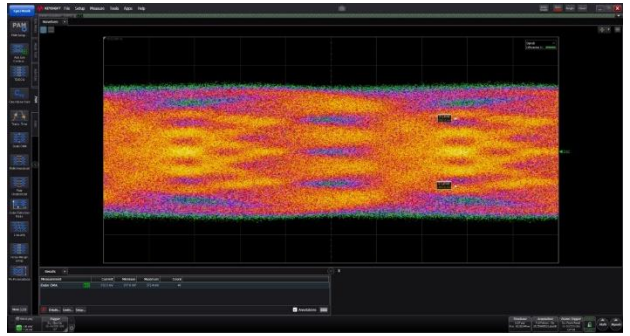
FPGA

- Experience with PAM4 COTS revealed
  - Evolving “standards”
    - WDM: diverse sets of wavelengths
    - Optoelectronics form factors still evolving!
  - Flexible data rates for FPGAs **but**…
  - Very strict data rates for optoelectronics devices
  - The low SNR requires high optical power at the receiver and FEC for error free data transmission
  - Existing components fully symmetric [High cost]

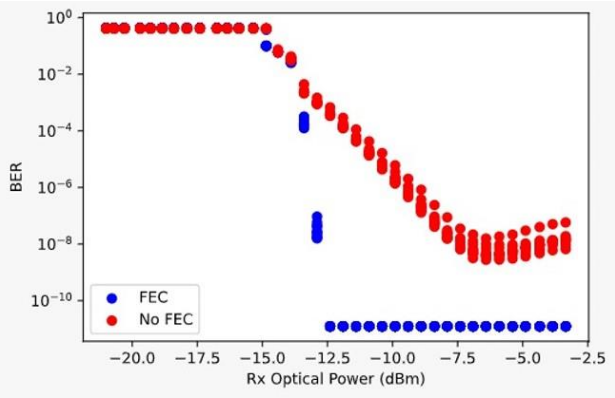
TX Output
56 Gbps optical



RX Output
56 Gbps optical



FEC Coding Gain



FPGA

- "FPGA" lessons learned, set constraints on the ASICs and OPTO activities
- Impact on the ASIC design:
  - PAM4 constrained [COTS] data rates not amenable to "LHC" clock synchronous operation
  - Strong FEC required (leaving less room for SEU handling)
  - Maximize the drive voltage ("incompatible" with advanced CMOS technology nodes)
- Impact on SiPh:
  - In the lab 1550 nm
  - Switch to 1310 nm system to match currently available commercial components
  - Optimize the modulation efficiency:
    - Trade-off with radiation tolerance

ASIC1/2 Challenge

	Radiation-hard		Non-radiation-hard (research)		Non-radiation-hard (commercial)				
Reference	**LPGBT '21** 	**GBTX '15** 	**IBM '19**		**Xilinx '21**	**Xilinx Ultra scale+**		**Intel Agilex F-Series**		**Xilinx Virtex-6 '09**
Technology	65nm CMOS	130nm CMOS	14nm Fin-FET		7nm Fin-FET	16nm Fin-FET		10nm Fin-FET		40nm CMOS
Modulation	NRZ	NRZ	NRZ	PAM-4	PAM-4	NRZ	PAM-4	NRZ	PAM-4	NRZ
Data Rate [Gb/s]	10.24	4.8	64	128	112	32.75	58	32	58	11.2
Radiation Hardness	200 Mrad	100 Mrad	Not applicable		Not applicable	Not applicable		Not applicable		Not applicable

ASIC1/2 Challenge

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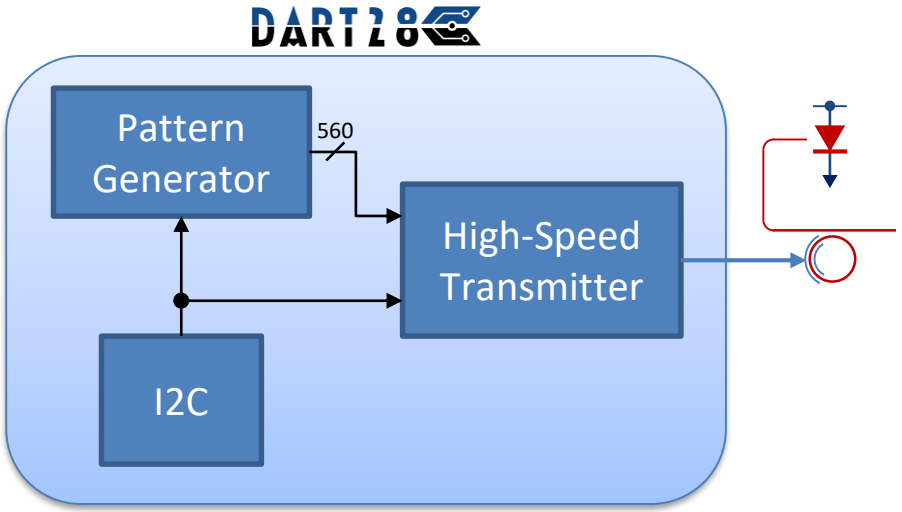
Technology	65nm CMOS	130nm CMOS	14nm Fin-FET	7nm Fin-FET	16nm Fin-FET	10nm Fin-FET	40nm CMOS
Modulation	NRZ	NRZ	NRZ	PAM-4	PAM-4	NRZ	PAM-4	NRZ	PAM-4	NRZ
Data Rate [Gb/s]	10.24	4.8	64	128	112	32.75	58	32	58	11.2
Radiation Hardness	200 Mrad	100 Mrad	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable

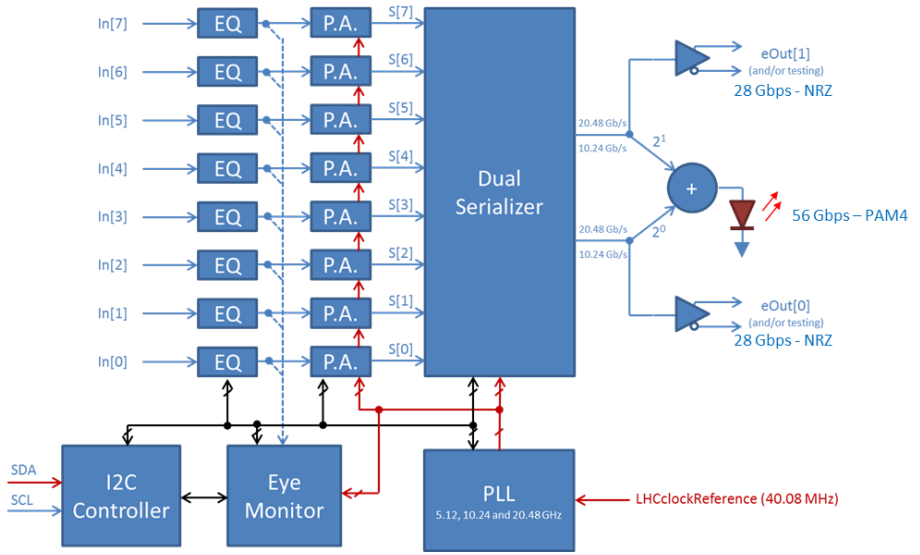
~12 year gap

ASIC1/2 “Design Targets”

2021 Design → Q3 2022 Testing

2023 Design → 2025 Testing





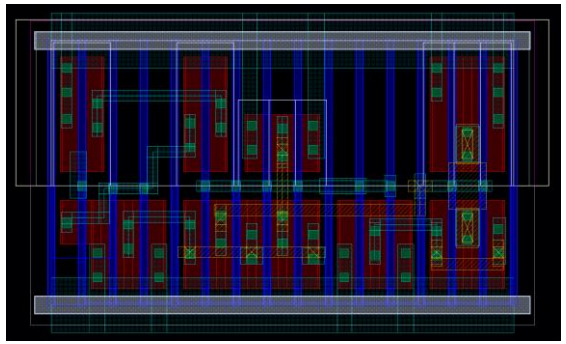
DART 28

- Merges ASIC1 / ASIC2 developments
- Test device [only] to soften the learning curve!
- Internal generated data [multitude of test patterns]
  - I2C Configurable
- 25.6 Gbps NRZ
- Ring modulator driver
- PLL / Serializer / Pre-emphasis / FEC
- 28 nm CMOS technology

High-Speed Data Aggregator

- Data inputs: 4 × 10 Gbps or 8 × 5 Gbps
- Data outputs: 2 × 28 Gbps NRZ / 56 Gbps PAM4
- RM / MZ driver
- Low jitter PLL
- PE / EQ circuits
- Phase-aligners (PA)
- 28 nm CMOS technology

DART28 (Demonstrator ASIC for Radiation-Tolerant Transmitter in 28nm)



DFF layout

Achievements

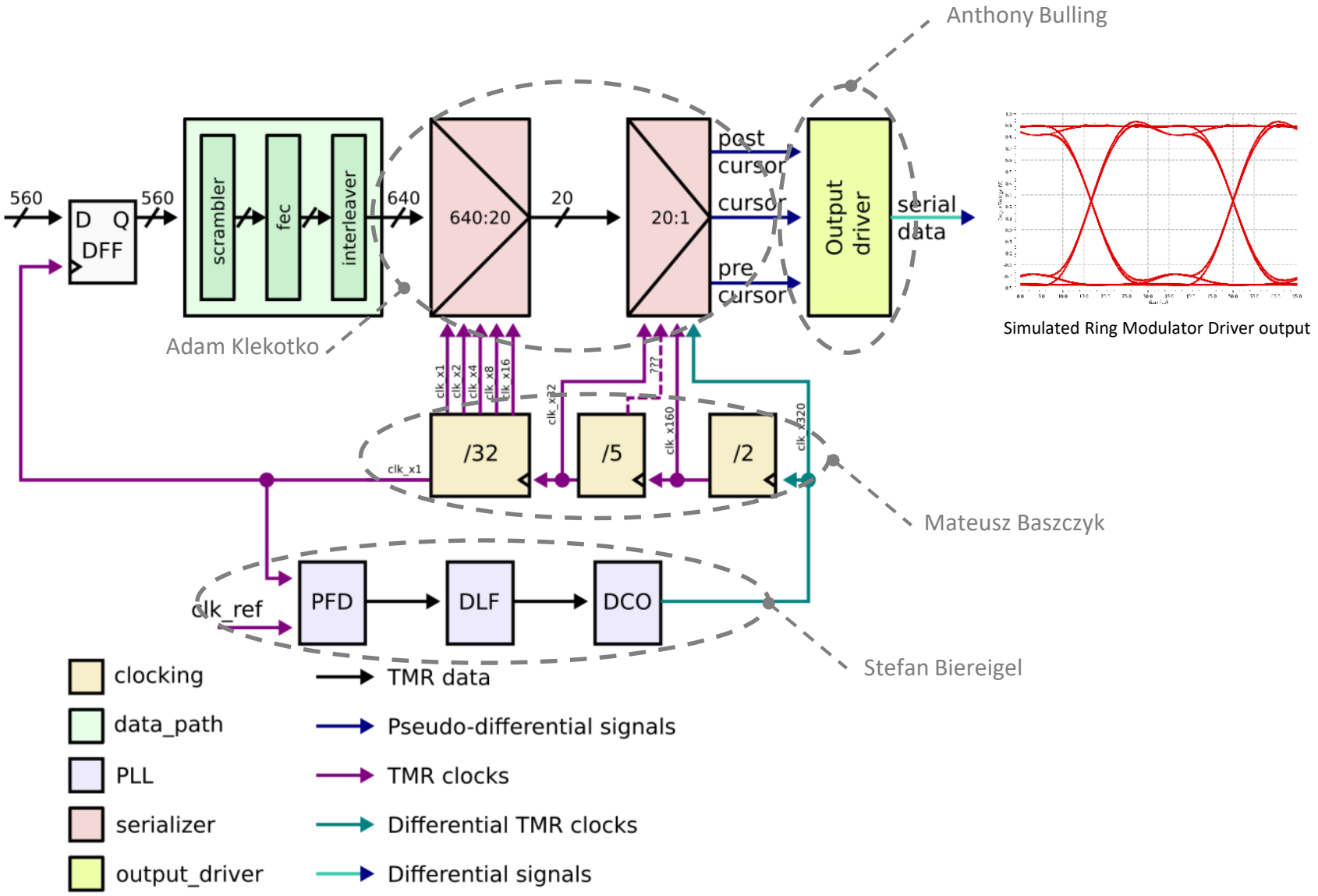
- Data path and control
- Behavioral model
- High-Speed Full custom digital cells

On the making

- Clock divider
- Serializer
- Output driver

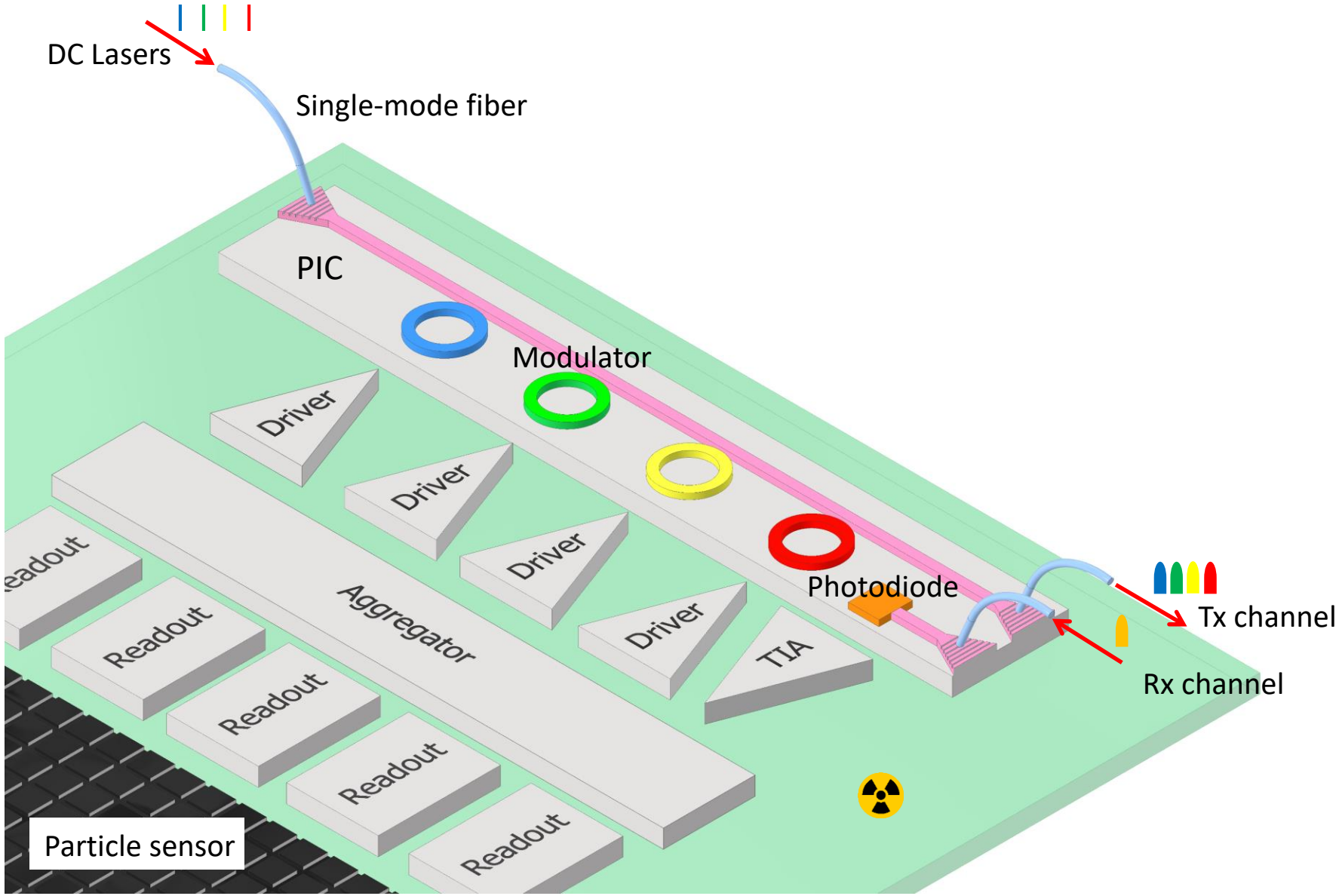
Starting soon

- PLL



Simulated Ring Modulator Driver output

Silicon Photonics

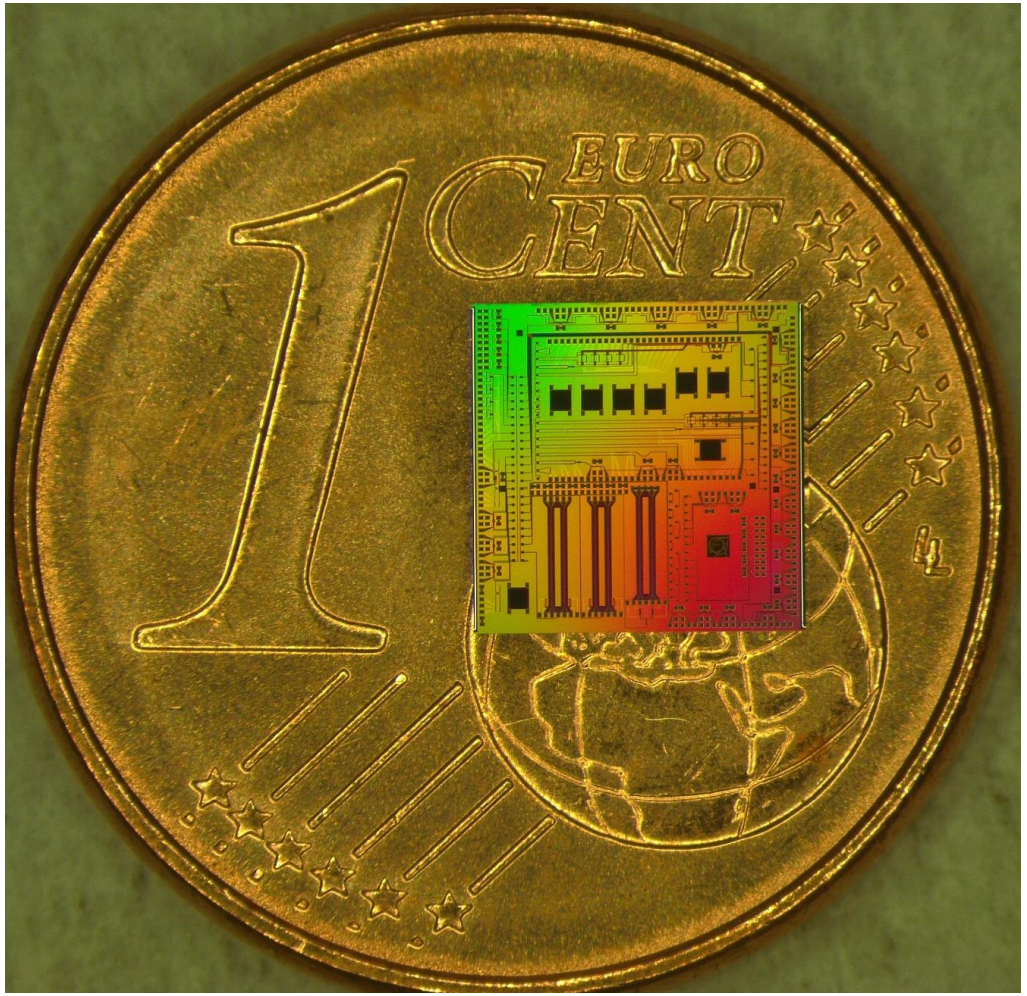


CERN Silicon Photonics Integrated Circuit – PIC

- Design submitted for fabrication before EP R&D programme start
- IP building blocks from CERN and industry
  - Imec ISIPP50G technology
  - Received at CERN in May 2020

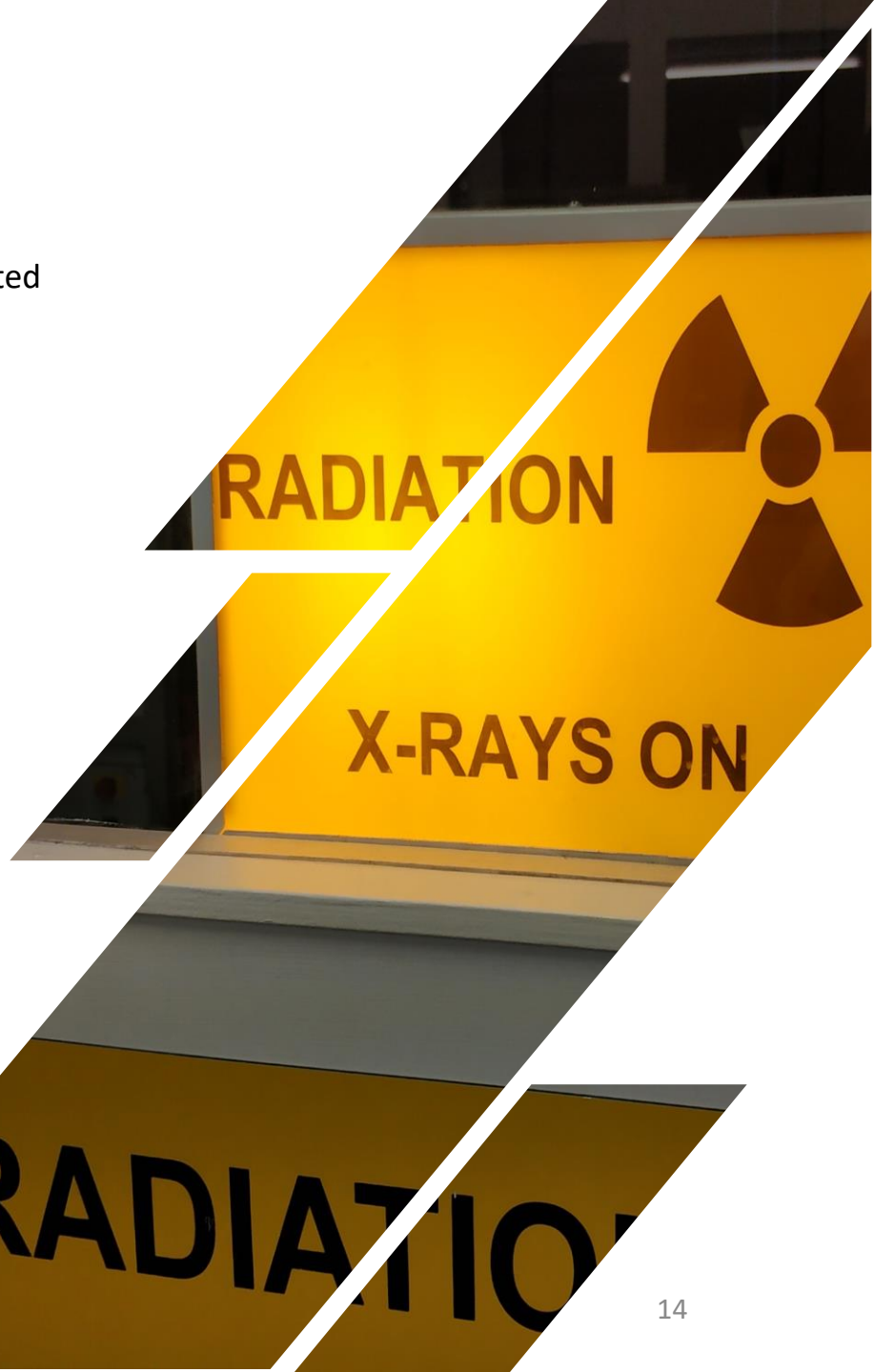
- PICv2 has been the test vehicle
  - 5 photodiode and 20 ring modulator designs
  - Carry out radiation tolerance characterization
  - Optical circuit test structures for data link development

PICv2

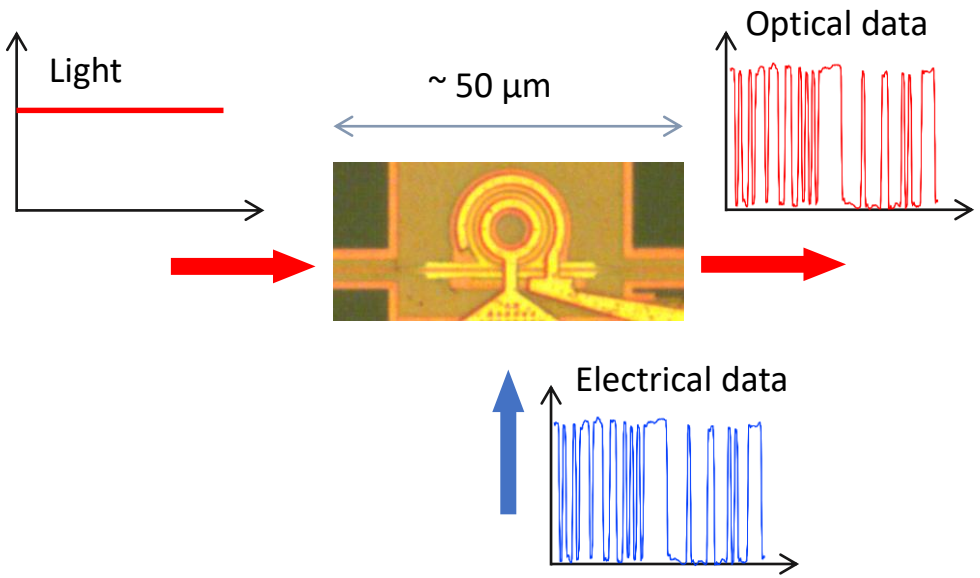


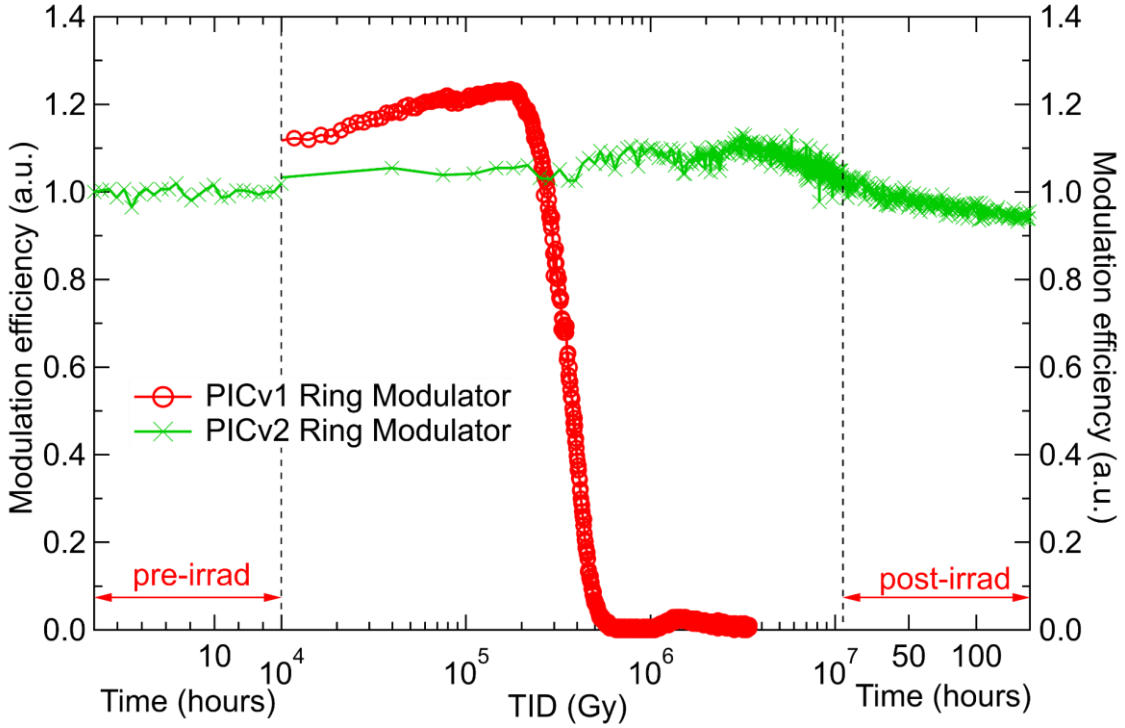
Silicon Photonics Radiation Hardness

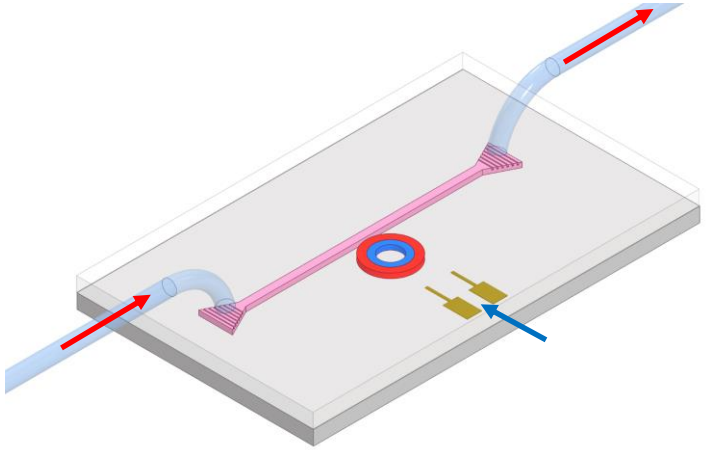
- The two radiation damage mechanisms for optical modulators and photodetectors were investigated
  - Total Ionising Dose (TID) ~ 10 MGy (= 1 Grad)
  - Non-ionising Energy Loss (NIEL): fluence ~ 3 x 10^{16} 20 MeV neutron/cm^2



Ring modulators TID tolerance



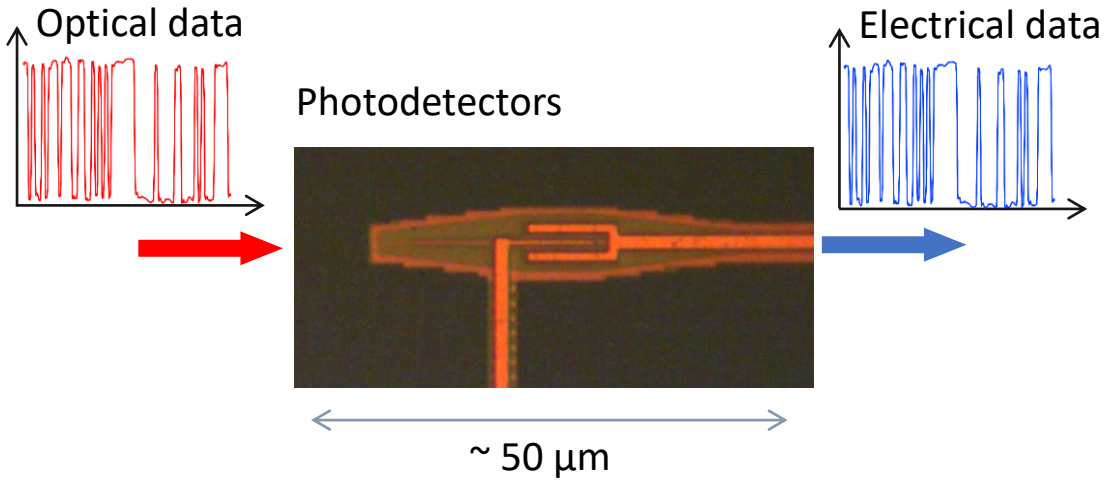


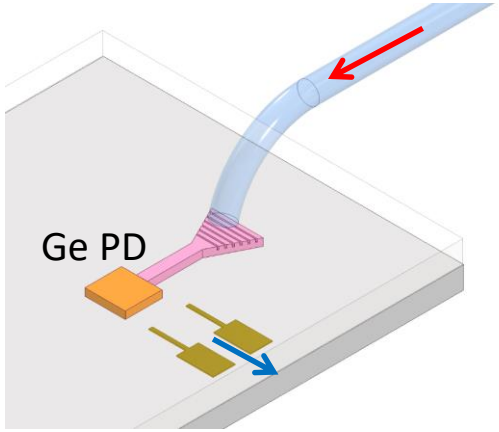


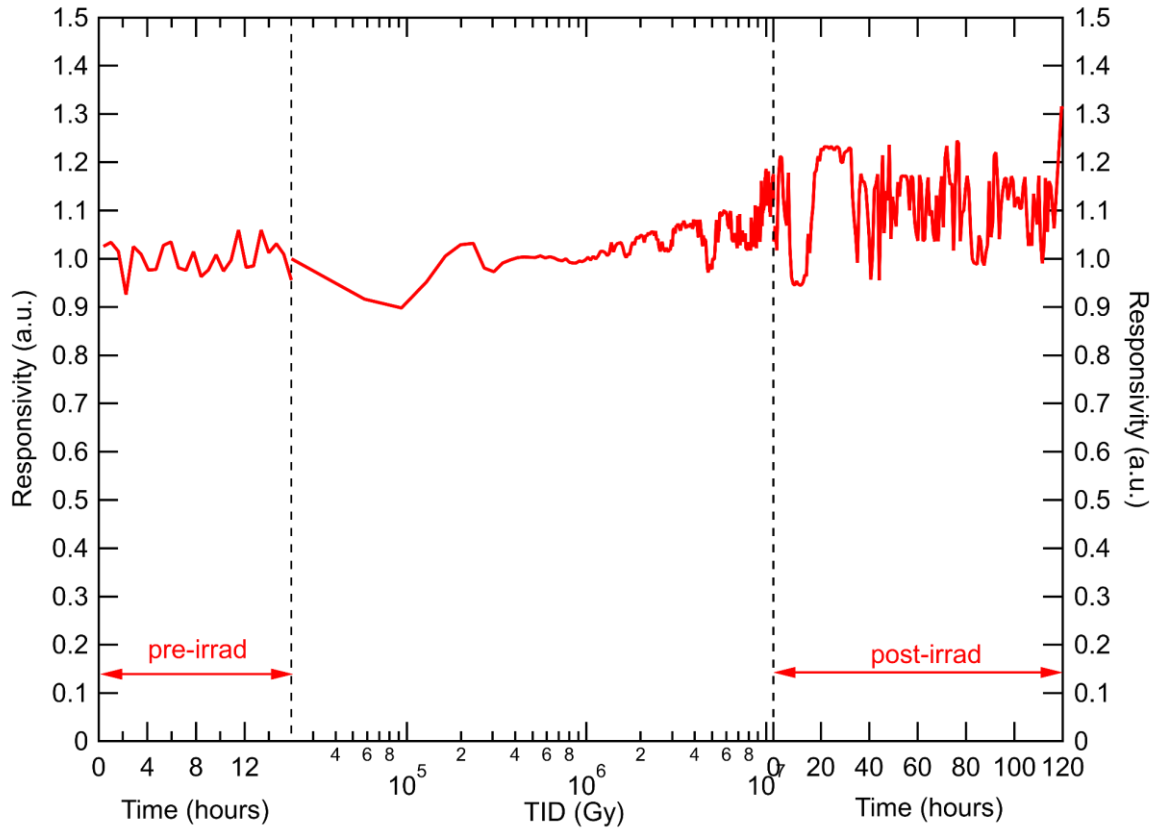
- Ring modulator PICv2 shows much higher radiation resistance than PICv1 *(at room temperature)*
  - As result of fabrication process changes to increase device frequency response
  - Negligible degradation after been irradiated up to 11 MGy TID
- Observed temperature dependence of TID tolerance: currently under investigation

M. Lalovic, et al. *"Ionizing Radiation Effects in Silicon Photonics Modulators"* RADECS, Vienna, Austria, (2021)

Germanium photodiodes TID tolerance



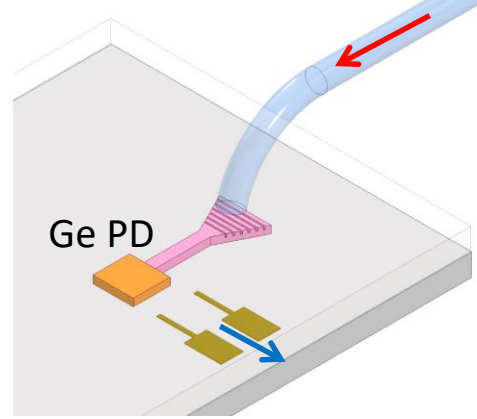


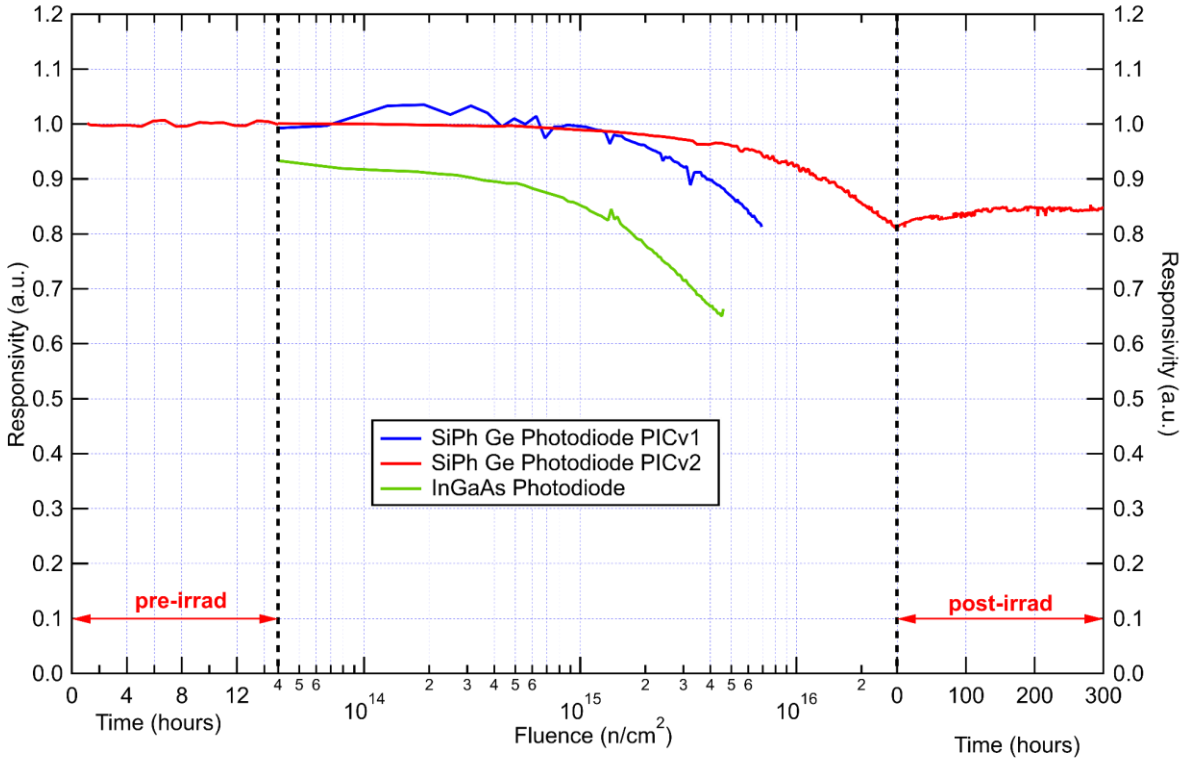


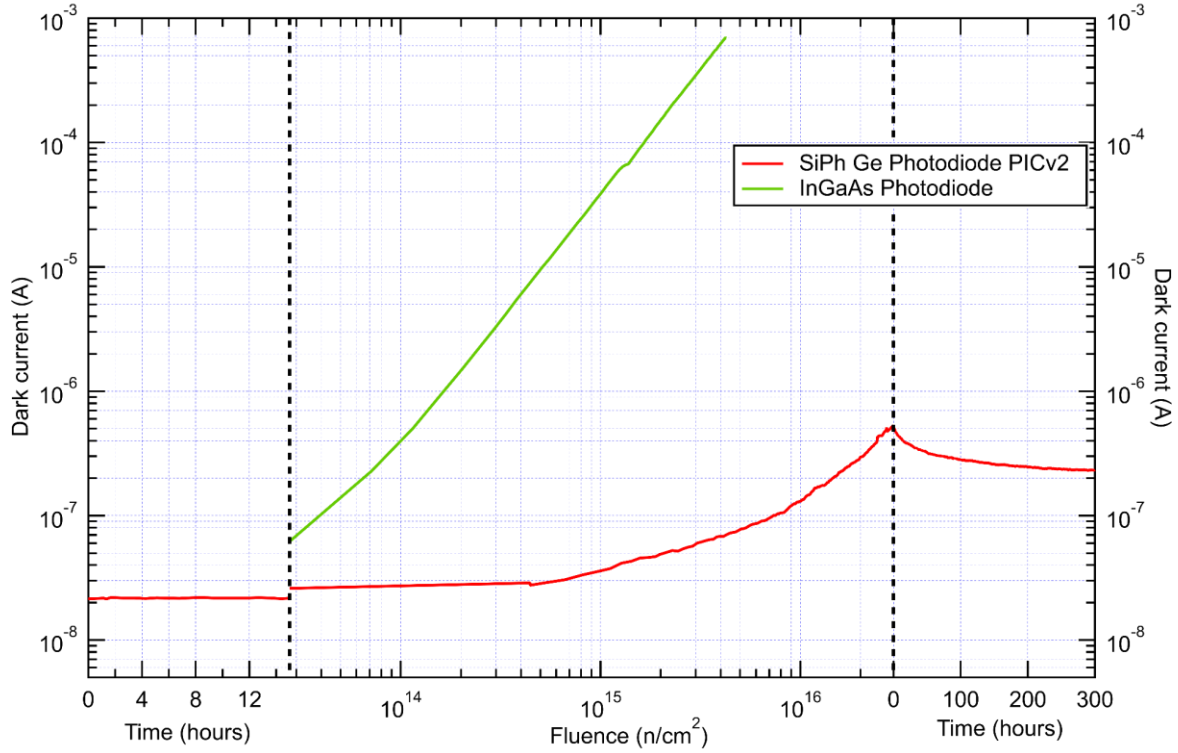
The tested Ge photodiodes do not show any TID induced degradation up to 11 MGy TID

Displacement damage in Ge photodiodes

- The tested Ge photodiodes on PICv2 shows better radiation tolerance than the design on PICv1
  - ~ 85% of the pre-irradiation responsivity after fluence ~ 3 x 10^{16} 20 MeV n/cm^2
  - 10 times more robust than the InGaAs pin photodiodes used in the rad- tolerant links deployed in the CERN Experiments
  - moderate dark current increase

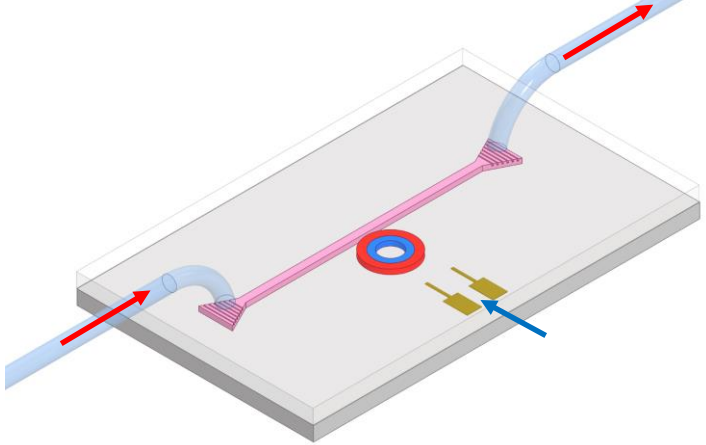




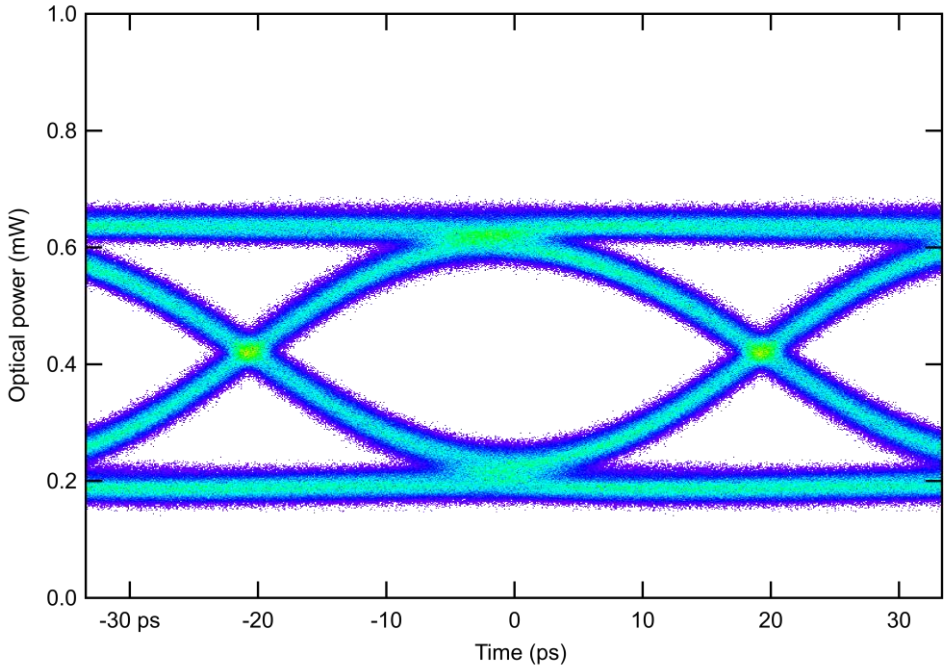


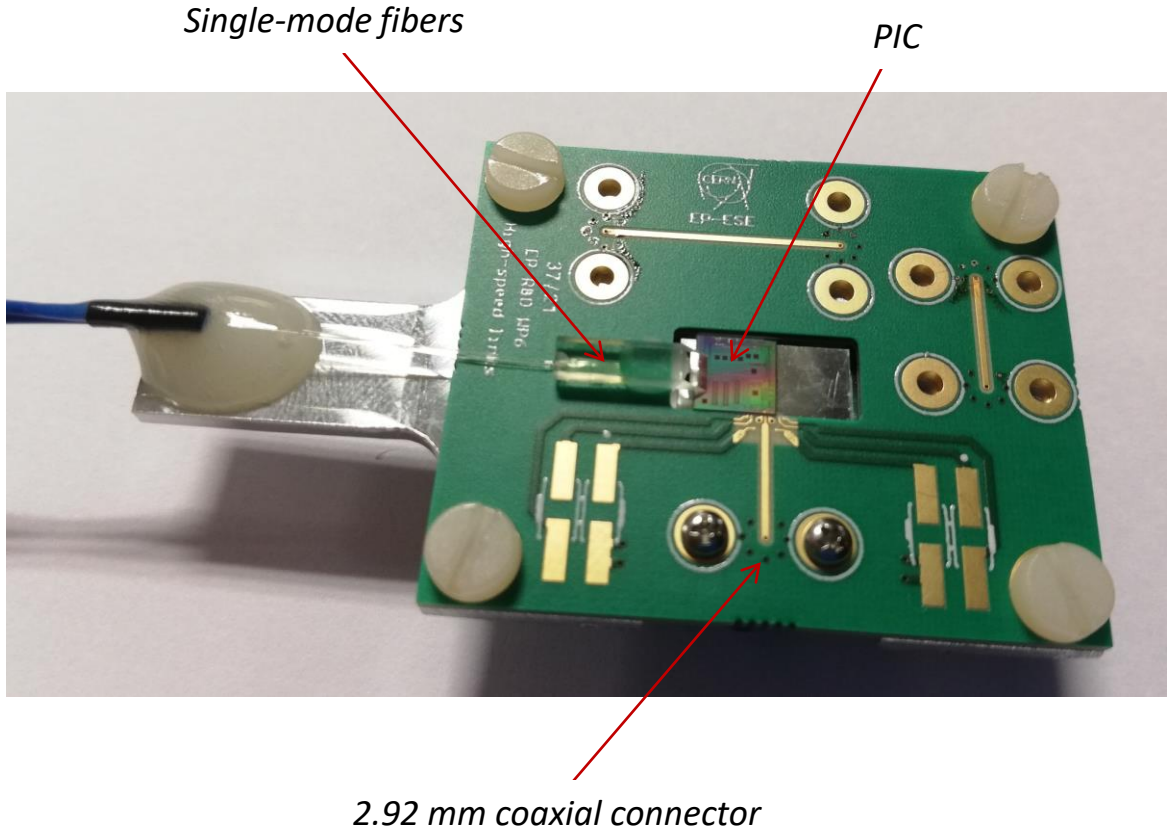
Ring modulator dynamic performance

- PIC mounted onto a test board with access to electrical and optical ports
- Lab instrumentation upgraded for 25G measurements
  - 33 GHz Sampling and Real-Time oscilloscopes
  - 32 Gbps pattern generator
  - 64 Gbps bit error rate tester
- Wide open eye diagram at 25 Gbps



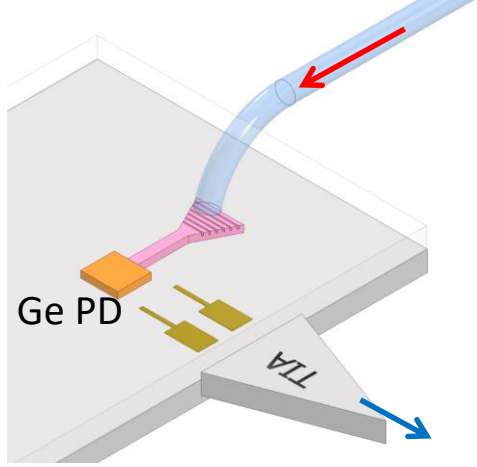
Ring modulator 25 Gbps optical eye diagram

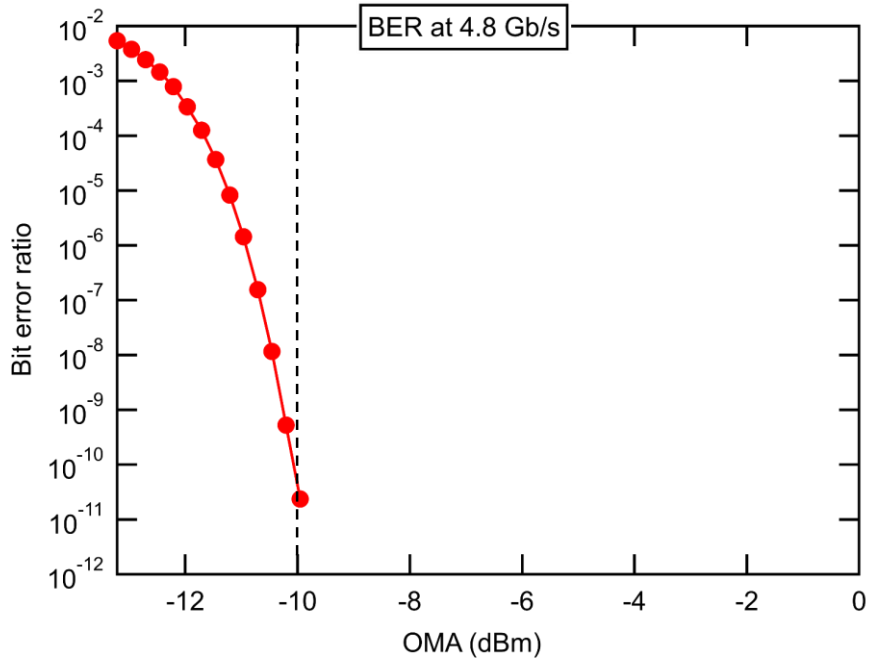


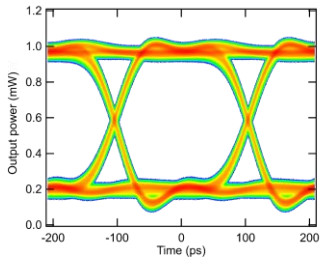


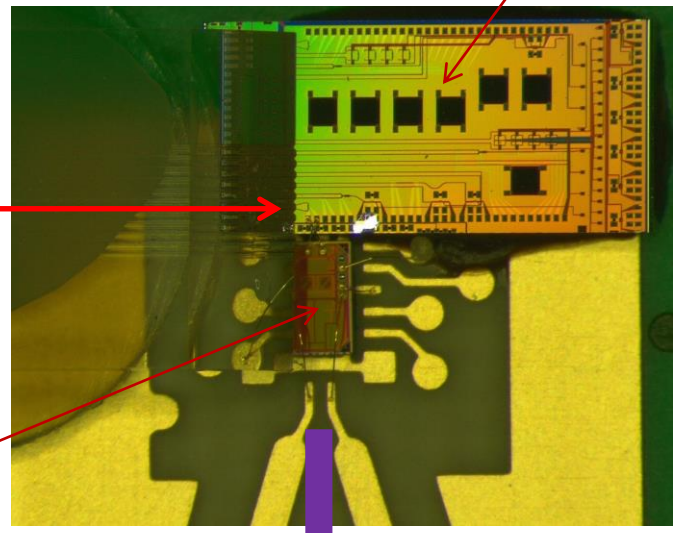
SiPh receiver prototype

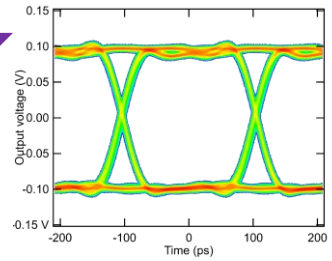
- Radiation tolerant receiver based on on-chip Ge photodiode and transimpedance amplifier (TIA)
- Downstream requires relatively low data rate (2.56 / 5.12 Gbps)
- First demo using GBTIA (5 Gbps radiation-hard optical receiver)
- Open eye diagram at the output of the receiver board
- Receiver sensitivity ~ - 10 dBm











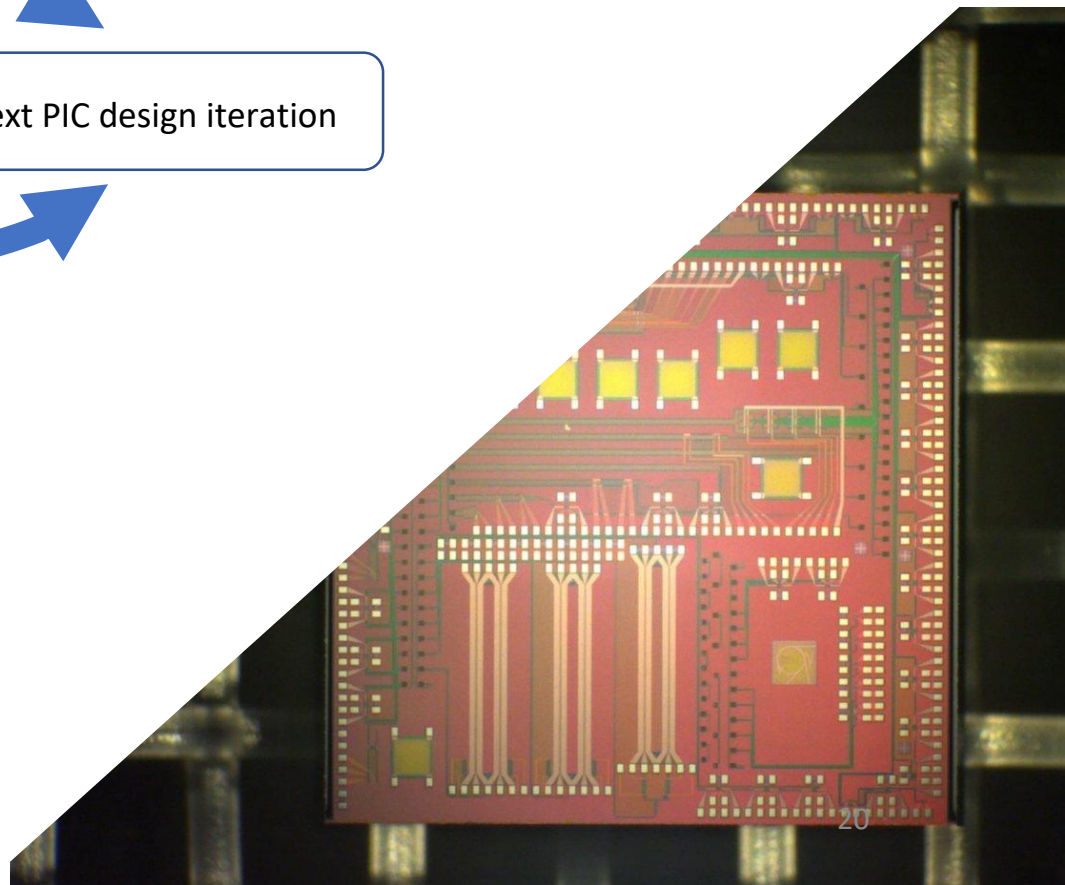
Thenia Prousalidi, et al. *"Towards Optical Data Transmission for High Energy Physics Using Silicon Photonics"* TWEPP 2021

Next Silicon Photonics steps

- Radiation tolerance
  - Neutron test on SiPh modulators
  - Modelling radiation damage

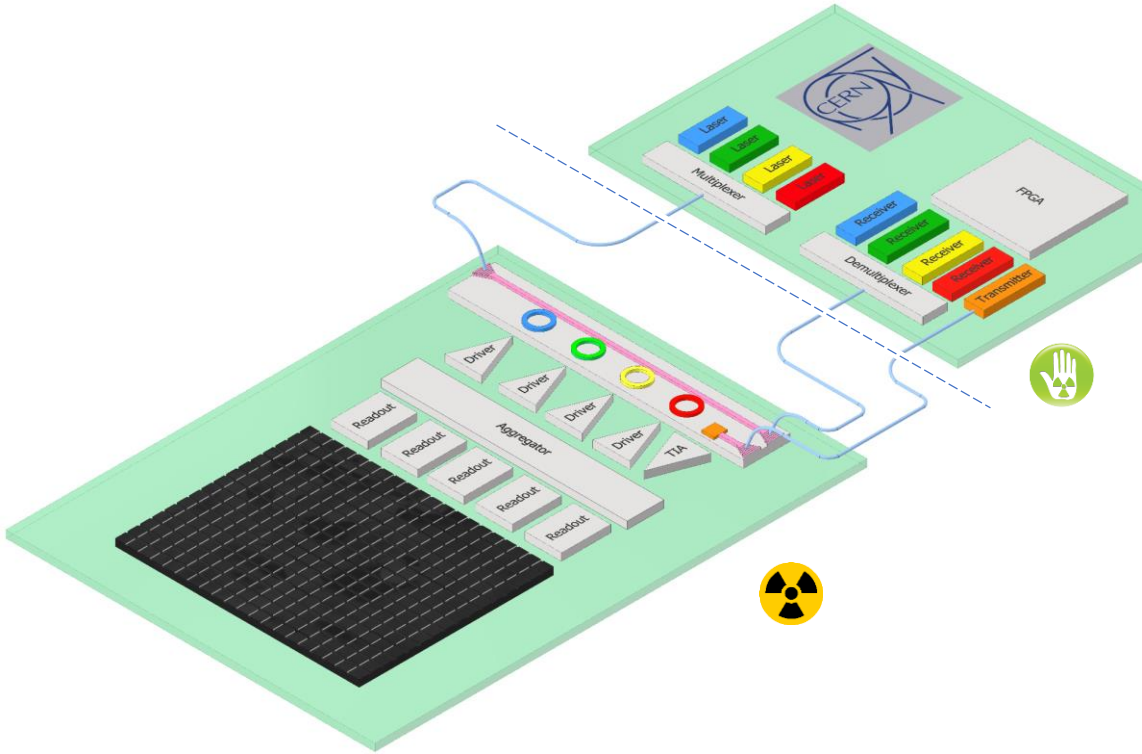
- Data link design
  - Integration of modulators with electrical drivers
  - Wavelength Division Multiplexing

Next PIC design iteration



Conclusions

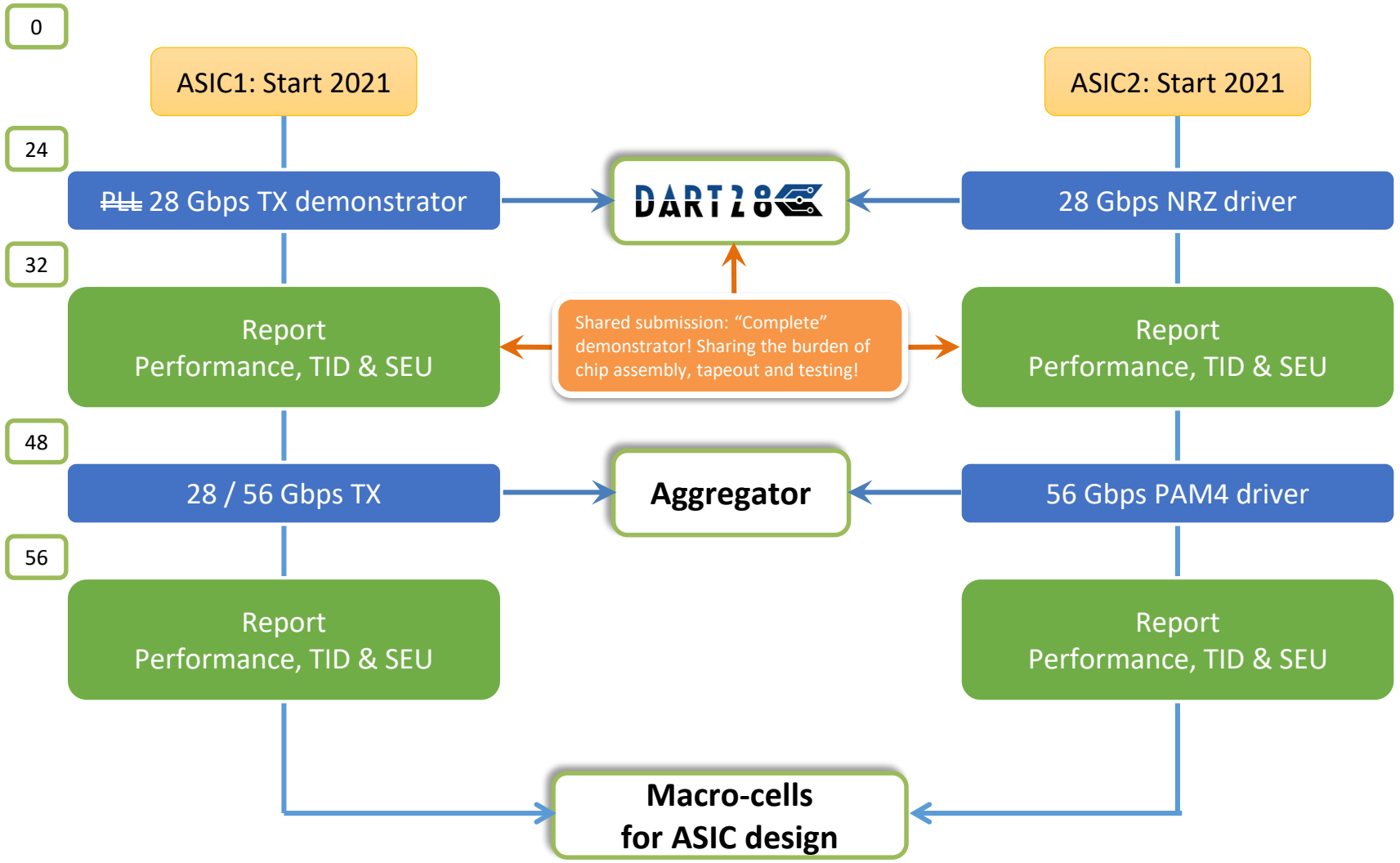
- **WP6 mission**
- Research towards high bandwidth, low-power & RadHard systems!
- Way forward:
  - Use advanced CMOS technologies [Rad qualified]
  - Design systems and devices compatible with top end
    - FPGAs
    - COTS, if possible!
  - Surf the wave of the SiPh field and develop RadHard optoelectronics



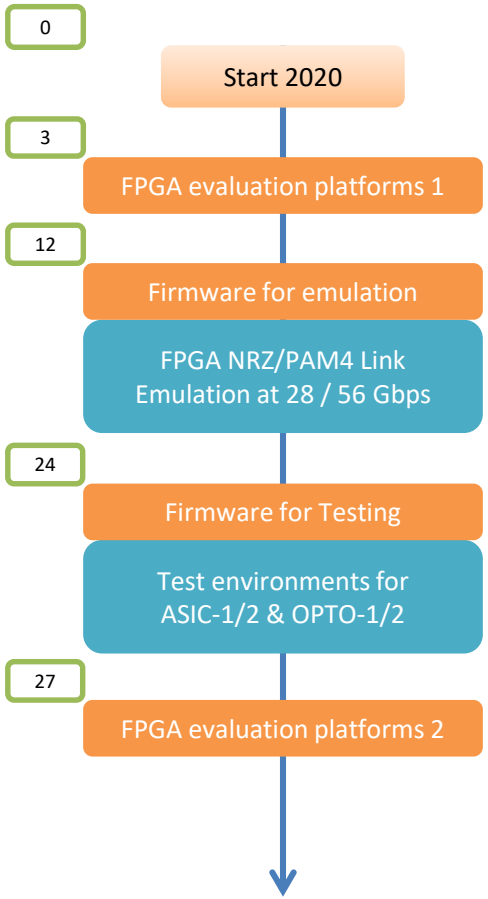
- **WP6 developments**
- 25 Gbps NRZ ASIC transmitter in the making
- Advanced FPGAs systems acquired and operation at 56 Gbps (PAM4 – 28 GBd) demonstrated
- Photonics Integrated Circuit (PIC) successfully tested
  - Ring Modulators (RM) and Germanium photodetectors present superior radiation hardness
  - 25G lab instrumentation upgrade and first 25 Gbps optical eye diagrams
  - SiPh radiation tolerant receiver demonstration

Backup slides

ASIC 1/2 VHS Transmitters & Drivers

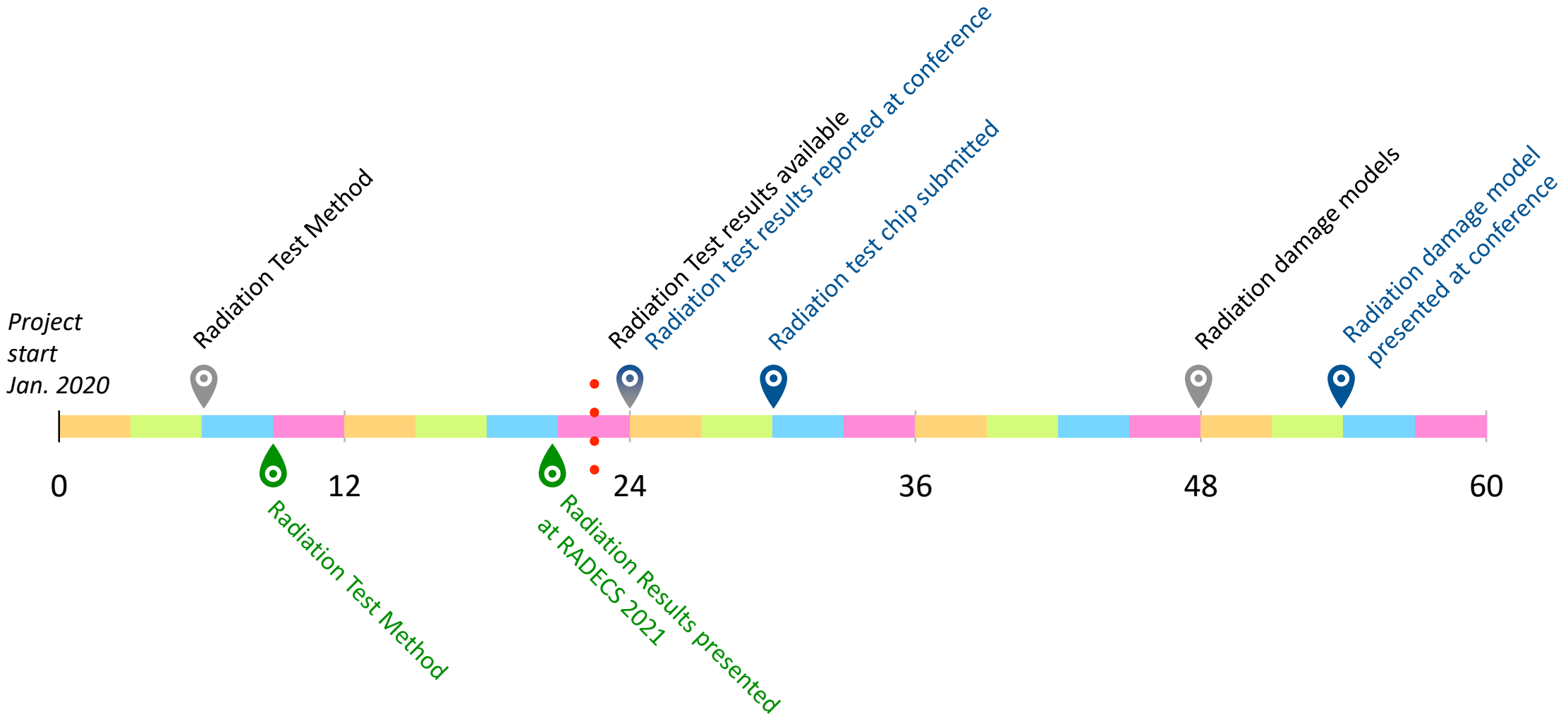


FPGA-based system testing and emulation

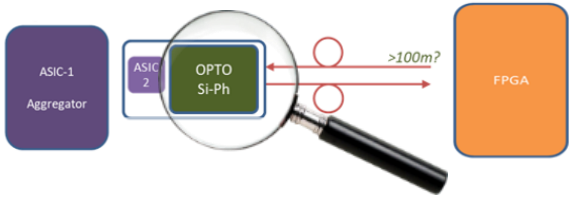


OPTO-1: Silicon Photonics System & Chip Design

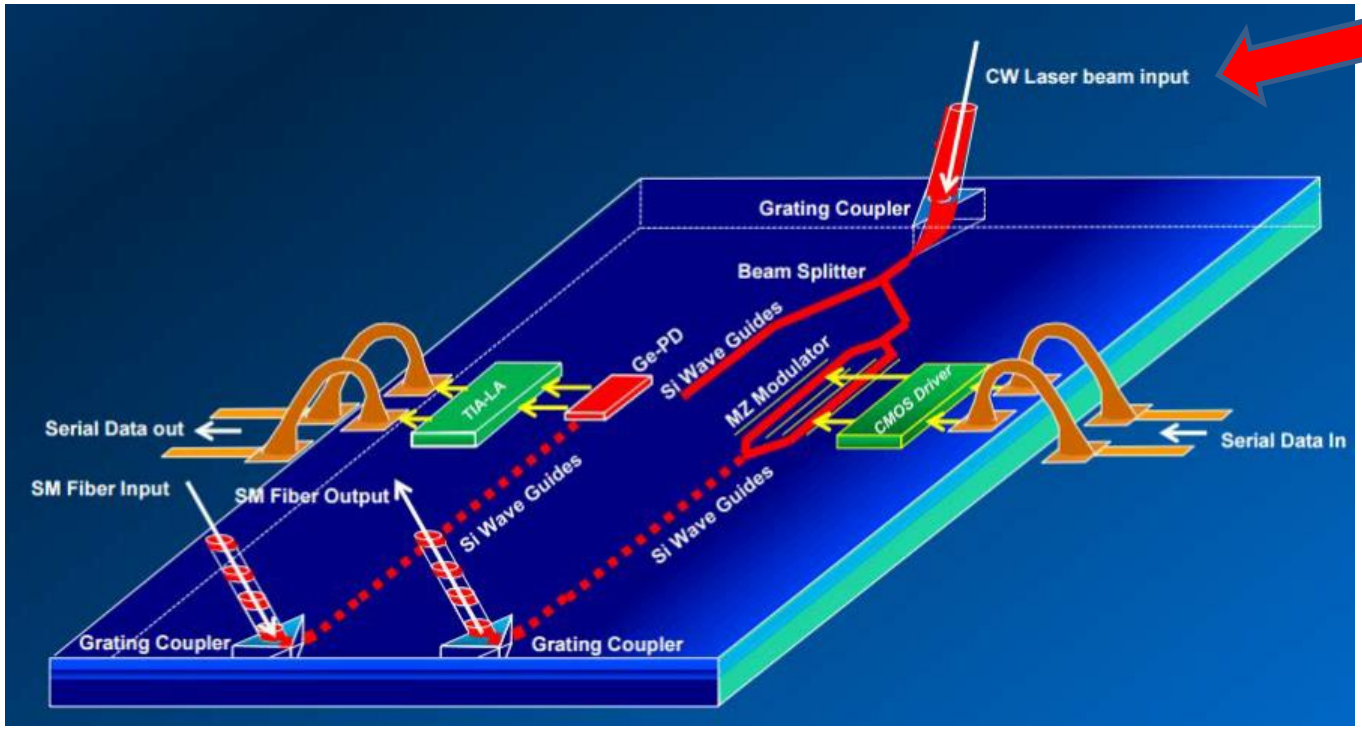
OPTO-2: Silicon Photonics Radiation Hardness



Silicon Photonics – co-packaging with CMOS



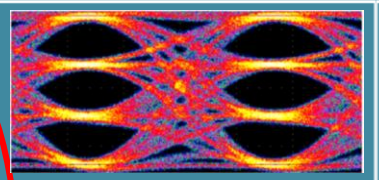
Note that the laser is off-chip



PAM-4 current «standards»

(NOTE: Standards still in development)

Optical Standards



	Modulation Format	Distance	Data Rate	Multiplex	Signaling Rate
200GBASE-SR4 (802.3cd) similar: 100GBASE-SR2, 50GBASE-SR	PAM4	70 m, 100 m	n lane x 50 Gbps	<n> par- allel MMF	26.56 GBd
200GBASE-DR4 (802.3bs)	PAM4	500 m	4 lanes x 50 Gbps	4 parallel SMF	26.56 GBd
400GBASE-DR4 (802.3bs) similar: 100GBASE-DR	PAM4	500 m	<n> lane x 100 Gbps	4 parallel SMF	53.125 GBd
400GBASE-FR8 (802.3bs) similar: 200GBASE-FR4, 50GBASE-FR	PAM4	2 km	<n> lanes x 50 Gbps	1 SMF 8λ WDM	26.56 GBd
400GBASE-LR8 (802.3bs) similar: 200GBASE-LR4, 50GBASE-LR	PAM4	10 km	<n> lanes x 50 Gbps	1 SMF 8λ WDM	26.56 GBd

Link