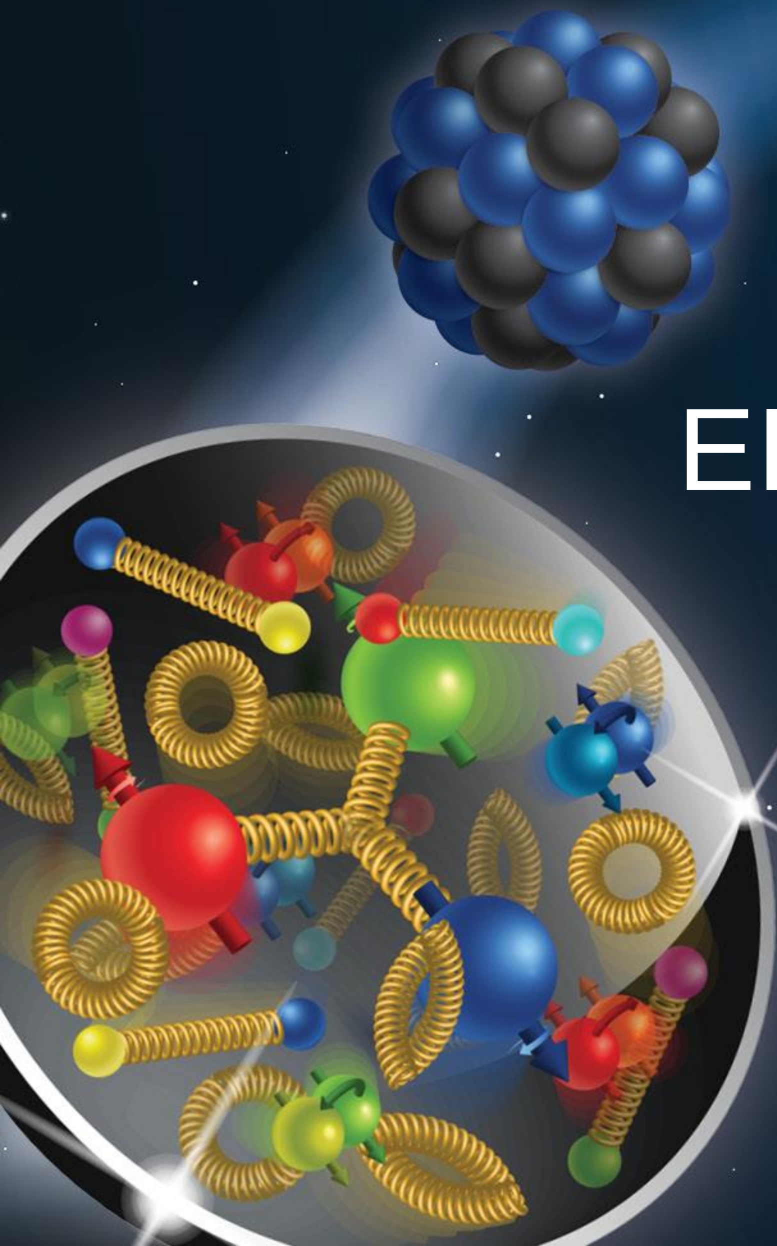

EIC Readout Overview

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Electron-Ion Collider

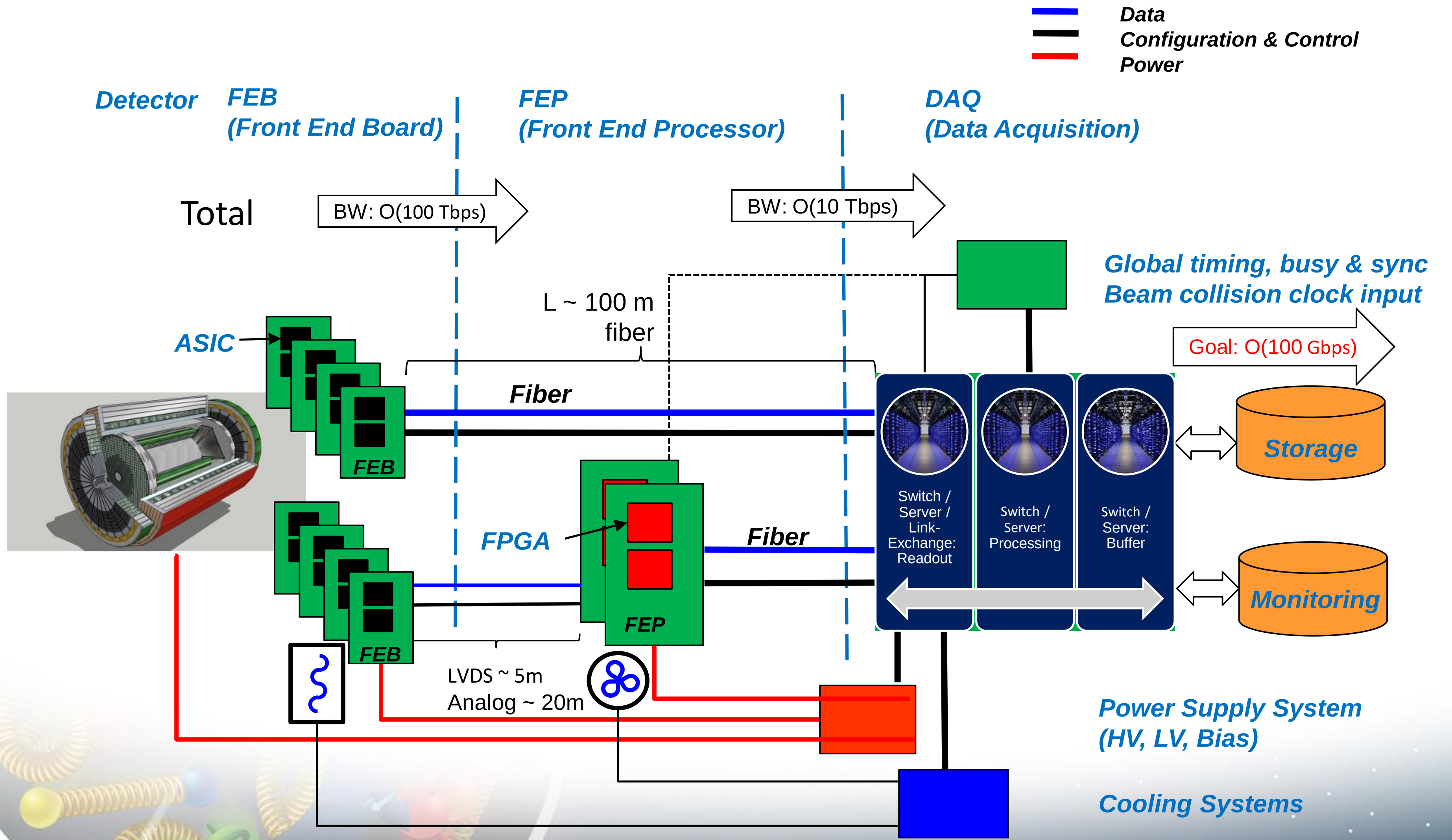
BROOKHAVEN NATIONAL LABORATORY · Jefferson Lab · U.S. DEPARTMENT OF ENERGY | Office of Science

Outline

- EIC Streaming Readout Architecture
- Readout Channels & Specifications
- DAQ/Computing
- Timing
- Outline of the EIC Needs
- Timeline
- Summary

- The EIC collision charged particle production rate is four orders of magnitude lower than that of the LHC:
  - LHC - aggressive reduction on the collision signal.
  - EIC - filtering out potential high background.

EIC Streaming Readout Architecture



EIC Streaming Readout

- **FEB – Front-End Boards**
  - Custom designed for each detector and populated with ASICs, large magnetic fields.
  - ASICs designed to process analog signals and digitization tailored to each type of detector technology. Data reduction (e.g. zero suppression) is desirable.
  - Simplification of testing and calibration operations with triggered-mode configuration.
  - Data transport via optical fibers to minimize cabling.
- **FEP – Front-End Processors**
  - Custom designed to process and aggregate data streams from multiple FEBs.
  - FPGAs are dominant components on these PCBs.
  - Algorithms reduce data flow (e.g., zero suppression)
  - Data transport via optical fibers to minimize cabling.
- **Global Timing**
  - High speed and precision combines custom designed and COTS componentry.
  - Provides synchronization of and clock distribution to the readout elements.
  - Jitter better than 1 ps.
- **Network Switches/Servers/Computing/Link Exchange (FELIX)**
  - High performance COTS infrastructure.
  - Enables further reduction of data flow prior to storage via sophisticated algorithms, e.g., ML and AI.
- **Radiation levels** are much lower than at LHC. Studies are being performed to inform readout technology selection, however.

Readout Channels

- Developed two documents summarizing the EIC readout requirements:
  - EIC Readout Specification Matrix.xlsx – Detectors, channels, requirements spreadsheet.
  - Development of the EIC Streaming Readout.doc – Roadmap to realization.

Detector	Sub-system	Type	Sub-type	Channels
Tracking				
	Silicon maps	Si MAPS	Pixel	200M
	TPC	MPGD	Pads	160K
	GEM	MPGD	Strips	217K
	uRWELL	MPGD	Strips/Pads	
	Cylindrical Micromegas	MPGD	Strips	60K - 80K
	sTGC	MPGD	Pad, Strip, Wire	
	TRD	MPGD	Strips/Pads	
Calorimetry				
	n-EMCal PWO	Cal	SiPM	1628
	n-EMCal SC Glass	Cal	SiPM	1168
	n-Hcal (KLM type) (10 layers)	Cal	SiPM	10k
	p-EMCal	Cal	SiPM	31k
	p-Hcal	Cal	SiPM	3/6/9k
	b-Hcal (KLM Type) (5 layers)	Cal	SiPM	24k
	b-Ecal (ScFI part)	Cal	SiPM	4k
	b-Ecal (Si layers)	Cal	Si Sensor	480M

PID				
	mRICH @ e-endcap	RICH	MCP-PMT (LAPPD) or SiPM	350k
	dRICH @ h-endcap	RICH	MaPMT	330k
	GEM RICH	MPGD	Strips	220k
	hpDIRC @barrel	DIRC	MCP-PMT	100k
	psTOF @barrel	TOF	LAPPD or LGAS	
	LGAD TOF	TOF	PMT/SiPM	
	LAPPD/MCP-PMT TOF	TOF	PMT/SiPM	
Far Forward Detectors				
	ZDC		PMT/SiPM	225(EMCAL) +36 (HCAL)
	Low Q2 tagger		PMT/SiPM	288 (2 EMCALs)
	Low Q2 tagger	Si strip	Si strip	6.4k
	Luminositymonitors		PMT/SiPM	288 (2 EMCALs)
	Roman Pots/OffM/B0	Si	Si	500k/750k/32M+320k
	Proton Spectrometer		PMT/SiPM	
	Lepton Polarimeter	Calorimeter	PMT/SiPM	110
		Strip/position	Diamond strip	1000
	Hadron Polarimeter		PMT/SiPM	

Two detector/sensor categories:
- ***MPGD***
- ***Photon***

Specifications

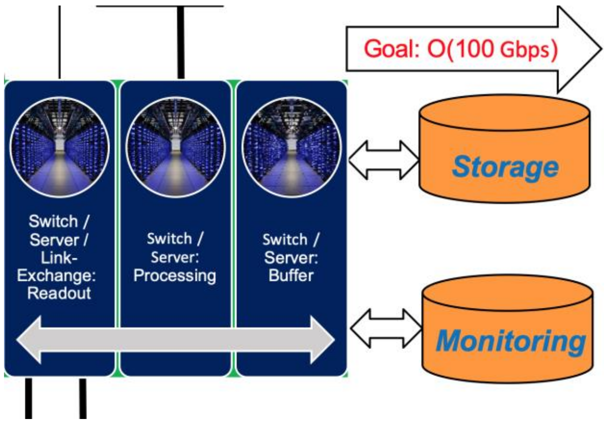
- Preliminary specifications for MPGD readout (ASIC)

Detector	
Capacitance	<200 pF nominal (500 pF maximum).
Noise	<3000 e^- @ 100 pF
Charge	25 fC – 100 fC (1 pC maximum).
Gain	$5x10^3 – 2x10^4$
Signal Time	100 ns – 500 ns (10 us ion drift time maximum), multiple hits per channel.
Signal Range	$<10^6$ e^-
Rates	<2 kHz per channel.
Readout	
Attributes	Amplification, digitization and buffering.
Features	Amplitude and time per hit; waveform samples for testing and calibration functions. Zero suppression; triggerless and triggered operation.
# Channels	64
Input Impedance	<70 Ohm
Gain	2 mV/fC – 30 mV/fC, configurable.
Peaking Time	40 ns – 250 ns shaping, configurable.
Crosstalk	<1 %
ADC Resolution	12 bit (>10 bit ENOB)
TDC Resolution	<20 ns
Sampling Rate	>80 MSPS
Optional	Discriminators and scalers are desirable.
Triggering	Streaming (triggerless) readout is the default mode. Triggered operation is required for testing and calibration functions.
Pulsing	Channel group pulsing desirable for testing function.
Output	TBD. Data format to be determined and to be consistent with optical fiber data transport between FEBs and FEPs.
Control Interface	TBD. Slow controls and configuration interface to be consistent with optical fiber data transport between FEBs and FEPs.
Technology Node	65 nm CMOS or higher.
Packaging	BGA or other SMT industry standard packages.
Power	1 W ± 0.25 W or < 20 mW per channel.
Supply	<+3 V DC

- Preliminary specifications for photon sensor readout (ASIC)

Detector	
Capacitance	60 pF – 5 nF (depending of cell size and grouping), <30 pF for PMTs.
Noise	1 p.e. @ <100 kHz, nominal (extends to 3 p.e.), lower for PMTs.
Gain	$<10^6$
Signal Time	3 ns – 80 ns
Rise Time	1 ns – 3 ns
Signal Range	<1 V into 50 Ohm or $<10^5$ pixels.
Rates	<50 kHz per channel.
Bias	Vop ~ 50 V DC for SiPMs.
Readout	
Attributes	Waveform sampling. Amplification, signal conditioning, digitization and buffering.
Features	Amplitude and time per hit. Zero suppression; triggerless and triggered operation. Input offset voltage adjustment.
# Channels	64
Input Impedance	<50 Ohm, depends on configuration.
Gain	1 - 10, configurable.
Peaking Time	<40 ns for SiPMs, ~1 ns for PMTs.
Crosstalk	<1 %
ADC Resolution	10 - 14 bit
TDC Resolution	1 ns for SiPMs, <100 ps for PMTs.
Sampling Rate	>80 MSPS for SiPMs, >1 GSPS for PMTs.
Optional	Discriminators and scalers are desirable.
Triggering	Streaming (triggerless) readout is the default mode. Triggered operation is required for testing and calibration functions.
Pulsing	Channel group pulsing desirable for testing function.
Output	TBD. Data format to be determined and to be consistent with optical fiber data transport between FEBs and FEPs.
Control Interface	TBD. Slow controls and configuration interface to be consistent with optical fiber data transport between FEBs and FEPs.
Technology Node	65 nm CMOS or higher.
Packaging	BGA or other SMT industry standard packages.
Power	1 W ± 0.25 W or < 20 mW per channel.
Supply	<+3 V DC

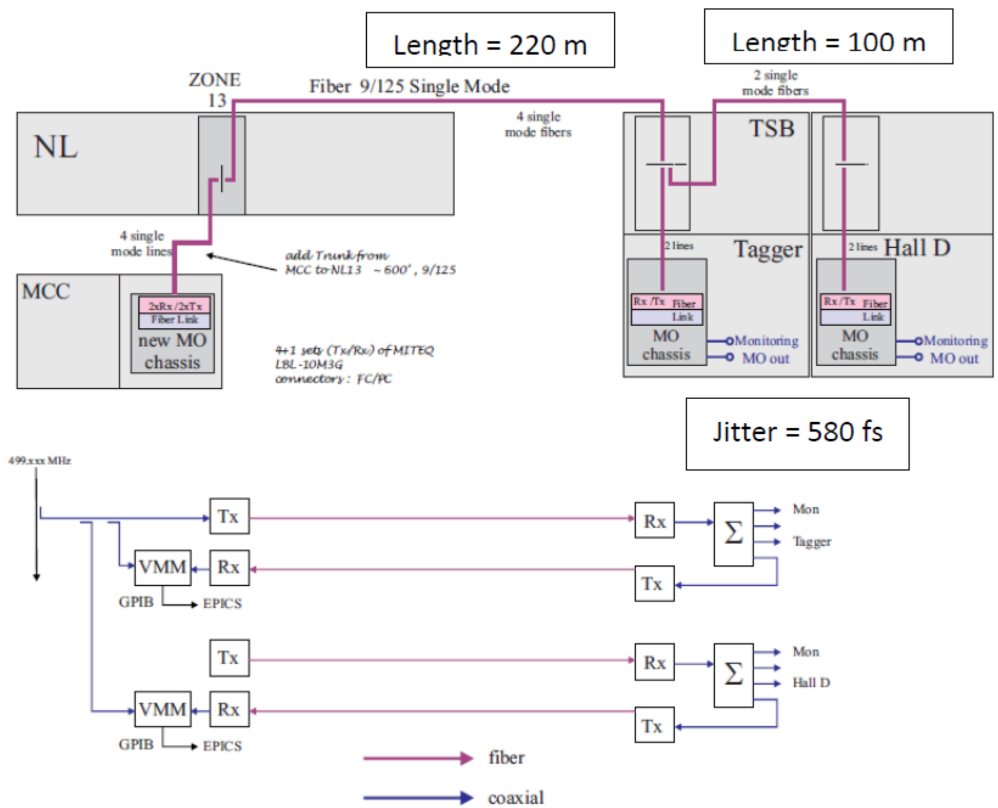
DAQ/Computing



- While EIC event rates are are expected to be 500 kHz, much smaller cross sections and multiplicities for (*e+p*, *e+A*) collisions will make event identification and reconstruction more manageable in the online system.
  - Machine (synchrotron) background levels still uncertain.
  - Detector choices (e.g. dark noise rate) can also affect requirements.
- A raw data rate to archival storage of the order 100 Gbps
  - Includes background and noise estimates.
  - Is still half the expected rates for sPHENIX.
  - Possible higher rate in the event of excessive background and noise, which would require filtering.
- Event reconstruction times for larger JLab experiments (GLUEX, CLAS12) are around 600 ms/event with current (2020) CPUs. Extrapolating to 2030 performances we expect a cluster of <300 nodes (128 cores/node) to be sufficient to support the 500 kHz interaction rate.
- Assuming 28 weeks of running and 70% facility efficiency this translates into around 148 PB/year of raw data only.

Timing

<u>Using GlueX@JLab as an example:</u>



RF Clock:

- ❑ 4 ns bunches.
- ❑ 580 fs Jitter, single-mode fiber.
- ❑ Feedback channel for phase compensation.

Experiment Clock:

- ❑ <4 ps jitter at DAQ crate level.
- ❑ Multi-mode fiber, LVPECL.

- ❑ Relative time measured via 25 ps TDCs.
- ❑ Calibration prior to every run.
- ❑ Bunch determination via 100 ps - 200 ps resolution scintillating detectors.

- ❑ Timing performance at EIC will be more challenging.
- ❑ Distribution and synchronization of front-end with 98.5 MHz with the EIC beam collision clock.
- ❑ 20 ps resolution detectors at EIC will require <1 ps clock jitter.

Outline of the EIC Needs

- **ASICs** – Application Specific Integrated Circuits
  - Design and/or Fabrication Services – e.g., MOSIS, TSMC, Global Foundries, etc. Multi-channel, low power, high speed. Qty. > 10,000 devices.
  - Considering design re-use from existing ASICs (SAMPA, VMM, lpGBT, etc.)

- **Photon Sensors (SiPMs/MCP-PMT/MaPMT)** – COTS. Qty. < 1 Million cells

- **Electronic components & PCBs** – by consignment or turnkey fabrication and assembly services – e.g., multi-layer with ASICs, FPGAs, etc. Qty. < 1,000.

- **Cabling** – Turnkey fabrication services of various types of cables and optical fibers (COTS) and per supplied specifications. Cables must meet a minimum of UL CL2 specifications. Qty. > 1,000.

- **Power Supplies** – Multi-channel, Low Noise, Floating, Modules:
  - Low Voltage (LV) - < 15 VDC, 5 A – 10A range per channel. Qty. > 1,000.
  - Bias - < 100 VDC, mA range per channel. Qty. > 10,000.
  - High Voltage (HV) - < 8 kV, mA range per channel. Qty. > 1,000.

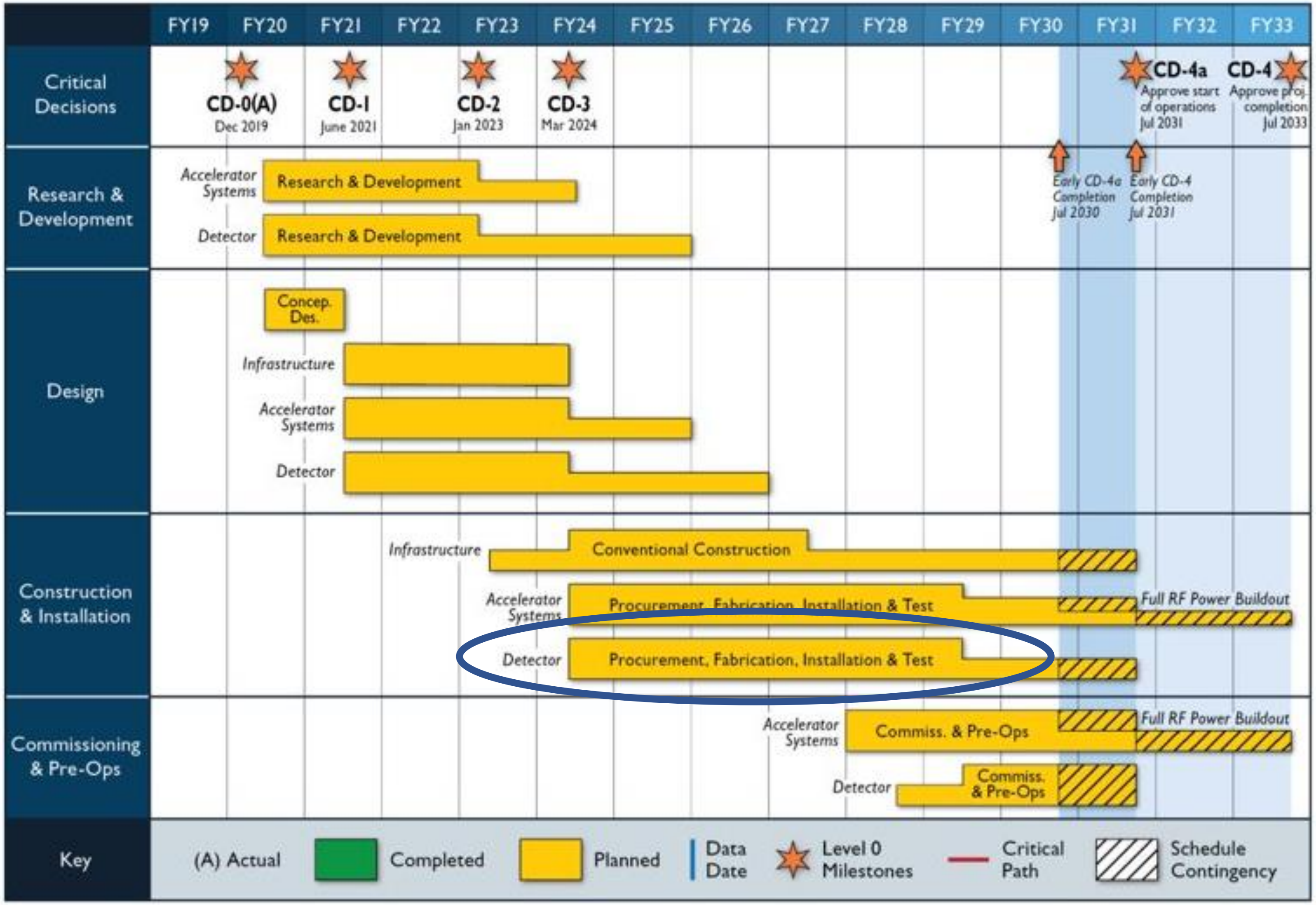
- **Racks and Cooling** – COTS. Qty. < 100.

- **Switch/Server/Computing** – COTS. Qty. < 100.

Timeline

Construction and Installation for Electronics & DAQ/Computing: March 2024 – March 2028

- **Construction and Installation includes procurements and deliveries and are initiated at different times of this phase.**



Summary

- The EIC community (proto-collaborations) is currently formalizing proposals for the EIC detector implementation. Selection is expected in early 2022.

- We have been working on a streaming readout & DAQ design roadmap, following an aggressive schedule and building upon Yellow Report work. Inputs and suggestions are appreciated.

- There is potential flexibility in many of the elements for the EIC electronics and DAQ/Computing architecture.
  - Early focus has been on specifications for detectors and ASICs (and their integration).
  - Front End Processing and DAQ/Computing stages will benefit from ongoing experiments and from new commercial technology developments.

- The EIC User community is growing internationally, and you will be an invaluable resource for input on design and implementation. We hope to benefit from your experience and on-going work.

- Thank you for your help!