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Development of a new front-end ASIC for MPGDs at EIC

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Introduction

Draft chip specifications

Prospects

VERSATILE READOUT CHIP FOR MPGD

Motivations of the project

- To study a new versatile multi-channel readout chip in the framework of the EIC project and beyond
  - adapted to streaming readout DAQ
  - for different kinds of MPGD detectors (trackers, TPC, photon detectors)
  - with optional extension to other kinds of detectors (calorimeters ? photon detectors ?) and/or specific constraints (ps-level time resolutions)
- Large ranges in term of signal amplitudes, electrode capacitances, peaking times
- TSMC 65nm technology instead of older 130nm for improved performances and sustainability

Common initiative of Sao Paulo Universities and CEA Saclay IRFU

- Sao Paulo University + associated institutes designed the SAMPA chip (readout chip for ALICE TPC), experts in on-chip digital processing
- IRFU developed several front-end chips (AFTER, AGET, DREAM,...) and other kinds of chips (SAMPIC and HGCROC TDC,..), experts in low-noise radiation-hard generic front-ends
- Large amount of complementary competences to build a common versatile front-end chip, with digitization and digital processing

PRELIMINARY CHIP SPECIFICATIONS

Versatile front-end characteristics

- For most kinds of MPGD (trackers, TPC, photon detectors), 64 channels
- Large input capacitance range, optimized for 200pF, reasonable gain up to 1nF
- Large range of peaking times (50-500ns) and gain ranges (50-5000fC), programmable scaling of the input stage
- Able to stand input rates of 25 kHits/s/channel (EIC conditions) and beyond
- Reversible polarity, front-end elements can be by-passed

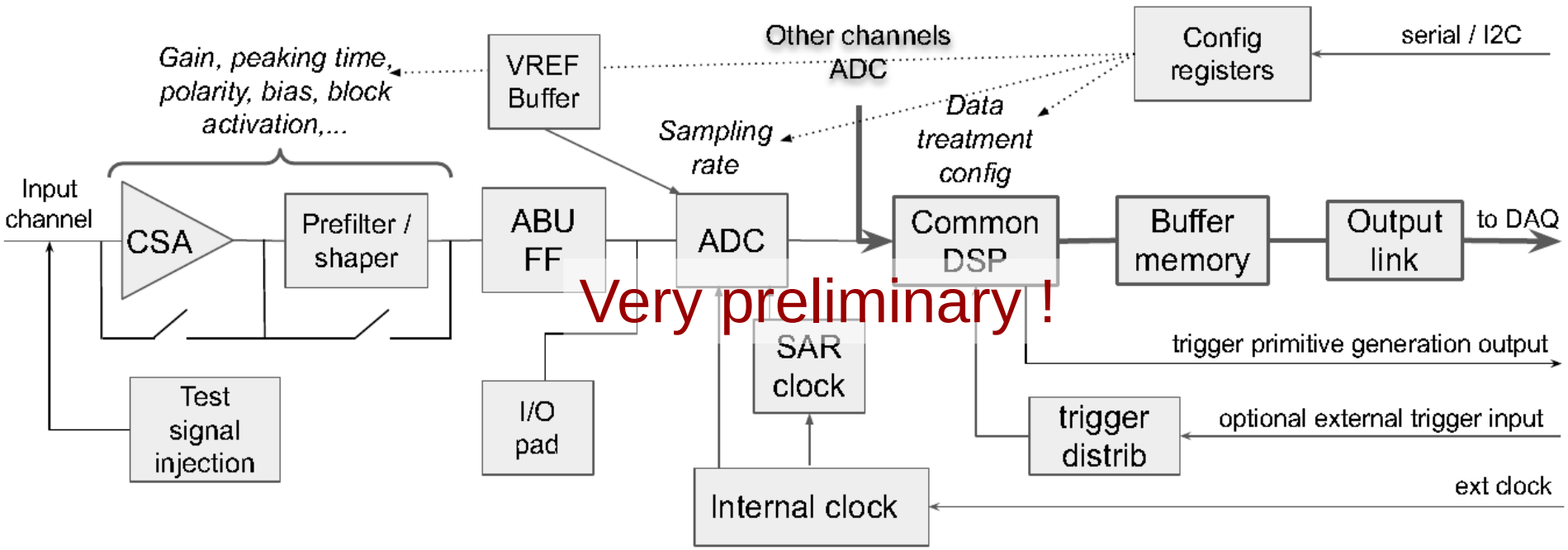
Digital stage

- Fast sampling ADC on 12 bits at up to 50 MS/s and beyond
- Integrated DSP for internal data processing and size reduction: pedestal subtraction, common mode correction, zero suppression, peak finding, trigger generation, optional digital filtering
- Continuous readout compatible with streaming DAQ foreseen at EIC
- One or several 1Gb/s output data links

General characteristics

- ~1 cm² die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel
- Radiation hardened (SEU, TID), working at 2T magnetic field

TENTATIVE CHIP ARCHITECTURE



PROSPECTS

Tasks in progress

- Finalization of specifications
- Studies ongoing on chip architecture and on different elements (front-end, ADC)
- Application for grant to French and Brazilian research agencies ongoing

Tentative timeline

- Development + prototype production + tests: ~ 2 – 2.5 years
- Preserial production and tests: ~ 1 year
- Full production: 0.5 – 1 year

Collaboration around the chip

- Common initiative of Sao Paulo University and CEA Saclay IRFU
- Other contributors are welcome !
- Major interest to collaborate with CERN on 65nm technology
  - lpGBT block for high speed up and down-links
  - Serial receivers and drivers
  - PLL / CDR
  - Other blocks ?
  - Help on batch submissions

POSSIBLE CERN-EIC COLLABORATION DOMAINS

- **ASIC developments**
  - Access to CERN blocks
  - Help to batch submissions for the different technologies
  - Experience sharing ?
- **Components developed at CERN**
  - Interest on radiation tolerant, resistant to magnetic fields, components
  - LV power distribution for front-end electronics
  - High speed VersatileLink+ technology, in particular lpGBT ASIC and VTRX+ optical transceiver
  - Clock distribution ? Others ?
- **Experience sharing**
  - Recent commercial components known to be resistant to radiation and/or magnetic field, depending to the exposition level (parts of EIC experiments would not require very strong radiation hardness), in particular
    - Optical transceivers (in particular compatible with lpGBT)
    - FPGA
    - Power regulators
- **Access to CERN facilities**
  - Irradiation facilities
  - Others ?

Spares