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## TOWARD A VERTEX DETECTOR CONCEPT EXPLOITING THE EVOLUTION OF CMOS PIXEL SENSORS AND THEIR SERVICES

The physics programme of FCCee requires a particularly high performance vertex detector, where spatial resolution and material budget prevail over radiation tolerance and read-out speed. As of today, CMOS pixel sensors provide promising

perspectives of detection performances matching this requirement ranking. Two CMOS technologies are currently developed for this purpose. Their potential will be exposed in the talk, integrated in a specific detector concept.

A full custom CMOS sensor, called MIMOSIS, is currently developed at IPHC-Strasbourg in a 180 nm technology to equip the Micro-Vertex Detector (MVD) of the CBM experiment

at FAIR/GSI. It is simultaneously addressing a wider panel of applications, including in particular tracking devices suited to a future Higgs-top factory, for which the design of MIMOSIS acts as a forerunner of a dedicated sensor.

The first full scale prototype, MIMOSIS-1, was fabricated in 2020, offering a 4.2 cm2 wide sensitive area composed of  $1024 \times 504$  pixels with integrated discrimination. Read out in 5 us, the sensor incorporates a data processing circuitry adapted to local hit densities of up to 100 MHz/cm2. To search for

an optimised sensor design, the prototype is composed of several alternative in-pixel micro-circuit flavours and was manufactured with various doping profiles of the 25 um thick epitaxial layer.

The detection performances associated to each pixel and epitaxy variant were examined with 60 um thin sensors exposed to minimum ionising particle beams. Detection efficiencies of 99.9 % were repeatedly observed over a wide range of threshold values and a spatial resolution close to 4 um was derived for the lowest threshold settings. Moreover, specific studies of the front-end circuitry suggest that a read-out time shorter than 1 us is achievable.

Based on these results, a more advanced prototype, MIMOSIS-2, is being sent for fabrication, based on thicker epitaxial layers expected to benefit to the spatial resolution. Its fabrication will be accompanied with a separate, smaller, prototype composed of 64x504 pixels based on a modified FE circuitry adapted to a read out shorter than 1 us, prefiguring a fast version of MIMOSIS addressing the requirements of a vertex detector suited to FCCee.

Besides the development of MIMOSIS, the potential of using the emerging 65 nm TPSCo CMOS process is also being evaluated at IPHC, essentially in partnership with the ALICE teams developing the ITS-3 vertex detector based on the novel

concept of nearly cylindrical and almost unsupported detector layers. IPHC is developing pixel arrays of 15 and 25 um pitch in this technology, with various sensing system and FE electronics designs. It is also contributing to the design of the first large, stitched, prototypes anticipated to be fabricated in Summer-Fall 2022. Moreover, efforts are also on-going for the

development of curved cylindrical detector layers such as those developed for the ITS-3.

The contribution to the workshop will first address the performances of MIMOSIS and the perspective it opens up with its faster read-out option for a vertex detector suited to Higgs-top factory experiments. It will next discuss the

status and potential of the 65 nm process wrt charged particle detection, examining its added value wrt the MIMOSIS development. Finally, a vertex detector concept derived from the ITS-3 design will be sketched. The talk will repeatedly address the issue of power saving, which will appear as a common thread of the underlying prospect.

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