Overview of silicon tracking and vertexing R&D in view of FCC-ee

Exploiting the evolution of CMOS pixels sensors and their services

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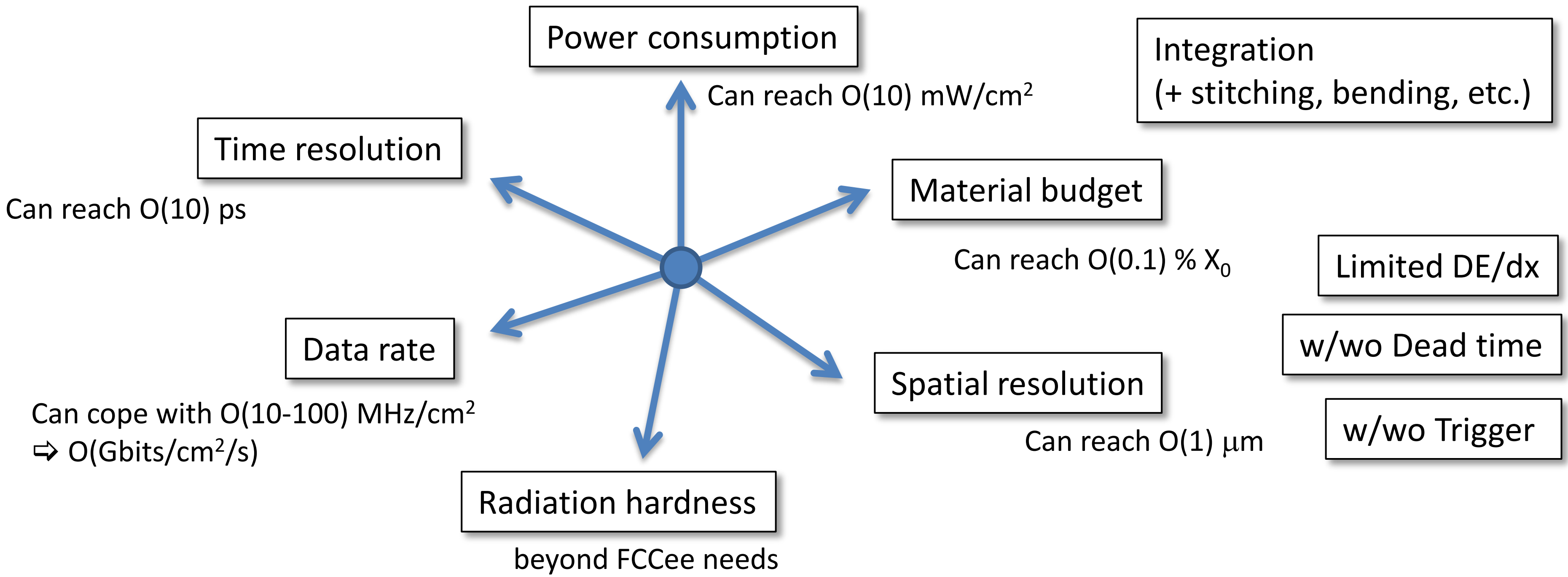
(IPHC-Strasbourg)

Inputs from CBM-MVD collaboration, ALICE ITS3, IPHC (PICSEL & C4PI)

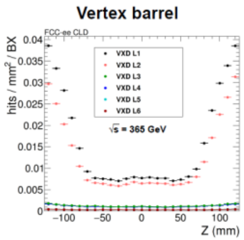
Silicon tracking detector figure of merit

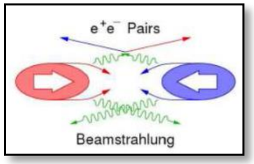


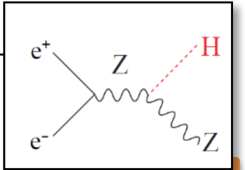
- Ultimate performances look like the ideal tracking or vertexing detector. However
  - ✓ Very precise ⇨ not that fast
  - ✓ Very fast ⇨ large pitch and/or large Power
- Need a **hierarchy** or **specialized** layers
  - ✓ Governed by physics requirements and experimental conditions @FCCee
  - ✓ Fast timing and small granularity/low material budget are very antagonist
  - ✓ R&D needed to improve the parameter space

	Z	Higgs	ttbar
√s [GeV]	91.2	240	365
Luminosity / IP ($10^{34}cm^{-2}s^{-1}$)	230	8.5	1.7
no. of bunches / beam	16640	393	48
Bunch separation (ns)	20	994	3000

FCCee Vertex detector requirements





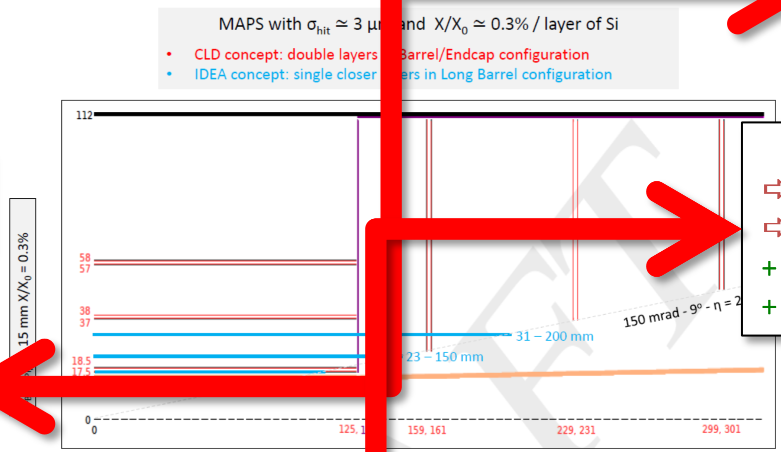


Physics
- ⇨ Flavour tagging
- ⇨ Low pT tracks
- ⇨ Vertex/Jet charge determination

Physics O(Hz/cm²)

Beam background O(10-50 MHz/cm²)

CLD and IDEA Vertex Detectors designs (superimposed)



(Figure: D. Contardo)

Vertex reconstruction
- ⇨ granularity
- ⇨ Pitch ~17-20 µm
- ⇨ (σ_{sp} ~3-4 um)

Material Budget
- ⇨ ~ 0.15% X_0 / layer
- ⇨ < 1% X_0 for the whole VTX
- + ~0.3 % X_0 for the beam pipe
- + 0.15% X_0 for 5 µm Gold coating

Beam background

Radiation hardness
O(100kRad/yr) & O(10^{11})n_{eq}/yr

Rad.Tol. devices

Time resolution
O(1 µs)

Power consumption
~< 50mW/cm²

Fast read-out & low Power Architectures (~ 20 mW/cm²)

No Power pulsing @FCCee

Cooling
Stiffness / Alignment

Low material detectors & supports structures

$$\sigma_{d_0} = a \oplus \frac{b}{p \sin^{3/2}\theta}$$

$a \simeq 5\,\mu m$ $\quad b \sim 15\,\mu m.GeV$

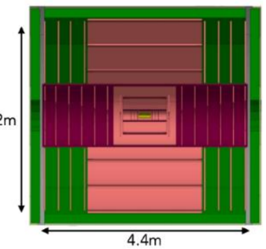
5 single layers or 3 double layers ?
Inner (1.7 cm or lower ?) and outer radius are key factors

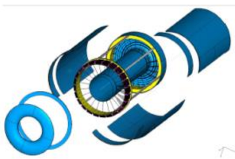
Tracking requirements

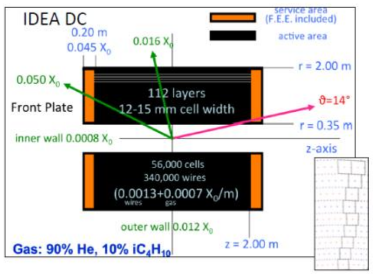
Central tracker

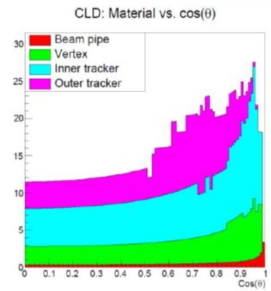
Two solutions under study

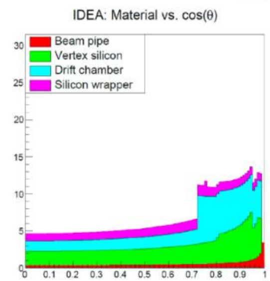
- CLD: All silicon pixel (innermost) + strips
  - Inner: 3 (7) barrel (fwd) layers (1% X_0 each)
  - Outer: 3 (4) barrel (fwd) layers (1% X_0 each)
  - Separated by support tube (2.5% X_0)
- IDEA: Extremely transparent Drift Chamber
  - GAS: 90% He – 10% iC_4H_{10}
  - Radius 0.35 – 2.00 m
  - Total thickness: 1.6% of X_0 at 90°
    - Tungsten wires dominant contribution
  - Full system includes Si VXT and Si "wrapper"











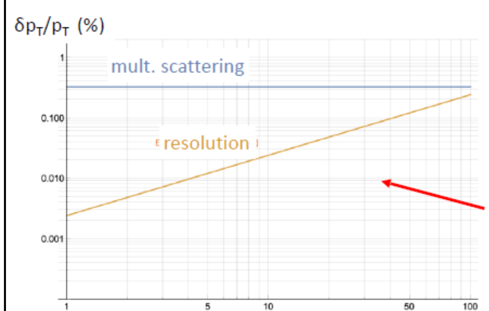
30/11/2021 Detector concepts for FCC-ee - Paolo Giacomelli 6

Paolo Giacomelli (Annecy 2021)

In reality, there is of course a resolution term (*a*) and a multiple scattering term (*b*)

$$\sigma(p_T)/p_T^2 = a \oplus \frac{b}{p\sin\theta}$$

For "standard" ultra-light detectors (e.g. full Si), multiple scattering dominates up to p_T of ~100 GeV



Here illustrated for the CLD detector at 90°:
Total material budget = 11% of X_0

From analytic expressions for track parameter resolutions.

Drasal, Riegler, https://doi.org/10.1016/j.nima.2018.08.078

$$\frac{\Delta p_T}{p_T}\Big|_{m.s.} \approx \frac{0.0136\,\mathrm{GeV}/c}{0.3\beta\, B_0 L_0}\sqrt{\frac{d_{tot}}{X_0\sin\theta}} \qquad \frac{\Delta p_T}{p_T}\Big|_{res.} \approx \frac{12\,\sigma_{r\phi}\, p_T}{0.3\, B_0 L_0^2}\sqrt{\frac{5}{N+5}}$$

Often, the "canonical" requirement is expressed as

$$\sigma_{p_T}/p_T^2 \simeq 2\times10^{-5}\,\mathrm{GeV}^{-1}$$

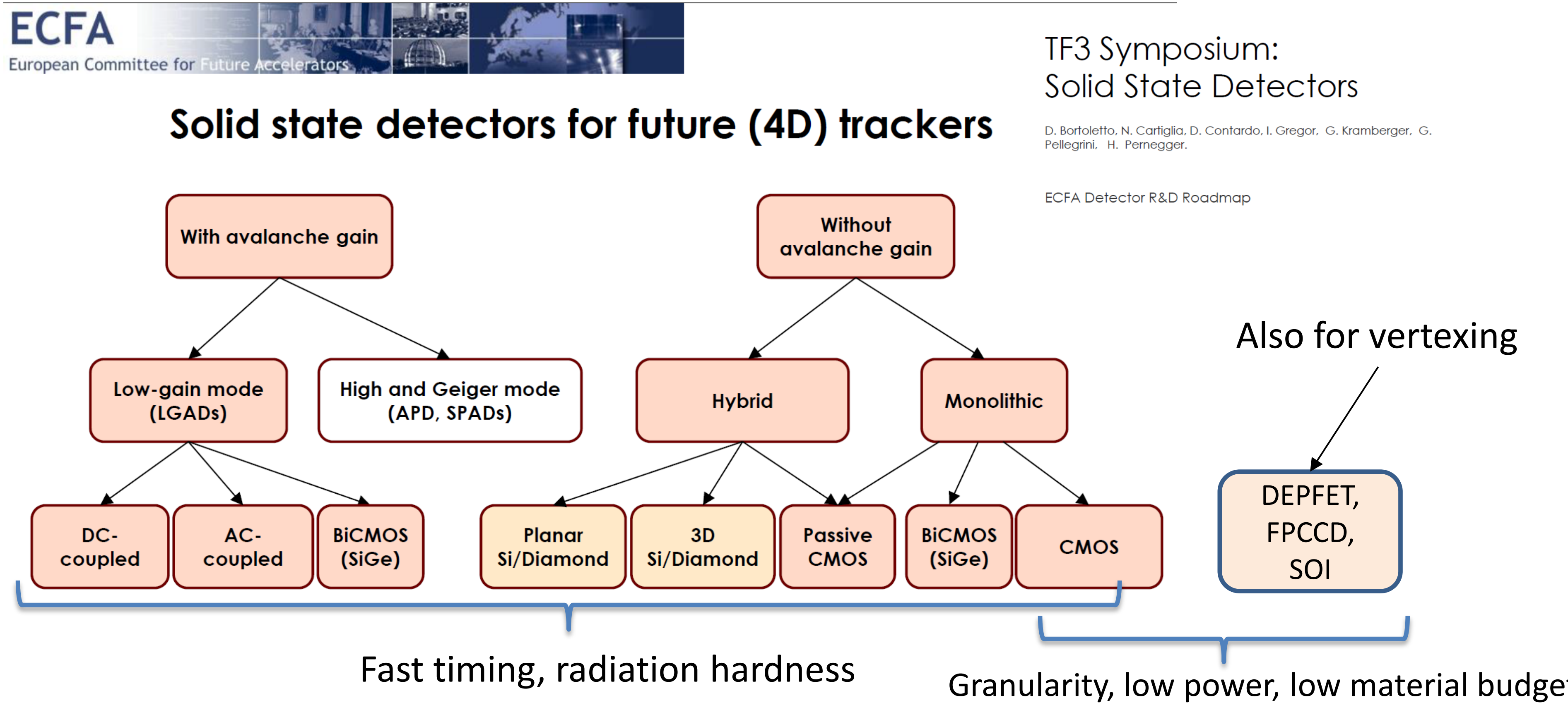
Questions:

- Is material budget mapping realistic ?
- Gaseou vs silicon ?
- Low or high momentum priority ?
- Standalone tracking capabilities at low radius ?

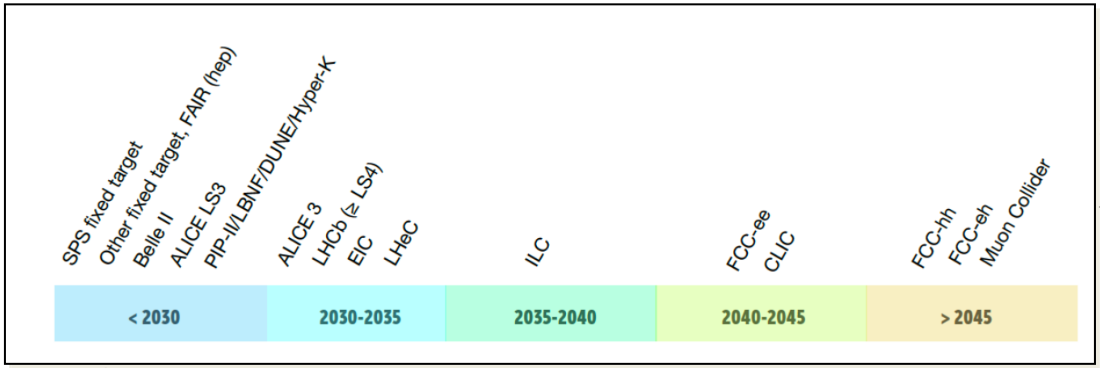
Silicon Detectors landscape

- A very active area. e.g. see
  - ✓ 2021: ECFA Detector R&D Roadmap Symposium of Task Force 3 Solid State Detectors
  - ✓ 2022: VCI 16th Vienna conference
  - ✓ 2022: 15th Pisa Meeting on Advanced Detectors
  - ✓ 2022: AIDAInnova Kick-off meeting
  - ✓ ALICE ITS-3 CERN Detector seminar (M. Mager)

(Most materials stolen from there)

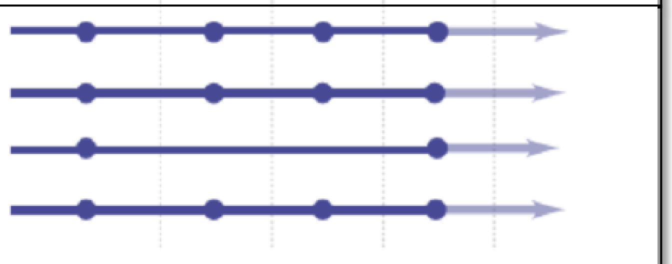


Detector R&D Roadmap: themes (DRDTs)



References: ECFA/RC/21/510
CERN-ESU-017
DOI: 10.17181/CERN.XDPL.W2EX

Solid state		< 2030	2030-2035	2035-2040	2040-2045	> 2045
DRDT 3.1	Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors					
DRDT 3.2	Develop solid state sensors with 4D-capabilities for tracking and calorimetry					
DRDT 3.3	Extend capabilities of solid state sensors to operate at extreme fluences					
DRDT 3.4	Develop full 3D-interconnection technologies for solid state devices in particle physics					



DRDT 3.1 - Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors.
Developments of Monolithic Active Pixel Sensors (MAPS) should achieve very high spatial resolution and very low mass aiming to also perform in high fluence environments. To achieve low mass in vertex and tracking detectors, thin and large area sensors will be crucial. For tracking and calorimetry applications MAPS arrays of very large areas, but reduced granularity are required for which cost and power aspects are critical R&D drivers. Passive CMOS designs are to be explored, as a complement to standard sensors

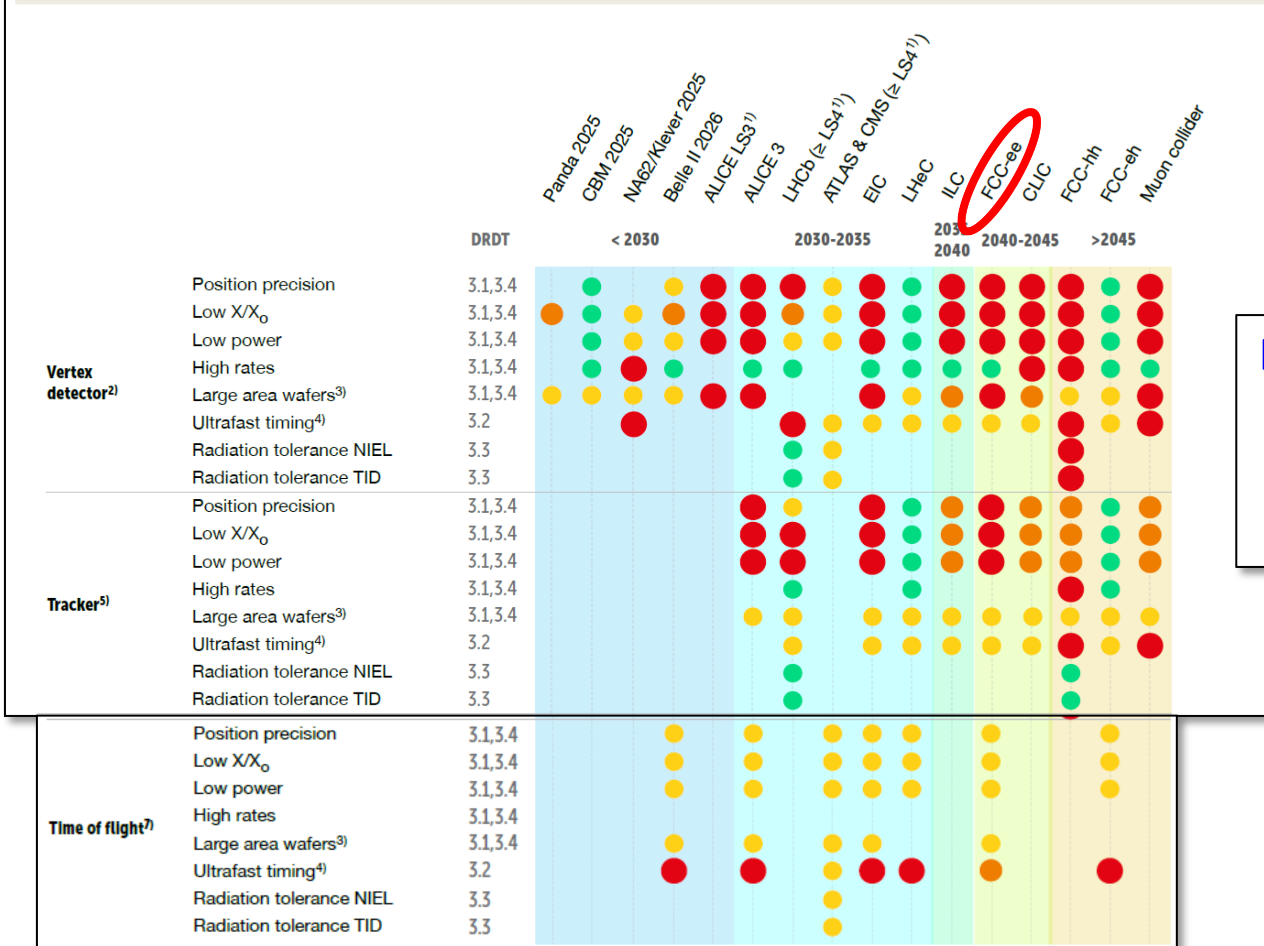
DRDT 3.2 - Develop solid state sensors with 4D-capabilities for tracking and calorimetry.
Understanding of the ultimate limit of precision timing in sensors, with and without internal multiplication, requires extensive research together with the developments to increase radiation tolerance and achieve 100%-fill factors. New semiconductor and technology processes with faster signal development and low noise readout properties should also be investigated.

Synergies

ECFA recognizes the need for the experimental and theoretical communities involved in physics studies, experiment designs and detector technologies at future Higgs factories to gather. ***ECFA supports a series of workshops*** *with the aim to* ***share challenges and expertise, to explore synergies in their efforts*** *and to respond coherently to this priority in the European Strategy for Particle Physics (ESPP).*

Goal: bring the entire e^+e^- Higgs factory effort together, foster cooperation across various projects; collaborative research programmes are to emerge

K. Jakobs, FCC Physics Workshop, Feb 2022

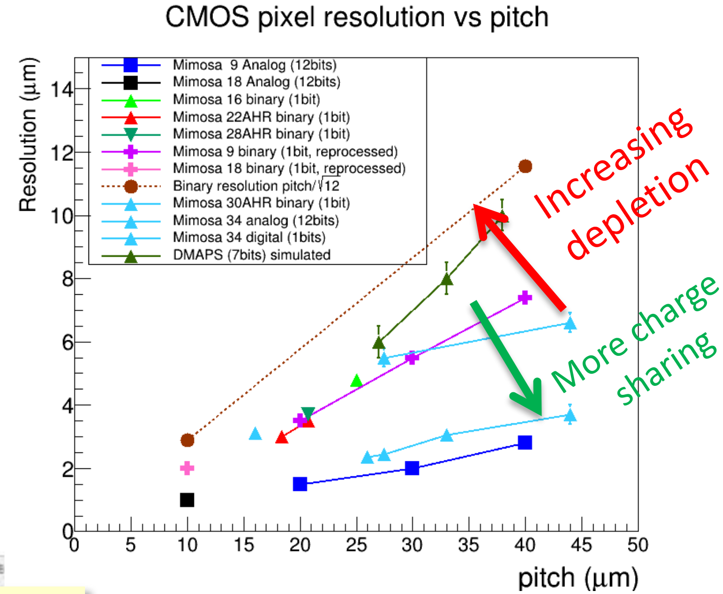


Must happen or main physics goals cannot be met · Important to meet several physics goals · Desirable to enhance physics reach · R&D needs being met

Important similarities between FCCee requirements & Heavy ions experiments (ALICE ITS3, ALICE3, EIC, etc.)

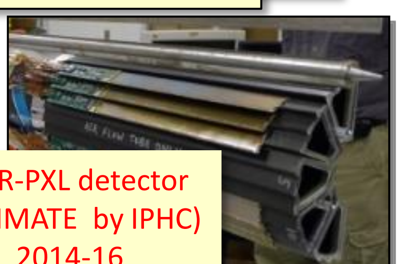
Granular and thin detectors: CMOS pixels sensors

- Single point resolution σ_{sp}
  - ✓ Small pitch limits in pixel circuitry
    - Impact hit rate or time resolution
  - ✓ Binary charge encoding
    - σ_{sp} ~ 3-4 µm ⇦⇨ pitch ~< 20 µm
  - ✓ Charge sharing & encoding (TOT, ADC)
    - Larger pitch needed
- CMOS sensors widely used in HEP



Process: 350 nm

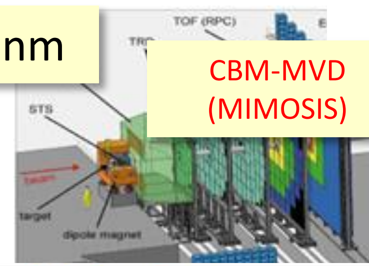
EUDET beam telescope (Mimosa 26) ~ 15 copies since 2009



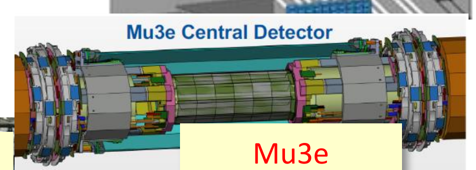
STAR-PXL detector (ULTIMATE by IPHC) 2014-16

O(100 µs)

Process: 180 nm



CBM-MVD (MIMOSIS)



Mu3e

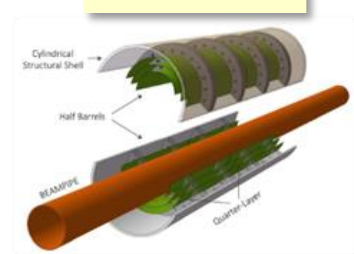
ALICE-ITS2 (ALPIDE)

ITS2 outer barrel, picture M. Mager

O(10 µs)

Process: 65 nm

ALICE-ITS3



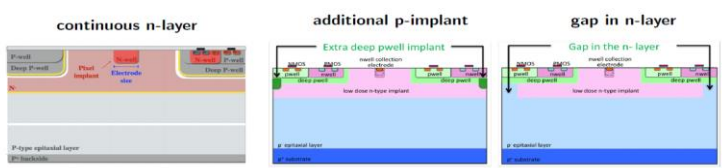
O(1 µs)

Example of trade off: MIMOSIS

- MIMOSIS-1 chip for CBM-MVD @ FAIR

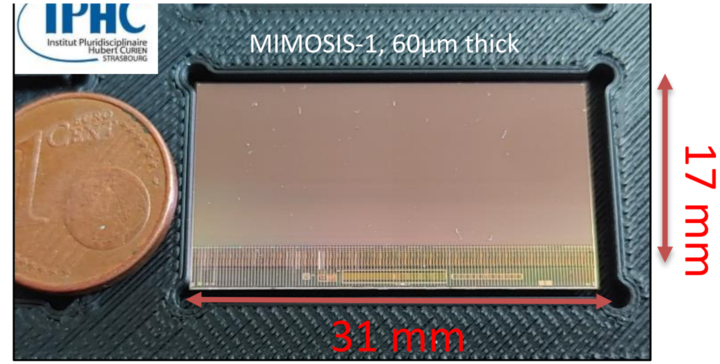
Parameter	Value
Technology	TowerJazz 180 nm
Epi layer	$\sim 25\,\mu m$
Epi layer resistivity	$> 1 k\Omega cm$
Sensor thickness	$60\,\mu m$
Pixel size	$26.88\,\mu m \times 30.24\,\mu m$
Matrix size	1024×504 (516096 pix)
Matrix area	$\approx 4.2\,cm^2$
Matrix readout time	$5\,\mu s$ (event driven)
Power consumption	40-70 mW/cm^2

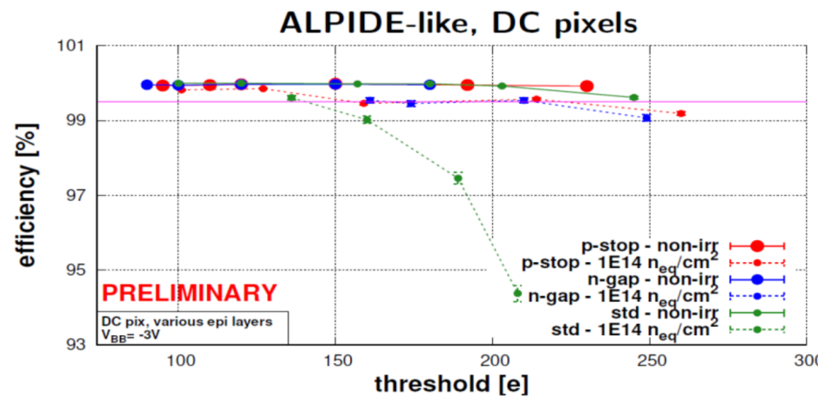
  - ✓ Based on ALPIDE architecture
    - Multiple data concentration steps
    - Elastic output buffer
    - 8 x 320 Mbps links (switchable)
    - Triple redundant electronics
  - ✓ Pixel variants: DC/AC (top bias up to >20V)
  - ✓ Different epitaxial variants tested

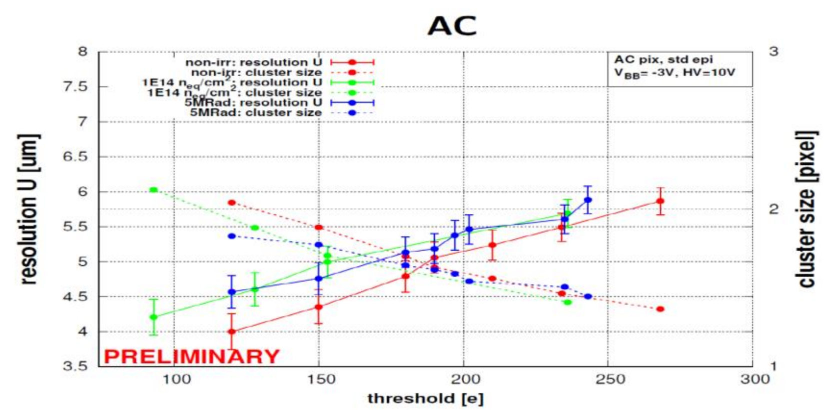


Pic from: Munker, Vertex 2018, Status of silicon detector R&D at CLIC
Carlos, TREDI 2019, Results of the Malta CMOS pixel detector prototype for the ATLAS Pixel ITK

- Intense test beam campaign (2021-22)
  - ✓ Mimosis-2 submission these weeks
    - Thicker epi layer tests
    - Test prototype for 1 µs readout time



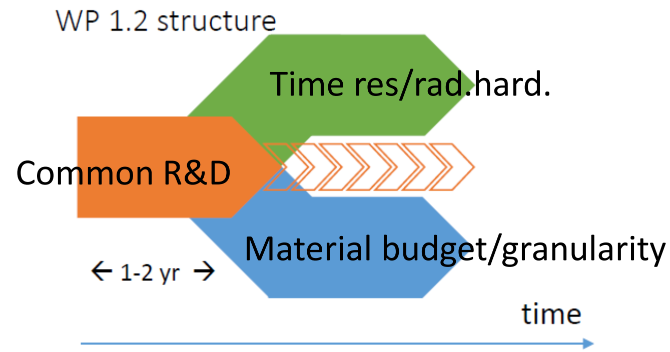


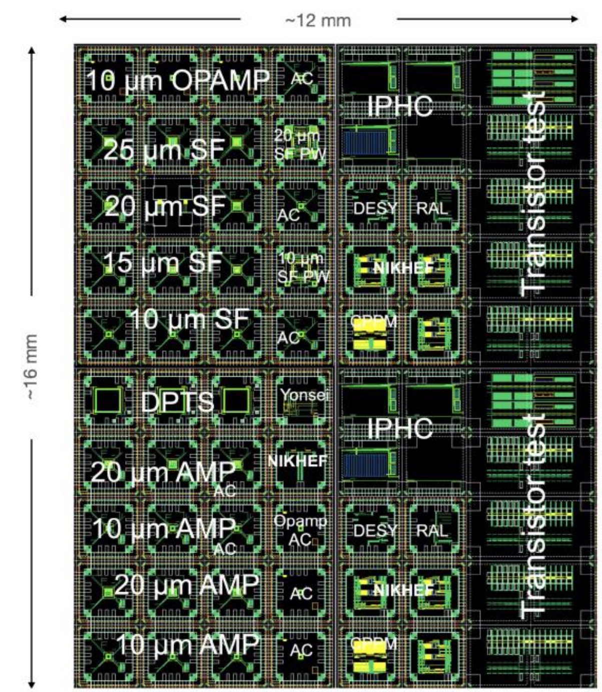


MIMOSIS = a milestone for Higgs factories (5 µm / ≤5 µs)

TJ-65 nm process: smaller feature size

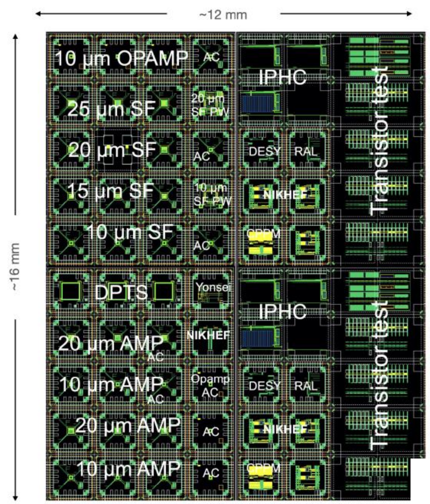
- 65 nm feature size technology
  - ✓ (ALPIDE & MIMOSIS fabricated in 180 nm)
  - ✓ Larger wafers (➪ 30 cm)
  - ✓ More functionalities inside the pixel
  - ✓ Keeps pixel dimensions small ➪ spatial res.
  - ✓ Potentially faster read-out
  - ✓ Lower Power consumption
- **TJ-65 nm 1st submission (MLR1)**
  - ✓ Main driver: CERN EP R&D WP 1.2 & ALICE ITS-3 upgrades
    - Privileged Relation between CERN with the foundry (access to options is a key factor)
  - ✓ Goal: **validate the process for charged particle detection**
    - First submission: MLR1 (Q4 2020)
    - Synergy with Higgs factories requirements

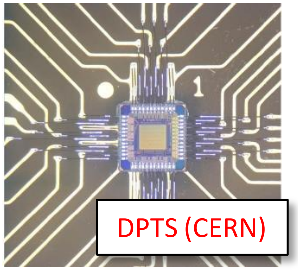


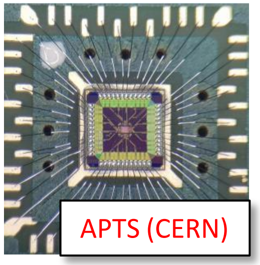


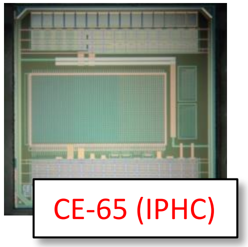
65nm MLR1

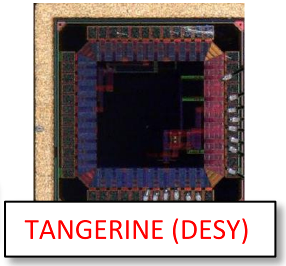
- Technology exploration
- Various pixel matrices and test structures
  - ✓ Radiation test structures
  - ✓ Amplification, DACs, LVDS, etc.
  - ✓ Pitch 15-25 um
  - ✓ Epi variants

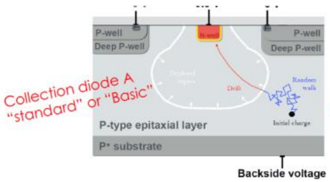


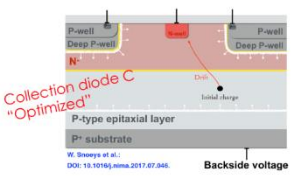

DPTS (CERN)


APTS (CERN)


CE-65 (IPHC)


TANGERINE (DESY)





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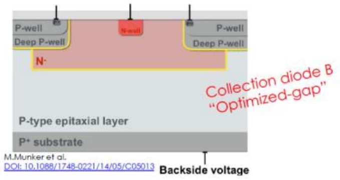
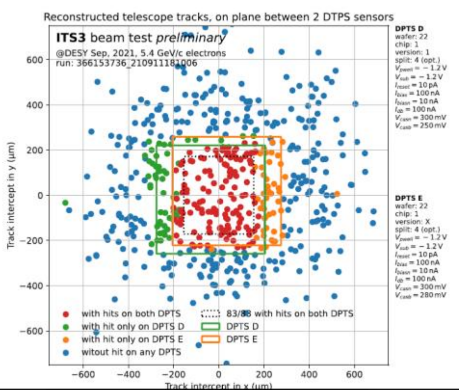
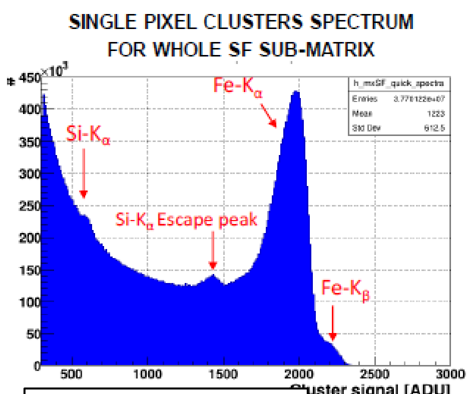




DPTS in test beam

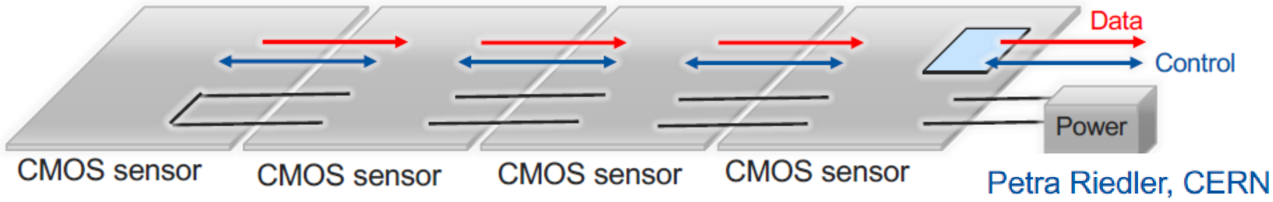


CE_65 with ^{55}Fe

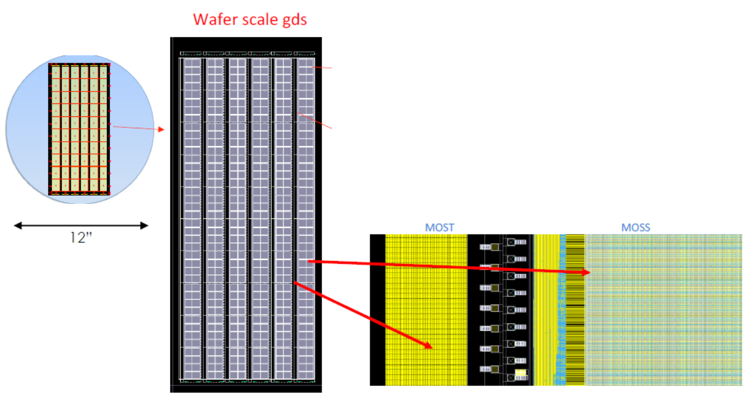
- Promising results
  - ✓ Excellent charge collection efficiency
  - ✓ no showstopper
  - ✓ Beam test performances analysis ongoing

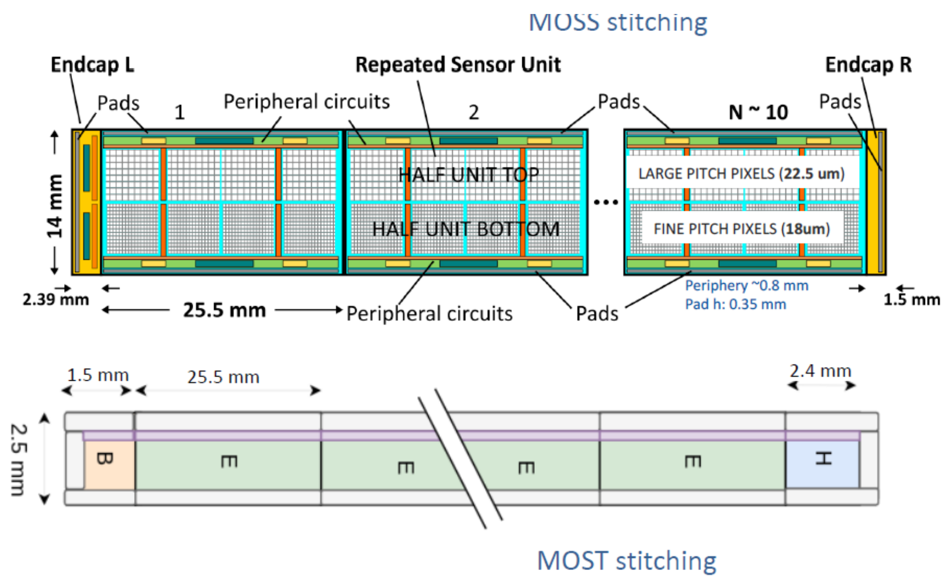
65nm future plans

Overcoming the reticle size limitation ⇨ stitching



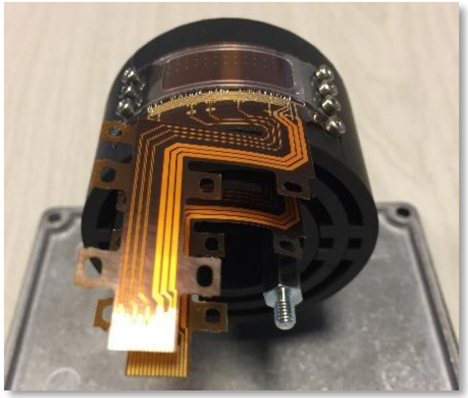
- Next submission: ER1 (2022)
    - CERN EP R&D WP 1.2 & ALICE ITS-3 upgrades (Submission: Q2 2022)
    - Monolithic Stitched Sensor (MOSS) driven by CERN
- ✓ Goal: study Stitching and interconnection (wafer scale)
    - Yield, Power distribution, signal routing, Noise, etc.

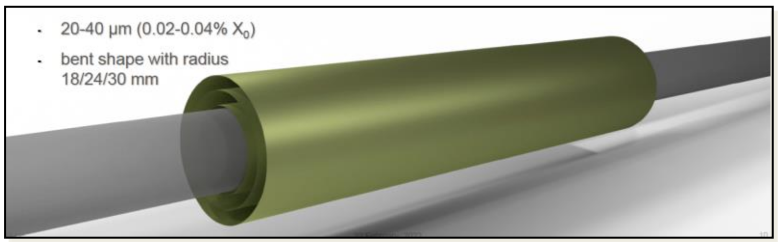


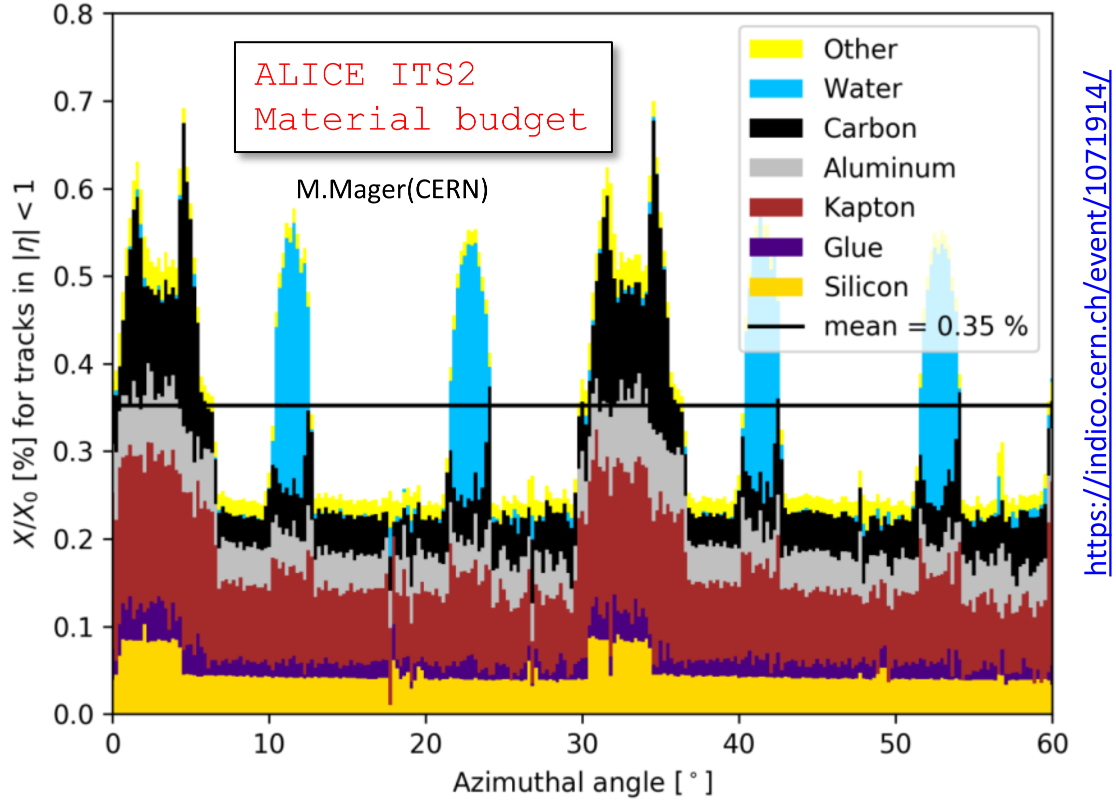


- Beyond ER1 ⇨ ER2 (2022-23) dedicated to ITS-3

ALICE ITS3: Bent sensors & stitching





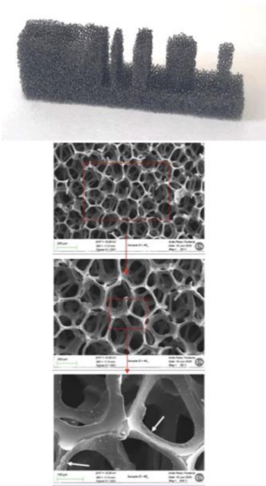


- Stitching + bent sensors:
  - ✓ Sensor part ~15% of total material budget
  - ✓ Minimizing overlapping regions, minimizing minimal radius around the beam pipe
- ALICE-ITS3/CERN drives the R&D
  - ✓ Cf. M. Mager CERN Seminar
- Challenges
  - ✓ Mechanics ? Bonding ? Air cooling only ?
  - ✓ Design: Minimizing peripheral circuits (Fill factor)
  - ✓ Bent sensor performances ? Yield ?

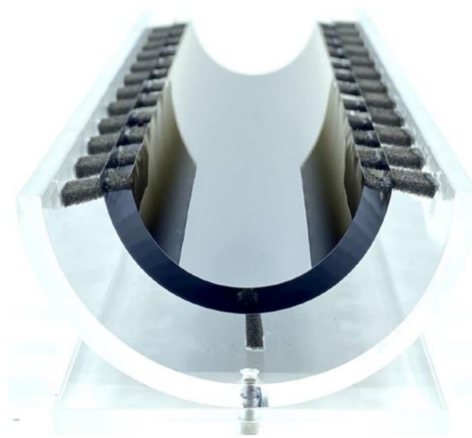
ALICE ITS3 tests

A. Kluge
on behalf of the ALICE collaboration
22 February, 2022
VCI

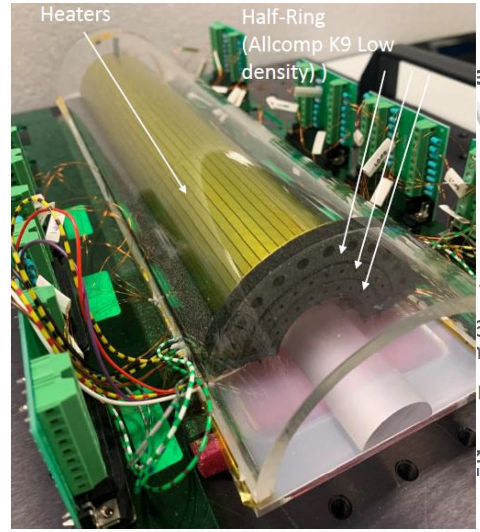
ERG DUOCEL_AR
0.06 kg/dm³
0.033 W/m·K

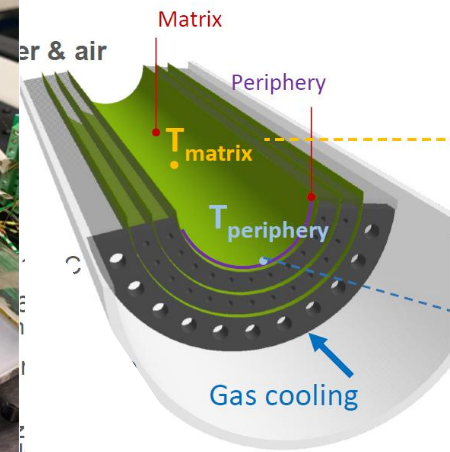


Layers 2+1

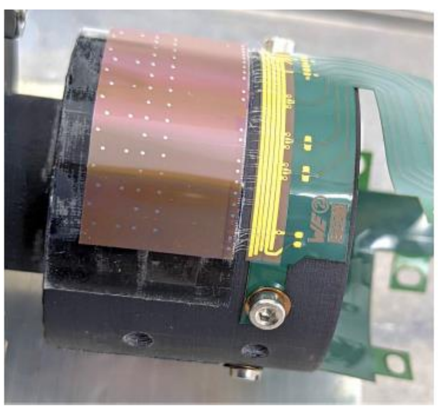


Carbon fiber foam spacer





Integration and cooling studies



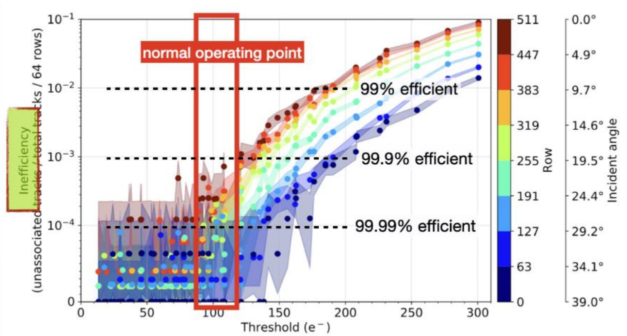
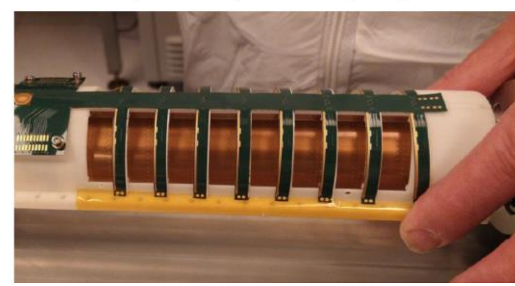
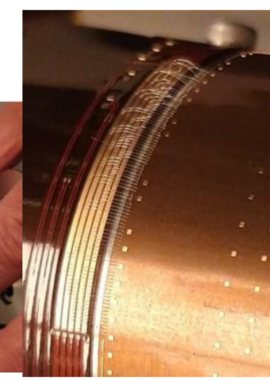


Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. Each data point corresponds to at least 8k tracks.

Bent sensors in test beam

- 1 silicon piece cut from one ALPIDE wafer (9x2 dies, ~1/2 of layer 0)





Inteconnexion tests (superALPIDE)

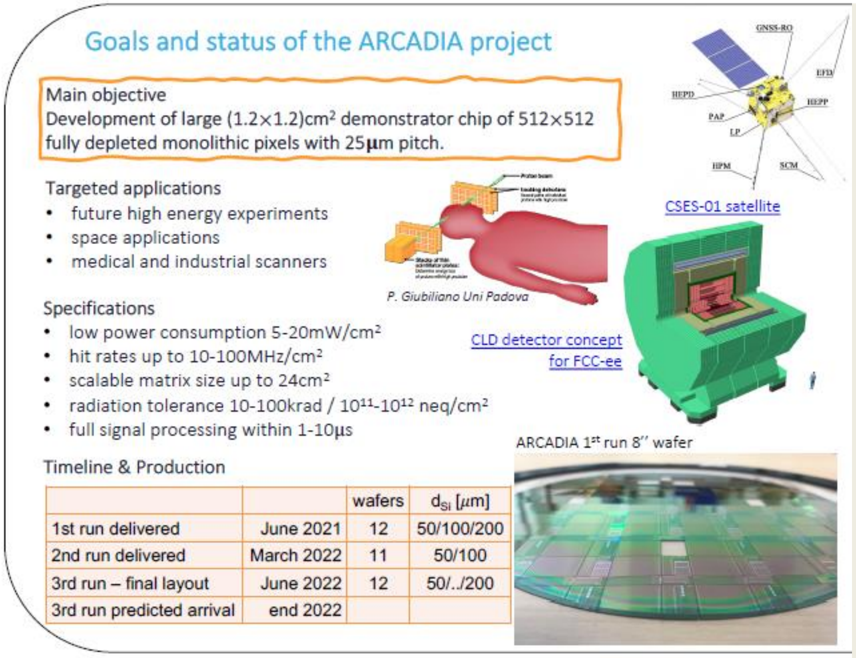
On going experiments pave the road for FCCee detectors
(many other examples, e.g. BelleII)

Example of R&D: Arcadia

ARCADIA

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

https://arxiv.org/pdf/2011.09723.pdf



Goals and status of the ARCADIA project

Main objective
Development of large (1.2×1.2)cm² demonstrator chip of 512×512 fully depleted monolithic pixels with 25µm pitch.

Targeted applications
- future high energy experiments
- space applications
- medical and industrial scanners

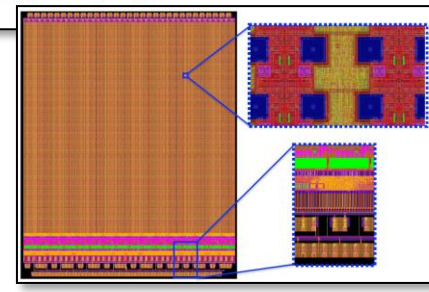
Specifications
- low power consumption 5-20mW/cm²
- hit rates up to 10-100MHz/cm²
- scalable matrix size up to 24cm²
- radiation tolerance 10-100krad / 10^{11}-10^{12} neq/cm²
- full signal processing within 1-10µs

Timeline & Production

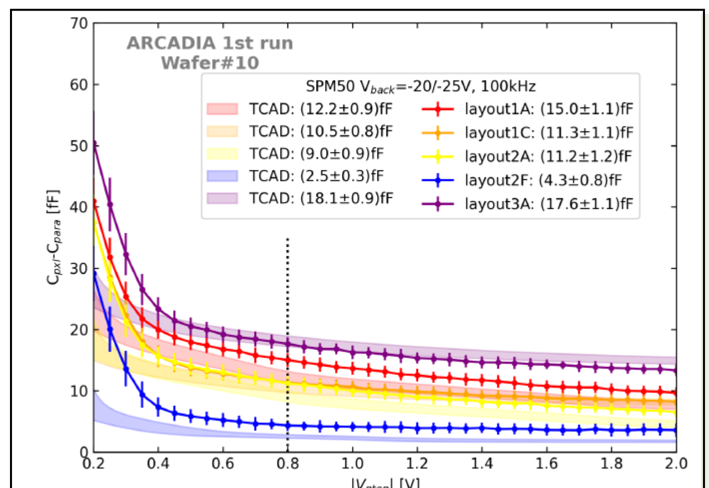
		wafers	d_{Si} [µm]
1st run delivered	June 2021	12	50/100/200
2nd run delivered	March 2022	11	50/100
3rd run – final layout	June 2022	12	50/../200
3rd run predicted arrival	end 2022		

Main Demonstrator (MD) chip

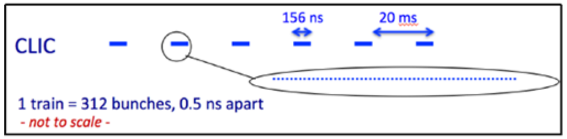
- matrix core 512×512 pixels of 25µm pitch
- pixels are ~(50/50)% analogue/digital
- 2 types of front-ends
- sensor diode about 20% of total area
- clock-less matrix (to minimize power dissipation)
- global shutter with serial readout
- output fully digital



- Technology validation: L-Foundry (110nm)
  - ✓ Goal for FCCee: low power, fully depleted CMOS
- TCAD simulations
  - ✓ (pixel optimization, charge sharing, radiation hardness etc.)
- Small prototypes (SEED, MATISSE prototypes)
  - ✓ Various pixels sizes and sensor thicknesses
- 1st Large prototype: MD prototype
  - ✓ Low power read-out architecture exploration
  - ✓ Functional. Tests ongoing
  - ✓ More results expected @ IWORID2022



R&D in CLICdp context

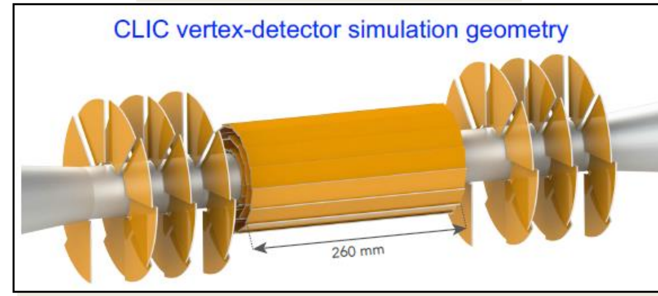


Linear

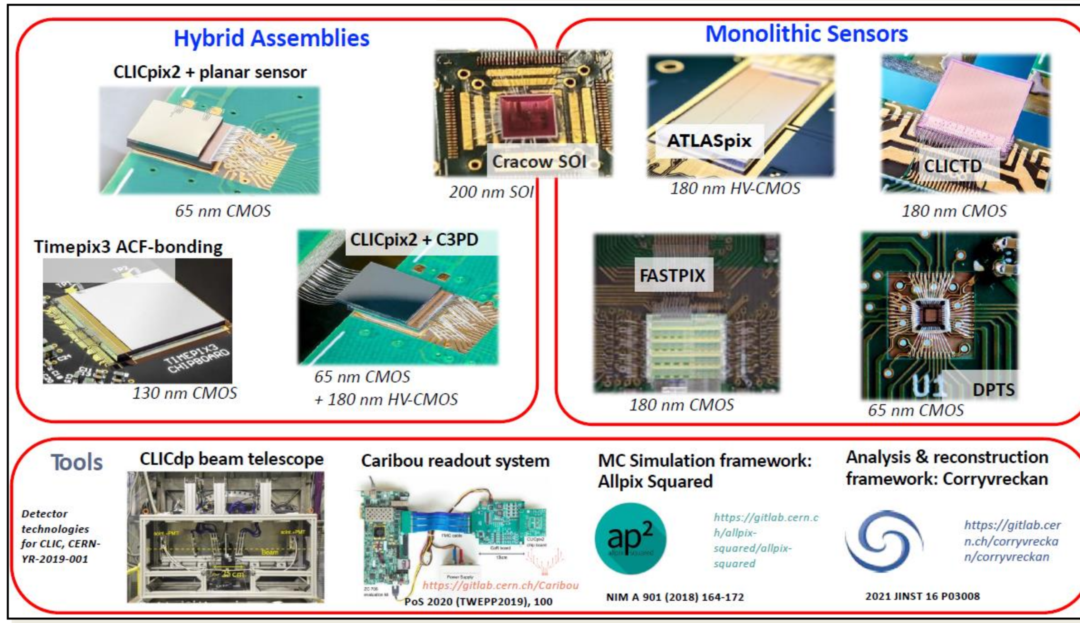
	ILC		CLIC		
Parameter	250 GeV	500 GeV	380 GeV	1.5 TeV	3 TeV
Luminosity L (10^{34}cm^{-2}sec^{-1})	1.35	1.8	1.5	3.7	5.9
L > 99% of √s (10^{34}cm^{-2}sec^{-1})	1.0	1.0	0.9	1.4	2.0
Repetition frequency (Hz)	5	5	50	50	50
Bunch separation (ns)	554	554	0.5	0.5	0.5

VCI2022 – The 16th Vienna Conference on Instrumentation
February 24th, 2022

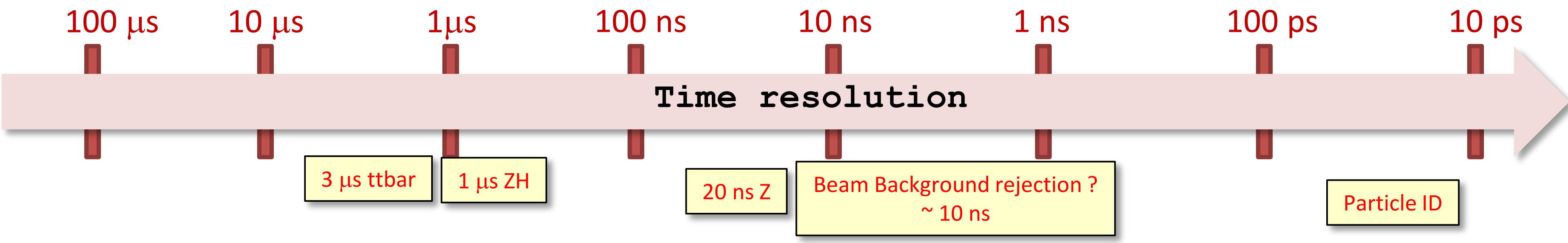
Dominik Dannheim (CERN)
on behalf of the CLICdp collaboration



- Different requirements w.r.t. FCCee
  - ✓ Shorter time resolution needed O(ns)
  - ✓ Power pulsing relaxes instantaneous Power consumption constraints
- Generic tools
  - ✓ Software (Allpix^2, Corryvreckan)
  - ✓ Hardware (Caribou read out system)
- Hybrid R&D
  - ✓ CLICpix2
    - Time (8bits) and
    - Charge (5bits)
  - ✓ Anisotropic Conductive Film (ACF)
    - adhesive epoxy & conductive microparticles
- CMOS R&D
  - ✓ CLICTD
  - ✓ Fastpix (ATTRACT)
    - Subns timing
  - ✓ 65 nm (DPTS)

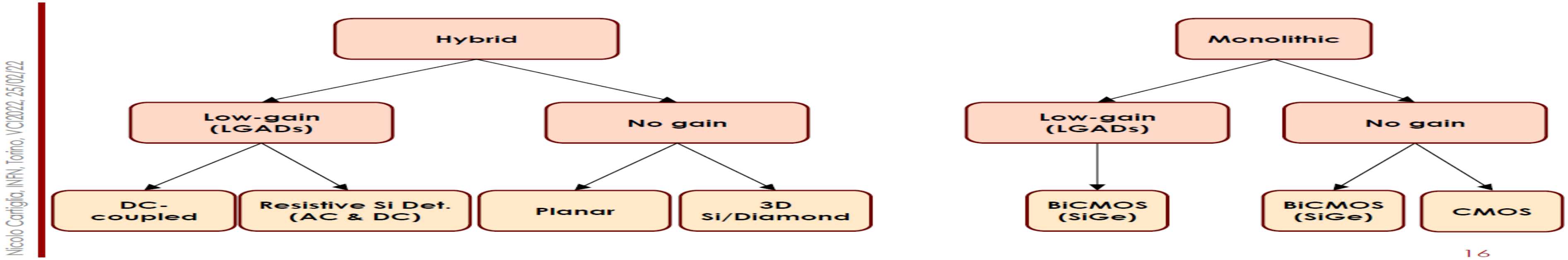


Timing & 4-D tracking

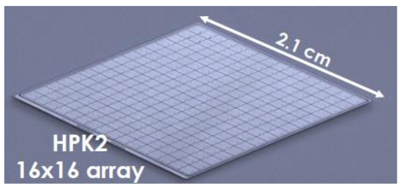


- Time resolution Δt
  - ✓ Bunch separation (3 μs / 1 μs / 20 ns)
  - ✓ Background rejection ?
  - ✓ Particle ID (<50-100 ps)
- Usual drawbacks
  - ✓ Power consumption
  - ✓ Active Cooling & geometrical acceptance due to services
  - ✓ In pixel circuitry ⇨ larger pixels (or multipixels)
  - ✓ Fill factor, dead time
  - ✓ PID Restricted to low momentum particles (~< few GeV/c)
- Still
  - ✓ Forward region not covered by a central gazeous detector
  - ✓ Added value for intermediate radii (LLPs ?)

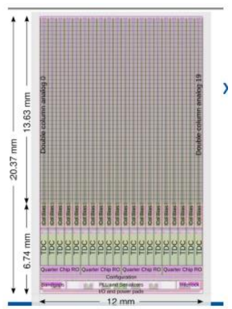
Timing Landscape



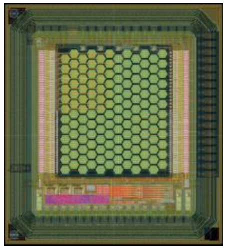
Low gain to minimize jitter



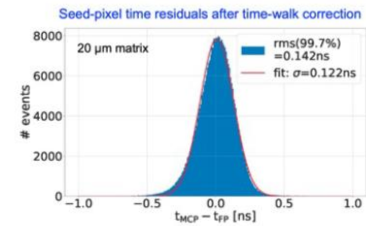
CMS & ATLAS
(LGAD DC coupled)



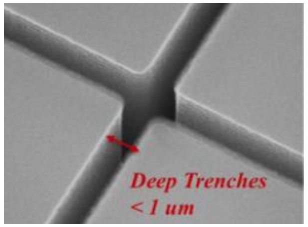
NA62 Gigatracker
(planar)



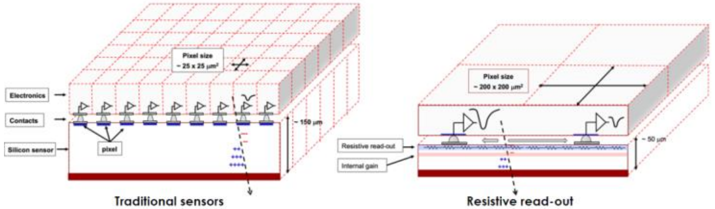
MonPicoAd
(BiCMOS)



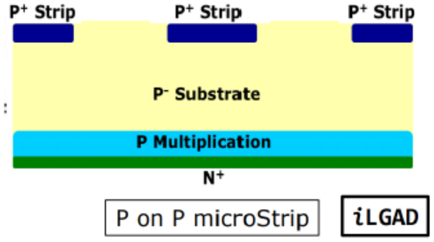
FastPix
(CMOS)



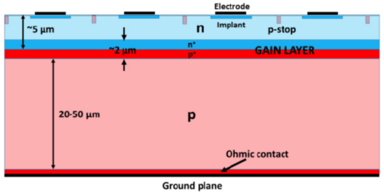
Trench Isolated-LGAD
(reduces no gain region)



Resistive read-out
AC-LGADS
(signal sharing)



Inverse ILGAD



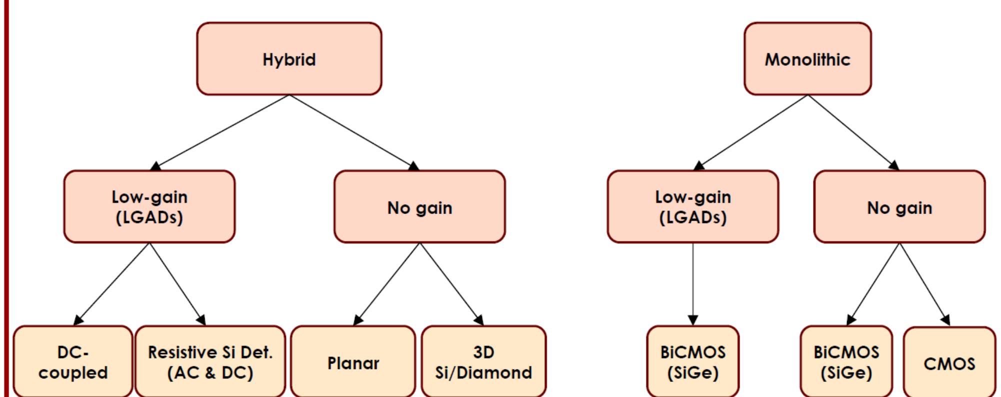
Deep Junction
DJ-LGAD

Power vs fast timing vs pixel size

Brief considerations about electronics: power

Name	Sensor	node	Pixel size	Temporal precision [ps]	Power [W/cm²]
ETROC	LGAD	65	1.3 x 1.3 mm²	~ 40	0.3
ALTIROC	LGAD	130	1.3 x 1.3 mm²	~ 40	0.4
TDCpic	PiN	130	300 x 300 µm²	~ 120	0.45 (matrix) + 2 (periphery
TIMEPIX4	PIN, 3D	65	55 x 55 µm²	~ 200	0.8
TimeSpot1	3D	28	55 x 55 µm²	~ 30 ps	5-10
FASTPIX	monolithic	180	20 x 20 µm²	~ 130	40
miniCACTUS	monolithic	150	0.5 x 1 mm²	~ 90	0.15 – 0.3
MonPicoAD	monolithic	130 SiGe	25 x 25 µm²	~ 36	40
Monolith	LGAD monolithic	130 SiGe	25 x 25 µm²	~ 25	40

Nicolo Cartiglia, INFN, Torino, VCI2022, 25/02/22



Price to pay: additionnal cooling system (addtionnal material)

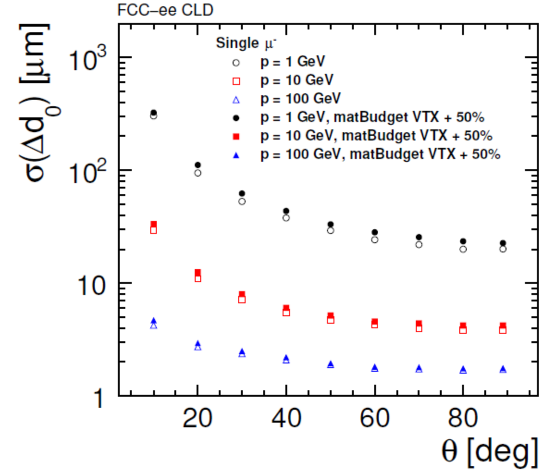
Inner tracking detector concept @ FCCee

- Progress in material budget optimization
  - ✓ Double sided layers approach may be replaced by stiched+bent sensors (à la ALICE ITS3) in the inner radius
- The beam pipe sets the limits
  - ✓ Beam pipe + cooling + Au coating ~ 0.45% X_0
  - ✓ Reducing the inner radius could compensate

$$\sigma_{d0}{}^2 = a^2 + \left(\frac{b}{p.\sin^{3/2}\theta}\right)^2$$

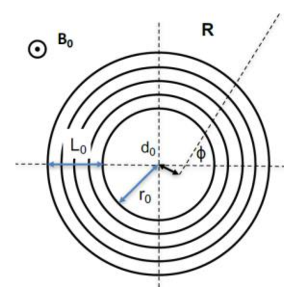
$$\Delta d_0|_{m.s.} \approx \frac{0.0136\,\mathrm{GeV/c}}{\beta p_T} r_0 \sqrt{\frac{d}{X_0 \sin\theta}} \sqrt{1 + \frac{1}{2}\left(\frac{r_0}{L_0}\right) + \frac{N}{4}\left(\frac{r_0}{L_0}\right)^2}$$

$$\Delta d_0|_{res.} \approx \frac{3\sigma_{r\phi}}{\sqrt{N+5}} \sqrt{1 + \frac{8r_0}{L_0} + \frac{28r_0^2}{L_0^2} + \frac{40r_0^3}{L_0^3} + \frac{20r_0^4}{L_0^4}}$$



(a) d_0 resolution

- Granular layers
  - ✓ Target: a design reaching 1µs/3µm/~<50mW/cm²
  - ✓ Still R&D efforts to be made (65 nm process)
  - ✓ The « Power paradox »
    - Small radius ⇨ Higher hit density and Power/cm²
    - Higher radius ⇨ higher total power/layer



- Timing layer
  - ✓ Probably somewhere at a mid range radius O(10-20 cm)
    - (1-2 layers ?)

Summary

- Apologies for not covering
  - ✓ Many technologies and on going R&D
    - (FPCCD, SOI, DEPFET, BiCMOS (SiGe), etc.
  - ✓ Cooling R&D (MCC, etc.)

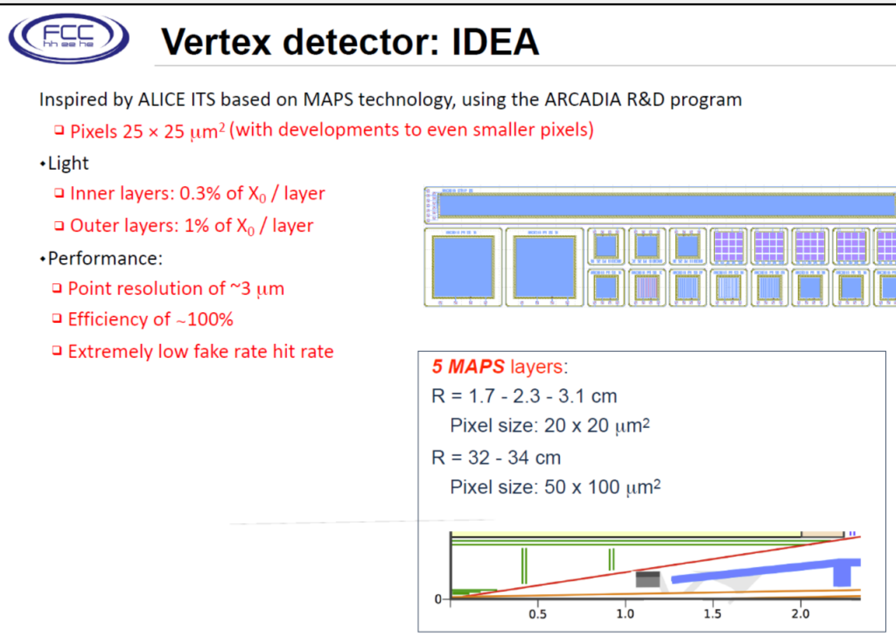
- The physics requirements impose a hierarchy between the conflicting parameters
  - ✓ Granularity and material budget first !
  - ✓ CMOS/MAPS Pixel sensors offer the best compromise for the inner vertexing/tracking layers @FCCee

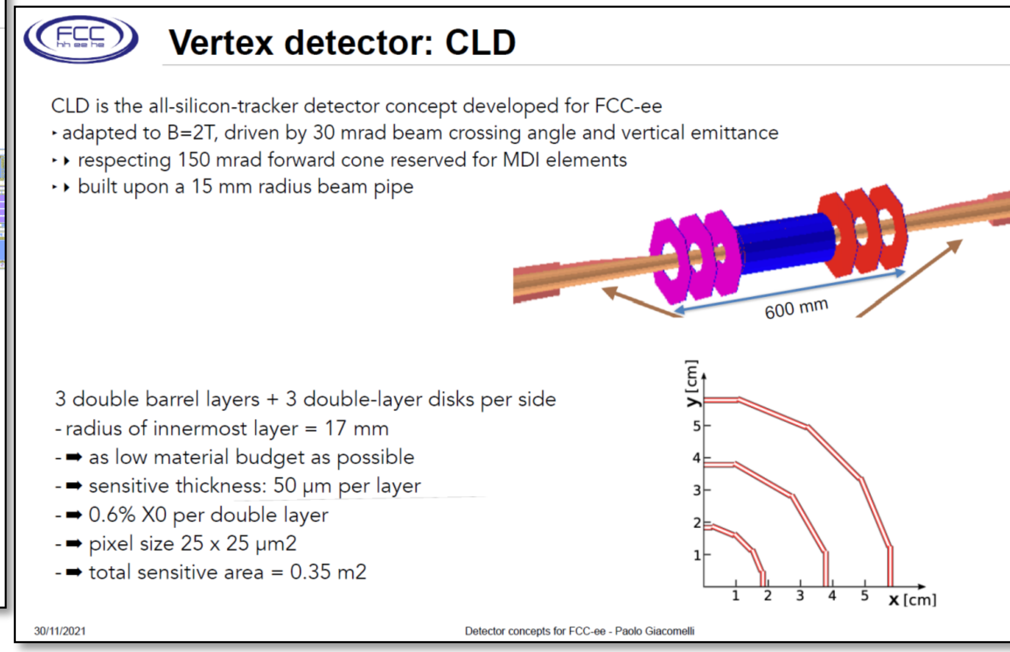
- Integration R&D is a final performances driver !
  - ✓ Fill the gap between nice ideas and real detectors
    - e.g. Stitching & bent sensors developed in ALICE-ITS3 context
    - e.g. Anisotropic conductive films

- Timing/4-D tracking Today
  - ✓ Timing layers must relax either Power (material budget) and/or spatial resolution
  - ✓ 1 or 2 timing layer could probably considered with some caveats:
    - Moderate spatial resolution (probably not an issue considering occupancies)
    - Radius >~ 10-20 cm
    - + Timing layer in the endcaps outside other PID detectors ?
  - ✓ Only detailed physics benchmark simulation will give an educated answer.
  - ✓ Intense R&D in Timing technologies may change the picture (breakthrough needed)

backup

Vertex detector IDEA/CLD



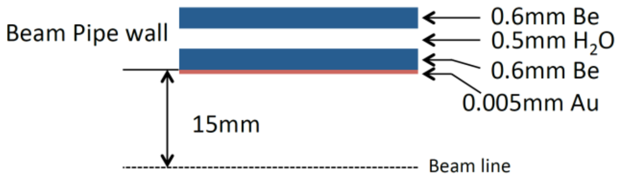


Paolo Giacomelli (Annecy 2021)

- Comments:
  - ✓ 25 μm pitch vs 3μm resolution
    - Needs: high S/N and/or no binary output
  - ✓ Material budget 0.3% X_0/layer:
    - Conservative value
    - Beam pipe material budget ~ 0.3%X0
  - ✓ 5 layers vs 3 double layers
    - Robustness (standalone tracking), low momentum vs high momentum,
    - New player: Stitching & bent sensors vs double sided approach
  - ✓ Inner and outer radius are key factors

Being generic: ILC & FCC differences

- Beam structure: « continuous » vs trains
  - ✓ Power Pulsing: allows a factor O(10) reduction in average power
  - ✓ ILC: However, avoiding PP is desirable (alignment)
- Beam pipe shape and material
  - ✓ ILC: ~0.14% X_0 for the beam pipe (500 µm)
  - ✓ FCCee: Sync. Radiations ⇨ Cooling of the beam pipe ⇨ higher Mat.Budget
  - ⇨ 800 (2 pipes) + 400 (water) ~ 0.34% X_0
  - ⇨ + 5 µm Au = 0.15% X_0
  - Smaller inner radius @ FCCee ?



- MDI:
  - ✓ CLD: Forward acceptance limited to 150 mradian (8.6°)
  - ✓ ILD: Froward acceptance (disks) ~ 5°
- TeraZ vs Giga Z
  - ✓ Specific timing and impact parameter resolution ?
    - e.g. lower radius ?
- Magnetic field:
  - ✓ ILC: 3.5/4 T (R_{max} ~1.8m)
  - ✓ CLIC: R_{max}(CLIC): 1.5m
  - ✓ FCC: 2 T max ⇨ compensate by larger level arm (R_{max} ~ 2.15m)

⇨ Overall most of the R&D can be fruitfully made common

References: ECFA/RC/21/510
CERN-ESU-017
DOI: 10.17181/CERN.XDPL.W2EX

"Technical" Start Date of Facility (This means, where the dates are not known, the earliest technically feasible start date is indicated - such that detector R&D readiness is not the delaying factor)				< 2030					2030-2035					2035 - 2040	2040-2045		> 2045		
				Panda 2025	CBM 2025	NA62/Klever 2025	Belle II 2026	ALICE LS3 [1)]	ALICE 3	LHCb (≳LS4) [1)]	ATLAS/CMS (≳LS4) [1)]	EIC	LHeC	ILC [2)]	FCC-ee	CLIC [2)]	FCC-hh	FCC-eh	Muon Collider
Vertex Detector [3)]	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.1 DRDT 3.4	Position precision σ_{hit} (µm)		≃ 5		≲ 5	≃ 3	≲ 3	≲ 10	≲ 15	≲ 3	≃ 5	≲ 3	≲ 3	≲ 3	≃ 7	≃ 5	≲ 5
			X/X_0 (%/layer)	≲ 0.1	≃ 0.5	≃ 0.5	≲ 0.1	≃ 0.05	≃ 0.05	≃ 1		≃ 0.05	≲ 0.1	≃ 0.05	≃ 0.05	≲ 0.2	≃ 1	≲ 0.1	≲ 0.2
			Power (mW/cm^2)		≃ 60			≃ 20	≃ 20			≃ 20		≃ 20	≃ 20	≃ 50			
			Rates (GHz/cm^2)		≃ 0.1	≃ 1	≲ 0.1		≲ 0.1	≃ 6		≲ 0.1	≃ 0.1	≃ 0.05	≃ 0.05	≃ 5	≃ 30	≃ 0.1	
			Wafers area (") [4)]					12	12			12			12		12		12
		DRDT 3.2	Timing precision σ_t (ns) [5)]	10		≲ 0.05	100		25	≲ 0.05	≲ 0.05	25	25	500	25	≃ 5	≲ 0.02	25	≲ 0.02
		DRDT3.3	Radiation tolerance NIEL (x 10^{16} neq/cm^2)							≃ 6	≃ 2						$\simeq 10^2$		
			Radiation tolerance TID (Grad)							≃ 1	≃ 0.5						≃ 30		
Tracker [6)]	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.1 DRDT 3.4	Position precision σ_{hit} (µm)						≃ 6	≃ 5		≃ 6	≃ 6	≃ 6	≃ 6	≃ 7	≃ 10	≃ 6	
			X/X_0 (%/layer)						≃ 1	≃ 1		≃ 1	≃ 1	≃ 1	≃ 1	≃ 1	≲ 2	≃ 1	
			Power (mW/cm^2)						≲ 100	≃ 100		≲ 100		≲ 100	≲ 100	≲ 150			
			Rates (GHz/cm^2)							≃ 0.16									
			Wafers area (") [4)]						12			12		12	12	12	12		12
		DRDT 3.2	Timing precision σ_t (ns) [5)]						25	≲ 25		25	25	≲ 0.1	≲ 0.1	≲ 0.1	≲ 0.02	25	≲ 0.02
		DRDT3.3	Radiation tolerance NIEL (x 10^{16} neq/cm^2)							≃ 0.3							≲ 1		
			Radiation tolerance TID (Grad)							≃ 0.25							≲ 1		
Time of Flight [8)]	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.2	Timing precision σ_t (ns) [5)]				≃ 0.02		≃ 0.02		≲ 0.03	≃ 0.02	≃ 0.02		≲ 0.01		≲ 0.01	≃ 0.02	
		DRDT 3.3	Radiation tolerance NIEL (x 10^{16} neq/cm^2)														$\simeq 10^2$		
			Radiation tolerance TID (Grad)														≃ 30		