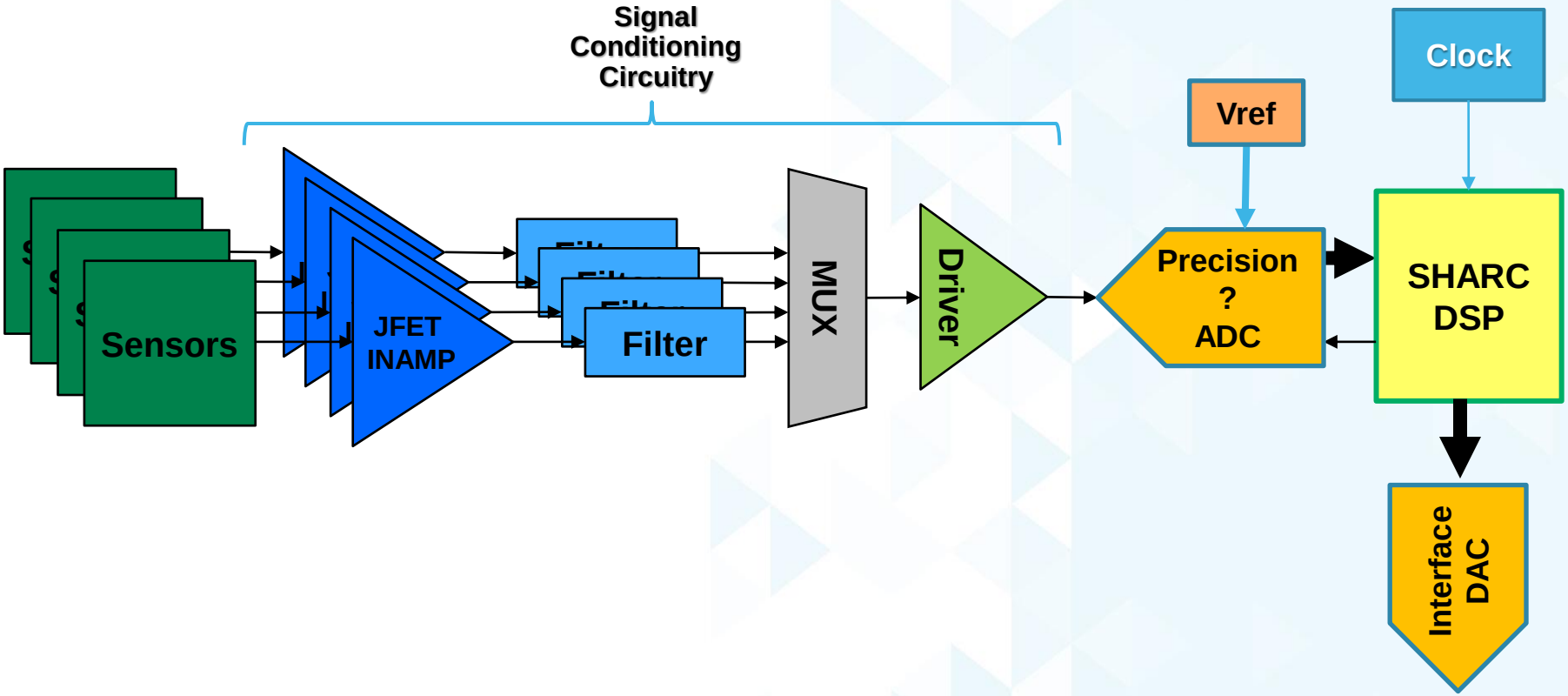
SAMPLING

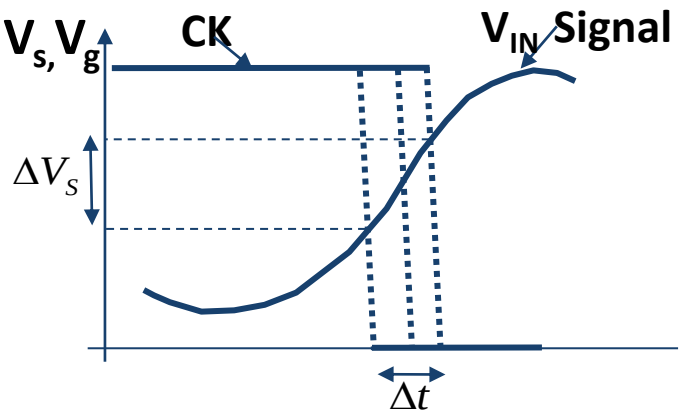
From continuous time to discret time

Industrial Analog Signal Chain -> Digital

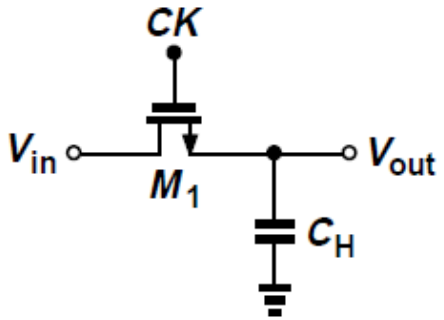


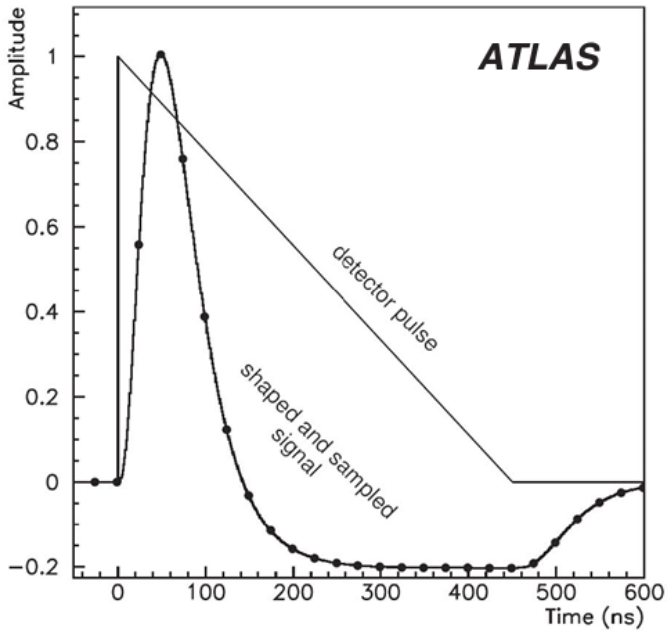
SAMPLING: *TIMING ACCURACY*

- ΔV_S is an error from Vin to sampled signal
- It depends on Vin frequency as well as the CLK jitter and the switch resistance etc…
- It will degrade the SNR for the sampled signal
- It can be defined by: $\Delta V_S = \left(\frac{dV_{IN}}{dt}\right)_{max} \cdot \Delta t$

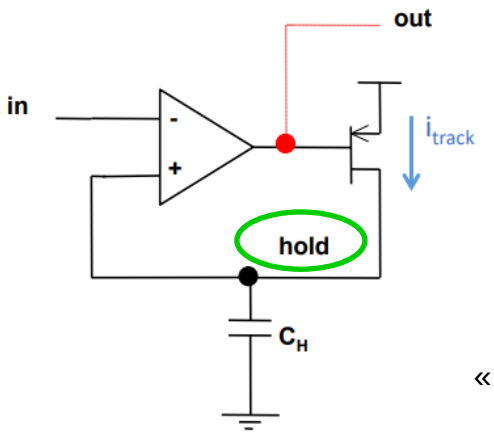


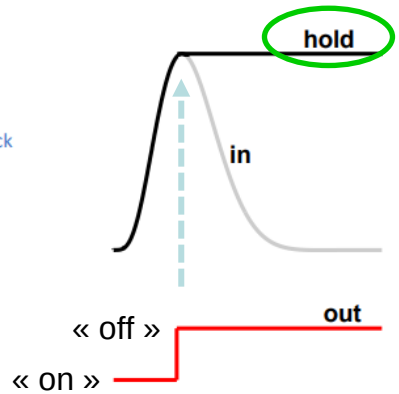
Sample / Hold + ADC



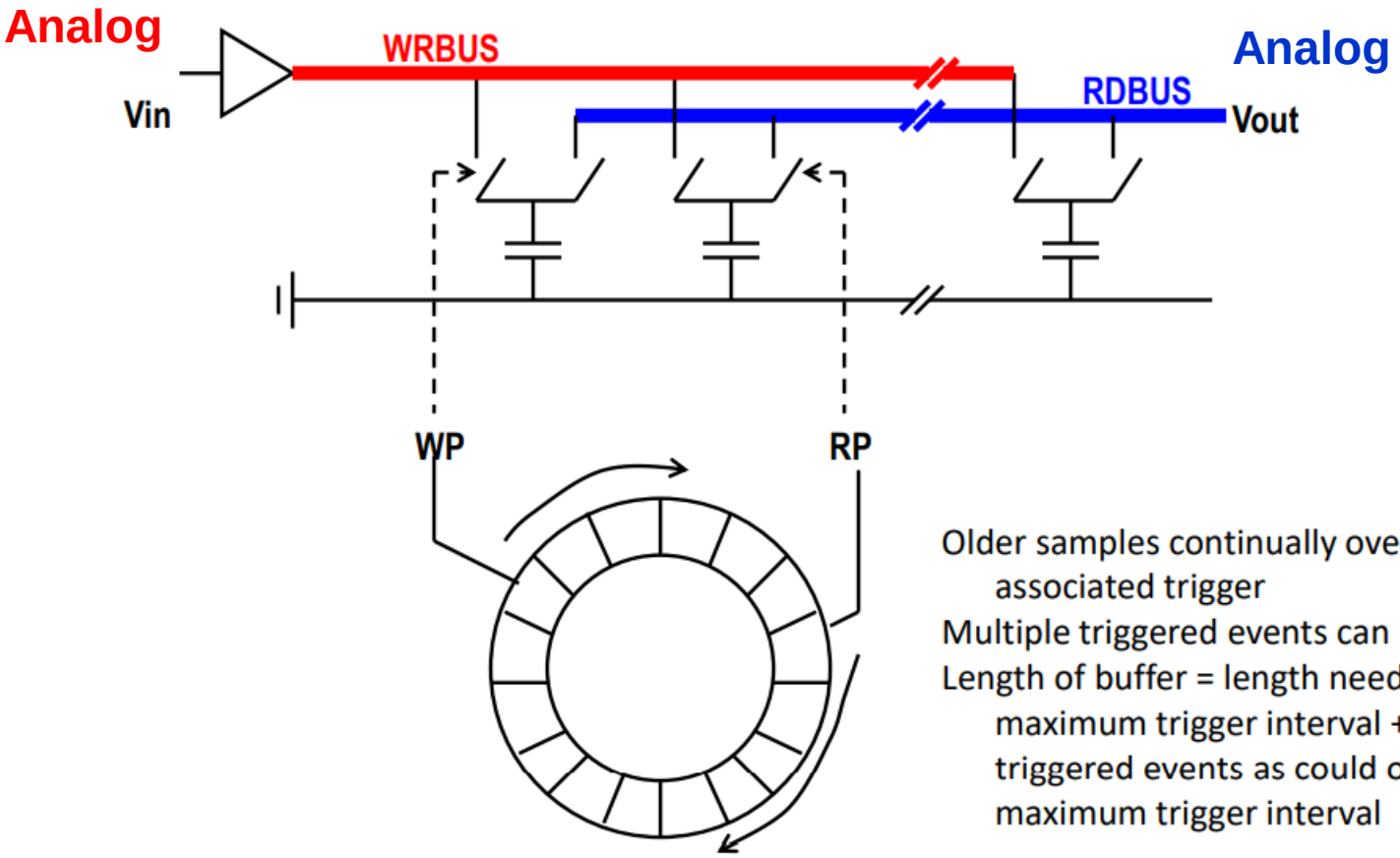


Peak detector + ADC





Analog Memory or wave recorder



Older samples continually overwritten unless associated trigger

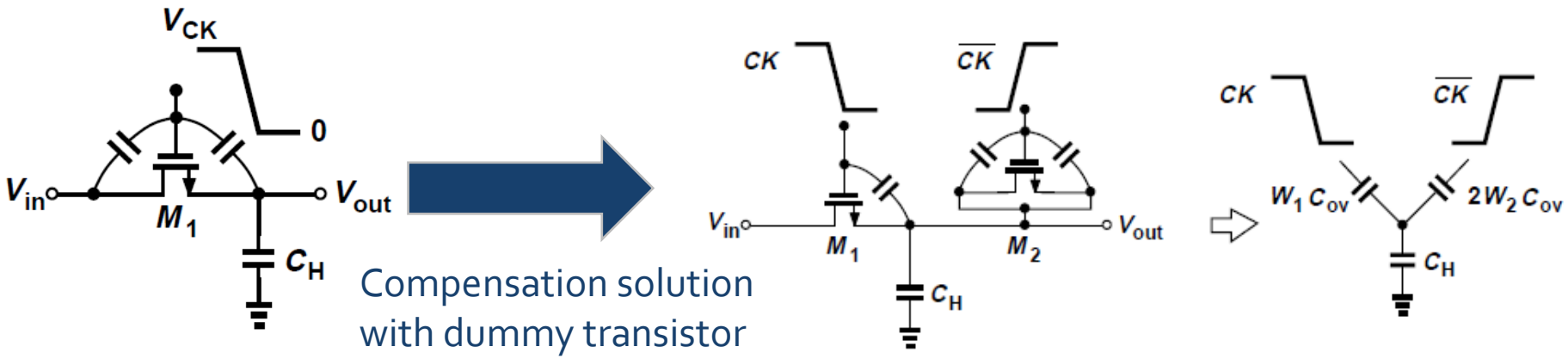
Multiple triggered events can be stored

Length of buffer = length needed to span maximum trigger interval + hold as many triggered events as could occur during maximum trigger interval

CHARGE INJECTION ISSUES: CLOCK FEEDTROUGH

- MOS switch couples the clock transitions to the sampling capacitor through its gate-drain C_{GD} or gate-source C_{GS} overlap capacitance, also denoted C_{ov} (the overlap capacitance per unit width)
- The effect introduces an error in the sampled output voltage:

$$\Delta V = V_{CK} \cdot \frac{W \cdot C_{ov}}{W \cdot C_{ov} + C_H}$$

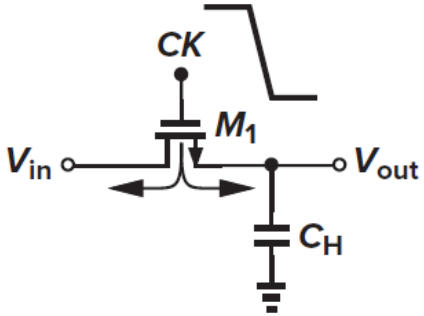


CHARGE INJECTION ISSUES: CHANNEL CHARGE INJECTION

- When input signal is sampled on a capacitor by turning off the transistor, charge Q_{CH} is puched out from the channel to either direction. For a NMOS transistor Q_{CH} is defined by:

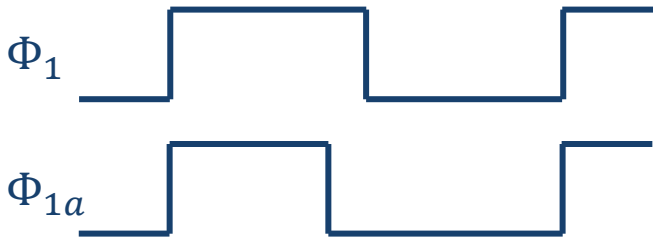
$$Q_{CH} = WLC_{ox}\left(V_{DD} - V_{in} - V_{t,n}\right)$$

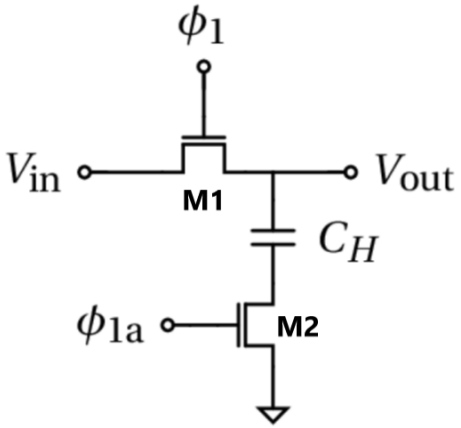
- This phenomenon is called "**channel charge injection**"
- The magnitude of Q_{CH} is a complex function of various parameters, such as the impedance seen at each terminal to ground and the transition time of the clock



CHANNEL CHARGE INJECTION: COMPENSATION TECHNIQUES

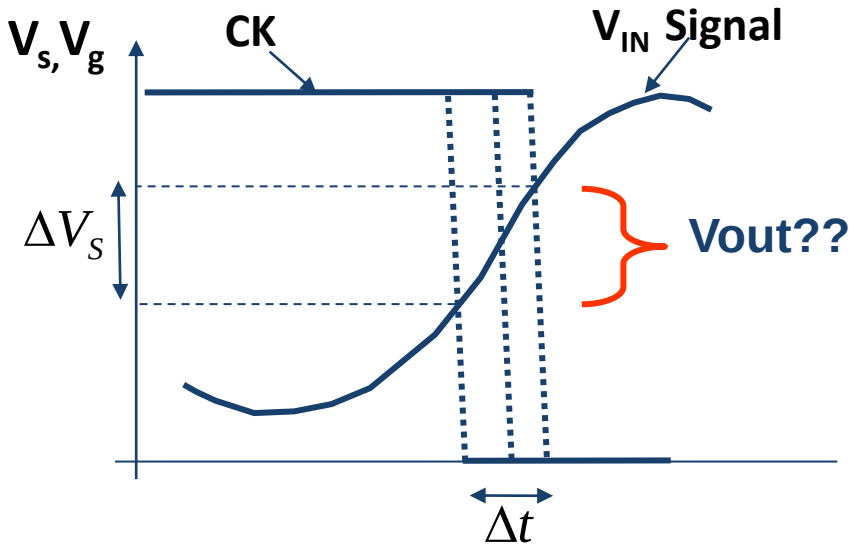
- **Bottom plate sampling** scheme is another technique to eliminate the charge injection error
- Two switches are used and the signal is sampled when M_2 turns off
- M_2 turns off slightly before M_1 injecting a constant charge
- Signal dependent charge from M_1 does not enter C_H because there is no path to ground



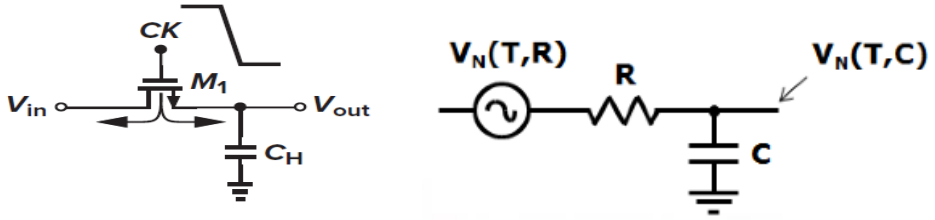


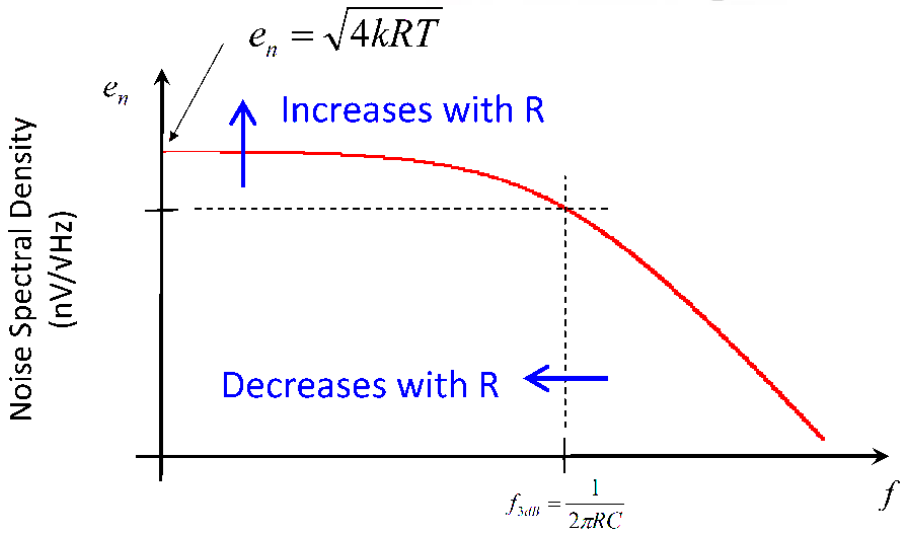
SAMPLING: CLK'S JITTER LIMITATIONS

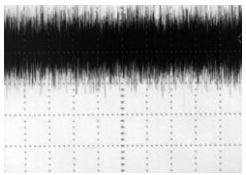
- ΔV_s can be considered as amplitude fluctuation (clk jitter)
- It will degrade the SNR of the sampling signal
- It can be defined by: $\Delta V_s = \left(\frac{dV_{IN}}{dt}\right)_{max} \cdot \Delta t$



THERMAL NOISE: KT/C







- C is not the fundamental cause; just have a thermal noise (R) and the bandwidth is limited by C.

C	Eq. Noise
1 pF	64.34 µV rms
10 pF	20.35 µV rms
100 pF	6.43 µV rms
1 nF	2.03 µV rms

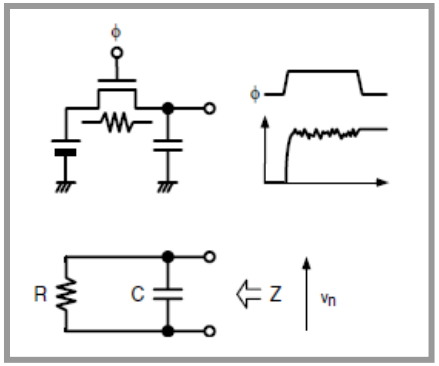
What happens:

- Increasing C?
- Increasing W/L of the switch?
- Increasing both?

Thermal noise KT/C

- From the switch capacitor circuit and the resistance of the switch, we can define the transfer function $\frac{V_{out}}{V_{in}}$ as:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + RCp}$$



- PSD Noise from **resistance** is defined by:

$$S_v(f) = 4kTR$$

- The Output PSD Noise is then:

$$S_{out}(f) = 4kTR \left| \frac{V_{out}}{V_{in}} \right|^2$$

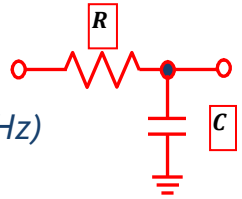
- The white noise spectrum of the resistor is **shaped by a low-pass** RC, and the the total noise power at the output is:

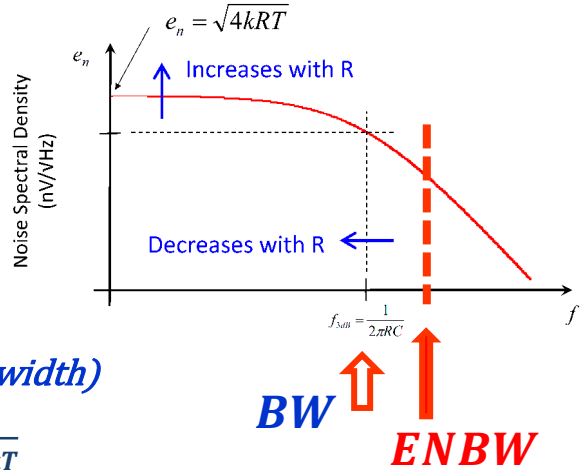
$$P_{n,out} = \int_0^\infty \frac{4kTR}{4\pi^2 R^2 C^2 f^2 + 1} df = \frac{kT}{C} \int_{-a}^{a} \frac{dx}{1 + x^2} = 2 \arctan a$$

- This noise is a function only of temperature and capacitance values

EQUIVALENT NOISE BANDWIDTH IN RC FILTER

- Consider a single pole RC low pass filter
  - $BW = Corner\ frequency = \frac{1}{2\pi RC}$
  - $Resistor\ Noise\ Density = \sqrt{4kTR}$ -> *V/sqrt(Hz)*
  - *Gain=1*
  - $ENBW = \frac{\pi}{2} BW = \frac{\pi}{2}\frac{1}{2\pi RC} = \frac{1}{4RC}$ *(Equivalent Noise Bandwidth)*
  - $Total\ output\ Noise = Noise\ Density * \sqrt{ENBW} = \frac{\sqrt{4kTR}}{\sqrt{4RC}} = \sqrt{\frac{kT}{C}}$





Magnitude

Value	Noise
1 pF	64.34 µV rms
10 pF	20.35 µV rms
100 pF	6.43 µV rms
1000 pF	2.03 µV rms

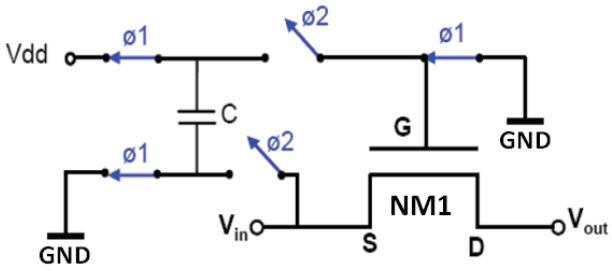
	Noise
1 kΩ resistor with BW limited to 1 MHz	5.1 µV rms
A LNA: E_N= 2 nV/√Hz, Unity gain buffer BW limited to 1 MHz	2.55 µV rms

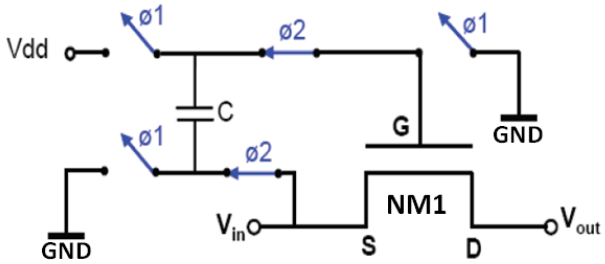
BOOTSTRAP SWITCH PRINCIPLE

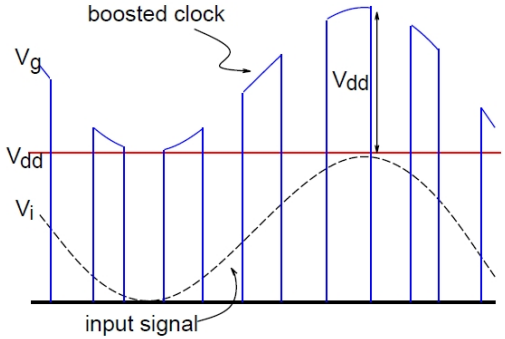
- Channel charge injection is a function of input signal V_{in}

$$Q_{CH} = WLC_{ox}(V_{GS} - V_{t,n}) = WLC_{ox}(V_{DD} - V_{in} - V_{t,n})$$

- Bootstrapping technique suppresses this dependence by making V_G varying as Vin, then V_{GS}= constante.





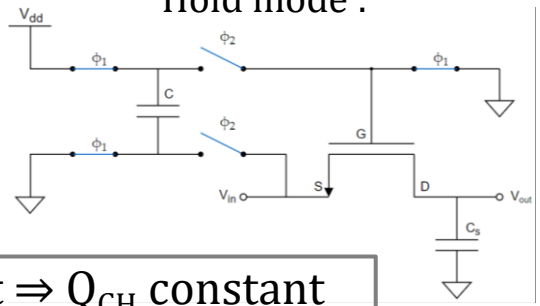


- Distorsion issues are also reduced

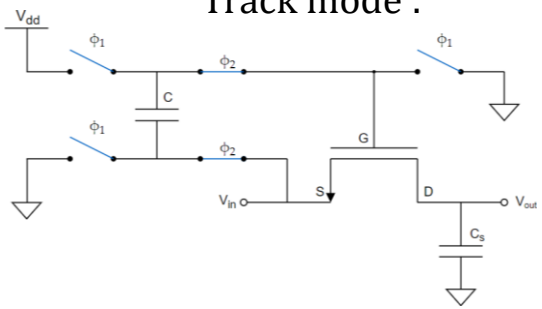
Simulation: sampling Linearities issues

Bootstrapped switch :

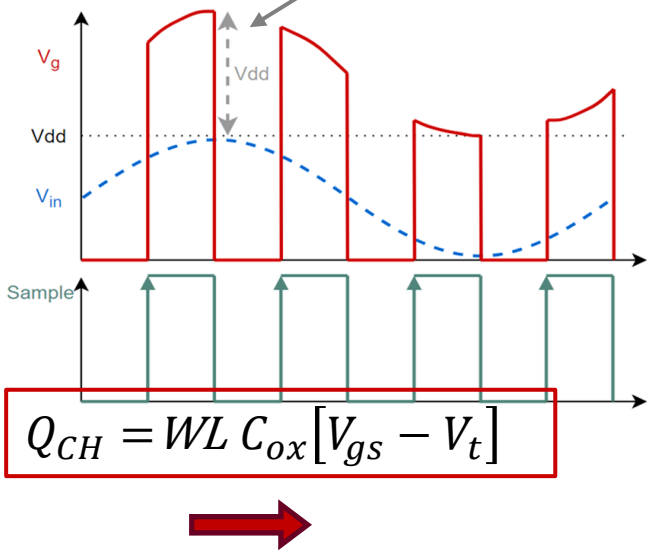
Hold mode :



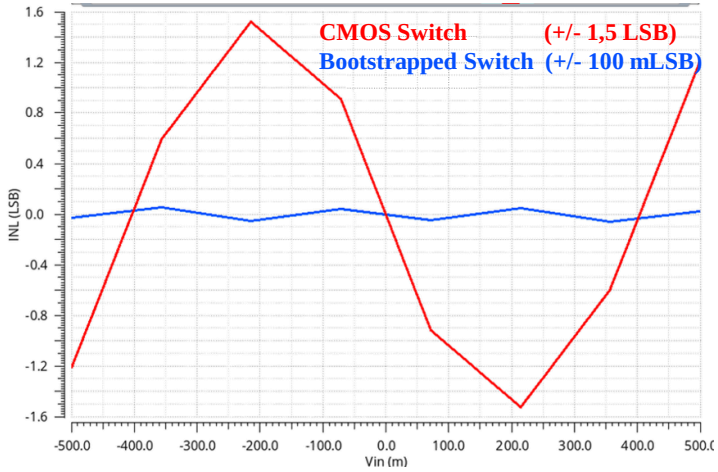
Track mode :



V_{gs} constant ⇒ Q_{CH} constant



$$Q_{CH} = WL\,C_{ox}\left[V_{gs} - V_t\right]$$



Q_{CH} constant

Low Sampling INL

Analog to Digital Converters ADC

ARCHITECTURES

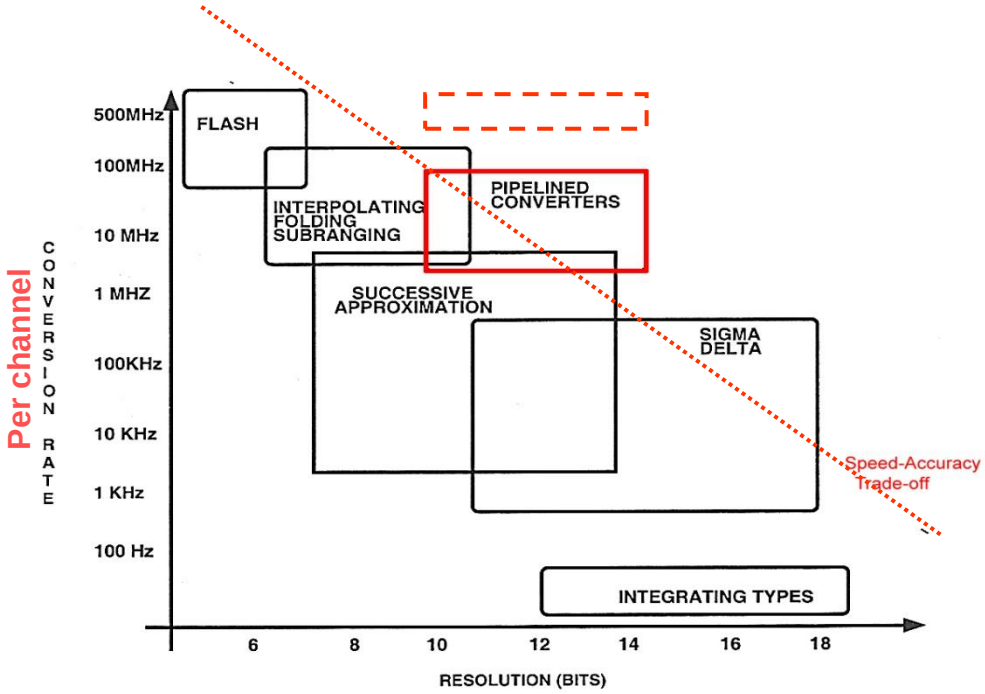
&

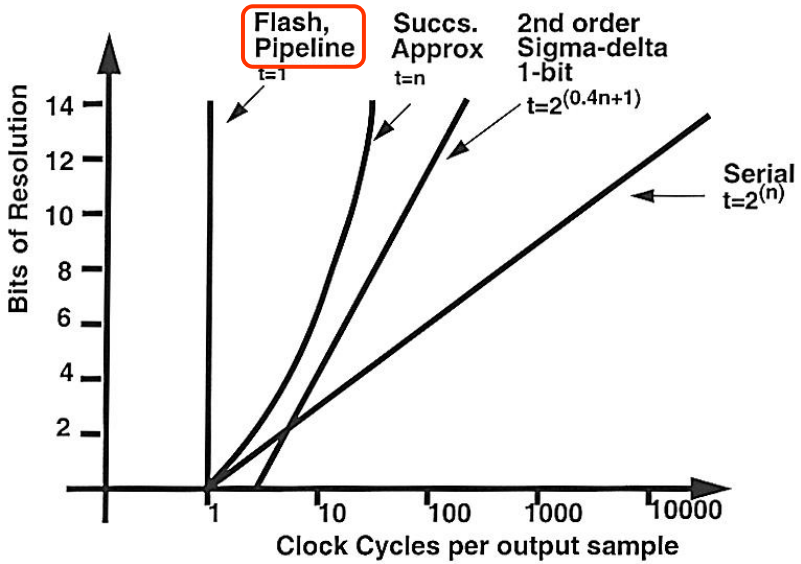
SPECIFICATIONS

What is an ADC?

- Mixed signal circuit:
  - Analog input signal
  - Digital output signal
- ADC **discretize** the **continuous input signal** in **time** and **amplitude**
- Output Code is defined by:
  - $\sum_{i=0}^{N} \frac{2^i (G \cdot V_{in})}{V_{ref}}$
  - G is the gain factor, N the resolution, V_{in} the input signal and V_{ref} is the dynamic range of the converter

High speed ADC: general overview





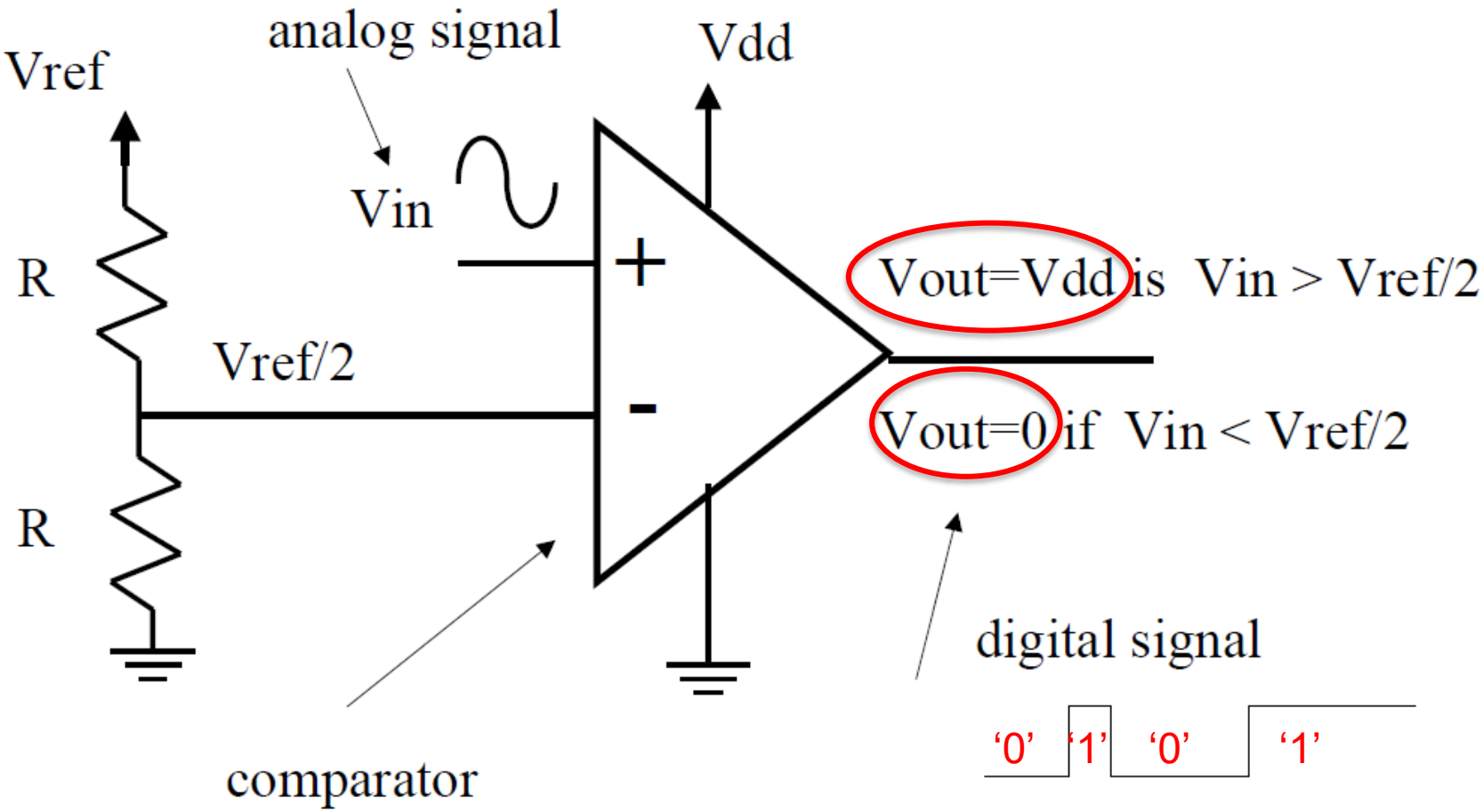
ADC architecture timeline (source: Analog Devices)

- 1939: Counting ADC (Reeves)
- 1946: Successive approximation
- 1948: Flash (electron tube coders)
- 1956: Bit-per-stage (binary and folding-Gray)
- 1956: Sub-ranging
- 1964: Sub-ranging with error correction
- **1966: Pipe line with error correction**

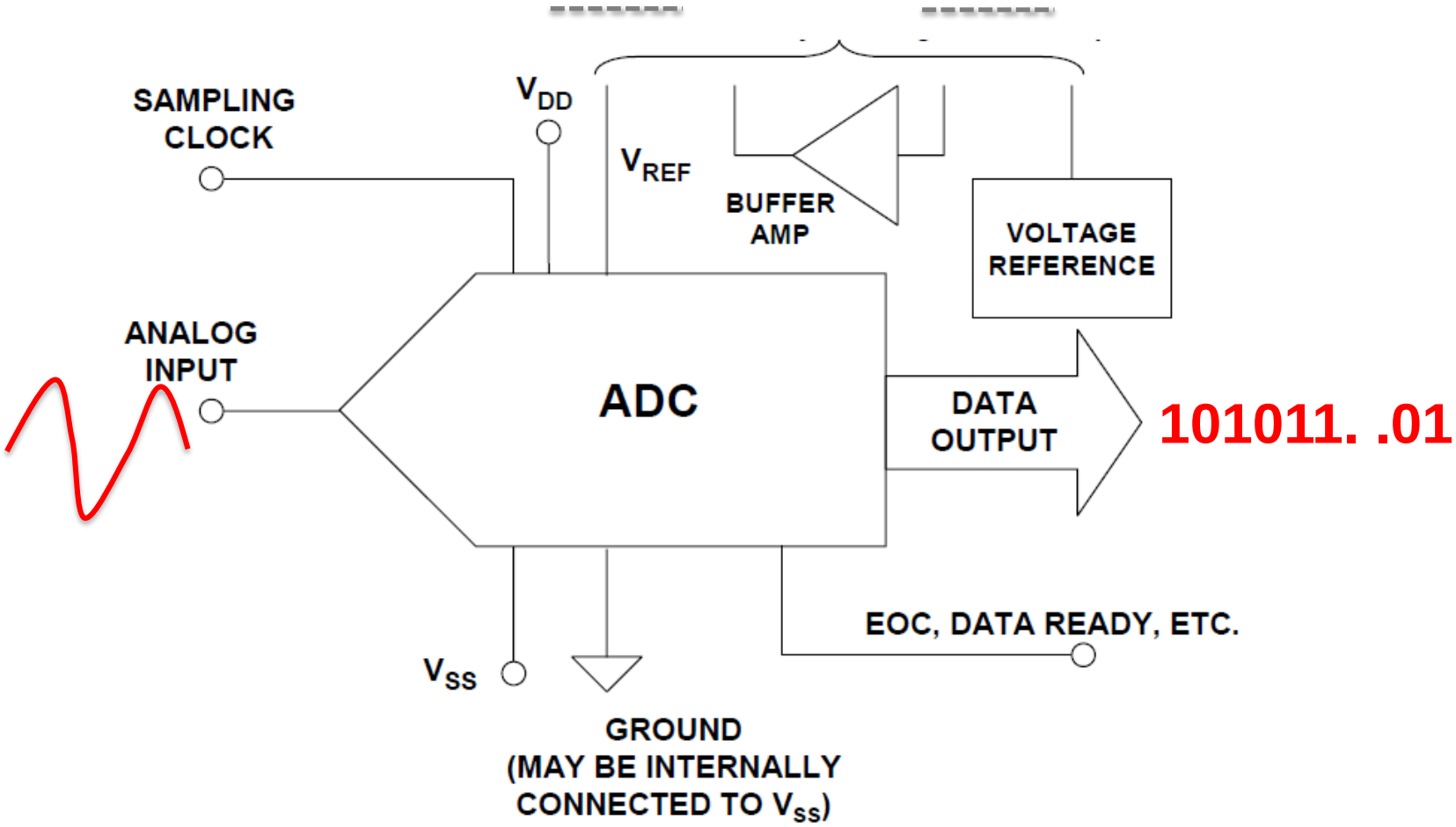
ADC Architectures

- Slope type converters
- Successive approximation
- Flash
- Time-interleaved / parallel converter
- Folding
- Residue type ADCs
  - Two-step
  - Pipeline
  - …
- Oversampled ADCs

From Analog signal to digital codes

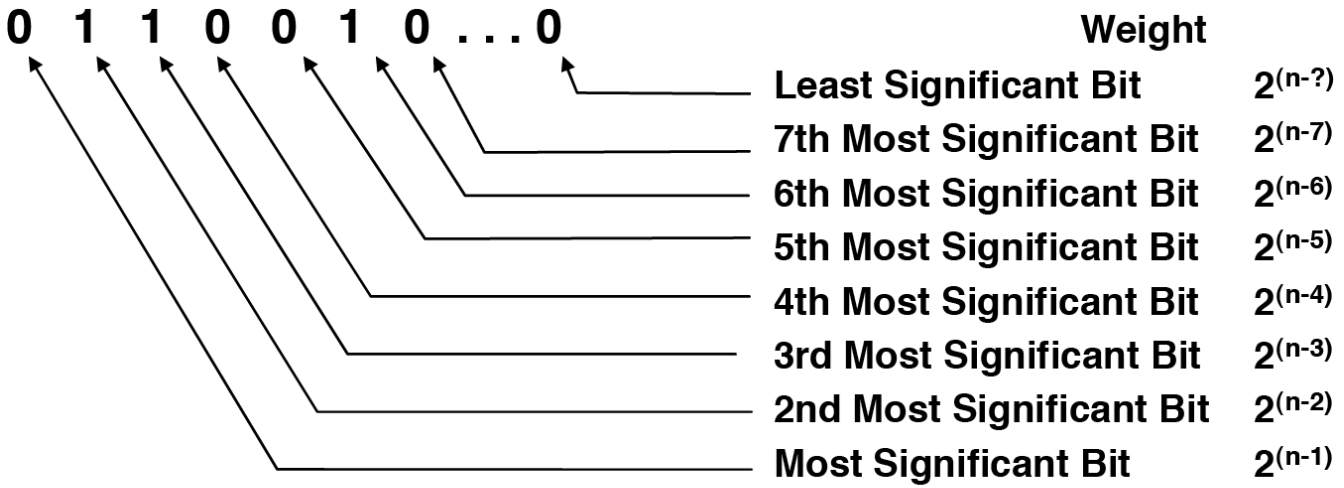


ADC inputs and outputs



definition

- **LSB**: Least Significant Bit
- **MSB**: Most Significant Bit



Bit Weights of an 8-Bit Word

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
128	64	32	16	8	4	2	1

LSB – Resolution – V_{ref}

V_{REF}	Resolution	1 LSB
1.00V	8	3.9062 mV
1.00V	12	244.14 μV
2.00V	8	7.8125 mV
2.00V	10	1.9531 mV
2.00V	12	488.28 μV
2.048V	10	2.0000 mV
2.048V	12	500.00 μV
4.00V	8	15.625 mV
4.00V	10	3.9062 mV
4.00V	12	976.56 μV

Digitization of **Pulse** Height – Analog to Digital Conversion

For data storage and subsequent analysis the analog signal at the shaper output must be digitized.

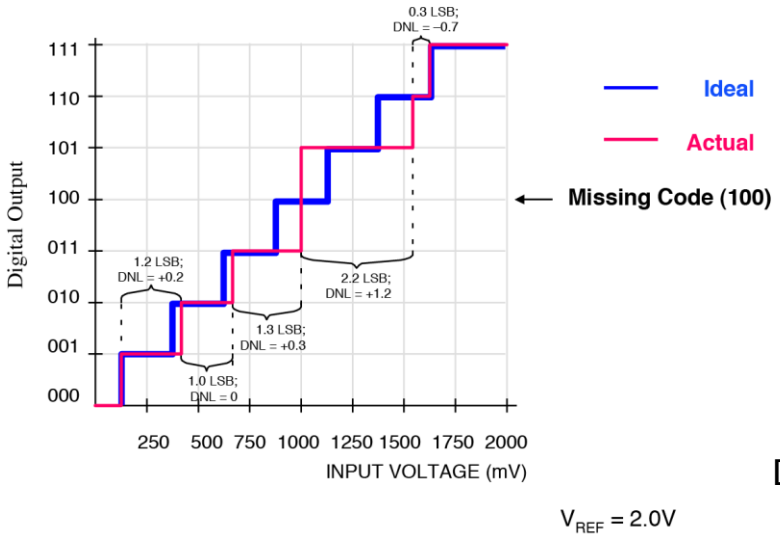
Important parameters for ADCs used in detector systems:

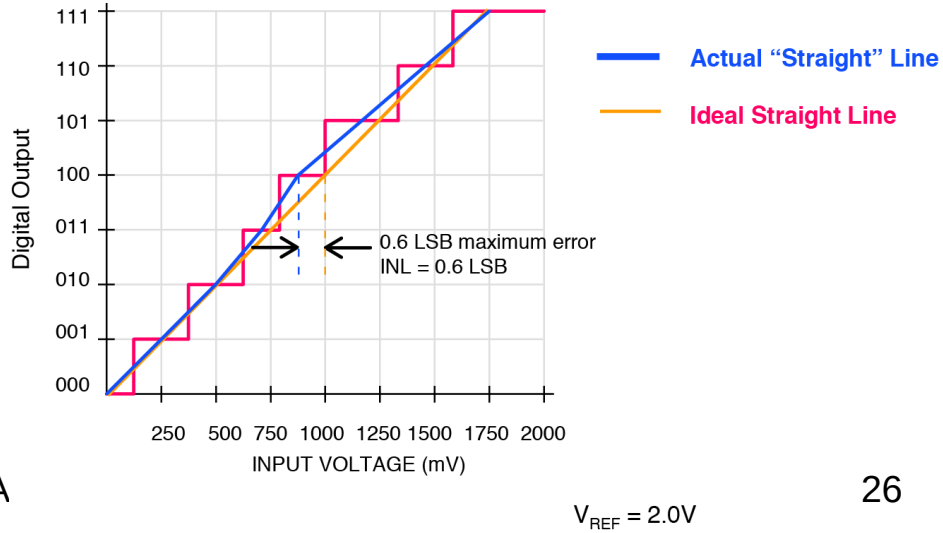
1. **Resolution**
   The "granularity" of the digitized output
2. **Differential Non-Linearity**
   How uniform are the digitization increments?
3. **Integral Non-Linearity**
   Is the digital output proportional to the analog input?
4. **Conversion Time**
   How much time is required to convert an analog signal to a digital output?
5. **Count-Rate Performance**
   How quickly can a new conversion commence after completion of a prior one without introducing deleterious artifacts?
6. **Stability**
   Do the conversion parameters change with time?

Instrumentation ADCs used in industrial data acquisition and control systems share most of these requirements. However, detector systems place greater emphasis on differential non- linearity and count-rate performance. The latter is important, as detector signals often occur randomly, in contrast to measurement systems where signals are sampled at regular intervals.

Static parameters: DNL/INL

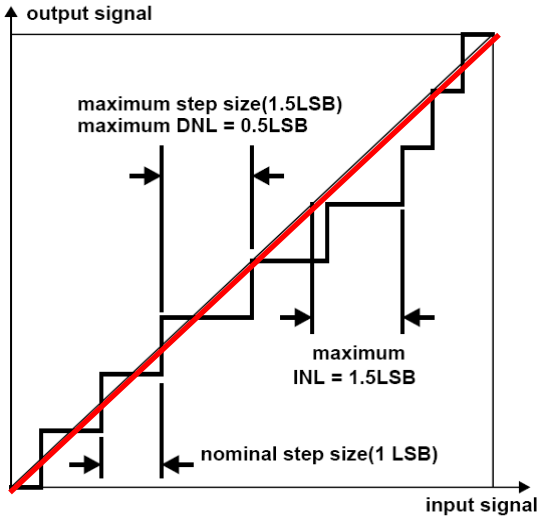
- Measure the linearity issue
  - Define how the gain can keep constant
- **DNL**: Differential Non Linearity
  - Proximity error between two successive codes
- **INL**: Integral Non Linearity
  - Deviation from a straight line on the whole dynamic





ADC Parameters

- Static
  - DNL $$DNL(k) = \frac{(X_{k+1} - X_k) - \Delta}{\Delta}$$
  - INL $$INL(k) = \sum_{i=0}^{k} DNL(i)$$

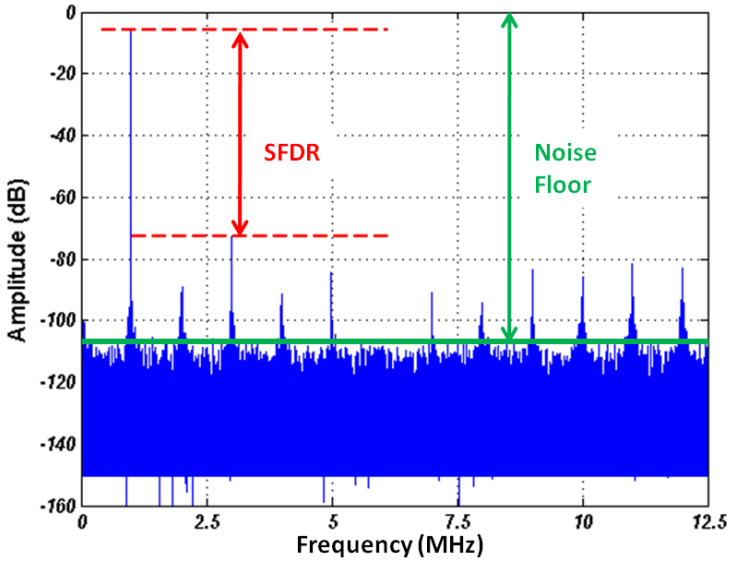


- Dynamic

$$SNR_{dB} = 10 \cdot \log_{10}\left(\frac{P_s}{P_n}\right)$$

$$SFDR_{dB} = 10 \cdot log_{10}\left(\frac{P_s}{P_h}\right)$$

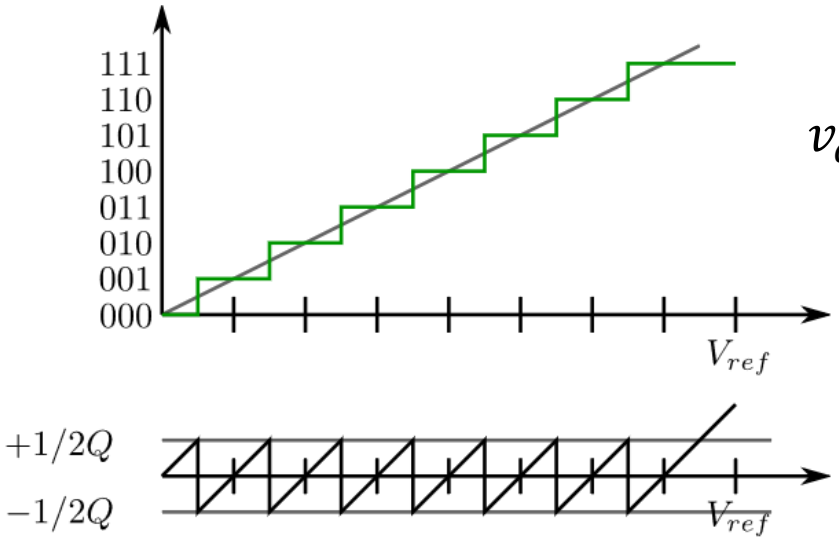
$$ENOB = \frac{SINAD_{dB} - 1.76}{6.02}$$



$$FoM = \frac{P}{2^{ENOB} \cdot f_s} \cdot V_{DD}$$

Quantization noise

- The fact that the input signal is *quantized* means that noise is added to it
- Quantization noise is less with higher resolution as the input range is divided into a greater number of smaller ranges
- It has a uniform distribution ranging from −Q/2 to +Q/2
- This error can be considered a quantization noise with **RMS**

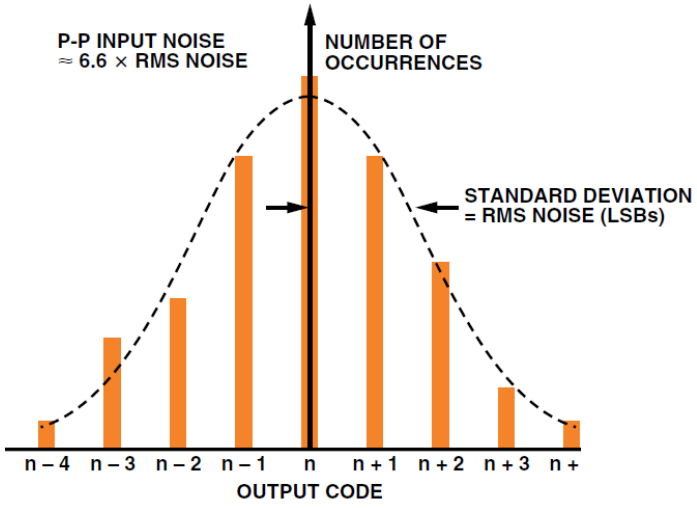


Summing the energy

$$v_{qn} = \sqrt{\frac{1}{Q} \cdot \int_{-Q/2}^{+Q/2} x^2 dx} = \sqrt{\frac{1}{Q} \cdot \left[\frac{x^3}{3}\right]_{-Q/2}^{+Q/2}}$$

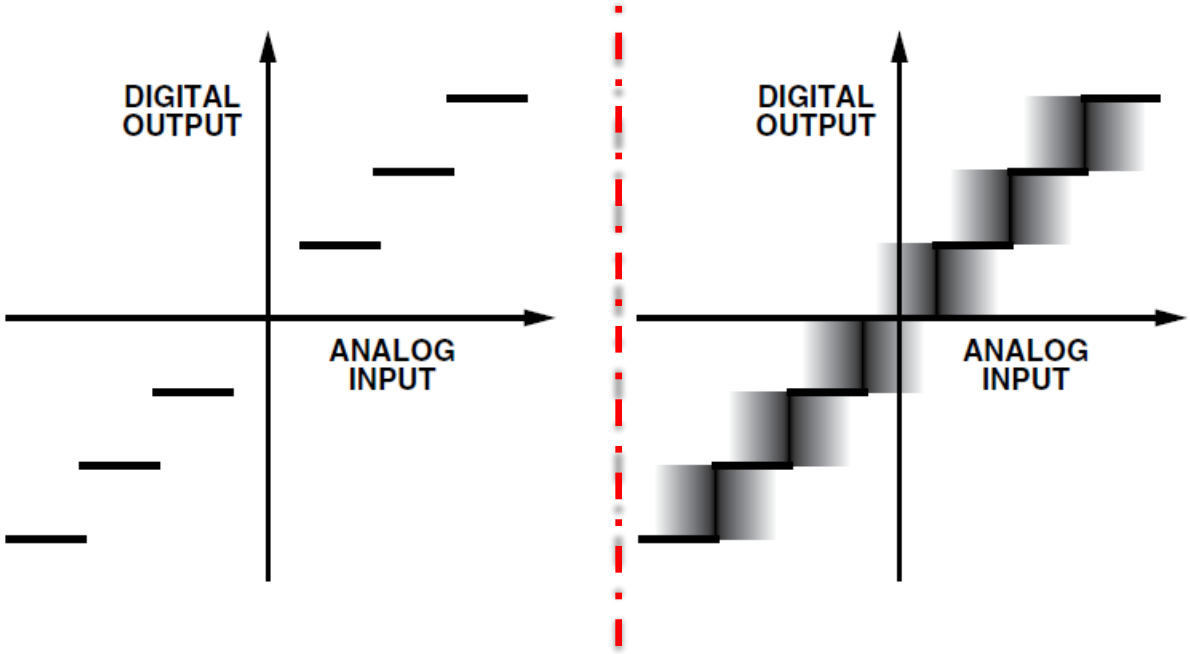
$$v_{qn} = \sqrt{\frac{Q^2}{2^3 \cdot 3} + \frac{Q^2}{2^3 \cdot 3}} = \frac{\boldsymbol{Q}}{\sqrt{\mathbf{12}}}$$

Noise issues in tranfert function



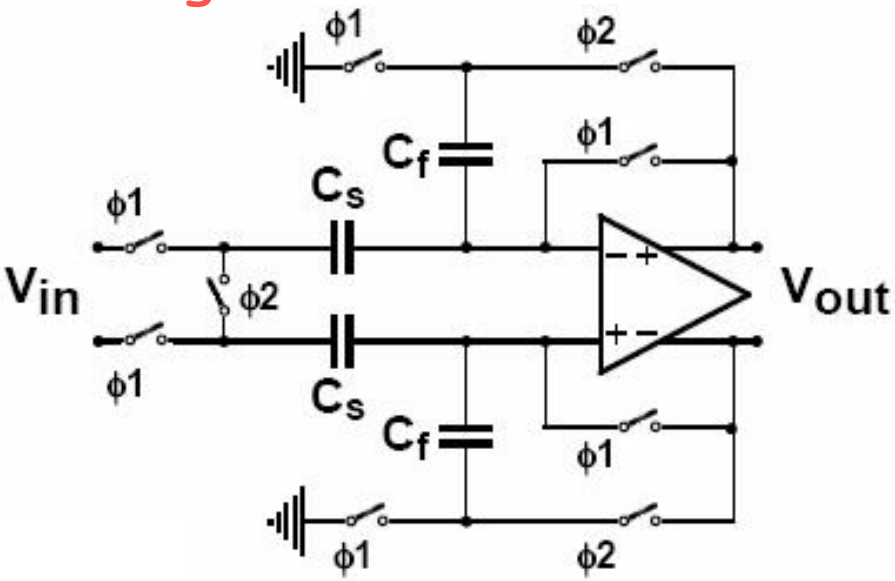
Ideal transfert function curve

Transfert function curve with $1LSB_{PP}$ transition noise



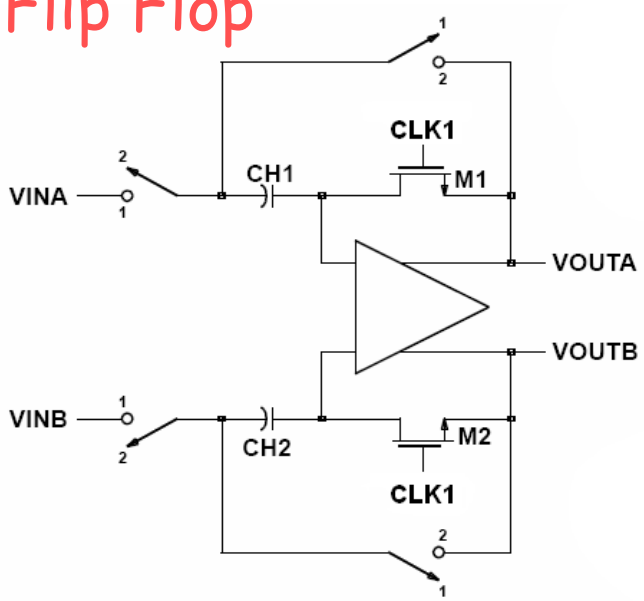
THE Track "Sample" and Hold

Charge redistribution



+ single ended to differential
+ less sensitive to CM error
+ Offset cancelled (differentially)
- Noise (a factor √2 more)
- Gain mismatch

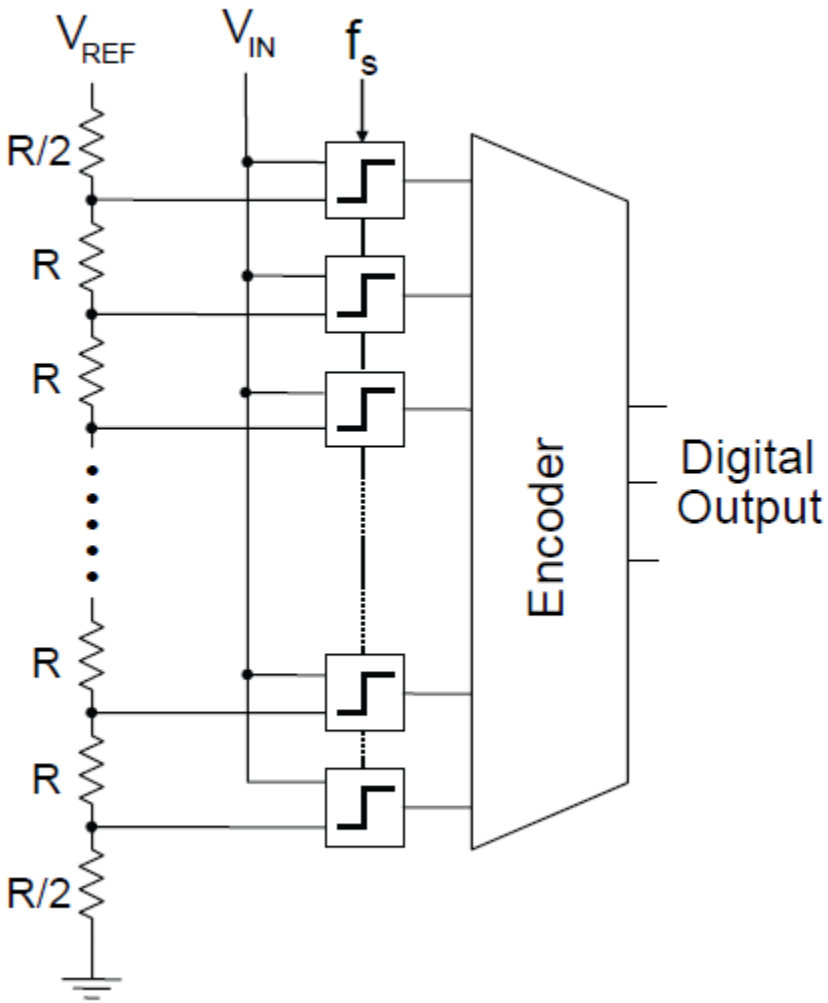
Flip Flop



+ Mismatch insensitive; gain=1
+ Less noise
+ Offset cancelled (differentially)
- Sensitive to CM fluctuations
- Need full differential inputs

ADC ARCHITECTURES

Flash Converter Sources of Error



- Comparator input:
  - Offset
  - Nonlinear input capacitance
  - Kickback noise (disturbs reference)
  - Signal dependent sampling time
- Comparator output:
  - Sparkle codes (… 111101000 …)
  - Metastability

Pros & Cons about Flash ADC

Flash is fast,

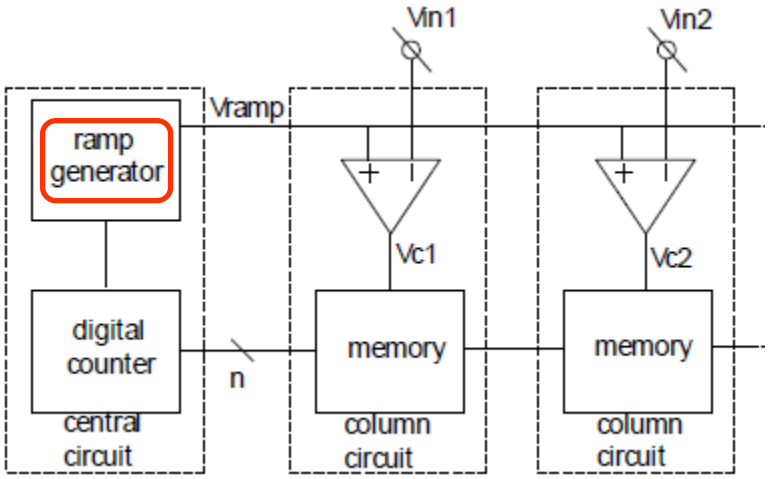
2^b - 1 comparators simultaneously sample the input signal

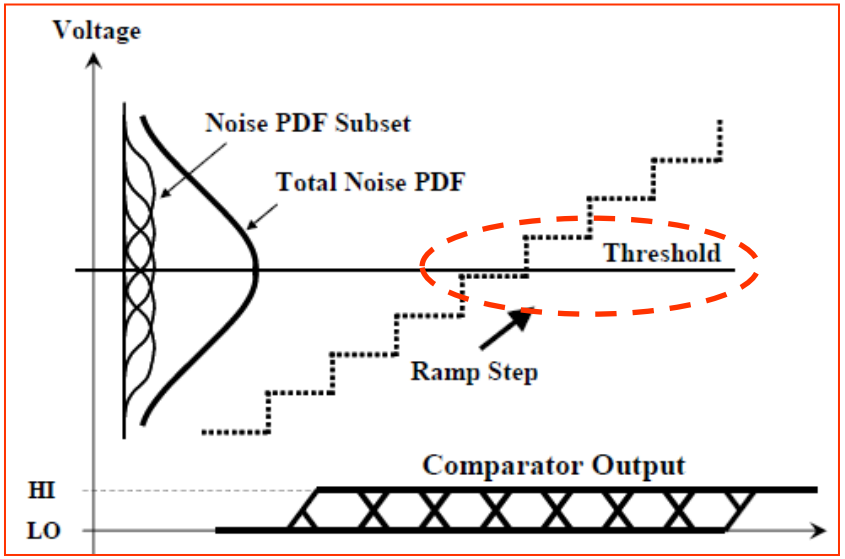
But, for high resolution,

Number of comparators increases exponentially with b

- very large ICs, high power dissipation, difficulty in matching components, and, the increasingly large input capacitance reduces analog input bandwidth
- currently available, $b \leq 8$

Rampe ADC





Widely used for CIS:

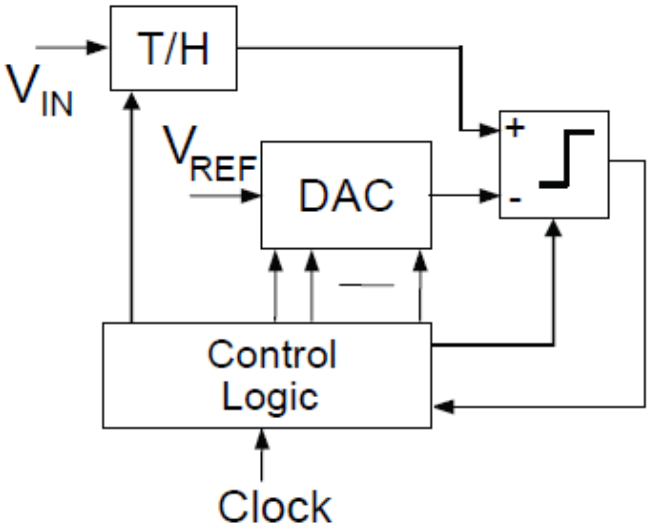
-inherently simple, scalable to small pitch

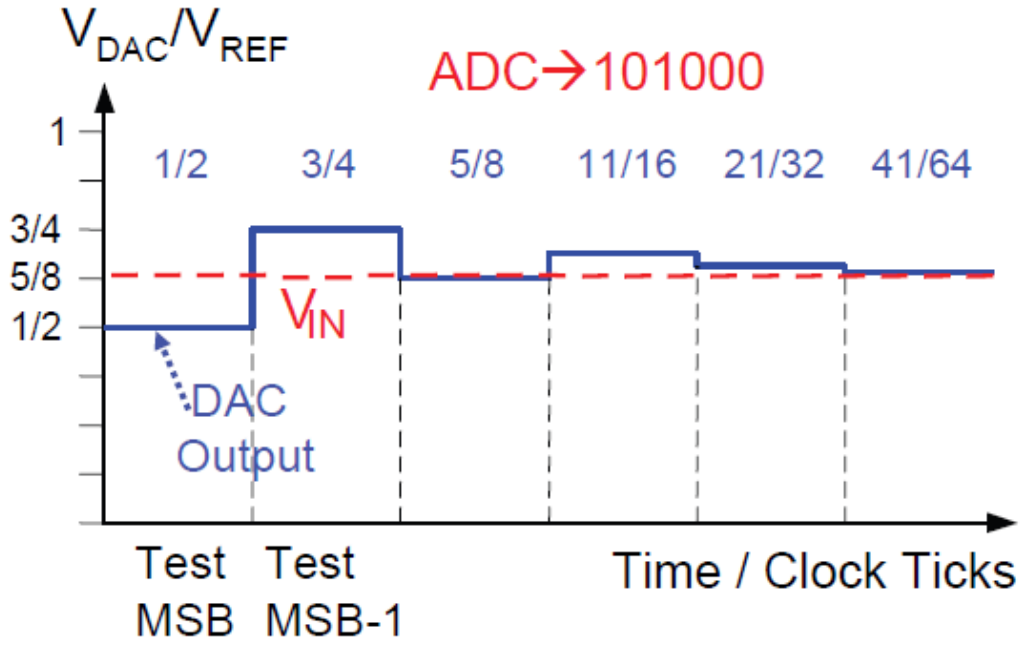
However: slow, sensitive to the noise of the common ramp driver and comparator, and the clock jitter while close to the threshold voltage and the noise estimator.

Toshinori Otaka; *2011 INTERNATIONAL IMAGE SENSOR WORKSHOP*

Successive Approximation ADC

Example: 6-bit ADC & $V_{IN}=5/8V_{REF}$

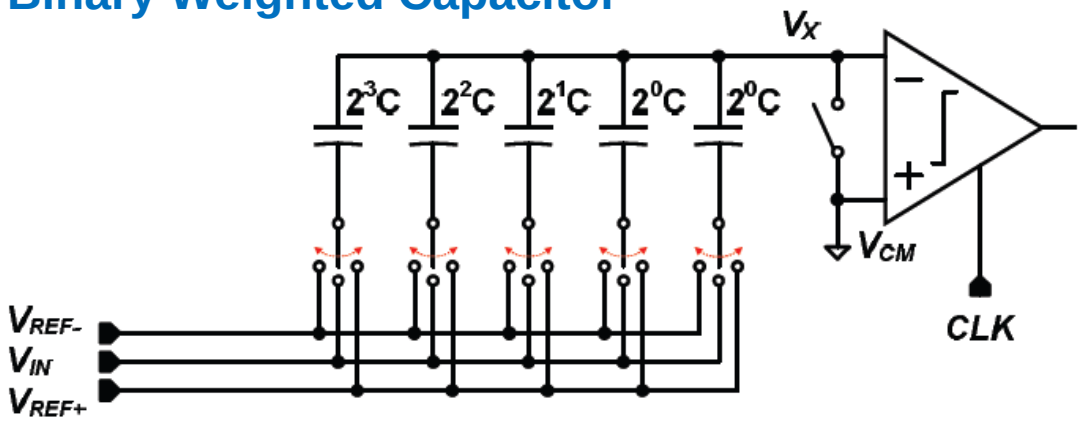




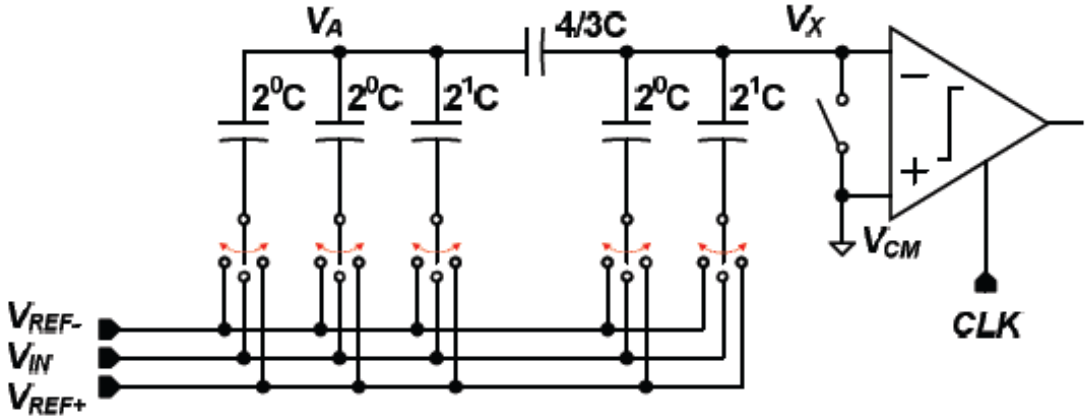
- High accuracy achievable (16+ Bits)
- Required N clock cycles for N-bit conversion (much faster than slope type)

Low power SAR => ADC with sampling capacitors

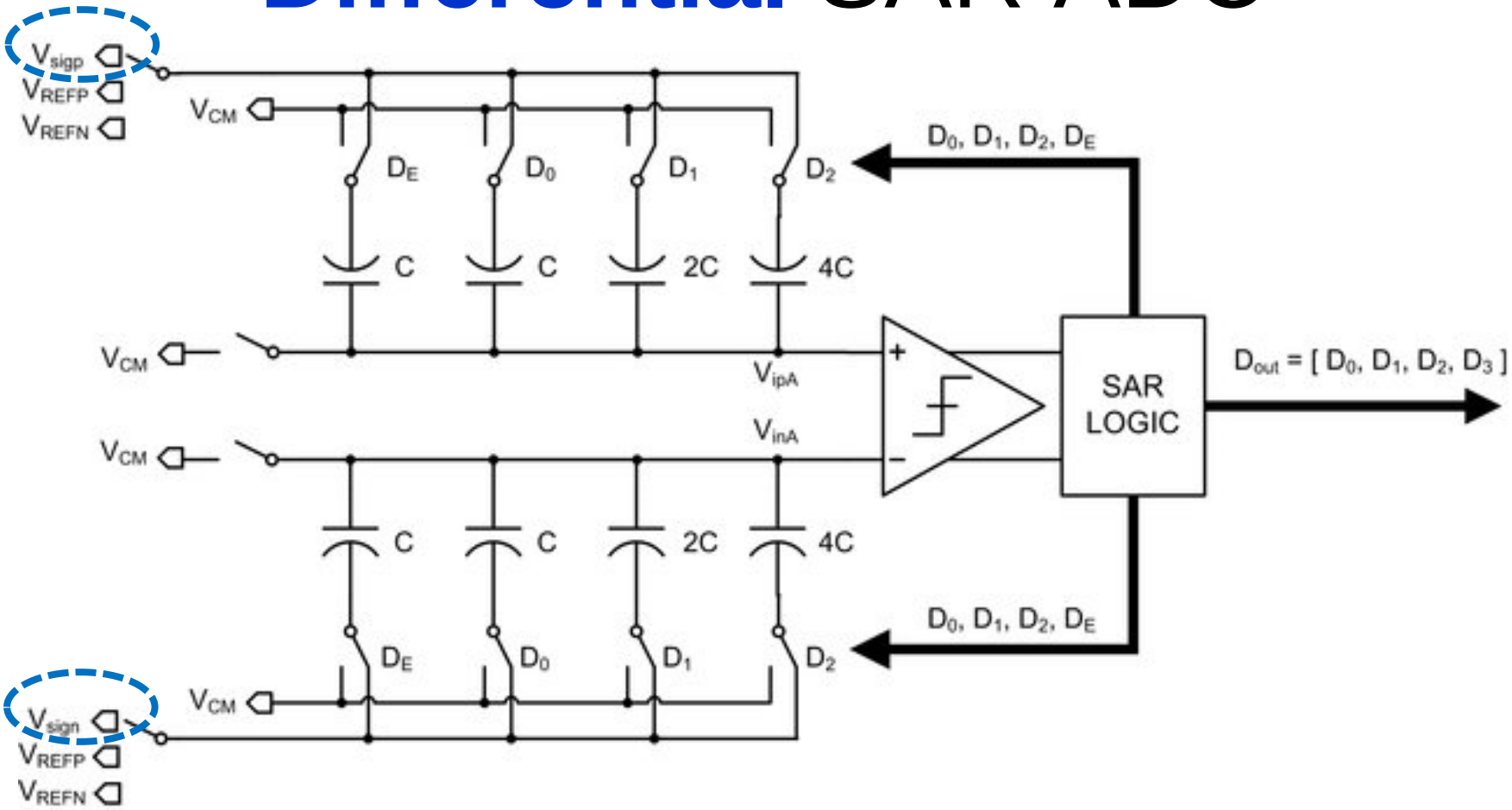
Binary Weighted Capacitor



Segmented-Binary Weighted Capacitors



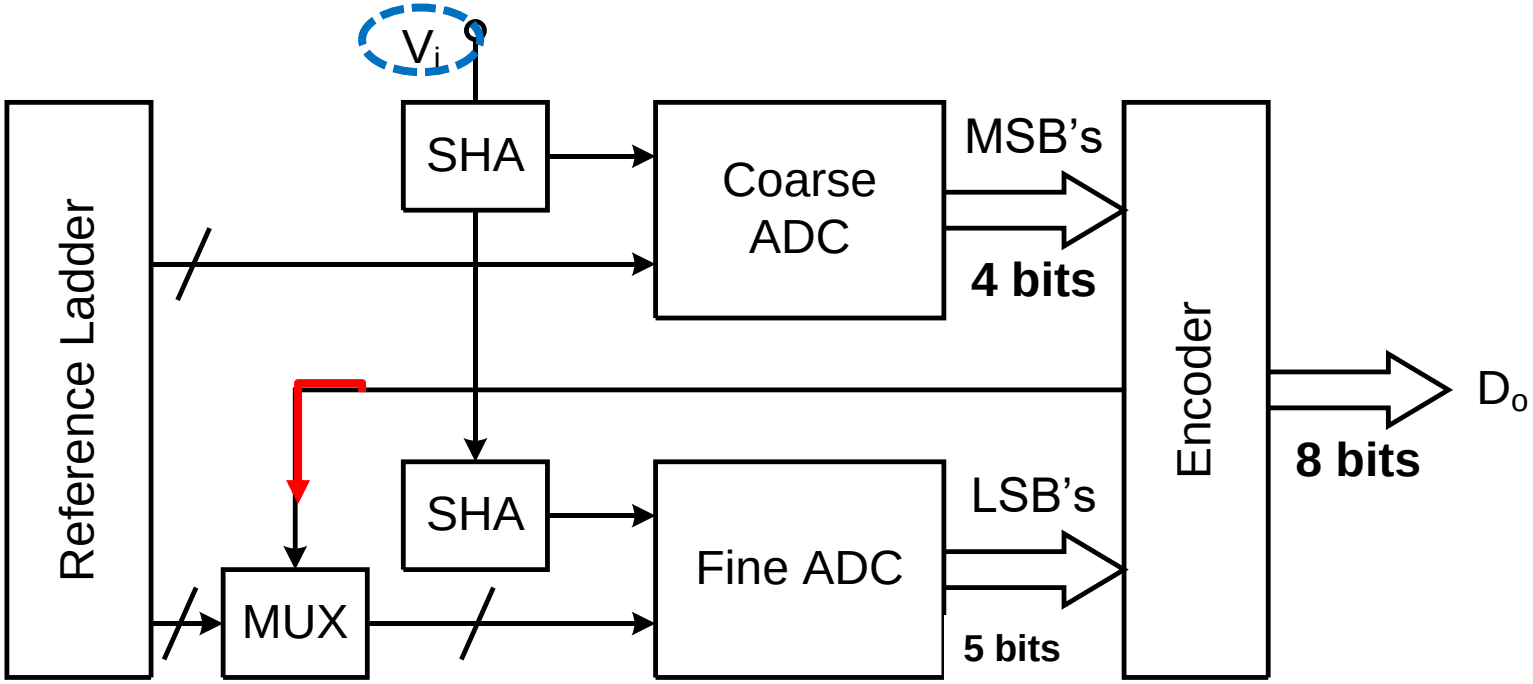
Differential SAR ADC



Lead to a better *compensation* of first order charge parasitics

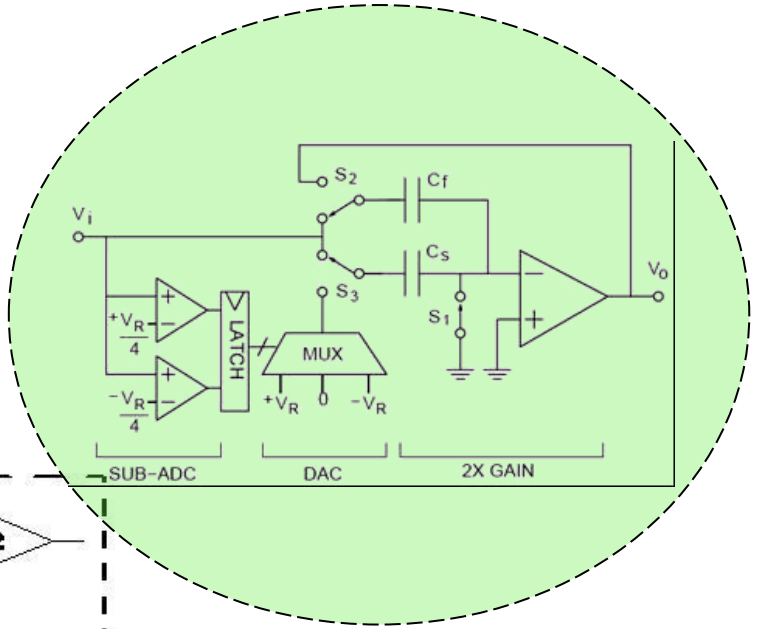
Sub-ranging ADC

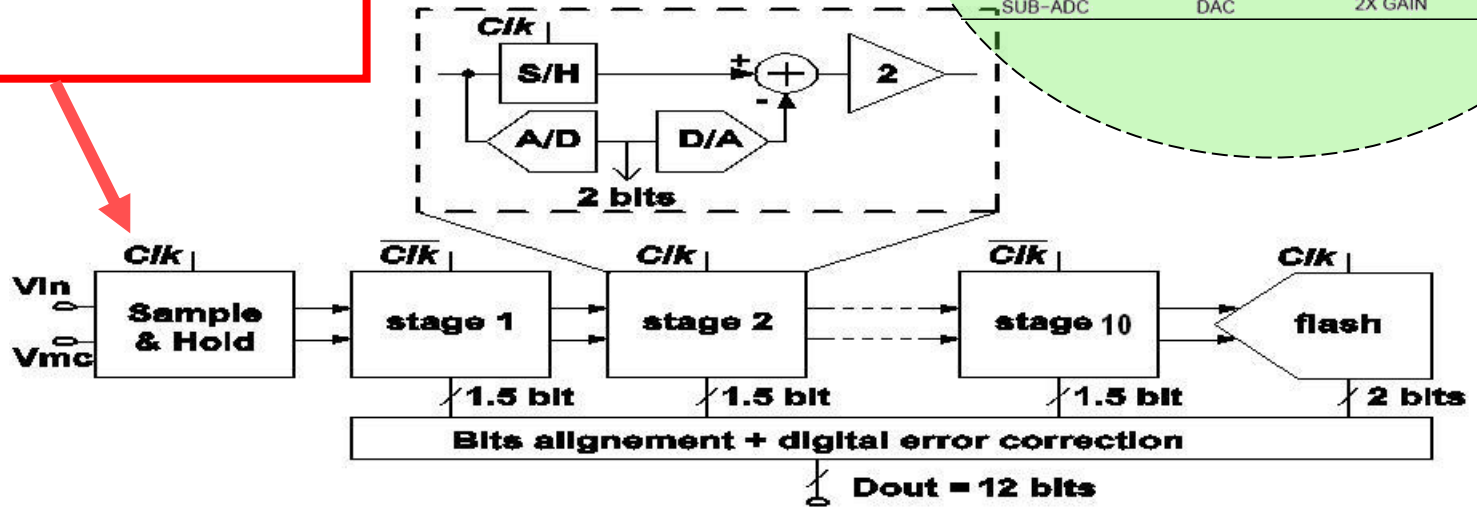
Sub-ranging ADC also doesn't require OpAmp and suitable for LV operation. However it requires high accuracy devices , for the "fine ADC".



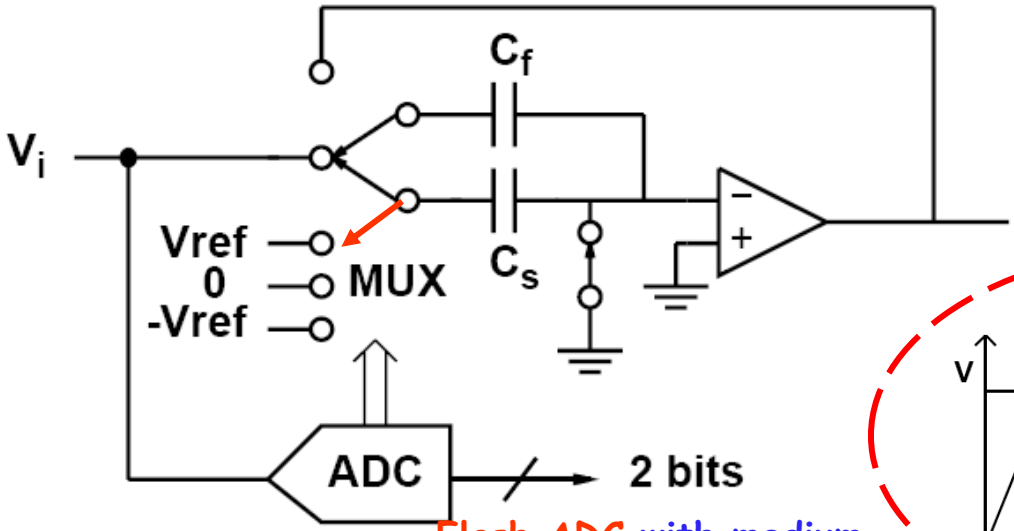
Pipe line ADC design: the baseline

Very very critical
Low signal amplification
Offset compensation
CM control
Noise issue, distorsion
….

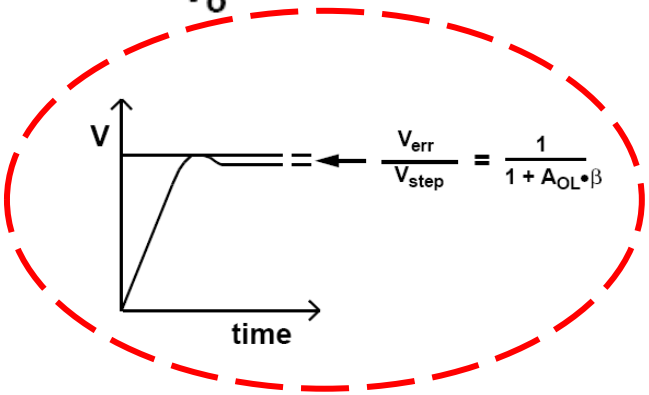




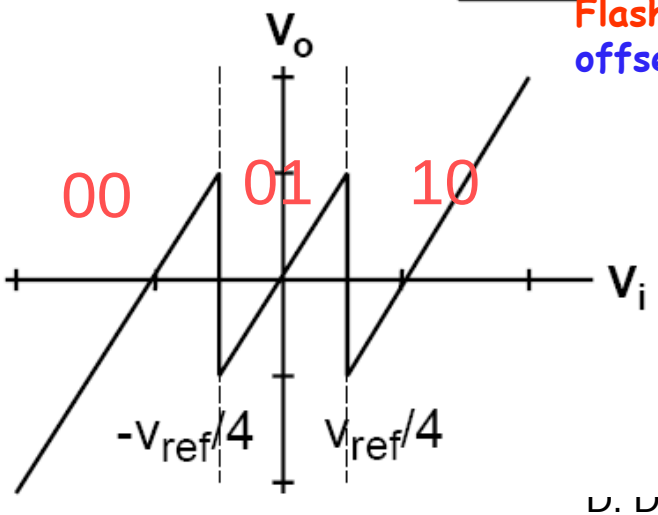
MDAC Function: Multiplier & DAC



The amplifier is the key point



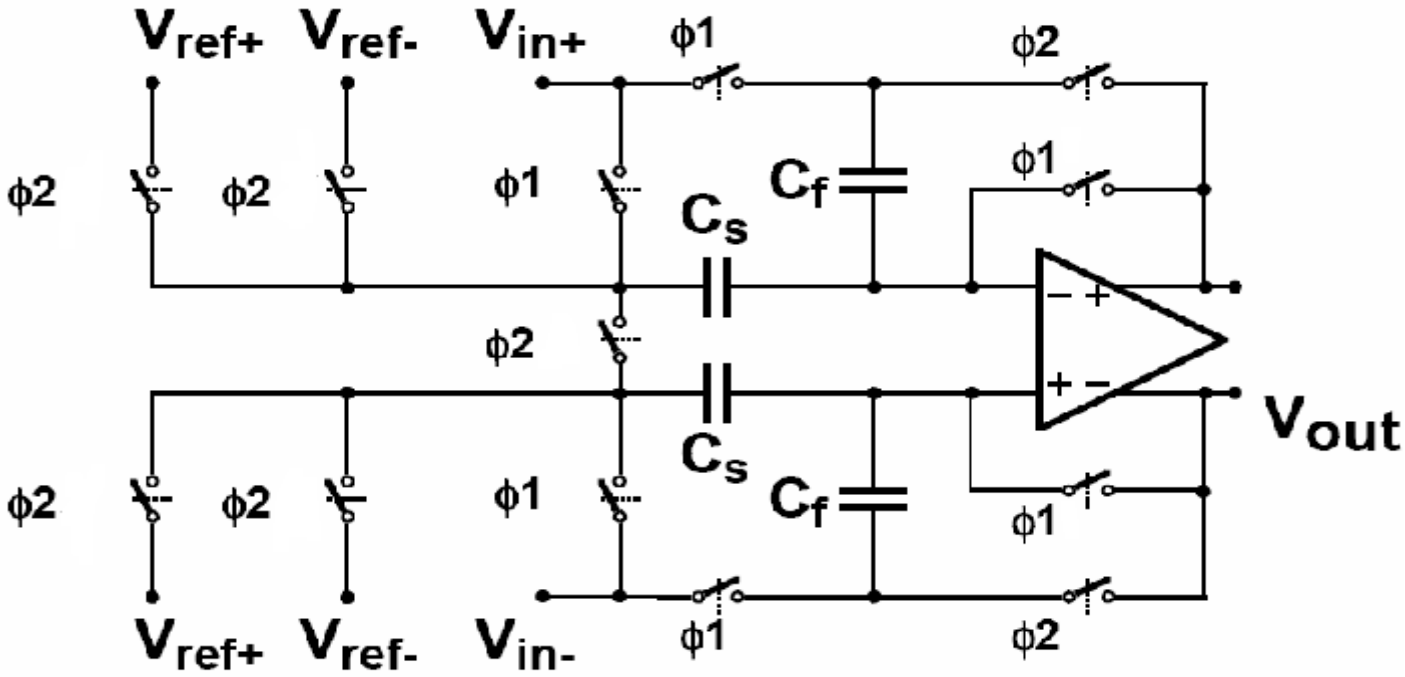
Flash ADC with medium offset (Vref/4)



$$V_o = \left(1 + \frac{C_s}{C_f}\right) V_i \pm \left(\frac{C_s}{C_f}\right) V_{ref}$$

Differential MDAC scheme

Vout = 2∗Vin ±α∗Vref; with α= ±1;0



Pipeline ADC Model (1)

- 1.5 bit MDAC stage
- 2.5 bit MDAC stage

Error sources:

Switches linearity

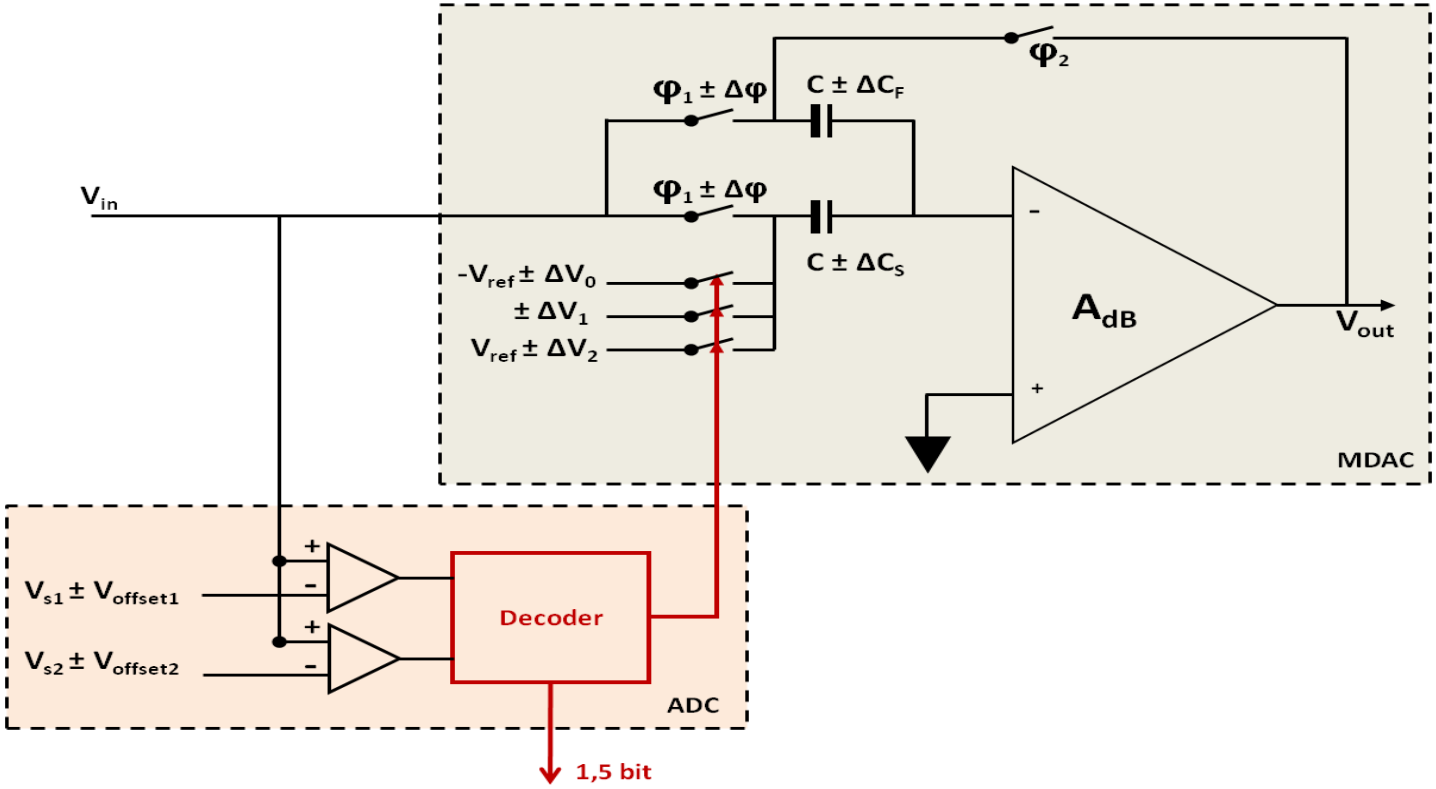
Clock distribution:(Sampling instant+Jitter)

Gain

OTA: A_{dB}

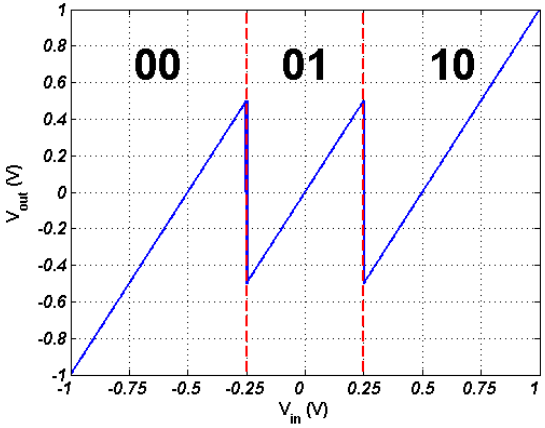
MDAC gain (capacitors)

Reference voltages ($\pm V_{ref}$): **drift & noise**



MDAC Transfer function

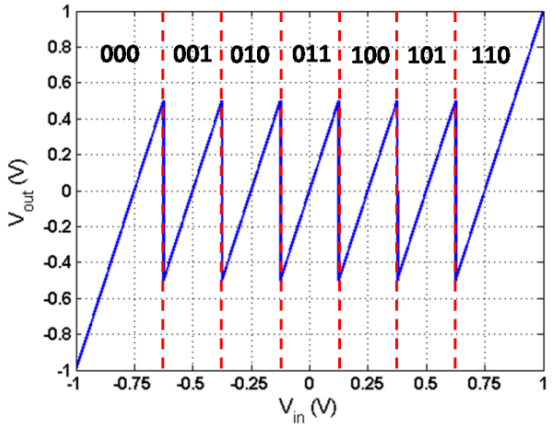
- 1.5 bit MDAC $V_{out} = 2 \cdot V_{in} - D_i \cdot V_{ref}$



$$D_i = [0, \pm 1]$$

$$V_{out} = 4 \cdot V_{in} - K_i \cdot V_{ref}$$

- 2.5 bit MDA



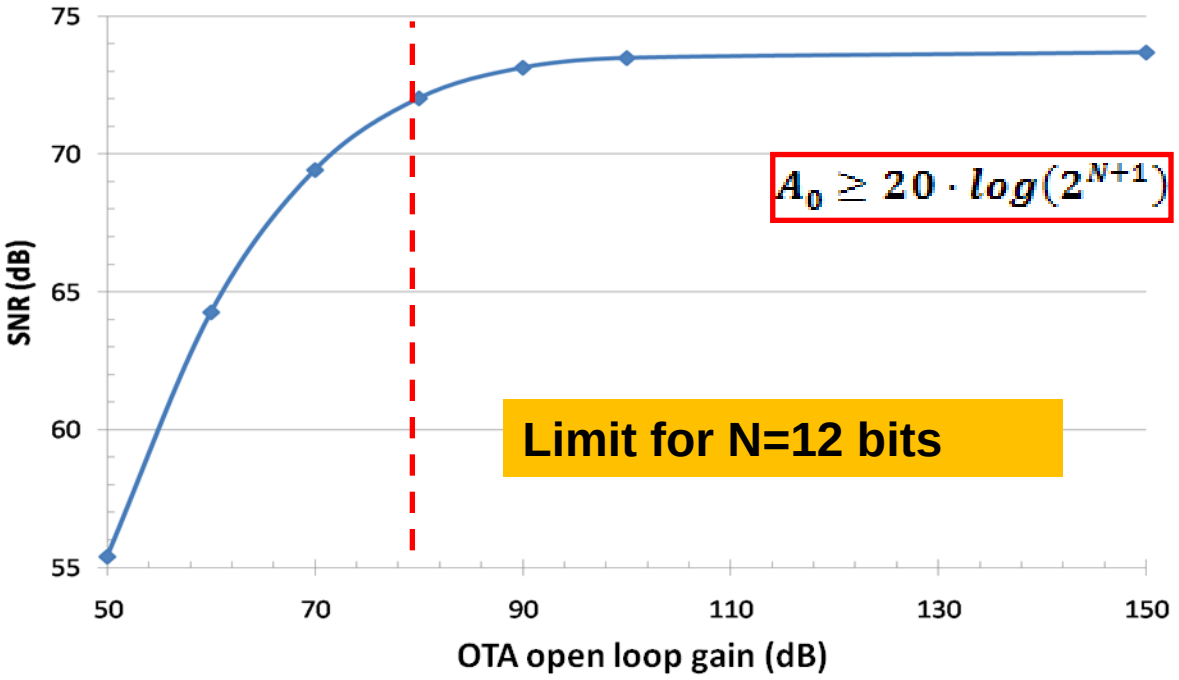
$$K_i = [0, \pm 1, \pm 2, \pm 3]$$

Pipelined ADC

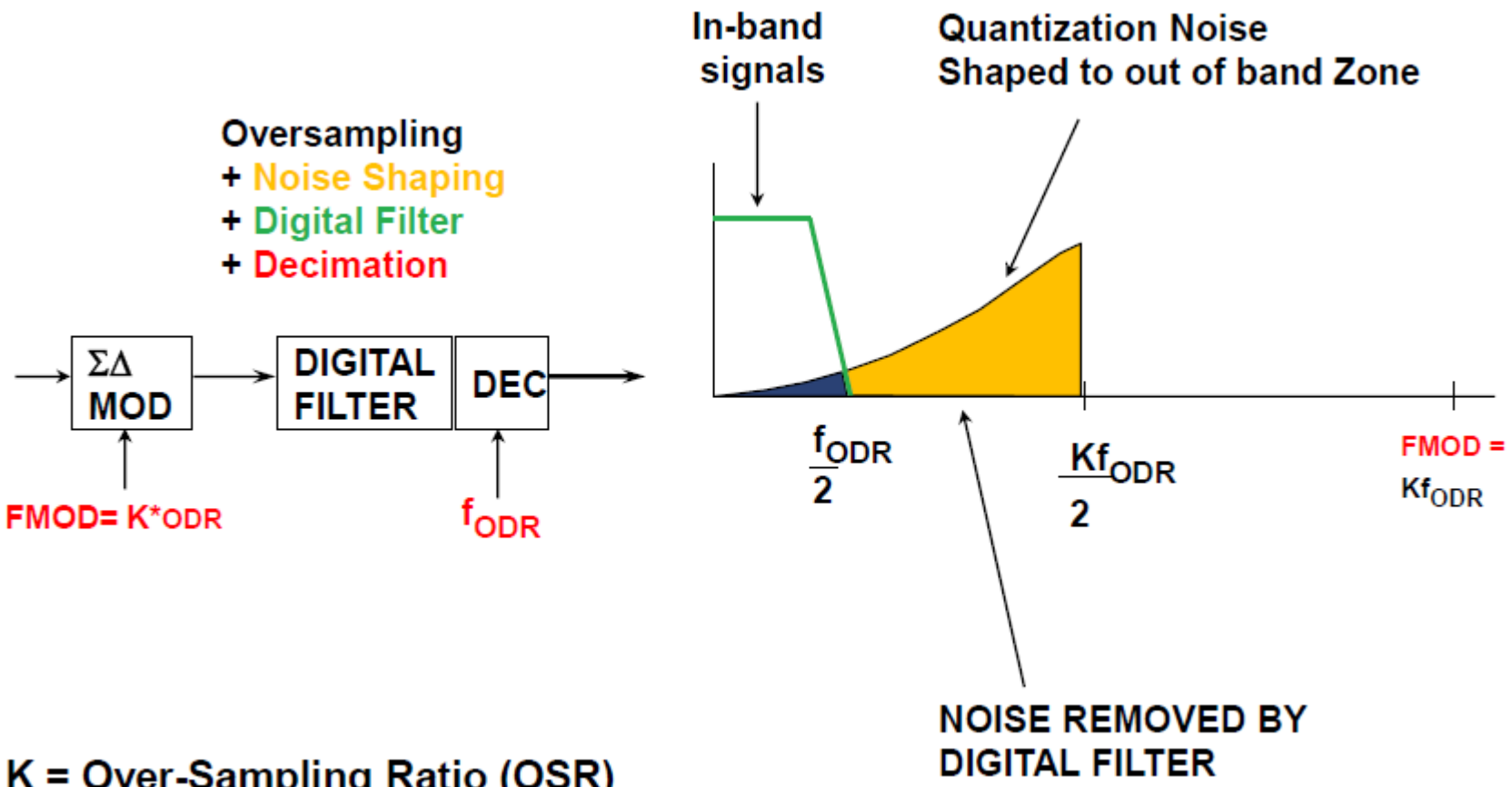
- **OTA Open loop gain issues**

$$V_{out} = \left(2.V_{in} - D_i.V_{ref}\right) \cdot \frac{1}{1 + \frac{1}{A_0 \cdot F_{fb}}}$$

with, $F_{fb} = \frac{C_f}{C_f + C_s + C_{in}}$

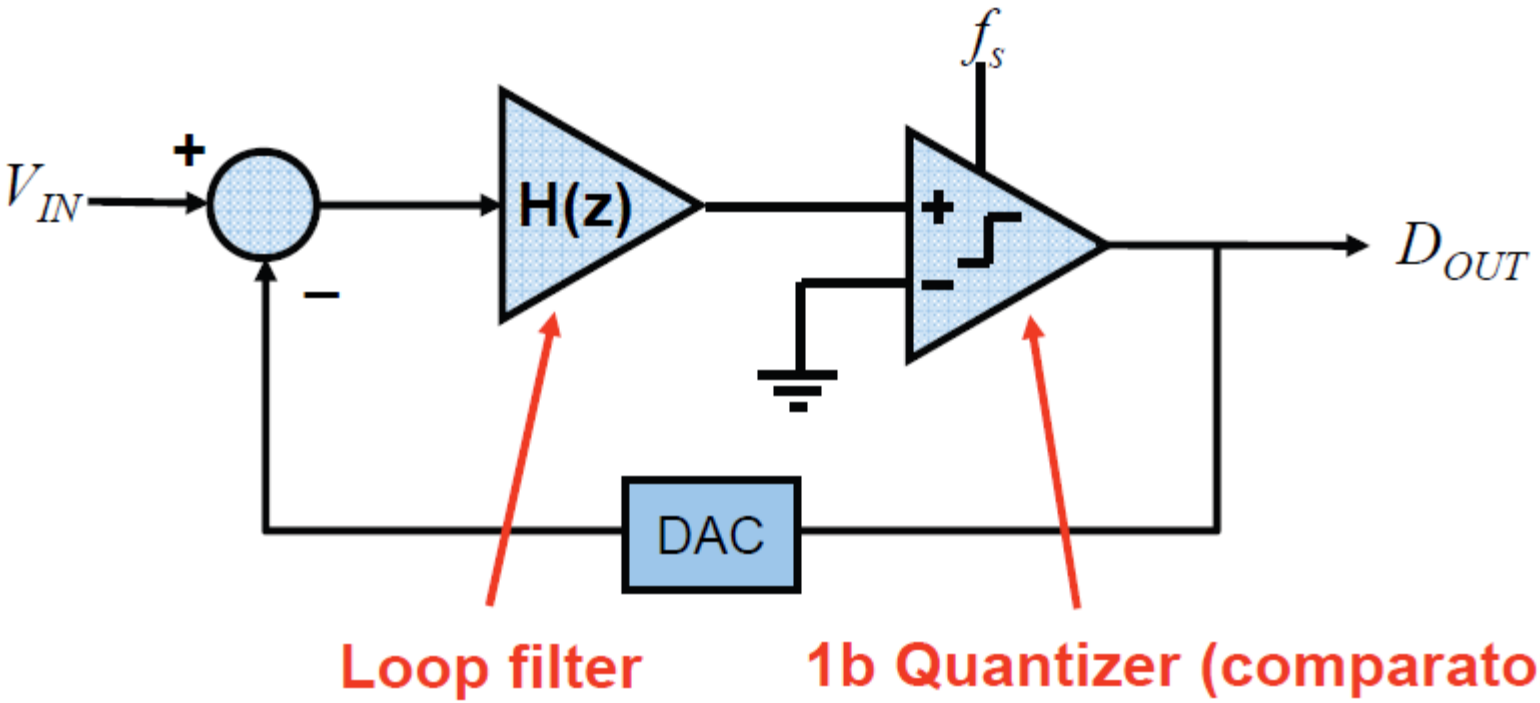


Fundamentals in Sigma Delta Modulators



Oversampling ADC: Sigma delta modulator

Analog 1-Bit ΣΔ modulators convert a continuous time analog input v_{IN} into a 1-Bit sequence D_{OUT}



Transfer Function: signal & bruit

In the simplest cases:
Loop filter response H(f) is low pass:

- Very high gain at low frequency.

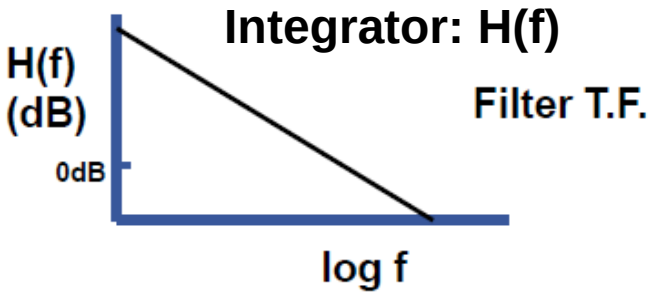
Usually,
The filter is a simple integrator or a cascade of integrators.
Note: noise is 'shaped' by the 1/[1 + H(f)] function.

Input Transfer Function

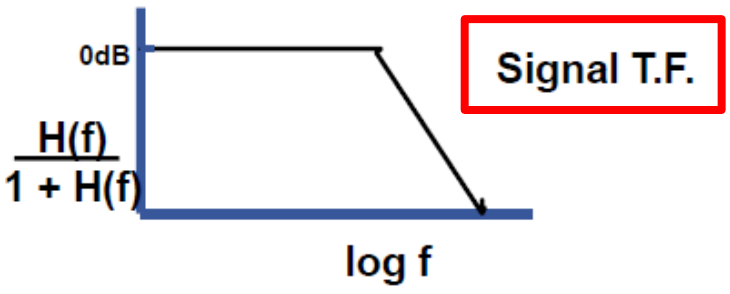
H(f)/ [1 + H(f)]

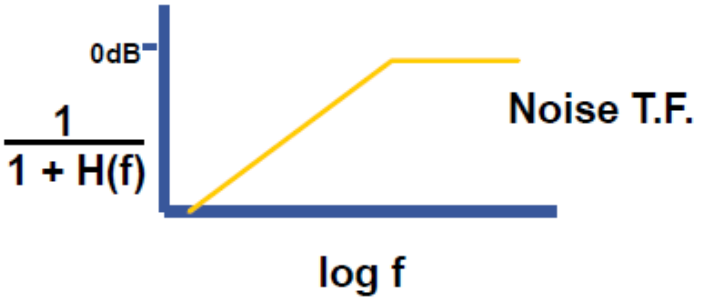
Noise Transfer Function

1/[1 + H(f)]

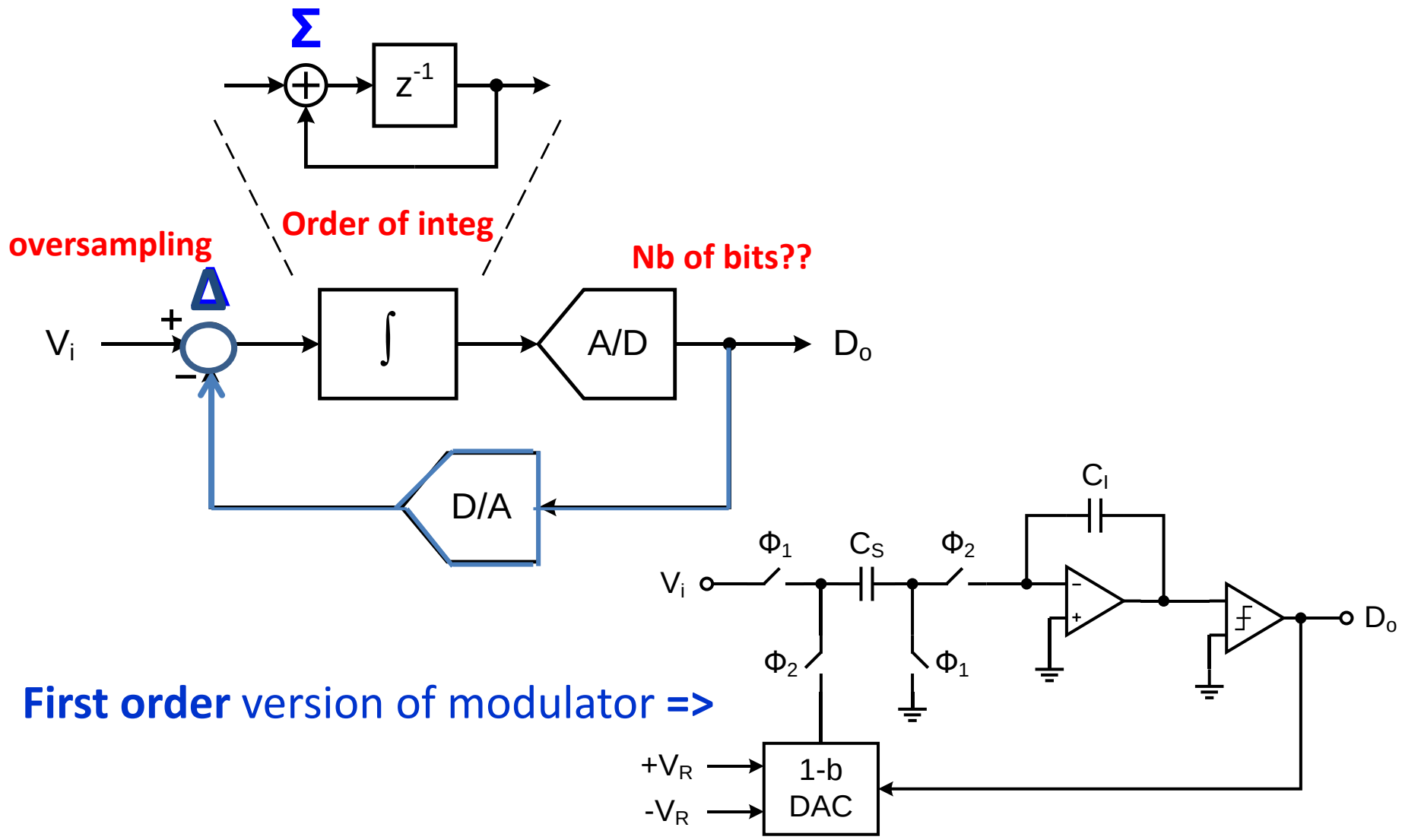


Noise Shaped





Sigma Delta Modulator



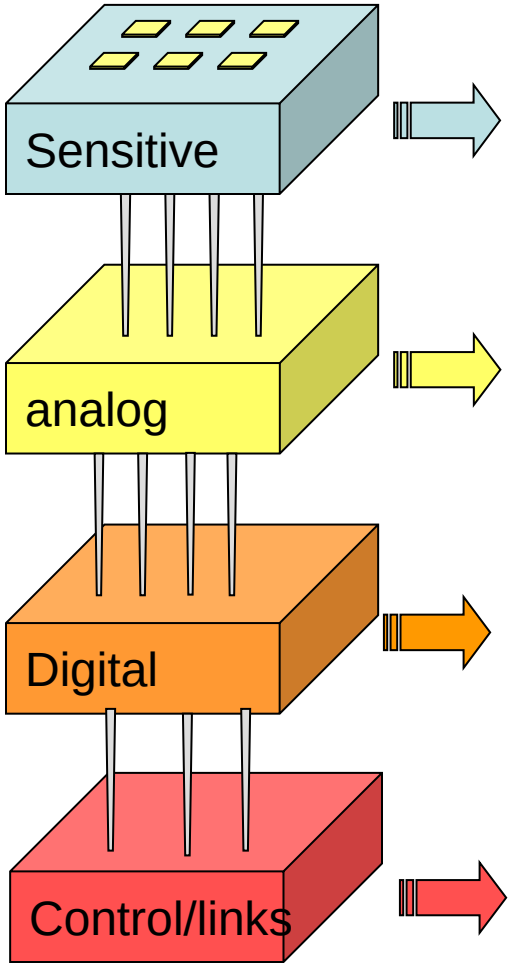
First order version of modulator **=>**

3D IT simplify view for SPECT-Xray CT

What we expect !

Large surface FOV=20x20 cm2

Megapixel Sensor



✓ Direct γ conversion CdZnTe/CdTe…
✓1-10 Megapixels – Pitch < 50 μm

✓ Amplifier
✓ Discriminator: two thresholds for “energy selection” or windowing for two simultaneous tracer imaging

✓ Fast readout-Photon counting strategy : ~10^6 ph/pixel/s for X-ray; Medipix or XPAD3 like architecture
✓ Time stamping

✓ Gating capability for X-ray and
✓Fast readout for dynamical imaging (cardiac movements)

Thanks !!