The lpGBT: from concept to a radiation-tolerant high-speed communication ASIC for the HL-LHC upgrade

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on behalf of the lpGBT team


28th June 2022
Outline

• Introduction [Pedro]

• UVM Verification [Adi]

• Testing / Validation [Stefan]

• Conclusions [Stefan]
The lpGBT Collaboration

• The lpGBT wouldn’t have been possible without our collaborators!

AGH UST
Poland
Marek Idzik
5 engineers

CTU
Czech Republic
Miroslav Havranek
2 engineers

CERN
Switzerland
Paulo Moreira
15 engineers
1 technician

KU Leuven
Belgium
Paul Leroux
3 Engineers

UNL
Portugal
Nuno Paulino
2 Engineers

SMU EE/PH
USA
Ping Gui / Jingbo Ye
8 engineers

CERN Coordination
lpGBTv1 Timeline

Dates of interest:
Specs frozen: 2015
lpGBT V0 submission: 07/2018
lpGBT V0 prototypes: 11/2018
lpGBT V0 extensive testing: Q4/18 - Q3/19

- 2021
  - 03/2021: lpGBT v1 submission
  - 27/Sept/2021: TWEPP 2021 Public presentation
  - 09/2021: Prototypes @ CERN
- 02/2022: 63 Wafer Ordered
  - 3089 die/wafer
  - 194k devices
- 02/2022: Neutron irradiation VLDB (VTRX+)
  - Target: 1014 n/cm^2
- 2022
  - Proton irradiation @ PSI
  - Functional validation and characterization started
  - Heavy ion @ UCL
- 2023
  - Start large scale testing
  - Start large scale packaging
  - End of Production
  - Industrial testing 8k ASICs
  - In house testing 2000 ASICs (reserved)

- ESE seminar on the lpGBT
  - 28 June 2022
  - Today!
  - Wafers on their way to CERN!
IpGBT Link Architecture

High radiation doses

LHC: up to 100 Mrad (10^{14} 1MeV n/cm^2)
HL – LHC: up to 1 Grad (10^{16} 1MeV n/cm^2)

No or small radiation doses

Short distance optical links: 50 to 300 m

Timing & Trigger

LD

LD

PD

TIA

FPGA

Custom optoelectronics

Custom ASICs

On-Detector

Radiation Hard Electronics

Off-Detector

Commercial Off-The-Shelf (COTS)

Electrical links to the frontend modules. Lengths: cm to few m

Timing & Trigger

DAQ

Slow Control

Timing & Trigger

DAQ

Slow Control

CERN EP-ESE Seminar, 28 June 2022

https://indico.cern.ch/event/1065136
What’s the lpGBT? [user point of view]

- Data transceiver with fixed and “deterministic” latency for both up and down links
  - Clocks and Data

- Downlink
  - 2.56 Gbps
  - FEC12
  - eLinks
    - Bandwidth: 80/160/320 Mbps
    - Count: 16/8/4

- Uplink
  - 5.12 Gbps or 10.24 Gbps
  - FEC5 or FEC12
  - eLinks
    - Data rates: 160 / 320 / 640 / 1280 Mbps
    - Count:
      - FEC5
        - Up to 28 @ 160 Mbps
        - Up to 7 @ 1.28 Gbps
      - FEC12
        - Up to 24 @ 160 Mbps
        - Up to 6 @ 1.28 Gbps

- Experiment control/monitoring functions
  - 10-bit ADC
  - 12-bit voltage DAC
  - 8-bit current DAC
  - Temperature sensor
  - Three I2C masters
  - Programmable parallel port: 16 x GPIO

- Package
  - 9 mm x 9 mm x 1.25 mm (pitch: 0.5 mm)
  - Pin count: 289 (17 x 17)
Specifications summary [radiation]

• The lpGBT is designed in 65 nm CMOS process

• Targets [not only] the innermost layers of the HL-LHC detectors
  • Total Ionizing Dose (TID)
    • 200 Mrad (two times safety factor)
  • Non Ionizing Energy Loss (NIEL) radiation
    • $\sim 10^{15} \text{ MeV } n_{eq}/\text{cm}^2$ (mainly a concern for the optoelectronics components)
    • [Over a 10 years lifetime]

• Operation robust to Total Ionizing Dose
  • Designed with ELT (enclosed-layout-transistor) whenever possible

• Operation robust to Single Events Upsets
  • Triple Modular Redundancy (TMR) used in the State Machines and the “low-frequency” section of the Data Path
  • Forward Error Correction used in the “high-frequency” section of the data path and over the optical links
  • Use of an LC-VCO architecture for increased SEU-Tolerance and low jitter.
  • Clock triplication at the output of the PLL
IpGBT - Verification

Adithya Pulli, CERN
on behalf of the IpGBT team

EP-ESE Seminar
28 June 2022 – CERN
**Verification - Introduction**

**What?**
- ASIC verification is one of the crucial steps of ASIC design process which ensures that the design specification is preserved in the actual design implementation.
- It can consume as much as 70-80% of the total ASIC design time.

**Why?**
- Humans tend to make mistakes.
- Cost of finding and fixing a mistake (AKA bug) increases significantly over project lifetime.

**How?**
- Build a realistic world (AKA verification environment) around a design (AKA Design Under Test - DUT).
- Exercise the DUT in all possible ways* using the verification environment.
- Check all the outcomes of the DUT are as expected.

*Note: All possible ways include both expected and unexpected scenarios to ensure thorough testing.
Verification - Introduction

• *Catch
  • It is impossible to exercise DUT in all possible ways in a reasonable amount of time
  • Algorithmically, verification is a PSPACE-complete problem

• What now?
  • Rely on constrained random stimulus to maximize the design space exercised
  • Use a methodology which supports efficient implementation of constrained random tests
  • Use metrics to gain confidence in the verification effort
    • *Quis custodiet ipsos custodes?* (Who will guard the guards themselves?)
    • Coverage, regression testing, bug-rate etc.

• Verification reduces the risk of finding a bug after fabrication. It cannot assure absence of any bugs
IpGBT Verification

- IpGBT verification landscape
  - Unit-level directed (and random) tests written in System Verilog and cocotb which mainly served as design sanity tests
  - Top-level directed tests written in System Verilog which mainly exercised debug features
  - Top-level highly random tests written in System Verilog following UVM methodology

- IpGBT UVM environment
  - The verification infrastructure built around IpGBT DUT to drive its inputs and observe its outputs

- IpGBT UVM tests
  - 11 tests were defined for IpGBT. 8 tests are very simple tests which mainly focus on checking the sanity of the environment
  - lpgbt_reg_rw_test exhaustively verifies register instantiation and connectivity from all configuration ports of IpGBT
  - lpgbt_fuse_burning_test exercises and verifies fuse burning process
  - lpgbt_rand_test randomly exercises most of the features of IpGBT
IpGBT UVM Environment

- Key design considerations
  - Modularity
  - Ease of randomization

- Supports RTL, triplicated RTL (tmr) and netlist (impl) versions of DUT

- Partially synthesizable drivers which are reused in post-si test setup

- SEE aware checkers

- Register Access Layer (RAL) with support for accesses through different interfaces

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IpGBT Rand Test

- Program PLL and datapath
- Trigger IpGBT to boot and get to a ready state
- Reports an error if the chip doesn’t get to ready state in expected duration
- Simulate a catastrophic event by injecting a sequence of operations which trigger frame-aligner/lock-filter/PLL/DLL/channel to unlock
  - Sequence blocks until chip recovers and reaches ready state
  - Data integrity checkers are disabled during this phase
- Continuous uplink/downlink data
  - I2C masters
  - Programmable IO
  - Random register accesses with error injection
  - Induce correctible FEC errors

Random variables:
- Number of operations and their order
- Config access mechanisms
- Configuration values
- clock phase and jitter

Mode:
- simplex_rx, simplex_tx, transceiver
- Boot config: fuses, ROM, none
- TX datarate: 5.12Gbps, 10.24Gbps
- TX FEC modes: FEC5, FEC12
- E-groups configuration: datarates, channels enabled etc
- CRC error injection in fuses
- config_mechanism: fuses, ROM, IC, EC, I2C

- Data integrity checks
- Clock frequency and phase checks
- Reset out check
- I2C master transaction check
- Dedicated checks for each operation
  - Data checks for I2CM
  - IO values for PIO tests
  - Expected register values after random register access with error injection
- Check status registers values of critical state machines
- Action counter values

Legend
- Description
- Random variables
- Checks
### IpGBT Rand Test

<table>
<thead>
<tr>
<th>Fault injection scope</th>
<th>Checkers</th>
<th>Fault injection frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Full injection</strong></td>
<td>Relaxed (allow up to 8 consecutive bits of data corruption in downlink and up to 3 consecutive frames corruption in uplink)</td>
<td>$F_{\text{clk}}/2$</td>
</tr>
<tr>
<td><strong>Partial injection</strong></td>
<td>Strict (doesn’t tolerate any corruption of uplink and downlink data)</td>
<td>$F_{\text{clk}}/2$</td>
</tr>
<tr>
<td><strong>No injection</strong></td>
<td>Strict (doesn’t tolerate any corruption of uplink and downlink data)</td>
<td>-</td>
</tr>
</tbody>
</table>
IpGBT Signoff

• **Tools and techniques**
  - Massive parallel regression testing using Oracle Grid Engine (OGE) batch system
  - Gitlab for content and project management using issues and merge requests
  - tmake based build system
  - vManager for regression management and metrics tracking

• **Metrics**
  - Regression pass-rate (98.24%)
    - 10k simulations on the final netlist
  - Code coverage (94.35%)
  - Functional coverage (100%)
  - Fault coverage (100%)
    - >2k SEU/node, 200 SET/node
**IpGBT verification timeline**

- **01-Jun-2020:** Start of verification framework development
- **June/July-2020:** Verification environment bring-up
- Configuration sequences
  - First functional tests
- **~21-Aug-2020:** First version of lpgbt_rand_test
- **Oct-2020:** Catastrophic events test phase added to lpgbt_rand_test
- **Dec-2020:** SEE tolerance built into checkers
- **Mostly SEE vulnerabilities**
- **Jan-2020 to Mar-2020:** Fault campaigns and netlist simulations

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IpGBT Verification – Key takeaways

• Verification can only show presence of bugs, but cannot prove their absence

• Start early! Verification is a resource intensive activity

• Before embarking on verification, define a verification strategy which considers
  • Functional verification
  • SEE verification
  • Netlist verification

• Use constrained random verification approaches. Randomize as much as possible

• Benefit from already existing verification IPs and verification productivity tools. Don’t reinvent the wheel
IpGBT - Validation and Testing

Stefan Biereigel, CERN
on behalf of the IpGBT team

EP-ESE Seminar
28 June 2022 – CERN
lpGBT - Testing Ecosystem

• Complex, rad-hard mixed-signal ASICs require extensive silicon validation efforts
• The „lpGBT tester“: dedicated, FPGA-based test system [1], enabling:
  • Lab characterization (functional tests & electrical characteristics)
  • Environmental testing (temperature)
  • Heavy Ion / Laser SEE testing
  • X-ray total ionizing dose testing
  • Automated volume production testing
• Based on high performance Xilinx Virtex 7 FPGA Reference Board (Xilinx VC707)
• Supplemented by further testing hardware (VLDB+ Demo Board, lpGBT characterization PCB)

lpGBT – Functional & Performance Characterization

- Extensive validation performed on lpGBTv0, functionality & performance OK for most features
- Remaining functional & performance issues identified successfully addressed in lpGBTv1
  - I²C Master yield issue fixed
  - Clock & data latency determinism now at ps-level
  - Phase shifter performance improved
    - Two channels had degraded performance: fixed
    - Improved low-voltage + TID performance
  - Deterministic jitter significantly reduced
    - Improvement about 2x
- Remaining issue: Reliability of eFuses
  - eFuses are foundry IP blocks
  - Fuse burning process unreliable in lpGBTv0 + v1
  - Fuses also degrade with TID (discussed later)
  - General advisory: Do not use eFuses, baseline other configuration mechanisms (ROM, I²C, IC, EC)
- Mitigations
  - Chip ID will be stored redundantly for mass production chips
  - Per-chip calibration data will be delivered through online database
Single-Event Effects Testing
Single-Event Effects Testing – General Information

- High complexity makes SEE testing challenging
  - Limited test time available
    - Exercise & monitor all modes/subsystems
  - Capture a-priori unknown chip failure behavior

- Testing of lpGBTv0 revealed several issues
  - Systematic design issue in configuration memory
    - Corruption of ASIC configuration
  - Critical part of clock distribution not TMR-protected
    - Bursts of errors on high speed link
  - SEE sensitivity of LC-VCO inductor
    - Transients of clock phase in PLL mode

- Known issues were addressed in lpGBTv1 design
- Qualification HI campaign in 2021 @ CRC HIF (Louvain-la-Neuve, Belgium)
Single-Event Effects Testing – General Information

• Scope of lpGBTv1 SEE qualification
  • Key modes of operation (Simplex RX, TRX modes)
  • Key high speed link modes (5 Gbps, 10 Gbps, FEC5, FEC12)
  • Different ePort/eLink configurations (data rate & group combinations)
  • Clock phase stability (eClock + Phase Shifters)
  • Slow-Control, power-up state machine (Configuration Memory, I²C Slave, I²C Master, IC, EC, config ROM, ...)

• Analog peripherals out of scope
  • Glitches & single conversion errors in ADCs & DACs to be expected, presence or magnitude not studied

• Similar expectations for all digital I/Os (Data, Clock, GPIOs, ...)
  • Part of their signal path is necessarily unprotected

lpGBTv1 installed in HIF Louvain, BE
**Dedicated Slow Control Testing**

- Exercised with single ion at UCL HIF CRC: LET = 32.4 MeV cm²/mg
- Power-up + configuration sequence w/ beam over 1 hour: no issues
- Exercised I²C Masters over 1 hour: no issues
- Saturation HI cross section for both subsystems < 2x10⁻⁸ cm²

**Power consumption**

- Monitored throughout all tests
- No latch-up sensitivity found

**Data path testing**

- Some data errors expected, since part of data path is not fully redundant
  - Some correctable: HS link protected by FEC
  - Some uncorrectable: eLink and associated logic cannot be fully protected
- Goal: Enable conservative estimates of in-experiment error rates
  - Using LET between 1.3 and 32.4 MeV cm²/mg - constrain threshold LET and saturation cross section
  - 1 hour per ion, 11 minutes per mode (TRX 5G FEC5, TRX 5G FEC12, TRX 10G FEC5, TRX 10G FEC12, TX 10G FEC12)
Data Path Reliability

- Key observation: Improved clock generator now fully robust against unlocks
  - In GBTX, BER is dominated by PLL unlocks producing long bursts of errors
- Link errors now dominated by single- and multi-bit errors
  - Originating in different parts of the data path
Single-Event Effects Testing – Data Path

Downlink Data Path

• Only small amount of downlink bit errors observed during 16 hours of testing

• Three main SEE signatures
  • FEC-correctable link errors: no impact
  • SET in eLink output driver: Single bit errors affecting one eLink
  • SET in deserializer: Frame corruption, simultaneous single errors in multiple groups

• Conservative estimate for high-fluence regions (e.g. CMS tracker): BER < 4x10^{-14} @ 1.28 Gbps
**Uplink Data Path**

- BER cross section depending on link data rate and FEC mode
- Similar SEE signatures
  - FEC-correctable link errors: *no impact*
  - Single-bit errors: affecting non-TMR'd parts of ePortRxGroup, scale with data rate
  - Frame errors: corrupt data of multiple links/groups in a single frame
- Conservative estimate for high-fluence regions (e.g. CMS tracker): BER < $1 \times 10^{-14}$ @ 8.92 Gbps
Single-Event Effects Testing – Inductor SEE Sensitivity

**Inductor SEE Sensitivity (1/2)**

- New type of radiation sensitivity, discovered during tests of lpGBTv0
  - Not reported in literature before
- Affects inductor used in 5.12 GHz VCO of lpGBT clock generator
  - Long-lived frequency shift (up to 100 ppm, depending on LET) of oscillator
  - Stimulates temporary phase shift of lpGBT clock generator in PLL mode
  - Large sensitive area (approaching $10^{-3} \text{ cm}^2$)
- Mechanism not yet fully understood (various studies underway), so only system-level mitigations available

**Inductor Micrograph**

**Heavy Ion Sensitivity Map**

Qualitative visualization of transient phase errors
Single-Event Effects Testing – Inductor SEE Sensitivity

Inductor SEE Sensitivity (2/2)

• Impact assessment performed
  • Dedicated 200 MeV proton test @ PSI
  • No danger to data transmission in any mode of operation
  • Concern only for timing derived from IpGBT clocks when in simplex TX mode
  • Effect suppressed in RX/TRX mode by higher CDR bandwidth

• Mitigation strategy
  • New default clock generator settings, minimize magnitude of effect
  • Recommendation: prefer clocks from transceiver-mode-lpGBTs for precision timing

• 200 MeV p+ cross section characterized for recommended settings

• Results & recommendations published in Application Note [2]

Total Ionizing Dose Testing
IpGBT X-ray TID Testing - Introduction

• TID design spec for IpGBT: **100 Mrad (200 Mrad with safety factor)**

• Common development makes qualification difficult
  • Large variability of use cases: expected lifetime dose, operational chip temperature
  • TID degradation highly dependent on dose rate, die temperature, bias conditions
  • Annealing behavior another important aspect

• Chosen approach
  • Small user survey carried out to identify application environments
  • Irradiation of 7 samples performed in different conditions (temperature, ultimate dose)
  • Dose rate: approx. 3 Mrad/h to limit the test time

• Caveat for data presented here
  • Due to high dose rate used, optimistic by 2x - 4x compared to in-experiment dose rates
  • Extrapolating the data to different temperatures is not straight forward
• Extensive X-ray campaign
  • Total test time: 4 weeks
  • Chips 1-6 irradiated deeply into failure in different conditions, to study TID margins of various blocks
  • Chip 7 irradiated up to 50 Mrad at room temperature, to study annealing behavior after low doses

• Main goals
  • Identify key failure mode and dose
  • Characterize degradation behavior of analog peripherals

<table>
<thead>
<tr>
<th>Mode</th>
<th>Die Temp (°C)</th>
<th>TID (Mrad)</th>
<th>Annealing with bias</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHIP1</td>
<td>10G FEC5</td>
<td>30</td>
<td>340</td>
</tr>
<tr>
<td>CHIP2</td>
<td>10G FEC5</td>
<td>30</td>
<td>400</td>
</tr>
<tr>
<td>CHIP3</td>
<td>5G FEC12</td>
<td>30</td>
<td>350</td>
</tr>
<tr>
<td>CHIP4</td>
<td>5G FEC12</td>
<td>30</td>
<td>400</td>
</tr>
<tr>
<td>CHIP5</td>
<td>10G FEC5</td>
<td>-5</td>
<td>560</td>
</tr>
<tr>
<td>CHIP6</td>
<td>10G FEC5</td>
<td>0</td>
<td>620</td>
</tr>
<tr>
<td>CHIP7</td>
<td>10G FEC5</td>
<td>30</td>
<td>50</td>
</tr>
</tbody>
</table>

TID test samples & test conditions
IpGBT X-ray TID Testing – General Information

**Configuration (Config Memory, EC, IC, I²C, ROM, CRC, PUSM)**

- No problems found during testing

**Power Consumption**

- Degrades gracefully, reducing during irradiation
- Changes in $P_{\text{tot}}$ smaller than variation over supply voltage range

**eFuses**

- Tend to lose information with TID
- High variability from chip to chip
- Once again: Strong advisory against using the eFuses!
IpGBT X-ray TID Testing – Data Path

- TID failure mode in all tested chips: Data transmission
- Uplink datapath is critical component
  - High speed serializer
    - Initially introduces correctable errors, gradually reducing link margin
    - At some point, too many errors are produced → user data corruption
  - Uplink eLinks (ePortRxGroup)
    - Fail to sample/forward data through uplink data path → user data corruption
- First failures always observed at low supply voltage
  - 100 Mrad difference between failures at 1.08 V and 1.20 V
  - No failures observed at 1.32 V
  - ASIC specification: 10% supply voltage variation → failures reported at 1.08 V
- Downlink data path did not experience any failures during testing

<table>
<thead>
<tr>
<th>CHIP</th>
<th>Temp</th>
<th>UL Errors (Correctable)</th>
<th>Data Errors @ 160 Mbps</th>
<th>Data Errors @ 320 Mbps</th>
<th>Data Errors @ 640 Mbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHIP3</td>
<td>30 °C</td>
<td>270 Mrad</td>
<td>335 Mrad</td>
<td>310 Mrad</td>
<td>310 Mrad</td>
</tr>
<tr>
<td>CHIP4</td>
<td>30 °C</td>
<td>285 Mrad</td>
<td>355 Mrad</td>
<td>320 Mrad</td>
<td>320 Mrad</td>
</tr>
</tbody>
</table>

Uplink data path failure (5 Gbps, VDD = 1.08 V)

<table>
<thead>
<tr>
<th>CHIP</th>
<th>Temp</th>
<th>UL Errors (Correctable)</th>
<th>Data Errors @ 320 Mbps</th>
<th>Data Errors @ 640 Mbps</th>
<th>Data Errors @ 1280 Mbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHIP1</td>
<td>30 °C</td>
<td>140 Mrad</td>
<td>210 Mrad</td>
<td>220 Mrad</td>
<td>210 Mrad</td>
</tr>
<tr>
<td>CHIP2</td>
<td>30 °C</td>
<td>200 Mrad</td>
<td>285 Mrad</td>
<td>285 Mrad</td>
<td>190 Mrad</td>
</tr>
<tr>
<td>CHIP5</td>
<td>-5 °C</td>
<td>385 Mrad</td>
<td>455 Mrad</td>
<td>470 Mrad</td>
<td>320 Mrad</td>
</tr>
<tr>
<td>CHIP6</td>
<td>0 °C</td>
<td>415 Mrad</td>
<td>520 Mrad</td>
<td>500 Mrad</td>
<td>325 Mrad</td>
</tr>
</tbody>
</table>

Uplink data path failure (10 Gbps, VDD = 1.08 V)
lpGBT X-ray TID Testing – Data Path

- Room temperature annealing after large TID
  - Chip 1/3 without bias
  - Chip 2/4 with bias
- Degradation observed when annealing with bias
  - Data path failures occur during annealing even at 1.2 V
  - Not seen for samples without bias
- Operational recommendation: Do not power lpGBTs when detectors are warmed up
  - For low-dose sample, no failures observed during long-term annealing with bias

Uplink data path failures during annealing
Bandgap Reference Generator

- Reference for all analog peripherals ($V_{\text{Ref}} = 1\,\text{V}$)
- Drift over TID larger than calibration accuracy ($\Delta V_{\text{Ref}} \sim -15\,\text{mV}$)
- Results obtained with X-ray irradiation, i.e. no DD effects
- Degradation observed during neutron testing: $\Delta V_{\text{Ref}} \sim -4\,\text{mV}$ at $2.8 \times 10^{14}\,\text{n/cm}^2$
On-Chip Temperature Sensor

- Sensor is based on bandgap-like circuit structure
- Output voltage is affected by TID
- Leads to uncertainty of up to 30 K across 200 Mrad TID spec
- Not useful for absolute measurements, but valuable for detecting transient changes

Current DAC

- Foreseen for PT1000-based temperature measurements
- Output current sensitive to VDD and TID
- Combined uncertainty of 20-30 K across 200 Mrad TID+VDD spec
- Similar performance as on-chip T-sensor
ADC/DAC

- Continuously characterized during X-ray irradiation
- Both very well-behaved
- When accounting for $V_{\text{Ref}}$ drift
  - Offset/slope changes limited to a few LSBs
- Performance limited by reference voltage drift
Conclusions

- **Silicon validation of lpGBTv1 successful**
- **All critical issues identified in lpGBTv0 successfully mitigated**
  - Includes performance, SEE, TID issues
- **SEE qualification campaign**
  - **Big leap in reliability compared to previous generation of high speed links**
  - Extensive SEE verification one of the keys to success
  - Novel radiation sensitivity of inductor characterized and mitigated to possible extent
- **Very reassuring TID response**
  - **High confidence of meeting demands of experimental environments**
  - Provided operational recommendations to experiments to maximize device lifetime
- **Volume testing commencing this year**
  - **Awaiting arrival of production wafers at CERN**
  - Next steps: packaging and testing at the contractor
Finding Information

• Official schedule
  • [https://ep-ese.web.cern.ch/content/lpgbt-vl-dcdc-schedule](https://ep-ese.web.cern.ch/content/lpgbt-vl-dcdc-schedule)

• LpGBT user manual
  • [https://lpgbt.web.cern.ch/lpgbt](https://lpgbt.web.cern.ch/lpgbt)

• LpGBT-FPGA core
  • [https://gitlab.cern.ch/gbt-fpga/lpgbt-fpga](https://gitlab.cern.ch/gbt-fpga/lpgbt-fpga)

• Contact and support
  • lpgbt-support@cern.ch
  • [https://lpgbt-support.web.cern.ch](https://lpgbt-support.web.cern.ch)
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Programming the lpGBT (1/2)

• The lpGBT is a highly flexible device:
  • Transceiver modes / Locking modes / Uplink data rate / FEC coding / Clock frequencies / Clock phases / Number of active eLinks / Phase-aligner modes / Pre-emphasis / Equalization / Driving strengths / ... / ...

• It won't simply work by just having it installed in your system...!

• It needs to be configured!

• There are:
  • 11 configuration pins to be “hardwired”;
  • 320 registers to be programed (240 R/W/F + 80 R/W + 142 R (status));

• Configuration pins define the “basic” operation mode;

• Configuration registers “customize” for the user application:
  • Some of them also affect the basic operation (e.g. PLLs, DLLs, startup procedure, etc.);
• Several options are available to read / write the configuration registers:
  • I2C port, always possible;
  • IC channel, only possible in Transceiver mode;
  • EC port, only possible in simplex TX or RX modes;
  • Access mode needs to be configured [pin “SC_I2C”].

• Optionally, the user’s configuration can be “burned into” the ASIC on a bank of “eFuses” and copied at startup into the configuration registers
  • Requires additional 2.5 V supply voltage during the programming cycle.
Electrically Interfacing with the Frontends

- FE Module
- Phase - Aligners + Ser/Des for E - Ports
  - E - Port
  - 160 Mbps to 1.28 Gbps ports
  - 1.28 Gbps ports
- LpGBT
  - DSCR, DEC, DeSER
  - SCR, ENC, SER
  - LD
- Control Logic
- Configuration (e-Fuses + reg-Bank)
  - ADC, PID
  - I2C Slave, I2C Masters
- I2C Port, I2C Masters
- 2.56 Gbps, 5.12 Gbps, or 10.24 Gbps
- LpGBTIA
- Ref CLK (optional)
- LR
- LpGBLD
- 1.28 Gbps
- 5.12 Gbps
- 2.56 Gbps
- 10.24 Gbps

-One 80 Mbps port
-GBT – SCA

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**eLinks Electrical “Standard”**

- **CLPS “CERN Low Power Signalling”**
  - [This should] **avoid any confusion with LVDS or SLVS**;

- **Link type**:
  - Point – to – point
  - Multi – drop transmitter

- **Max data rate**:
  - 1.28 Gbps (NRZ)

- **Max clock frequency**:
  - 1.28 GHz

- **Programmable signalling level**:
  - 100 mV to 400 mV (single-ended PP amplitude)
  - 200 mV to 800 mV (differential PP amplitude)

- **Common mode voltage**:
  - 600 mV (nominal)

- **Load impedance**:
  - 100 Ω

---

Common mode in the middle of the supply (Vdd/2) for best tolerance to ground fluctuations between modules;
eLink Line Receiver (eRx)

**Specs**
- **Data rate:**
  - Up to 1.28 Gbps
- **Common mode voltage range:**
  - 70 mV – 1.13 V
- **Differential input voltage:**
  - 140 mV – 450 mV

**Programmable**
- **ON/OFF receiver** (for power saving)
- **Data polarity** (to simplify routing)
- **ON/OFF termination** (100 Ω)
- **ON/OFF common mode setting** (for AC coupling, \( V_{dd}/2 \))
- **Programmable equalization:**
  - Optimized for cables with bandwidths of “infinite” (equalization off), 448, 299 and 224 MHz

---

Remember: AC coupling introduces a zero at \( f = 1/(2\pi \times Cc \times 100 \ \Omega) \) reducing the number of consecutive zero and ones that can be sent over the line reliably (DC base wander).
An external termination can be used to improve this but will certainly complicate your layout.

Off chip capacitors if AC coupling needed!

Macro cell, available for front-end designers (upon request)

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Using the eRx(s)

**Equalization:**
- Should only be used if needed (low bandwidth transmission line)
- Only effective for the high bit rates
- Equalization has (only) three coarse settings
  - User must choose the most appropriate!
- This requires a verification / scanning procedure from the user:
  a) Ideally the front-end designer implements a PRBS7 that the lpGBT can automatically verify;
  b) The user verifies the transmitted data at the counting room;
  c) A detailed scan procedure will also be proposed by the lpGBT team…

**eRx Check list:**
- Turn ON the receivers corresponding to the eLinks in use.
  - Obviously the others should be OFF
- Choose the polarity (non-invert / invert)
  - Turn on the termination:
    - Most likely the case (unless the chip in a multiple drop configuration – unlikely, or AC coupling to be optimized)
    - Enable the internal bias, if using AC coupling
  - Choose the appropriate equalization setting
eLink Data Sampling and “Deserialization”
Up eLink – Phase Alignment

- The phase of the incoming data signals is “unknown” in relation to the internal sampling clock!
- There are up to 28 eLinks inputs (potentially) all with random phase offsets

The solution:
- “Measure” the phase offset of each eLink input
- Delay individually each incoming bit stream to phase align it with the internal sampling clock
Automatic, semi-automatic or user driven procedures:

1. “Examine” all the eLink phases
2. Detect where the data “edges” are in relation to the clock;
3. Choose the phase that has the edges better centred around the clock
4. In automatic mode:
   - Once aligned, the PA can track the data phase wanders that cover virtually a full clock cycle:
   - To allow for this, the delay line covers more than one bit period: $1.75 \times T_{\text{bit}}$
   - And, during initialization only phases 4 to 11 are allowed
Using the Phase-Aligner(s)

• There are 8 phase-aligners in the lpGBT:
  • 7 serve 28 data eLinks;
  • 1 serves the EC eLink.
• A phase-aligner serves 4 eLink channels:
  • Called an eLink Group.
• The four channels in a Group share a calibration DLL:
  • User must setup:
    • The calibration DLL
    • The individual phase-aligner channels corresponding to the eLinks in use.

Phase Aligner Check list:
• Set the group data rate;
  • This sets the maximum number of eLinks per group (see next slides);
• Configure the DLL parameters;
  • Reset the DLL;
• Set the phase alignment mode:
  • Static phase selection:
    • User intervention needed.
  • Initial training with learned static phase selection:
    • User intervention needed
  • Automatic phase tracking;
• Enable and reset the channels in use;
eLink Rx Groups

- eLinks are “clustered” in groups of 4:
  - Simply called groups.
- The number of available groups is determined by the FEC uplink code in use;
- The number of available eLinks within a group is determined by the Group data rate;
- The possible data rates depend on the uplink bandwidth (5.12 or 10.24 Gbps)
- The data rate of each group can be set independently:
  - A couple of [over complicated] examples:
    - uplink 5.12 Gbps & FEC12: 8 eLinks x 160 Mbps + 4 eLinks x 320 Mbps + 2 eLinks x 640 Mbps
    - uplink 10.24 Gbps & FEC5: 8 eLinks x 320 Mbps + 4 eLinks x 640 Mbps + 3 eLinks x 1.28 Gbps

<table>
<thead>
<tr>
<th>Input eLinks (uplink)</th>
<th>5.12</th>
<th>10.24</th>
</tr>
</thead>
<tbody>
<tr>
<td>uplink bandwidth [Gbps]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FEC coding</td>
<td>FEC5</td>
<td>FEC12</td>
</tr>
<tr>
<td>Bandwidth [Mbps]</td>
<td>160</td>
<td>320</td>
</tr>
<tr>
<td>Maximum number</td>
<td>28</td>
<td>14</td>
</tr>
</tbody>
</table>
Note about eLink Input Pin Names

Input to the lpGBT

Group number: 0, 1,... 6 (there are 7 groups)

Pin Polarity: P – Positive, N – Negative
(Remember: polarity can be inverted at the output of the corresponding eRx)

Channel number within a group: 0, 1, 2 or 3 (there are 4 eLinks associated with every group)

Example: EDIN32N – eLink data input group 3 channel 2 negative polarity pin
The EC “Group”

- The EC “group” is a special case!
- It is composed of a single eLink!
- It only works at 80 Mbps!
- EC channel eLink Functionality is only available in Transceiver mode;
- In transceiver mode it is always available independently of the other Groups activity;
- Its mission is to implement an “experiment control” link, however it can be used as a general purpose link;
- [As seen before, this input can be used to control the ASIC in the simplex modes (TX / RX) but not in transceiver mode]
- Pins:
  - EDINECP (eLink Data In EC channel Positive pin)
  - EDINECN (eLink Data In EC channel Negative pin)
eLink Deserialization

• eLink inputs receive serial data from the frontend devices;

• These data is de-serialized and inserted in the uplink frame to be transmitted to the counting room (more on this soon):
  • The frame is processed in parallel in the chip before it is itself serialized for uplink transmission.

• In the case of transmission at 5.12 Gbps an eLink Group is always associated with the same 16-bits in the frame, the group bits.

• The same is true for 10.24 Gbps but in this case the group bits are 32 (the uplink frame is twice as long)

• The user knows from the position of the bits in the frame from which eLink group the data belongs to!

• Moreover, depending on the data rate, a specific eLink is identified by the position of the corresponding bits within the “group bits” (or simply, the position within the frame).

• After the eLinks input data is de-serialized, scrambling, FEC coding, interleaving header insertion and high-speed serialization takes place in the uplink data path...
Uplink Data Path

- FE Module
- Phase - Aligners + Ser/Des for E - Ports
- E - Port
- GBT - SCA
- One 80 Mbps port
- 160 Mbps to 1.28 Gbps ports
- Data-down
- Data-up clock
- eLink
- LpGBTIA
- LpGBLD
- 2.56 Gbps
- 5.12 Gbps or 10.24 Gbps
- Control Logic
- Configuration (e-Fuses + reg-Bank)
- SCR
- ENC
- SER
- I2C Masters
- I2C Slaves
- CDR/PLL
- LD
- LR
- ADC
- PID
- I2C Port
- I2C Ports
- LpGBT
- EOM
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High – Speed Uplink Frame

- The LpGBT supports the following uplink data rates:
  - 5.12 / 10.24 Gbps
- Data is transmitted as a frame composed of:
  - Header
  - The data field
  - A forward error correction field: FEC5 / FEC12
- The data field is scrambled to allow for CDR operation at no additional bandwidth penalty
- Efficiency = # data bits/# frame bits

<table>
<thead>
<tr>
<th></th>
<th>uplink</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>5.12 Gbps</td>
</tr>
<tr>
<td>FEC5</td>
<td></td>
</tr>
<tr>
<td>FEC12</td>
<td></td>
</tr>
<tr>
<td>Frame [bits]</td>
<td>128</td>
</tr>
<tr>
<td>Header [bits]</td>
<td>2</td>
</tr>
<tr>
<td>Data [bits]</td>
<td>116</td>
</tr>
<tr>
<td>232</td>
<td>204</td>
</tr>
<tr>
<td>FEC [bits]</td>
<td>10</td>
</tr>
<tr>
<td>20</td>
<td>48</td>
</tr>
<tr>
<td>Correction [bits]</td>
<td>5</td>
</tr>
<tr>
<td>10</td>
<td>24</td>
</tr>
<tr>
<td>Efficiency</td>
<td>91%</td>
</tr>
<tr>
<td></td>
<td>91%</td>
</tr>
</tbody>
</table>

- Data (User data payload)
- Forward Error Correction (Allows to correct transmission errors)
**Example: 5.12 Gbps FEC5 Uplink Frame**

Note: This is how you will see the uplink frame after it has been processed by the lpGBT-FPGA receiver but not how it is actually transmitted by the lpGBT ...

<table>
<thead>
<tr>
<th>Frame</th>
<th>Function</th>
<th>I/O Group</th>
</tr>
</thead>
<tbody>
<tr>
<td>FRMUP[9:0]</td>
<td>FEC[9:0]</td>
<td></td>
</tr>
<tr>
<td>FRMUP[25:10]</td>
<td>Data[15:0]</td>
<td>0</td>
</tr>
<tr>
<td>FRMUP[41:26]</td>
<td>Data[31:16]</td>
<td>1</td>
</tr>
<tr>
<td>FRMUP[57:42]</td>
<td>Data[47:32]</td>
<td>2</td>
</tr>
<tr>
<td>FRMUP[89:74]</td>
<td>Data[79:64]</td>
<td>4</td>
</tr>
<tr>
<td>FRMUP[121:106]</td>
<td>Data[111:96]</td>
<td>6</td>
</tr>
<tr>
<td>FRMUP[123:122]</td>
<td>EC[1:0]</td>
<td>EC</td>
</tr>
<tr>
<td>FRMUP[125:124]</td>
<td>IC[1:0]</td>
<td></td>
</tr>
<tr>
<td>FRMUP[127:126]</td>
<td>H[1:0] = 2'b10</td>
<td>HFH[1:0] = 2'b10</td>
</tr>
</tbody>
</table>

Number of data ports:
- 28 eLinks @ 160 Mbps
- 14 eLinks @ 320 Mbps
- 7 eLinks @ 640 Mbps
The order of operations is important

We avoid the details here since you will not have to worry with them, they will be “handled” by lpGBT-FPGA
High-Speed Line Driver
Accommodate the large capacitive load

On-chip 100 Ω matching

$\text{modDAC}<6:0>$

Modulation DAC

$\text{modDAC}<6:0>$

Modulation DAC

$\text{EmpDAC}<6:0>$

Emphasis DAC

$\text{EmpDAC}<6:0>$

Emphasis DAC

$I_{\text{max}} = 12 \text{ mA}$

$I_{\text{max}} = 8 \text{ mA}$

Pre-emphasis current driver

Reference Generator

Limiting Amplifier

Buffer Stage

Delay Stage

Emphasis Stage

Limiting Amplifier

Buffer Stage

Delay Stage

Emphasis Stage

IN$+$

IN$-$

OUT$+$

OUT$-$

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65
Line driver simulations (@5.12Gbps)

\[ I_{cc} = 40 \ mA \]
\[ I_{mod} = 12 \ mA \]
\[ I_{pre} = 8 \ mA \]
\[ C_{out} = 500 \ fF \]
Process: SS_100C_1.2V

**Advantage:**
- Pre-emphasis is made by subtracting the “bit stream” to itself after inversion and scaling!
- No narrow pulses required (as needed for the eTx scheme)

**Disadvantage:**
- The pre-emphasis is done by reducing the amplitude rather than peaking the signal during the pre-emphasis phase.
- The driver consumes in permanence \( I_m + I_{pre} \).

\[ I_{pre}(t) = -\alpha \cdot I_m(t - \Delta t) \]

\[ I_{m}(t) \]

\[ I_{out} \]

\[ V \ (mV) \]

\[ \text{time (ns)} \]

“long” delay

“short” delay

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Using the Line Driver

The user must:

• Enable the line driver for Transceiver and Simplex Transmitter modes:

• Enable the pre-emphasis if needed;

• Set the amplitude of the:
  • Modulation current;
  • Pre-emphasis current.

• Set the pre-emphasis pulse duration;

• It is possible to invert HS output polarity to simplify the PCB design:
  • The inversion is done @40M (before the Serializer) at the frame level.
High-Speed Line Receiver / Equalizer
The Equalizer in the LpGBT

- To be used in case of “low bandwidth” downlink
  - “Bypassed” by default.
- If needed, user programs the positions of the zeros of the four CTLE stages (and the 1st stage attenuation)
- It is an iterative process in a “case-by-case” basis
Eye Opening Monitor

- FE Module
- E-Port
- Phase - Aligners + Ser/Des for E-Ports
- E-Port
- E-Port
- E-Port
- E-Port
- E-Port
- Phase - Aligners + Ser/Des for E-Ports
- E-Port
- E-Port
- E-Port
- E-Port
- One 80 Mbps port

- GBT - SCA
- E-Port

- LpGBT
- DSCR
- DEC
- DeSER
- CLK Manager
- CDR/PLL
- SCR
- ENC
- SER
- LD
- Control Logic
- Configuration (e-Fuses + reg-Bank)
- ADC
- PID
- I2C Slave
- I2C Masters
- aIn[7:0]
- IO[15:0]
- I2C Port
- I2C Ports

- I2C Masters
- I2C Slaves
- PIO

- LpGBTIA
- LR
- Ref CLK (optional)

- 2.56 Gbps
- 5.12 Gbps or 10.24 Gbps
- 160 Mbps to 1.28 Gbps ports

- eLink
- data-up
- data-down
- clock

- 1.28 Gbps ports
- 2.56 Gbps
- 5.12 Gbps
- 10.24 Gbps

- One 80 Mbps port

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Eye Opening Monitor

- **Y-axis:**
  - 31 points, step = ~20 mV (covers from $V_{DD}/2$ up to $V_{DD}$)

- **X-axis:**
  - 64 points, step = ~6.1 ps in typical

- **Operation:**
  - Controlled through the I2C interface
  - Eye reconstruction at the "backend"

![Eye Opening Monitor Diagram]

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PLL / CDR and Clock Manager

- PLL / CDR and Clock Manager
- FE Module
- Phase - Aligners + Ser/Des for E - Ports
- E - Port
- Phase - Aligners 1, 2, 3, 4 - Ports
- 160 Mbps to 1.28 Gbps ports
- One 80 Mbps port
- GBT – SCA
- I2C Masters
- I2C Slaves
- I2C Port
- Control Logic
- Configuration (e-Fuses + reg-Bank)
- ADC
- PID
- I2C Port
- I2C Masters
- I2C Slaves
- SCR
- ENC
- SER
- DeSER
- DEC
- DSCR
- CDR / PLL
- CLK Manager
- Ref CLK (optional)
- LR
- LD
- LpGBTIA
- LpGBLD
- 2.56 Gbps
- 5.12 Gbps
- 10.24 Gbps
- 1.28 Gbps ports
- One 80 Mbps port
- eLink
- data-up clock
- data-down clock
Clock Syntheses

• This circuit generates all the clocks needed by the ASIC:
  • 40 MHz, 80 MHz, ..., 5.12 GHz
  • The 10.24 Gbps Serializer uses a DDR scheme
    • Simplex TX:
      • A 40 MHz external reference is needed
  • Simplex RX and Transceiver:
    • The downlink serial stream is used as a clock reference
      • CDR Locking modes:
        • External reference aided
        • Reference-Less Locking
Down Link Data Path

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Downlink Data Path

The order of operations is important

Once again] We avoid the details here since you will not have to worry with them, they will be “handled” by IpGBT-FPGA
eLink Groups and Serialization

- **FE Module**
  - E-Port

- **Phase-Shifter**
  - E-Port
  - 160 Mbps to 1.28 Gbps ports
  - data-down
  - data-up
  - clock

- **GBT – SCA**
  - E-Port
  - One 80 Mbps port

- **LpGBT**
  - 2.56 Gbps
  - 5.12 Gbps
  - 10.24 Gbps

- **Control Logic**
  - ADC
  - PID
  - I2C Slave
  - I2C Masters

- **Configuration (e-Fuses + reg-Bank)**
  - I2C Port
  - I2C Ports

- **I2C Masters**
  - aIn[7:0]
  - I0[15:0]

- **I2C Slaves**
  - I2C Port
  - I2C Ports

- **CLK Manager**
  - CDR/PLL

- **DeSER**
  - ENC
  - SER

- **LD Manager**
  - CDRL/PLL

- **LR**
  - Ref CLK (optional)

- **DSCR**
  - DEC
  - DeSER

- **I2C Slave**
  - PIO

- **I2C Masters**
  - I2C Port
  - I2C Ports
eLink Tx Groups & Serialization

- Tx eLinks are “clustered” in groups of 4 (similar to RX eLinks):
- The data rate of each group can be set independently: 80 / 160 or 320 Mbps
- The number of available eLinks within a group is determined by the Group data rate;
- [Similar to the uplink] Tx eLinks are associated with specific bits within the downlink frame (geographical addressing):
  - The user knows, from the position of the bits (and the selected data rate) in the frame, to which eLink the data will be serialized to.
- EC outputs (pins: EOUTECP / EOUTECP) are fixed data rate (80 Mbps) that can be used for Experiment Control in Transceiver mode or participate in the control of the ASIC itself in Simplex TX or RX modes

<table>
<thead>
<tr>
<th>Bandwidth [Mb/s]</th>
<th>80</th>
<th>160</th>
<th>320</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum number</td>
<td>16</td>
<td>8</td>
<td>4</td>
</tr>
</tbody>
</table>
To help implementing broadcast of data to the frontends, a “mirror” function is implemented for the Tx eLinks:

- Call it “buffering” if you prefer!

Since the number of active Tx eLinks depends on the selected data rate, “unused” transmitters can be used to “repeat” the data of the active channels

This called “mirror” function

The possibilities are:

- 80 Mbps:
  - No mirroring
- 160 Mbps:
  - Each channel is [can be] available on 2 outputs
- 320 Mbps:
  - Each channel is [can be] available on 4 outputs
eLink Line Transmitter (eTx)
eLink Driver

- **Data rate:**
  - Up to 1.28 Gbps
- **Clock frequency:**
  - Up to 1.28 GHz
- **Driving current:**
  - Programmable: 1 to 4 mA in 0.5 mA steps
- **Receiving end termination:**
  - 100 Ω
- **Voltage amplitude in 100 Ω:**
  - 100 mV to 400 mV (SE PP amplitude)
  - 200 mV to 800 mV (DIFF PP amplitude)
- **Common mode voltage:**
  - 600 mV
- **Selectable polarity**
- **Pre-emphasis:**
  - Driving current: 1 to 4 mA in 0.5 mA steps
  - Pulse width:
    - Externally timed
    - Self timed: 120 ps to 960 ps in steps of 120 ps
    - Clock timed: $T_{bit}/2$

Macro cell, available for front-end designers (upon request)
eTx Functionality

- Programmable delay line allows to generate pre-emphasis pulse widths between 120 and 960 ps
- Controls the polarity of the driver
- Half bit period pre-emphasis pulse width
- Pre-emphasis self-timed pulse width selectable
- Pre-emphasis mode selectable
- Pre-emphasis amplitude programmable

Diagram:

- invertData
- data
- Programable Delay line
- "0"
- 00
- 01
- 10
- 11
- bitRateClock
- preEmphasisWidth [2:0]
- preEmphasisMode [1:0]
- driverStrength [2:0]
- preEmphasisStrength [2:0]
eTx – Pre-Emphasis

No Pre-Emphasis
Driver Strength = 2 mA
Pre-Emphasis Strength = 0 mA
Pulse width = n.a.

With Pre-Emphasis
Driver Strength = 2 mA
Pre-Emphasis Strength = 2 mA
Pulse width = T/2

Data: PRBS 7
Data rate: 2.56 Gb/s
$C_L = 2 \times 5 \text{ pF}$
Note about eLink Output Pin Names

Output from the lpGBT

Group number: 0, 1, 2 and 3 (there are 4 groups)

Pin Polarity: P – Positive, N – Negative
(Remember: polarity can be inverted at the output of the corresponding eTx)

Channel number within a group: 0, 1, 2 or 3 (there are 4 eLinks associated with every group)

Example: EDOOUT32N – eLink data output group 3 channel 2 negative polarity pin
eLink Clocks

• Same drivers as for the Tx data eLinks, thus:
  • Programmable: polarity, driving strength and pre-emphasis

• 4 programmable Phase/Frequency clocks:
  • 4 independent
  • Phase resolution: 50 ps
  • Frequencies: 40 / 80 / 160 / 320 / 640 / 1280 MHz

• eLink Clocks:
  • 28 independent
  • Fixed phase
  • Frequency programmable
  • Frequencies: 40 / 80 / 160 / 320 / 640 / 1280 MHz
Experiment Control and Environment Monitoring
Digital

• Three I2C Masters:
  • Three general purpose masters
    • But one typically dedicated to control the laser driver (LDQ10)
  • Transfer rates: 100 KHz, 200 KHz, 400 KHz, 1 MHz
  • 7-bit and 10-bit addressing standards
  • Single-byte and multi-byte I2C read/write bus operations
  • Masters themselves controlled by:
    • The I2C slave port (always possible)
    • The IC – channel (only possible in transceiver mode)
    • The EC – port (Only possible in Simplex RX or TX mode)

• General Purpose I/O
  • 16-bit I/O port
  • Optional internal pull-up / pull-down resistors
  • Controlled by the same means as the I2C masters

• Output reset pin
  • Active low
  • Programmable pulse duration
Analogue Peripherals

• 10 bit ADC
  • Core: fully differential SAR
  • 8 channels (single ended or differential)
  • Voltage amplifier (x1 .. x32)
  • Sampling rate up to ~ 1MSps (limited by the control channel)
  • Monitoring of internal signals (like VDD)

• 12 bit voltage DAC
• 8 bit current DAC
  • can be attached to any analog input
  • range: 0-1mA (8bit)
• Temperature sensor
Example: Using an External Temperature Sensor
Package

• Small Footprint BGA package:
  • Size: 9 mm x 9 mm x 1.25 mm
  • Fine Pitch: 0.5 mm
  • Pin count: 289 (17 x 17)

• Routing of high speed signals optimized and simulated
  • Very small loss @ 10GHz
  • Models used for line driver simulations
The lpGBT-FPGA provides a back-end counterpart to the lpGBT ASIC

**Warning:**

- “Strategy” departures from that used for the GBT-FPGA
- Not a single generic “block”;
- But a set:
  - Of modules;
  - Of implementation examples;
  - Of reference notes.
- To help the user designing its own system!
The lpGBT model (will be) available to the users:
  • To simplify the design and verification of front-end (ASIC) and back-end (FPGA) systems

Contains all essential features related to the data transition and slow control interfaces:
  • Some of the chip’s analogue features are not modelled:
    • e.g.: pre-emphasis, equalization, analogue I/O (ADC,DAC), pull up/down resistors;

“Distributed” as one System Verilog file, compatible with:
  • Cadence Incisive
  • Mentor Questa
  • Synopsys VCS
IpGBT UVM Agents
lpGBT tests

- AliveTest
- EcAliveTest
- IcAliveTest
- I2cAliveTest
- FuseAliveTest
- RalTest
- I2cMastersTest
- RegRandRwTest
- PioTest
- FuseBurningTest
- RandTest
**lpGBT – Functional & Performance Characterization**

- Data path validation
  - High speed links (5G/10G, FEC5/FEC12)
  - RX / TX ePort characterization (BER testing, phase aligners, data jitter, ...)
  - Equalization / pre-emphasis on high-speed optical link and eLinks

- Clock performance testing
  - PLL and CDR clock quality, deterministic and random jitter, clock latency
  - High-Resolution clock phase shifter

- Analog peripheral characterization
  - Bandgap reference
  - Voltage ADC
  - Current DAC
  - Voltage DAC (linearity, noise, stability, temperature)

- Configuration/Start-Up/Watchdog Testing
  - Power-Up state machine
  - Configuration flows: I²C, EC, IC, ROM, eFuses, CRC, ...
  - I²C Master, GPIOs

- List not exhaustive!
Glitches on Clock Signals

- eClocks are not fully redundant all the way through the chain
  - Short (100s of ps) SETs might appear on the clock outputs
- eClock and PSclock were monitored during irradiation
  - Sensitive to pulses longer than 100 ps
- Frequency of occurrence characterized
  - No further data collected (typical length of individual pulses unknown)

Heavy ion cross section for glitches on eClocks and phase programmable clocks
Clock and Data Delay

• Clock and data delay through chip varies with VDD and TID
  • Variations across supply range on the same level as drift over TID

• Achieves excellent repeatability across power cycles
  • Only long-term drift needs to be accounted for

• Degradation of different eClocks is consistent
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Single-Event Effects Testing – Clock Glitches

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