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School of Engineering

Presentation for CERN Power Electronics

Single-Event Effects in Silicon Carbide High Voltage Power Devices for Lunar Exploration

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29-09-2022

Vanderbilt University

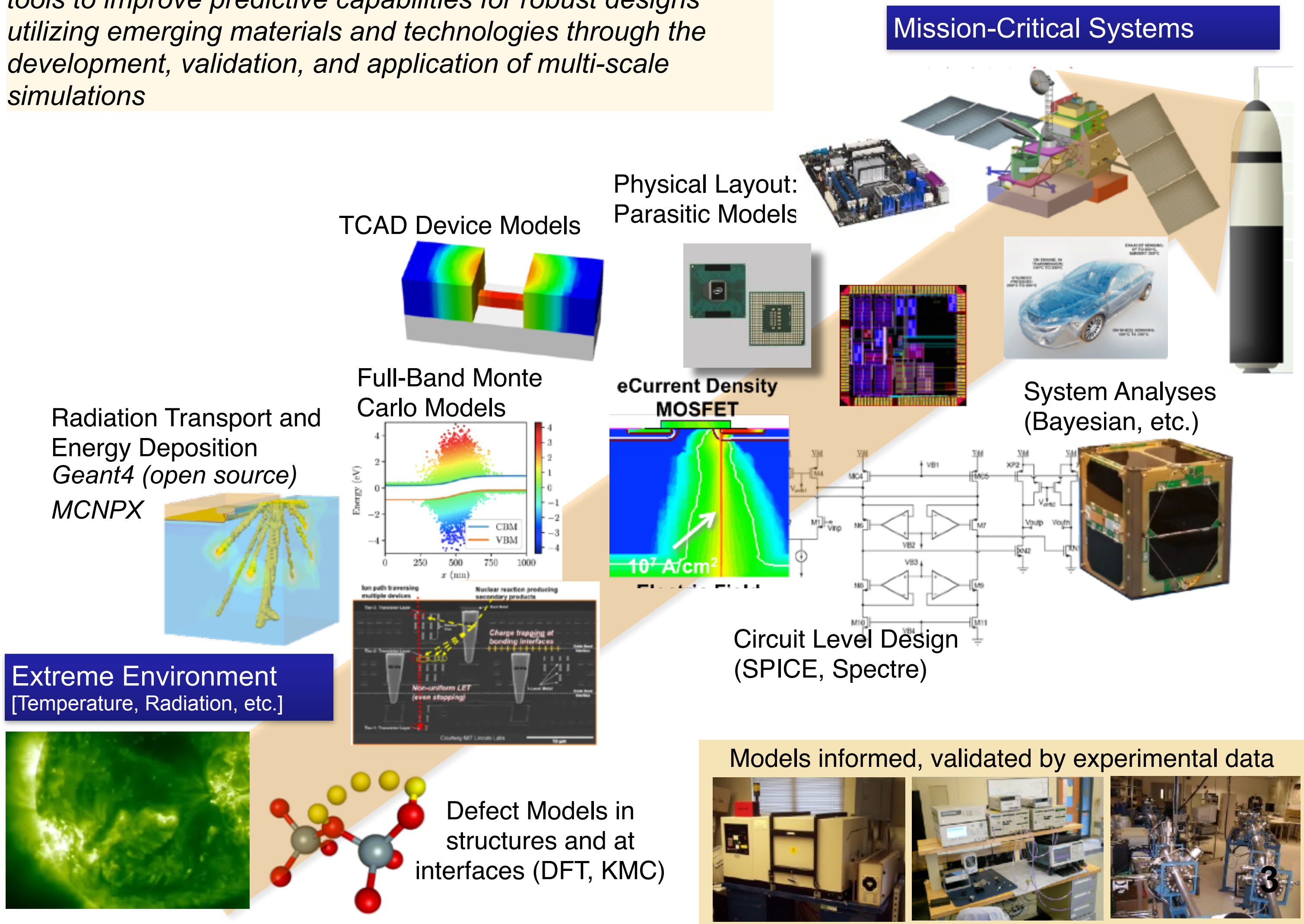
Supported by the NASA LuSTR Program under Grant Number 80NSSC21K0766

Institute for Space and Defense Electronics

Institute for Space and Defense Electronics

- Academic/professional research organization established by the School of Engineering of Vanderbilt University in 2003 to meet sponsor microelectronics reliability needs through physical circuit modeling, analysis, and design
- Personnel:
  - 9 Research Faculty & Engineers
  - 10 Faculty
  - 2 Admin Staff
  - 25 Graduate students
- ~$6M expenditures per year
- ~30 research programs

Goal: *Leverage advances in computing power and simulation tools to improve predictive capabilities for robust designs utilizing emerging materials and technologies through the development, validation, and application of multi-scale simulations*



ISDE Test Capabilities

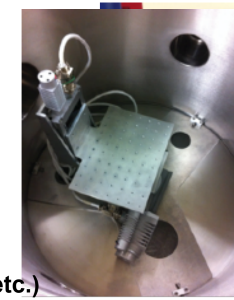
Institute for Space and Defense Electronics

Extensive test and characterization capabilities for understanding the effects of radiation on electronic devices and circuits

Facilities and Equipment
- Pelletron accelerator with vacuum test chamber
  • 250 keV to 4 MeV protons
  • 500 keV to 6 MeV alphas
  • 14 MeV oxygen
  • 16 MeV chlorine
- ARACOR 4100 10 keV x-ray irradiator
- Three Cs-137 irradiators
- Low temperature dewar
- Alpha and fission fragment button sources
- Two-photon absorption laser testing for single-event effects
- Array of test & measurement equipment, from DC to 50 GHz

Applications
- Emerging technologies
- Mechanisms studies
- Device/process characterization
- Degraded parameter extraction
- Parts evaluation

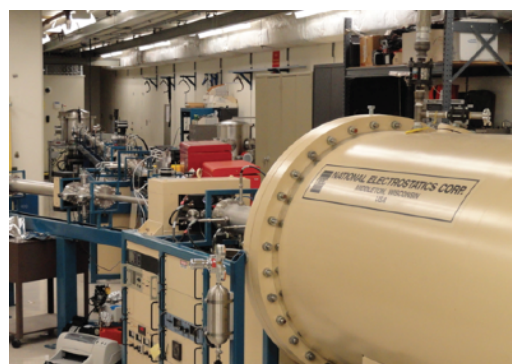
Supporting Services
- Device & circuit simulations
- SPICE model development
- Integrated circuit design (RHBD, etc.)



Extensive Off-site Experience
- Argonne National Laboratory
- Boeing Radiation Effects Laboratory
- Brookhaven National Laboratory
- Idaho Accelerator Center
- Indiana University
- ISIS/Rutherford Appleton Laboratory
- Lawrence Berkeley National Laboratory
- Los Alamos National Laboratory
- Michigan State University
- NSWC Crane
- Sandia National Laboratories
- Texas A&M University
- The Svedberg Laboratory
- TRIUMF
- University of California Davis

Mil-Std-883/750 testing
- Total ionizing dose - 1019
- Dose rate - 1020, 1021
- Neutron - 1017

JEDEC, EIA/JESD 57, ASTM 1192
- SEE



Lunar Surface Technology Research (LuSTR): Part of NASA Artemis Lunar Exploration Program

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NASA's Lunar Exploration Program Overview Sept.2020

The Lunar Surface Environment

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Moon rotates on its axis ~28 earth days
Lunar days and nights are 14 earth days long!
Moon irradiated by solar particles, gamma, galactic cosmic rays (GCR)
When ions strike surface elements of moon, create secondary particles, called “albedo”

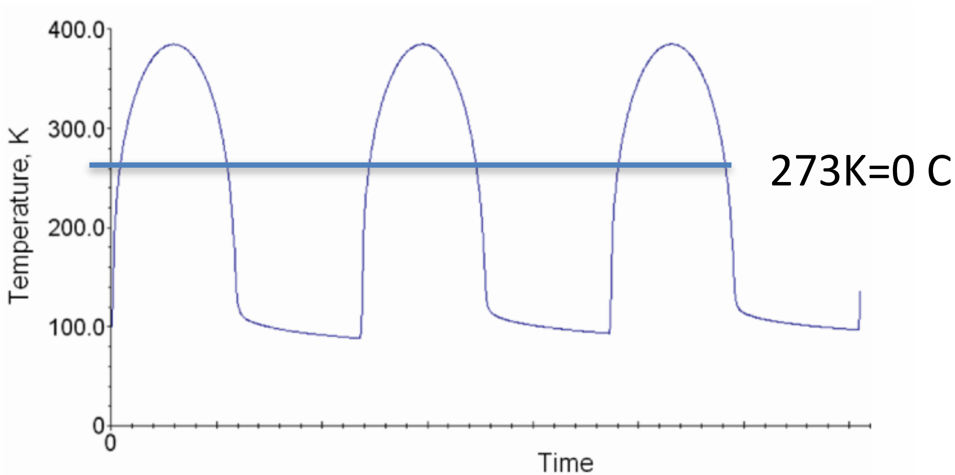
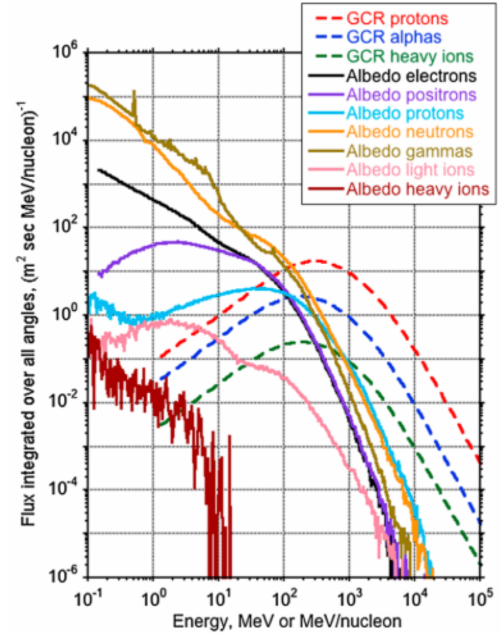


Figure 7.—Daily lunar equatorial surface temperatures.

Christie, et al, NASA/TM-2008-215300



Looper, et al, Space Weather, Vol 11, 2013

NASA LuSTR SiC Program Call for Proposals

Electrical Performance:

- **SEE-tolerant SiC power diodes: Minimum 1200 V, 40 A, with maximum recovery time of 40 ns**
- **SEE-tolerant SiC power transistors: Normally off (enhancement mode), minimum 600 V, 40 A, Rds_on < 24 mOhms while preserving low switching losses.**

Radiation Goal:

- **No heavy-ion induced permanent destructive effects upon irradiation while in blocking configuration (in powered reverse-bias/off state) with ions having a silicon-equivalent surface incident linear energy transfer (LET) of 40 MeV-cm^2/mg of sufficient energy to maintain a rising LET level throughout the epitaxial layer(s).**

GE

Power Device Landscape – Why SiC?

An estimated 50% of the electricity in the world is controlled by power devices…

Baliga 2010

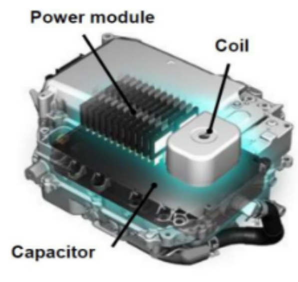
By End-Use Vertical

- Energy & Power
- Automotive
- Power Electronics & Telecommunication
- Defense
- Others

By Application

- Power Grid Device
- RF Device & Cellular Base Station
- High-Voltage, Direct Current (HVCD)
- Flexible Ac Transmission Systems (FACTS)
- Lighting Control
- Power Supply and Inverter
- Flame Detector
- Industrial Motor Drive
- EV Motor Drive
- Flame Detector
- Electronic Combat System
- Solar Energy
- Wind Energy
- Others

https://www.alliedmarketresearch.com/silicon-carbide-market

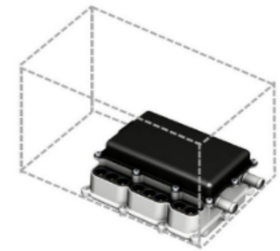


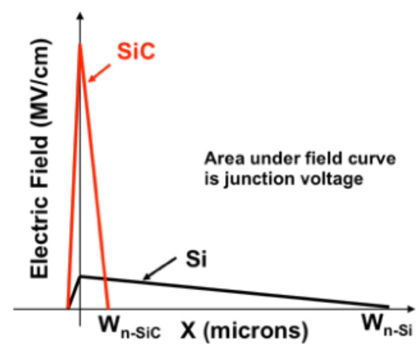
Silicon to SiC:

80% less volume

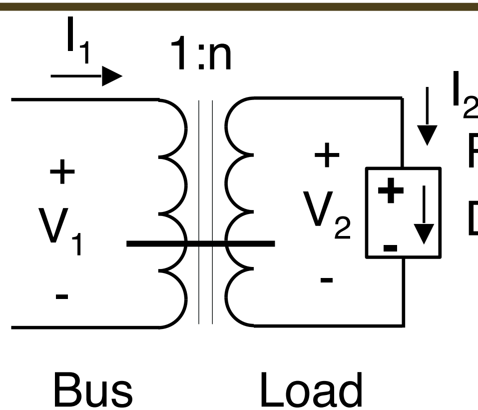
10X Higher $V_{BREAKDOWN}$

https://global.toyota/en/download/3523189





Justification for Using High Voltages



DC/DC Converter Model

P_2: Constant Power Load-
Determined by Spacecraft Power Budget

Buck Converter: $V_2=DV_1$ and $I_1=DI_2$

DC/DC converter at 100% efficiency modeled by DC (not magnetic) transformer

DC/DC Converter: $P_1= P_2 =V_2I_2$, fixed by the required output voltage, load power
Bus voltage goes up-> Bus current goes down
Bus conduction $I_1{}^2R$ loss goes down
Example: Micro-grid on moon: want 1kV or higher to carry power long distances

Effects of Bus Design on Spacecraft Parameters

Table 3.—Design Impacts of System Voltage With Power Electronics Mass Scaling

Design Characteristic	28-V NiH_2	50-V NiH_2	120-V NiH_2	300-V Low-V/NiH_2	300-V NiH_2	300-V Li Ion	300-V D2HET Li Ion
EPS Masses (kg)							
Solar Array	253.2	198.6	167.2	159.1	153.9	153.9	148.3
Battery	33.5	26.2	35.6	33.5	88.4	10.3	10.3
PMAD Boxes	116.4	72.4	51.5	20.3	20.0	20.6	9.3
PMAD Cabling	20.7	10.6	4.1	0.8	0.8	0.8	0.8
Total	423.8	307.8	258.4	213.7	263.1	185.5	168.7
Array Wing Area (m^2)	31.7	26.6	24.9	25.2	24.4	24.4	23.5
# Solar Cells / String	18	28	64	154	154	154	154
# Array Strings / Wing	624	336	138	58	56	56	54
Battery Cell Capacity (Amp-hrs)	50	20	10	50	10	4.5	4.5
Battery # Series Cells	20	34	81	20	201	74	74
HET PPU Mass (kg)	35	35	35	35	35	35	18
PPU Current (Amp)	382	205	84	33	33	33	32
PPU Heat Rejection (W)	1000	1000	1000	1000	1000	1000	500
PPU Heat Rejection Mass (kg)	44	44	44	44	44	44	29

EFFECT OF VOLTAGE LEVEL ON POWER SYSTEM DESIGN FOR SOLAR ELECTRIC PROPULSION MISSIONS

Thomas W. Kerslake
National Aeronautics and Space Administration
Glenn Research Center

Objective: Off-state voltage >= 1 kV, on-state I>=40 A

1kV Si MOSFET can conduct only 1-2 A

Radiation in Space: Ions, Protons, Electrons

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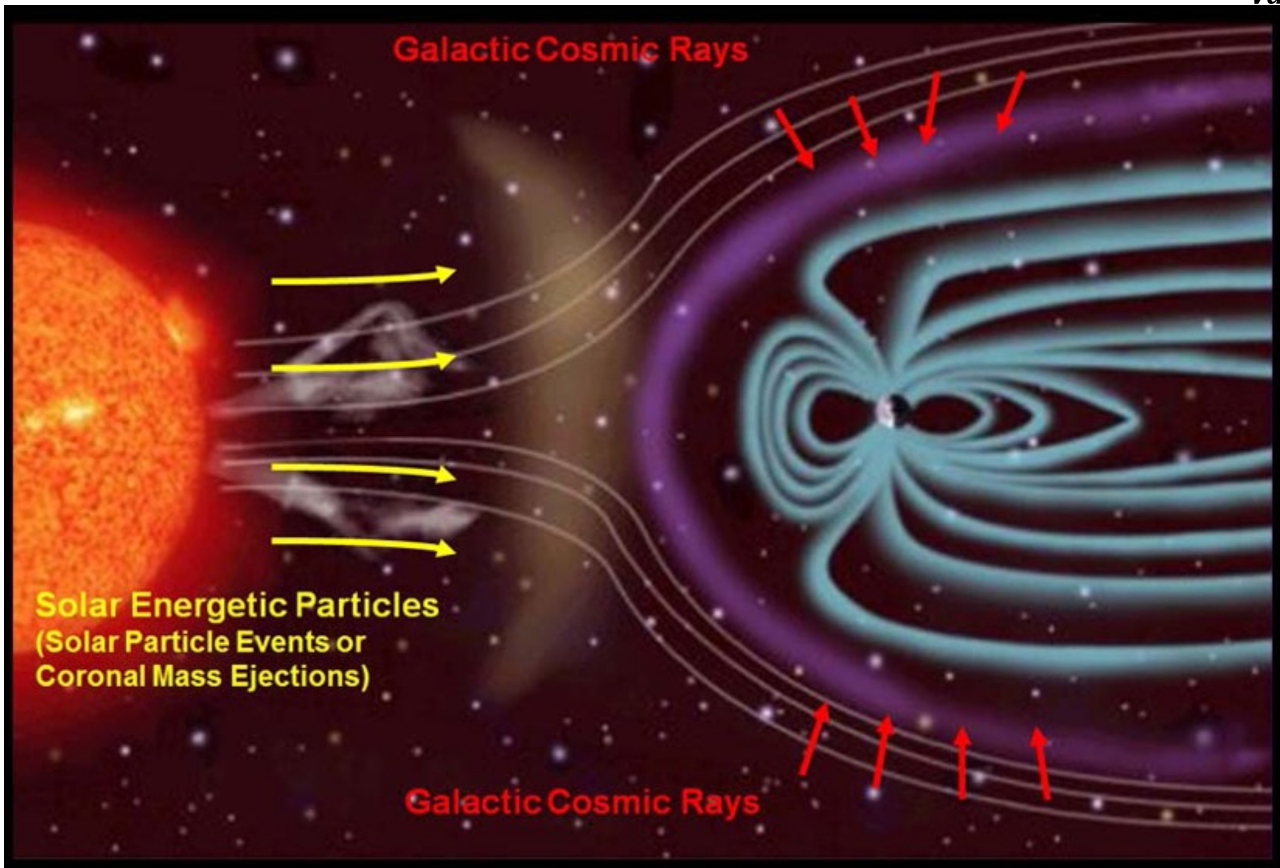


Image credit: NASA/JPL-Caltech/SwRI

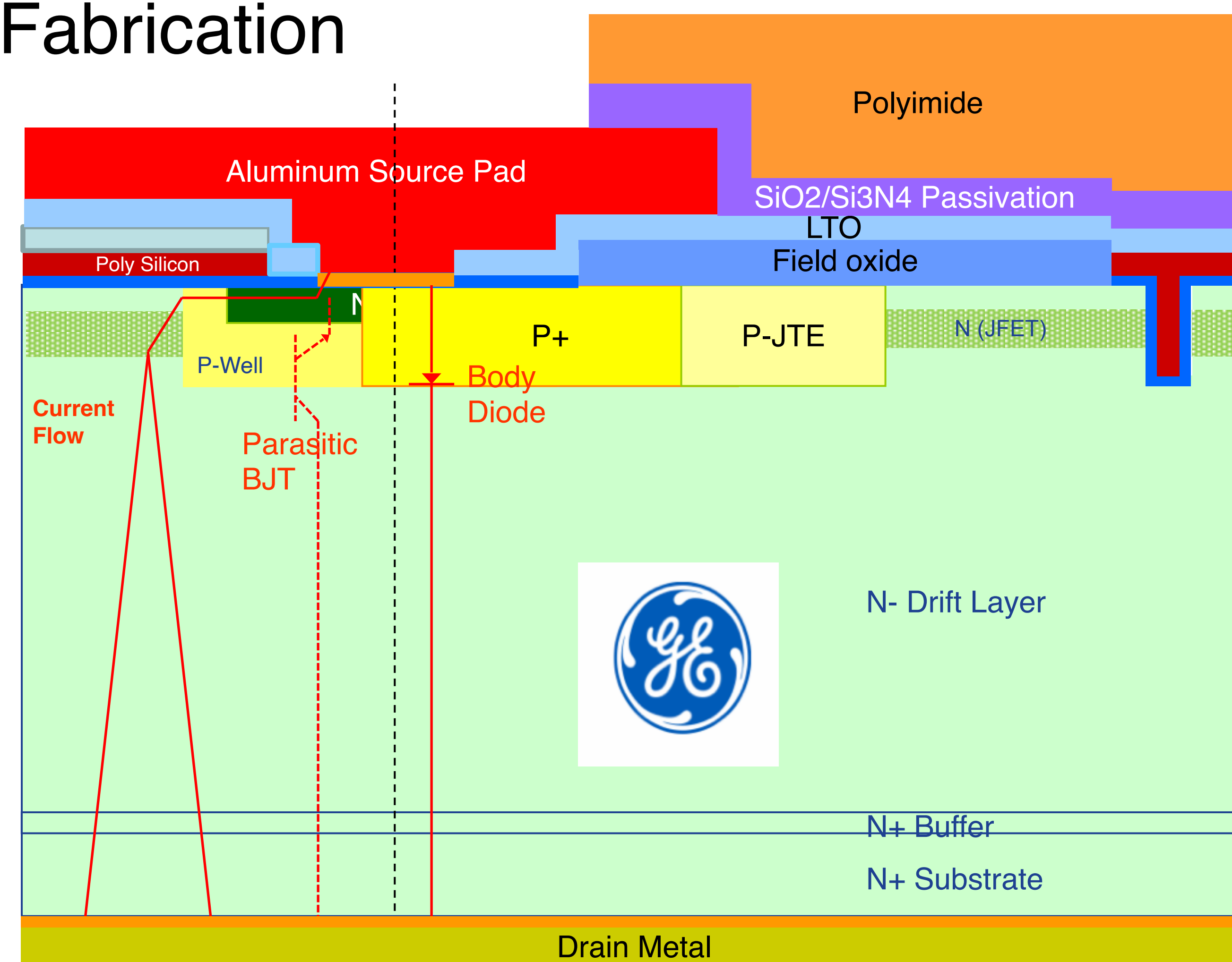
Terrestrial Ion Accelerator

Terrestrial accelerators can simulate parts of the radiation environment in space

VU Pelletron

SiC MOSFET Fabrication

- Starting epitaxial wafer with JFET Implants
- ↓ Alignment and dicing marks
- ↓ P-Well implantation
- ↓ Spacer formation
- ↓ N+ source implants
- ↓ P+ body implants
- ↓ Junction edge termination implants
- ↓ Graphitization and ion activation anneal
- ↓ Gate and field oxidation
- ↓ Gate Metal formation
- ↓ Ohmic Metal formation
- ↓ Gate Contact Via formation
- ↓ Bond Pad Metal formation
- ↓ Passivation and Back metal formation
- ↓ Polyimide protection



22 steps; 10 Masks

Power Device – Safe Operating Area (SOA)

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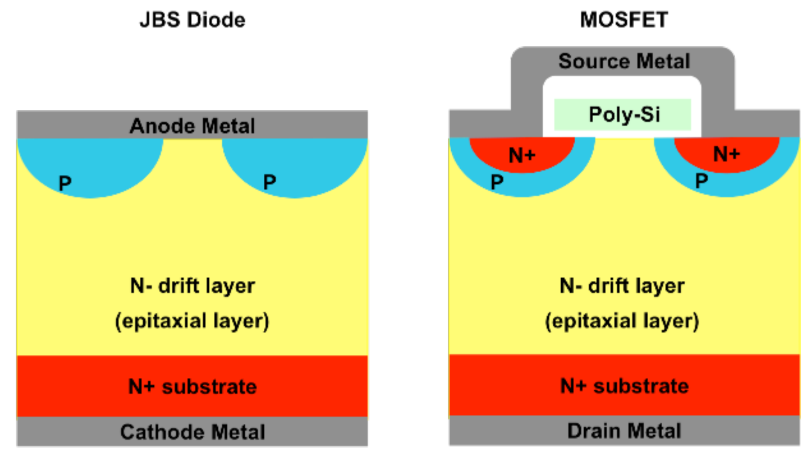
- Vertical power device
  - Suitable for diodes and MOSFETs
  - Vertical current flow
  - Performance influenced by epitaxial region resistance, R_{EPI}

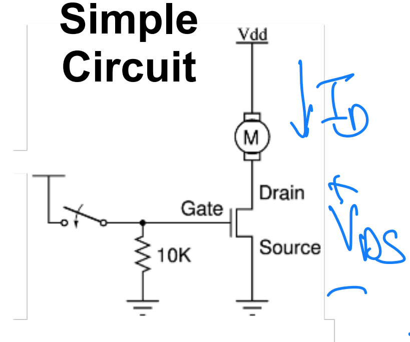
Doping Density ≈ e14's-e16's
L_{EPI} ≈ 10's-100's μm

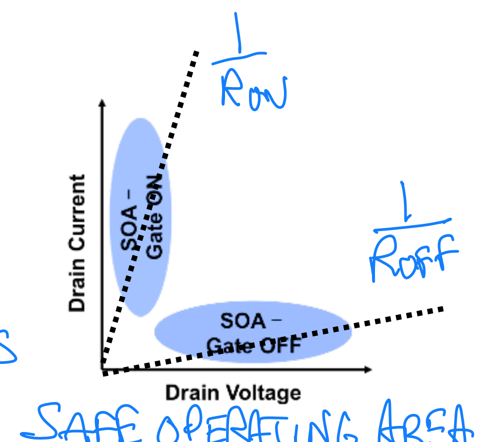


$$R_{EPI} = \rho * L_{EPI}/A_{EPI}$$

Power = $I^2 * R_{EPI}$

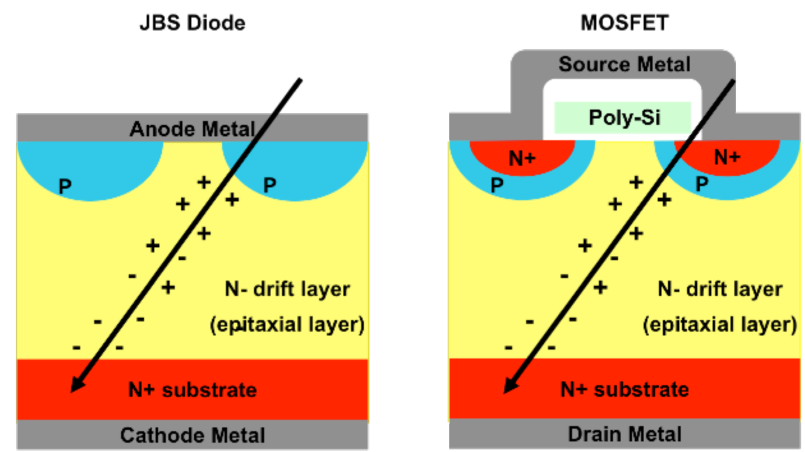
Simple Circuit





Power Device – Ion-Induced Operating Area

- Ion strike
  - Deposits charge along track
  - Vertical current flow
  - Creates resistive shunt between source and drain

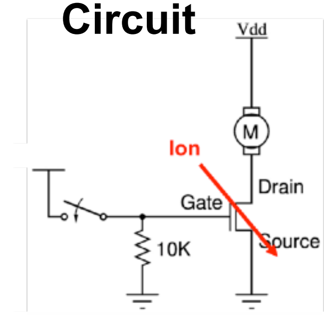


Ion Density ≈ e18's-e20's
L_{ION} ≈ 10's-100's μm

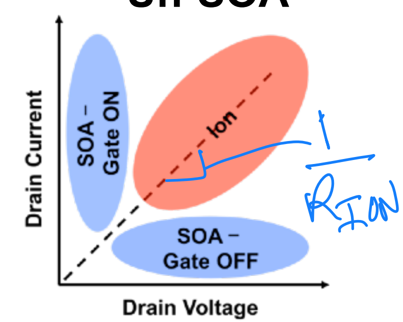
$$R_{ION} = \rho_{ION} * L_{ION}/A_{ION}$$

Power = $I_{ION}^2 * R_{ION}$

Simple Circuit



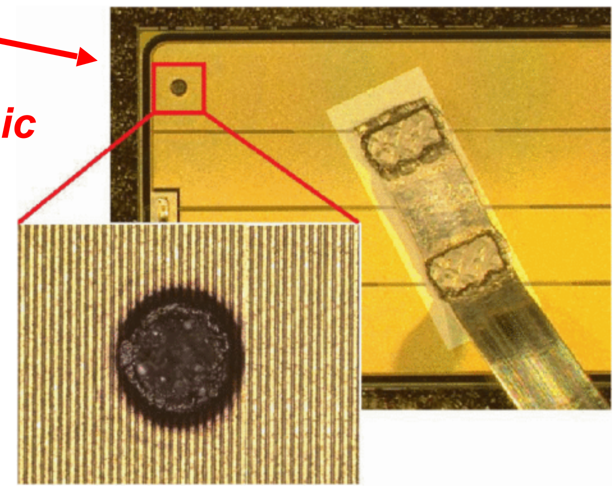
Un-SOA



Radiation Effects in Power Devices

- Total Ionizing Dose (TID) – charge trapped in insulating layers
  - Parametric shifts in device electrical characteristics (i.e. threshold voltage)
- Single Event Effects – ions deposit charge in active device regions
  - Transient current/voltage pulses
  - *Parametric shifts in leakage currents*
  - *Single event burnout (SEB) - catastrophic*
  - *Single event gate rupture (SEGR) - catastrophic*

From: G. Consentino et. al, 2014 IEEE Applied Power Electronics Conference and Exposition



Space applications: Catastrophic failure is not an option!

SEB in Silicon Vertical DMOS vs. SiC

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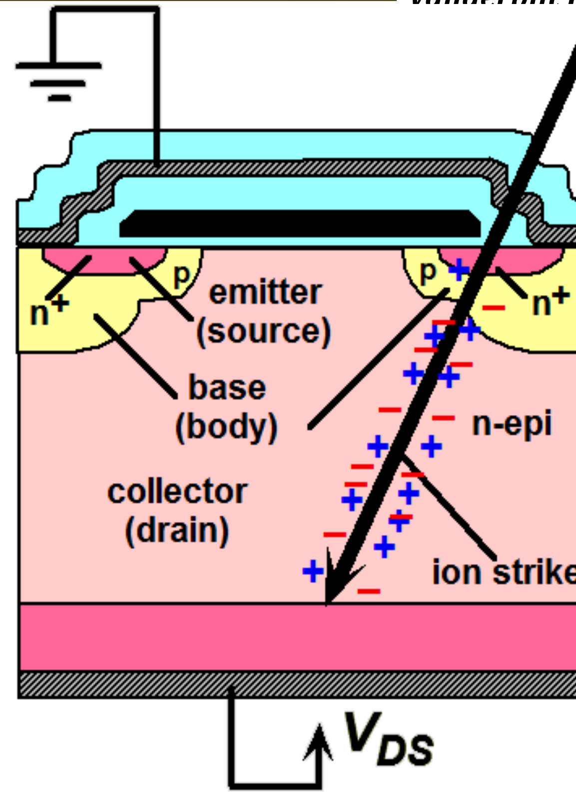
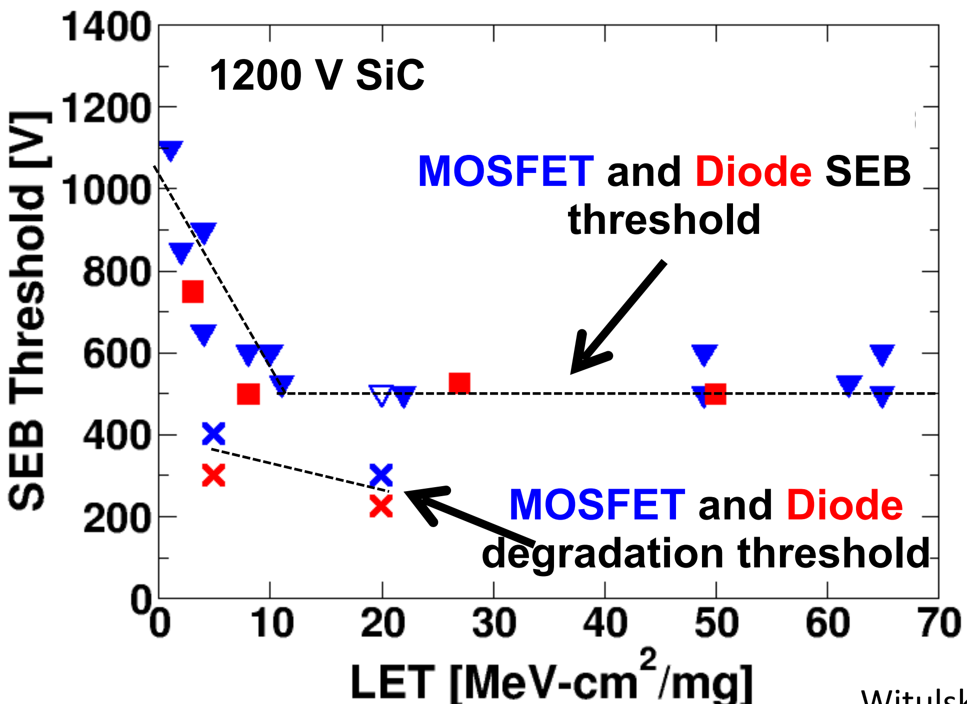
- Si Vertical MOSFET same structure as SiC
- Epi Region approx. 10x thicker than SiC
- Dominant means of SEB is conduction of parasitic bipolar for Si MOSFET, avalanche+thermal damage for Si diode
- In Si, the SEB can be interupted by including a resistor in the drain
    - R prevents permanent damage
    - Makes possible measurement of a cross-section
- Silicon Carbide MOSFET
    - BJT is not the SEB mechanism
    - External R cannot prevent SEB
    - No cross section available without destroying many devices



SEB in 1200 V SiC Vertical DMOS and JBS Schottky



Witulski, et al, IEEE TNS, 2018

Heavy ion-induced SEB and degradation data for SiC MOSFETs and diodes from:

Mizuta 2014
Lauenstein 2015 (LBNL)
Witulski 2018 (RADEF and TAMU)
"Hockey Stick" curve

- Note that SiC and diodes have the same SEB Bias-LET boundary
- Indicates a similar SEB mechanism

Heavy ion data suggests common mechanism(s) responsible for SEB and degradation in SiC

Ion-Induced SEB: TCAD Simulation Analysis

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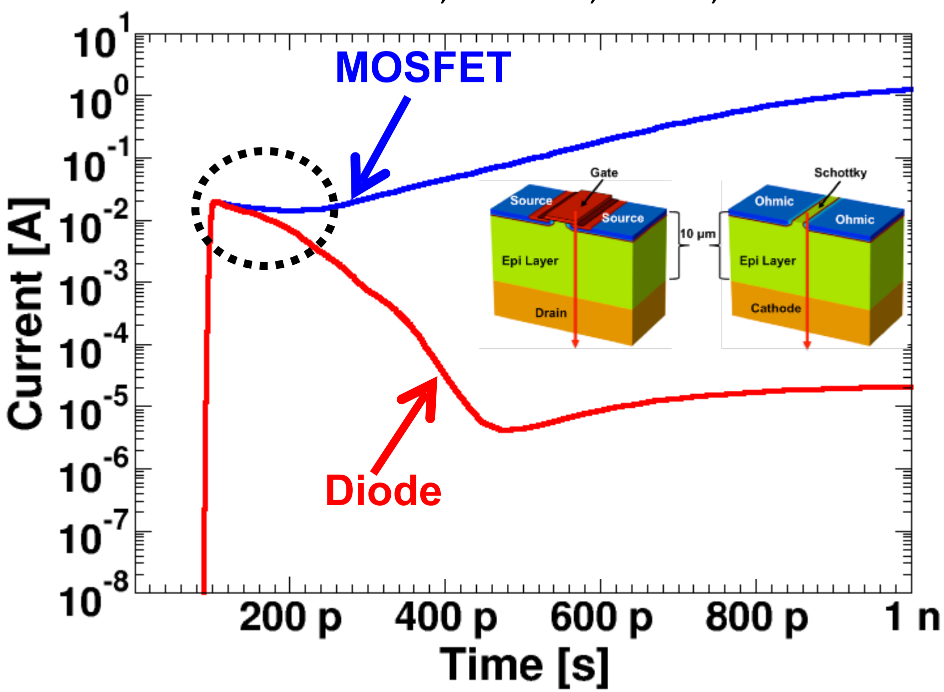
D.R. Ball et al, IEEE TNS, Vol. 67, 2020



3D TCAD simulations show virtually identical behavior for ≈ 100 ps following the ion strike

MOSFET and Diode TCAD Simulations:

- **Peak current identical**
- **Current transients differ significantly 1ns following the strike**
  - **Laser data shows parasitic BJT**
  - **Heavy ion data shows same SEB threshold**

SEB occurs faster than device can respond…

Energy pulse?

Ion-Induced Current Densities and Re-Distribution of Electric Field

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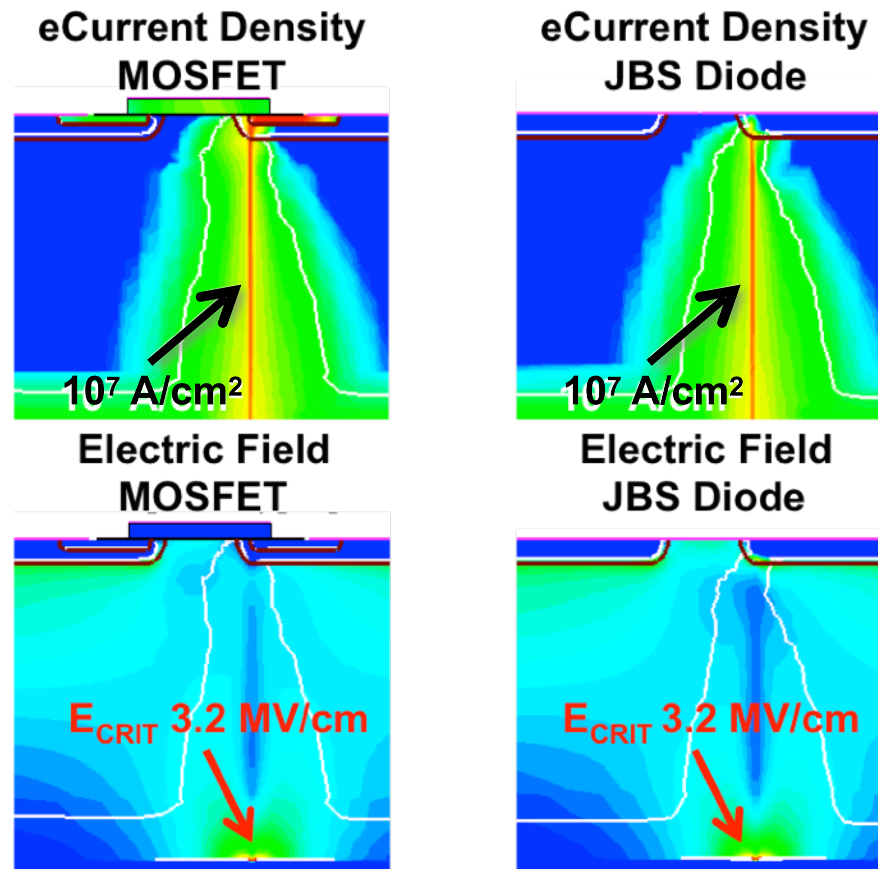
3D TCAD heavy ion simulation of 1200 V SiC

- LET = 10 MeV-cm²/mg @ 500 V
- Short circuit from high carrier density
- Re-distribution of electric field
- Maximum field goes from 2 to 3.2 MV/cm



Power density is extremely high along strike path, high current density and high electric field

$$Pd = J \cdot E$$

D.R. Ball et al, IEEE TNS, Vol. 67, 2020

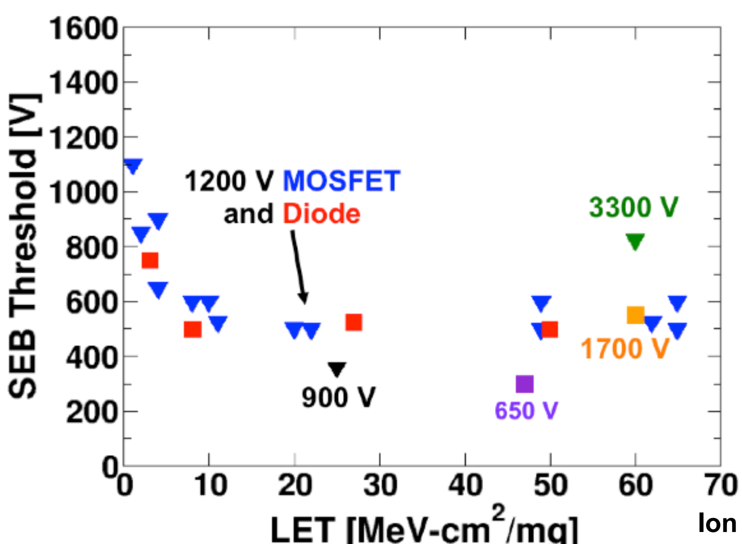
J. McPherson et al, IEEE TNS Vol. 68, 2021

Impact of Voltage Rating on SEB Threshold

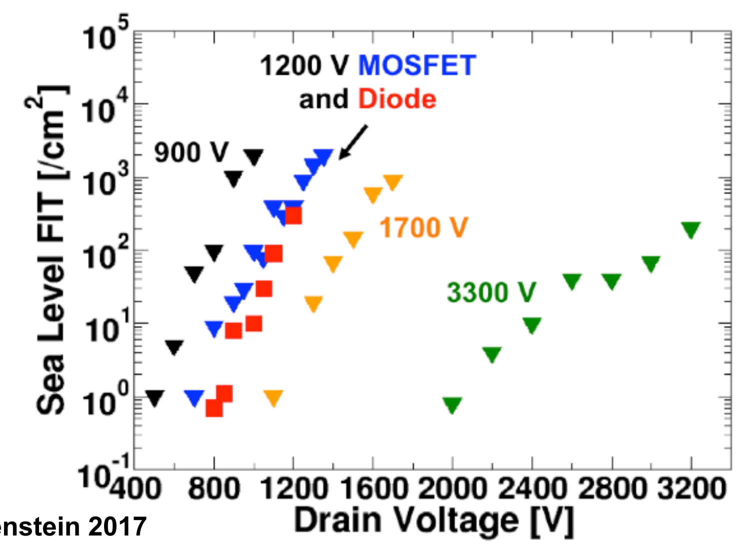
- Ion-induced SEB threshold increases with increasing voltage rating
- Terrestrial neutron-induced SEB FIT rate decreases with increasing voltage rating

Data show increased SEB tolerance for thicker, more lightly-doped epitaxial regions

Ion-Induced SEB



Terrestrial Neutron-Induced SEB



Ion Data from Lauenstein 2017
Neutron Data from Lichtenwalner 2018

Single-Event Leakage Current (SELC)

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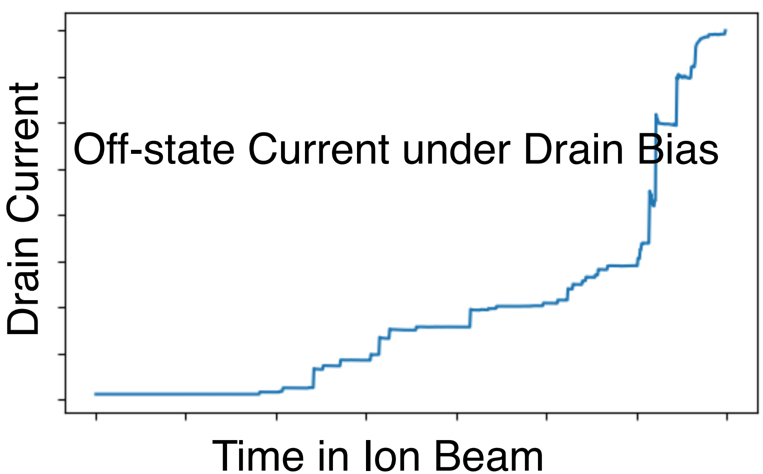
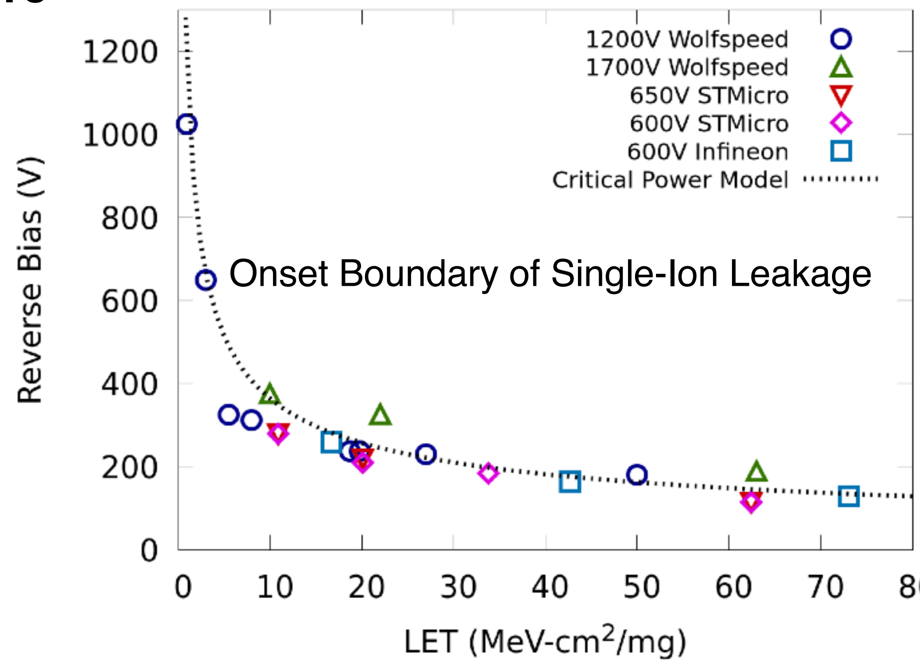
- SiC devices show step changes in off-state current for single ion strikes
- SiC devices show onset of the effect at reverse biases ~20% of rated breakdown voltage.
- Leakage independent of manufacturer or breakdown voltage (epi depth)
- Large enough for parametric failure





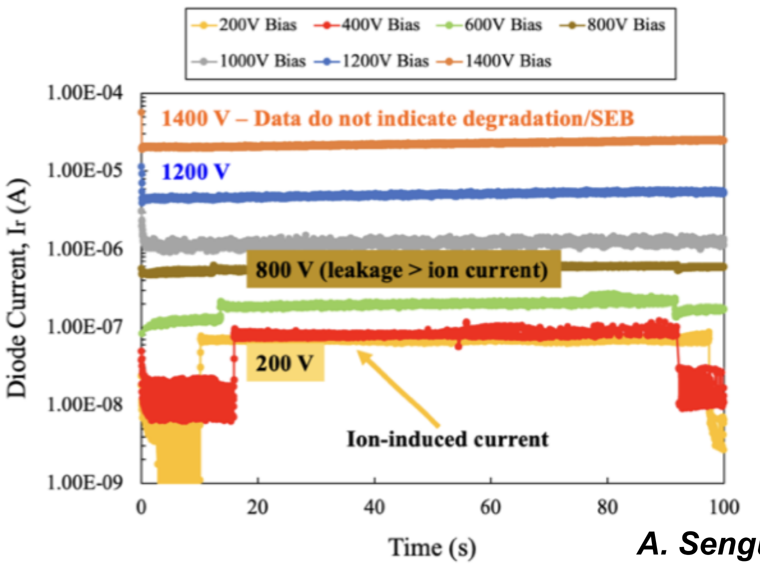
R.A. Johnson, et al, IEEE TNS, Jan. 2020

1200 V SiC Heavy Ion Irradiation With Short Range Ions

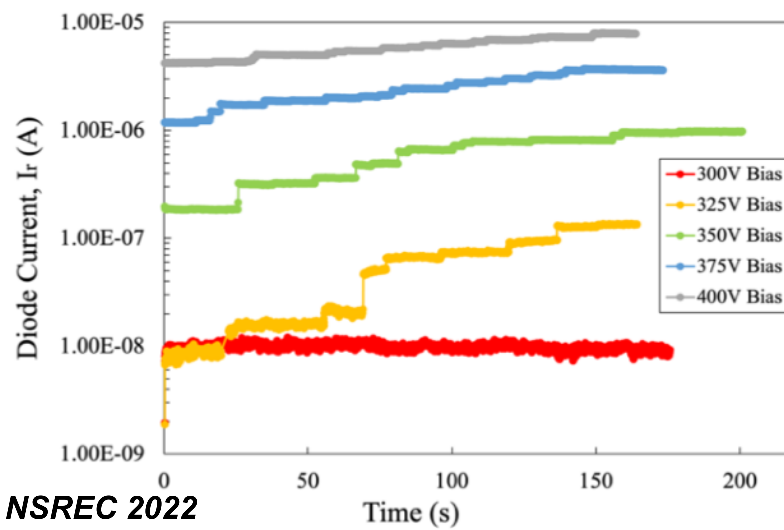
Vanderbilt Engineering

- **Heavy ion radiation testing of 1200 V SiC diode with 10 um thick epi layer**
  - **Ion LET=7 MeV-cm²/mg with range of 6 um performed at VU Pelletron**
  - ***Device shows no ion-induced leakage, nor catastrophic SEB***
  - ***Key point: the ion must traverse the entire epi to produce SEB or SELC***

Pelletron Irradiation -short range ions



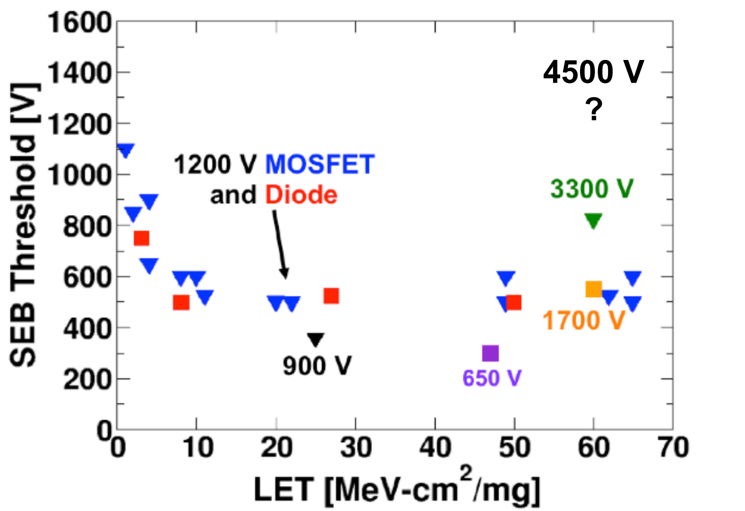
TAMU Irradiation - long range ions

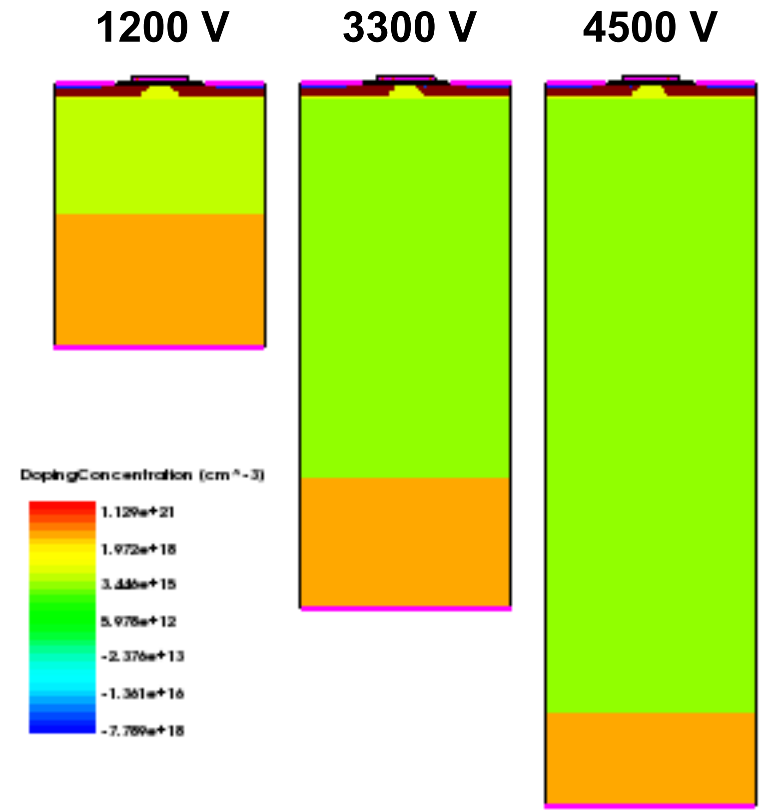


A. Sengupta, et al, NSREC 2022

Goal: Design Radiation-Tolerant Diode/MOSFET

- VU and GE design device intended to survive catastrophic SEB
- 3D TCAD heavy ion sensitivity study – VU
    - Increase epi thickness
    - Decrease epi doping
    - Effective increase in voltage rating
    - Note: 3300 V device shows SEB @ 850V

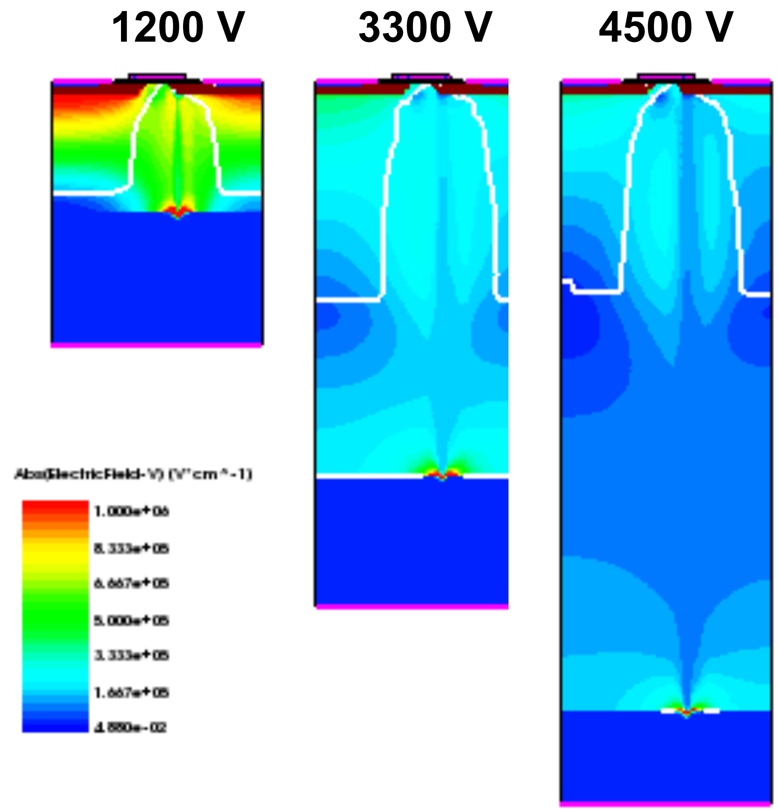




Ion-Induced Electric Field Redistibution

3D TCAD heavy ion simulation of SiC MOSFET variants

- LET = 60 MeV-cm^2/mg @ 500 V
- 3300 V and 4500 V device show significantly lower electric fields compared to the 1200 V device

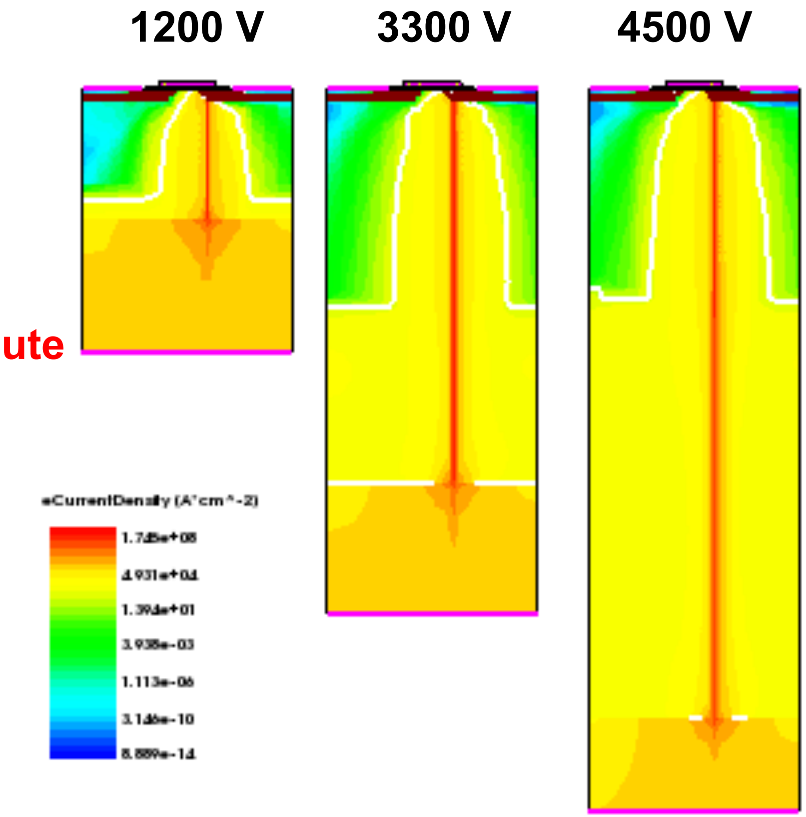


Ion-Induced Electron Current Density

Vanderbilt Engineering

3D TCAD heavy ion simulation of SiC MOSFET variants

- **LET = 60 MeV-cm²/mg @ 500 V**
- **3300 V and 4500 V device show significantly lower electric fields compared to the 1200 V device**
- **Current densities similar for all variants, however, significantly more series resistance for the wider epi regions to distribute ion-induced current**



Ion-Induced Power Density

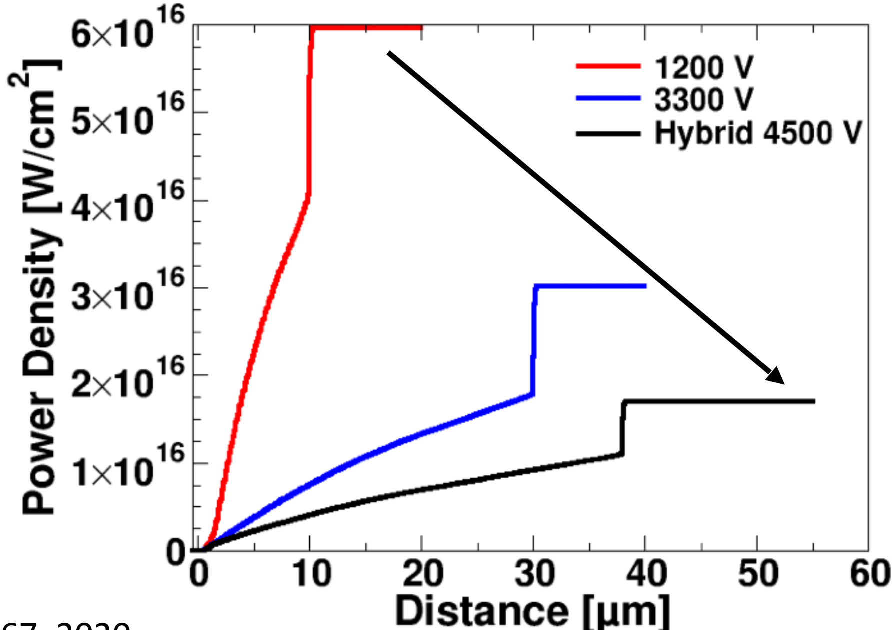
3D TCAD heavy ion simulation of SiC MOSFET variants

- **LET = 60 MeV-cm²/mg @ 500 V**
- **Integrated power density along ion track significantly reduced as breakdown voltage increases**

Power dissipation

J•E

70% reduction in ion-induced power along the ion track



D.R. Ball et al, IEEE TNS, Vol. 67, 2020

Technical Approach Plan for Baseline 3.3 kV Devices

Deliver Standard Devices

#	Device Type	Project Scope	
1	Standard planar MOSFET (1.7kV OR 1.2kV)	Test & establish baseline	Radhard design and fabrication
2	Standard Schottky diode 3.3kV	Test & establish baseline	Radhard design and fabrication
3	Charge-balanced diode 3kV	Test & establish baseline	
4	Charge-balanced MOSFET 3kV	Test & establish baseline	

Design & Fabricate RadHard Devices

TECHNICAL INSIGHTS

- Onset of SEB is almost identical for planar MOSFETs and diodes
- 3.3kV device shows a dramatic reduction in total power during the ion strike compared to the 1200 V baseline
- Gate related device failures are believed to be caused by large electric field in the gate oxide

DESIGN, FAB, TEST, PACKAGE

- Vary epi thickness and doping to lower peak electric fields
- Wafer split for a "hybrid design" that optimizes both SEE and electrical performance -
- Parallel lots: diodes (~4 months) and MOSFETs (~6months)
- Post-fab tests: Vth, $R_{DS(on)}$, Vdss
- Parylene coating of open-can packages

TECHNICAL CHALLENGES

- Material quality issues including defects, impurities → test bare wafers
- Device design that ensure both electrical performance and rad-tolerance

Apply insights on radiation impact on SiC to implement SEE tolerant power devices

MOSFET and JBS Design

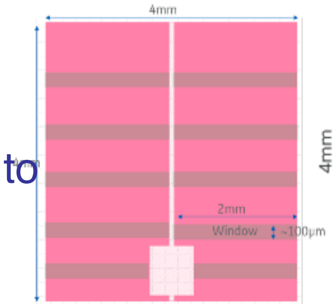
- **Design Strategy**:
  - Design ~4.5 kV device structure. Operate them at 600 V (MOSFETs) or 1200 V (Schottkys) for extra SEE tolerance due to voltage derating
  - “Hybrid MOSFET/JBS” – 4.5 kV devices require optimization of drift layer and doping compared to 1.2 kV devices

- **Metal Window Splits**:
  - Baseline (No window), 25% opening & 50% opening
  - Designs to be distributed uniformly across the wafer
- **Termination Design***: 4500 V

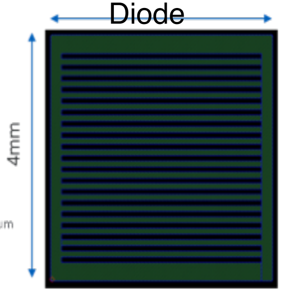
- **Top JBS Design**: Identify an optimized 4.5kV JBS diode architecture for the lowest surface electric field and lowest Ron.
- **Epi Splits**:
  - Low doping/ Thick epi & High doping / Thick epi

Windows in the active area

MOSFET



JBS Diode



Termination design

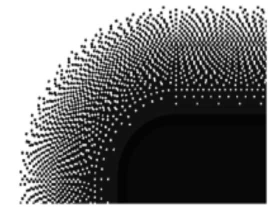
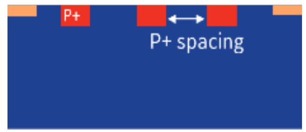


Figure 6. Graded Junction Termination Extension (G-JTE) used to fabricate HV SiC MOSFETs

Top JBS



Tradeoff between Ron and surface electric field

*Losee P. A., et al., *SiC MOSFET Design Considerations for Reliable High Voltage*

Achieve SEE resistance by voltage derating of 4.5 kV devices

Single Event Leakage Degradation a function of Bipolar Degradation?

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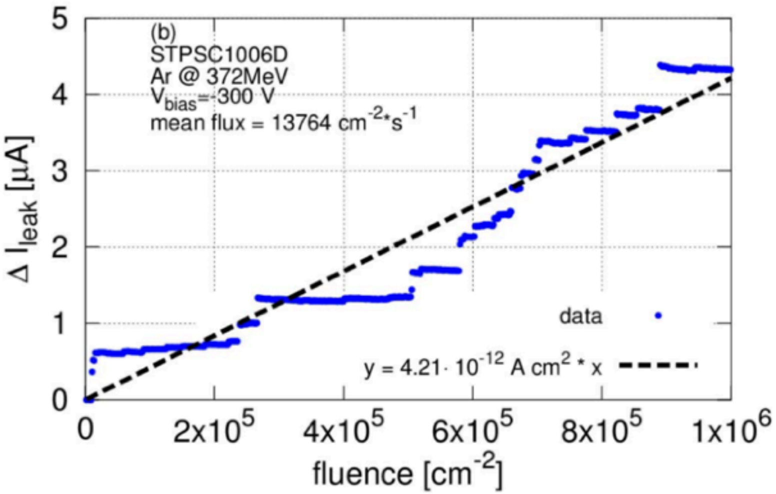
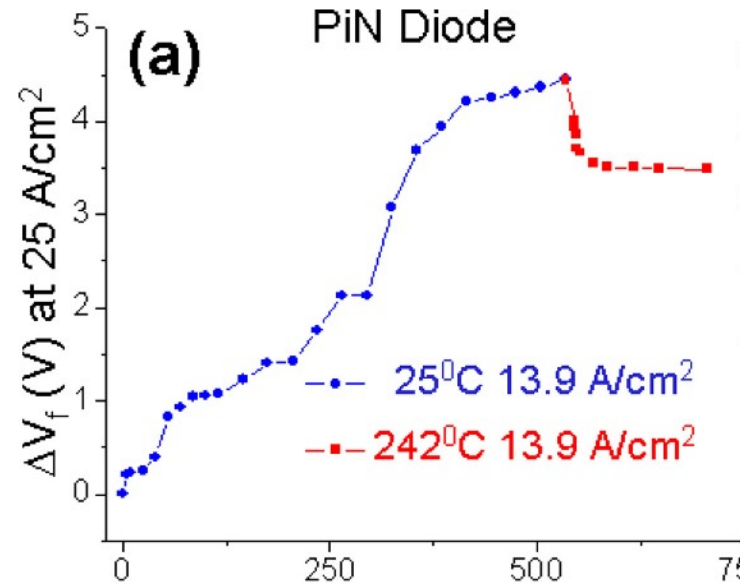
Ion-Induced Leakage "Steps" in Reverse-biased JBS Diode



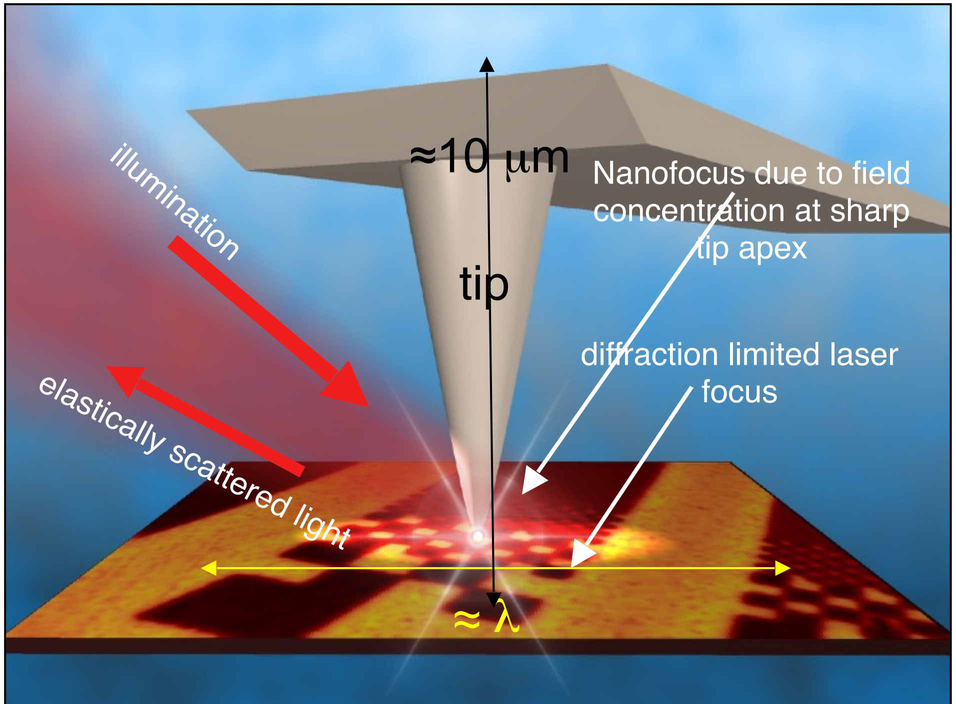
Forward-bias induced degradation



- Ion-induced leakage degradation function of LET and bias
- Data shows discrete "steps" → similar step-wise degradation observed in pin diodes
  resulting from stacking fault formation and expansion
- Each ion-strike results in a localized "plasma" wire…high current density short time

VU Nanophotonic Materials and Devices Lab

Vanderbilt Engineering



- **Professor Joshua Caldwell**
- **Nano-Optic Probes**
  - Scatter long-wavelength light off of metal AFM tip
  - Use evanescent fields at tip to locally probe optical properties of materials by electroluminescence
- **s-SNOM →** spatially map the optical amplitude and phase at one frequency w/ <20-nm spatial resolution!
- **Nano-FTIR →** measure FTIR spectra w/ same spatial resolution
- **Pump-probe nano-FTIR →** measure FTIR spectra w/ 200 fs temporal resolution following UV (390 nm) or NIR (1560 nm) 130-fs pulse

Silicon Carbide Reliability – Material Defects

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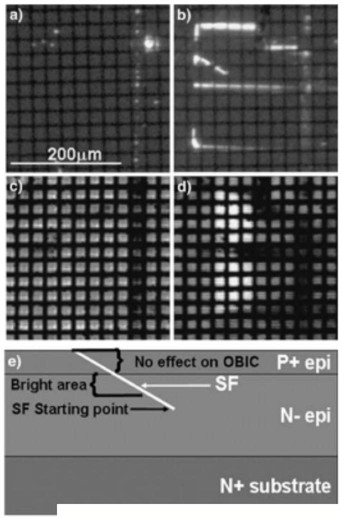
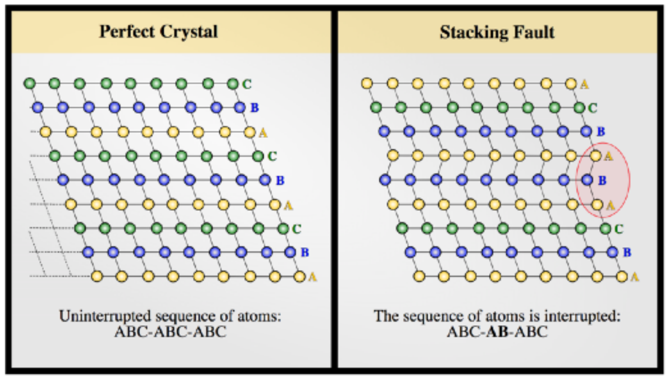
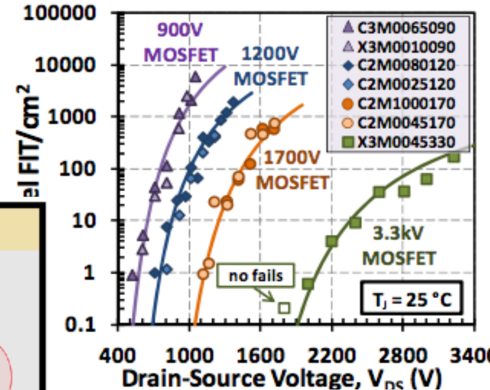
Material

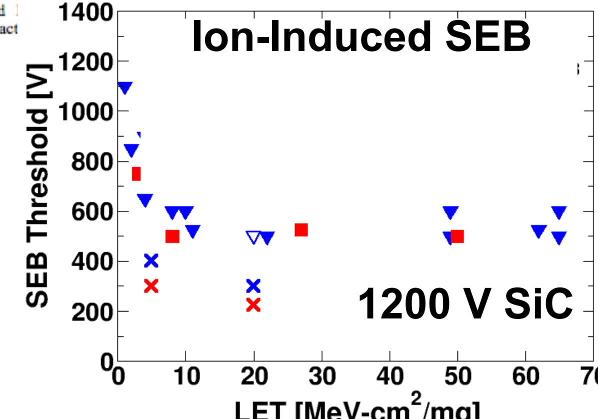


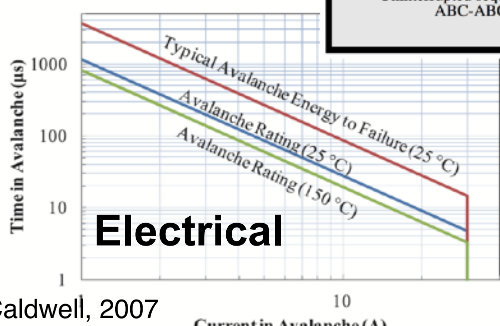
Stacking Fault



Terrestrial Neutron-Induced SEB





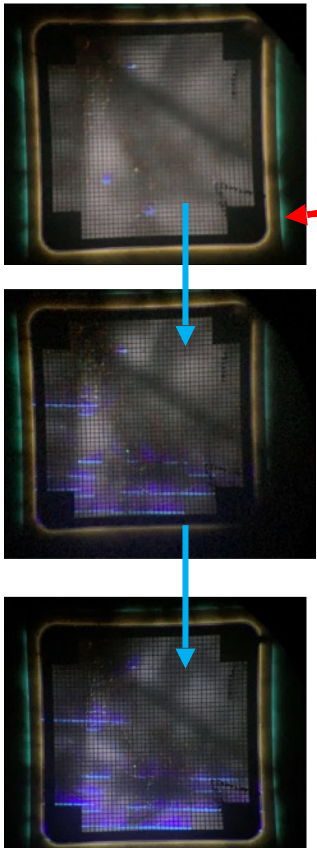


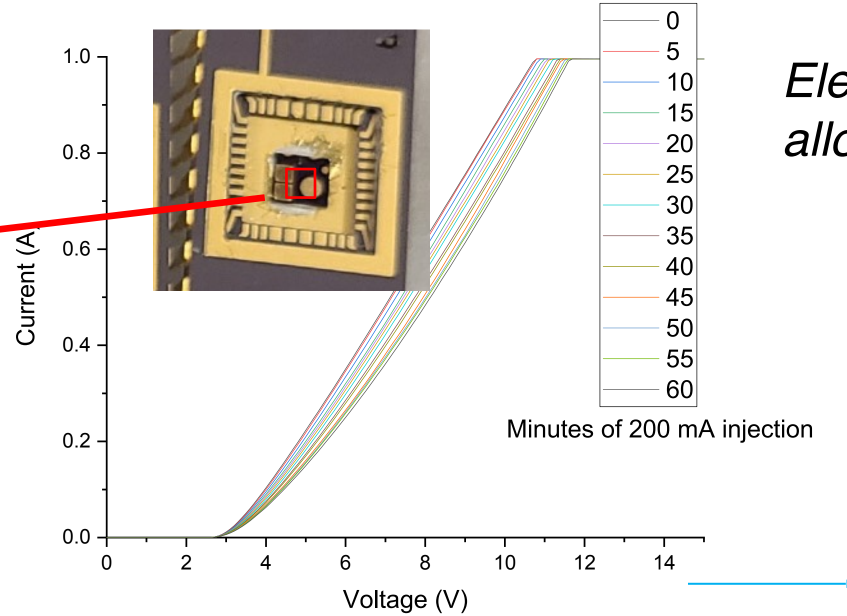
"if we can design a more robust device for neutron-induced SEB we gain reliability" – Dan. L, Wolfspeed

J. Caldwell, 2007
V. Pala, 2015

https://msestudent.com/close-packed-crystals-and-stacking-order/

Device Degradation - Forward Voltage Drift





Electroluminescence imaging allows identification of defects

- **Forward bias operation of SiC ambipolar (e.g. pin diodes) devices results in nucleation and expansion of stacking faults**
- **Stacking faults act as a quantum well causing a continuous increase in the turn-on voltage**
- **Similarities between stacking fault induced degradation with SEB implies stacking faults may be induced following irradiation**

Presentation from ICSCRM 2022 on 600 V GaN

Vanderbilt Engineering

GaN Devices for the 600V Range

O. Häberlen, G. Deboy
Infineon Technologies Austria AG, Siemensstrasse 2, 9524 Villach, Austria
E-mail: oliver.haeberlen@infineon.com

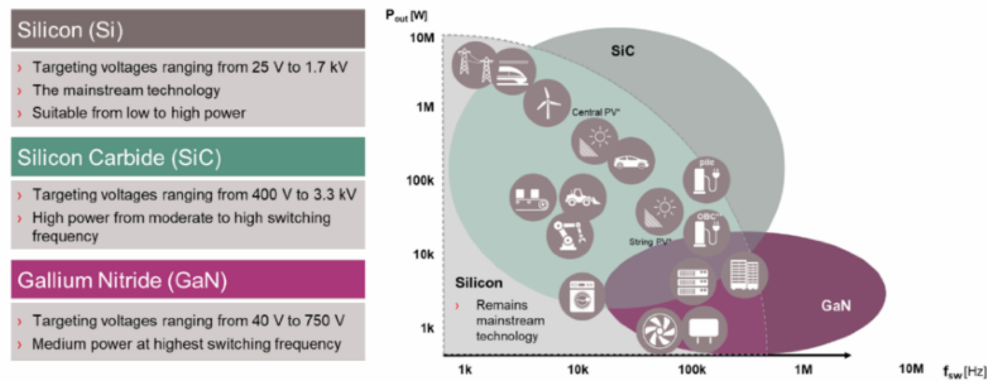


Fig. 1. Technology positioning of Si, SiC and GaN power devices.

DEVICE	$V_{(BR)DSS}$ [V]	$R_{DS(on)}$*Q_{rr} [mΩ * μC]	$R_{DS(on)}$*E_{oss} [mΩ * μJ]	$R_{DS(on)}$*Q_g [mΩ * nC]	$R_{DS(on)}$*Q_{oss} [mΩ * μC]
CoolMOS™ 7	600	100%	100%	100%	100%
CoolMOS™ 7 Fast Diode	600	10%	104%	108%	104%
CoolGaN™ Gen 1	600	0%	84%	6%	13%
CoolSiC™ Gen 1	650	2%	133%	41%	21%

Table I. Relative performance comparison of 600V/650V class silicon, SiC and GaN devices.

ICSCRM 2022 600 V GaN Continued

GaN Devices for the 600V Range

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E-mail: oliver.haeberlen@infineon.com

True Integrated Bidirectional Switch in GaN

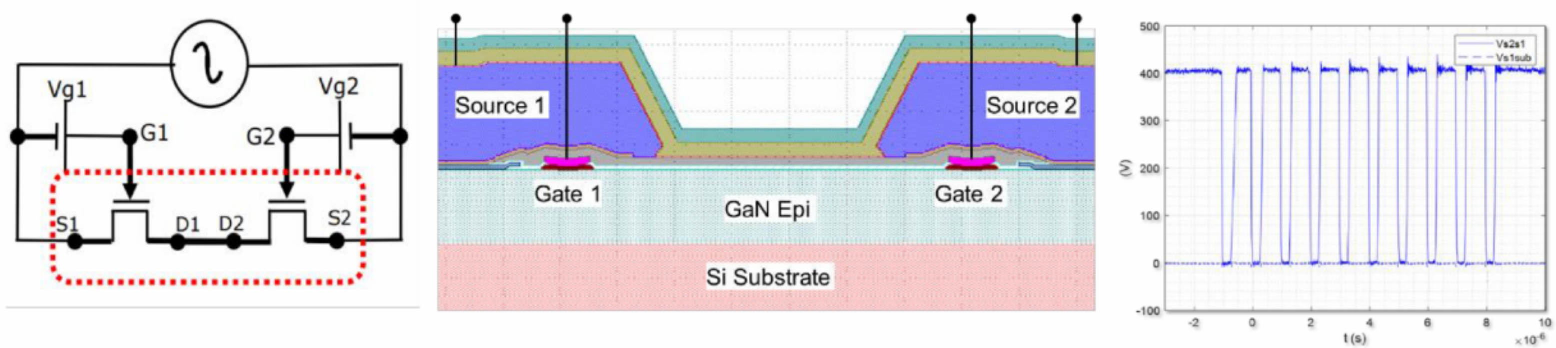


Fig. 3. Monolithic drain-to-drain connected bidirectional GaN switch sharing a common drift region [3] (left: schematic, middle: device cross section, right: 400V / 1 MHz clean hard switching wave form).

GaN Commercial Device Comparison - Single Event Effects

- "Static SEE results have shown that high-voltage GaN is sensitive to high-LET heavy ions contrary to low-voltage components that are much more robust, even if GaN Systems (commercial manufacturer) components still need additional studies (influence of beam angle, reliability evaluation of part after irradiation) to safely define its SOA."
  - J.B. Sauveplane, et al., "Heavy-Ion Testing Method and Results of Normally OFF GaN-Based High-Electron-Mobility Transistor," in IEEE Trans. on Nuc. Sci., vol. 68, no. 10, pp. 2488-2495, Oct. 2021.

TABLE II
SEE RESULTS SUMMARY

Part number	V_{DS} max (V)	Manufacturer	Ion	V Pass (V)	V Fail (V)
EPC2001C	100	EPC	Xe	100	-
EPC2012C	200	EPC	Xe	200	-
GS61008P	100	GaN System	Xe	90	-
PGA26E19I	600	Panasonic	Xe	300	350
PGA26E19I	600	Panasonic	Rh	350	375
IGOT40R07	400	Infineon	Xe	350	400
IGOT40R07	400	Infineon	Rh	375	375

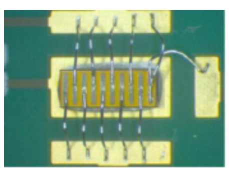
Wide variety of response to heavy ions observed for GaN

Immediate catastrophic SEB in some instances

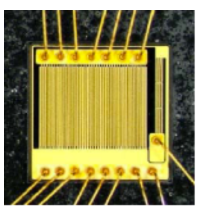
Gradual failure also possible at lower VDS

SEBV~RatedV for 100, 200, 400 V Rated Devices

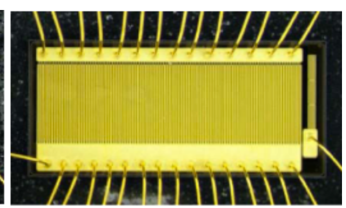
SEBV<RatedV for 600 V Devices



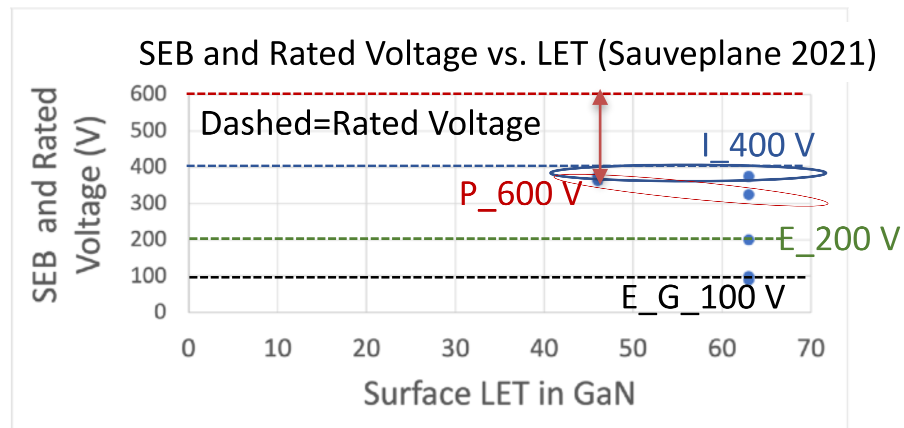
EPC Bare Die 100-200 V



Panasonic 600 V



Infineon 400 V



Points are average of Pass and Fail Values

Heavy Ion Leakage Effects in GaN

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L. Wang, Y. Jia, Y. Zhao, L. Wang and Z. Deng, "Experimental study of the Single Event Effects in E-mode GaN HEMT with Heavy Ion Irradiation," 2021 4th International Conference on Radiation Effects of Electronic Devices (ICREED), 2021, pp. 1-5

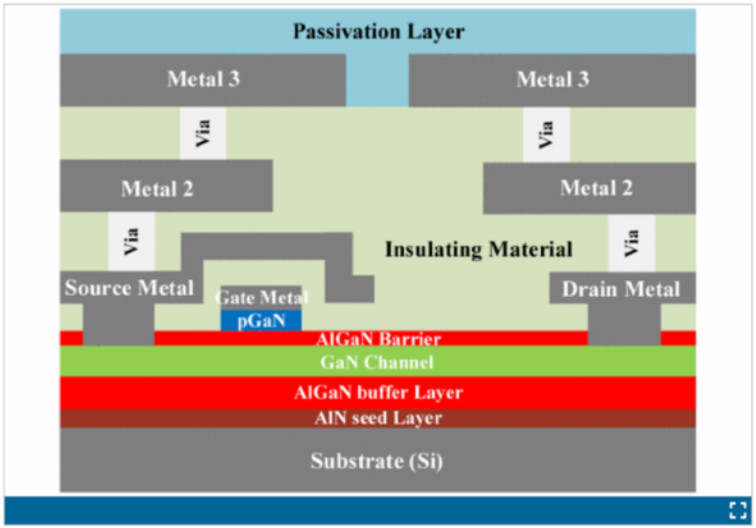

Fig. 1
Schematic diagram of the enhancement-mode GaN HEMT made by Efficient Power Conversion Corporation

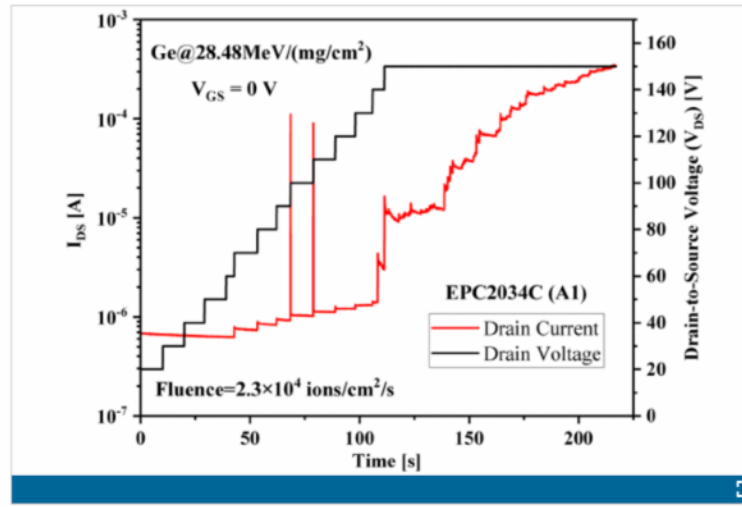

Fig. 5
Drain leakage current measured after irradiations with ^{74}Ge at 212MeV.

Degradation of Device Parameters with Heavy Ions

L. Wang, Y. Jia, Y. Zhao, L. Wang and Z. Deng, "Experimental study of the Single Event Effects in E-mode GaN HEMT with Heavy Ion Irradiation," 2021 4th International Conference on Radiation Effects of Electronic Devices (ICREED), 2021, pp. 1-5

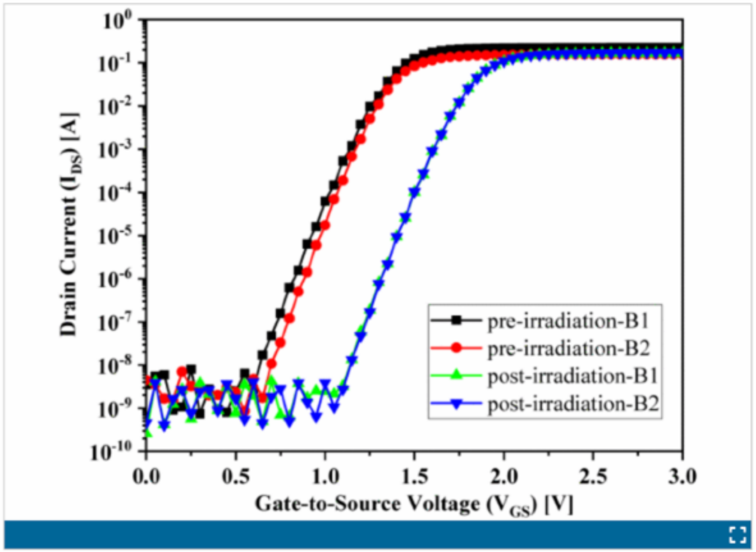

Fig. 12
Transfer characteristic curves for devices before and after [32] Si ion radiation.

Shift in Threshold Voltage

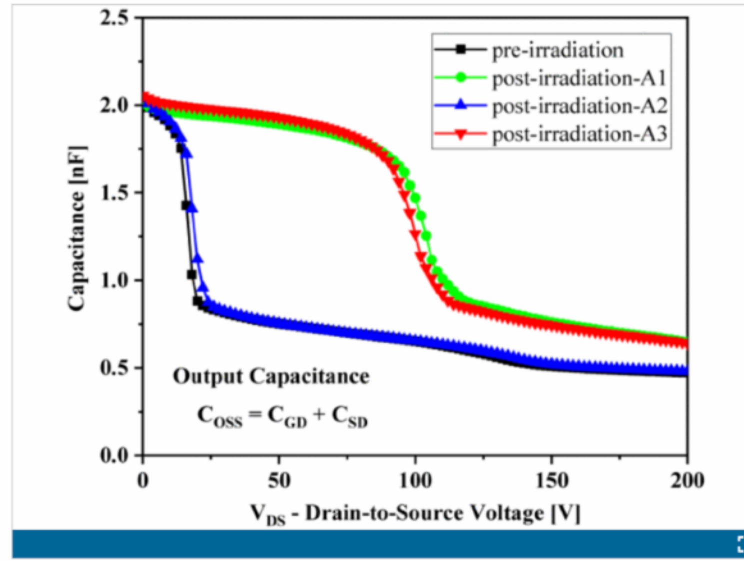

Fig. 14
Output capacitance curves for devices before and after [74] Ge ion radiation.

Change in Output Capacitance

Notice Device Variability

Summary

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- Silicon Carbide devices are a key technology for human exploration of the moon
- Lunar thermal and radiation environments much more “extreme” than earth
- Heavy ions in space induce both SEB and SELS in SiC power devices
  - Both appear to be due to ion path through epi connecting source and drain
  - Extremely high current densities and peak electric field in ion path
  - Peak local power density appears to cause the damage in the device
  - Boundaries appear dependent on epi doping and depth
- Vanderbilt and GE creating a “hybrid device” that has good electrical performance but also survives heavy ion strikes with no latent damage
  - SiC diodes and MOSFETs in fab, expected delivery early 2023
  - Accelerator tests on new devices expected mid-2023
- SEB and SELC are present in both SiC and GaN but have different mechanisms