LAr HL-LHC Upgrade: The COLUTA ADC

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On behalf of the COLUTA Team

CERN EP-ESE Seminar, https://indico.cern.ch/event/1065139/
October 11, 2022

Outline

- LAr HL-LHC Upgrade
  - Context
  - Requirements
  - Evolution of The Readout Architecture
- COLUTA(V4) ADC
  - History of the COLUTA ASIC Development & Team Profile
  - Target Specifications & Channel Architecture
  - MDAC & SAR Implementation
  - Chip Architecture & Implementation
  - Foreground Calibration, Radiation Hardening By Design
  - Third-Party IP, Verification Strategy
- Measurements & Forward Plans
  - Analog & Physics Measurements
  - Radiation SEE/TID Measurements
  - Forward Plans
  - BGA Packaging & Mass Validation

Upgrade: Context

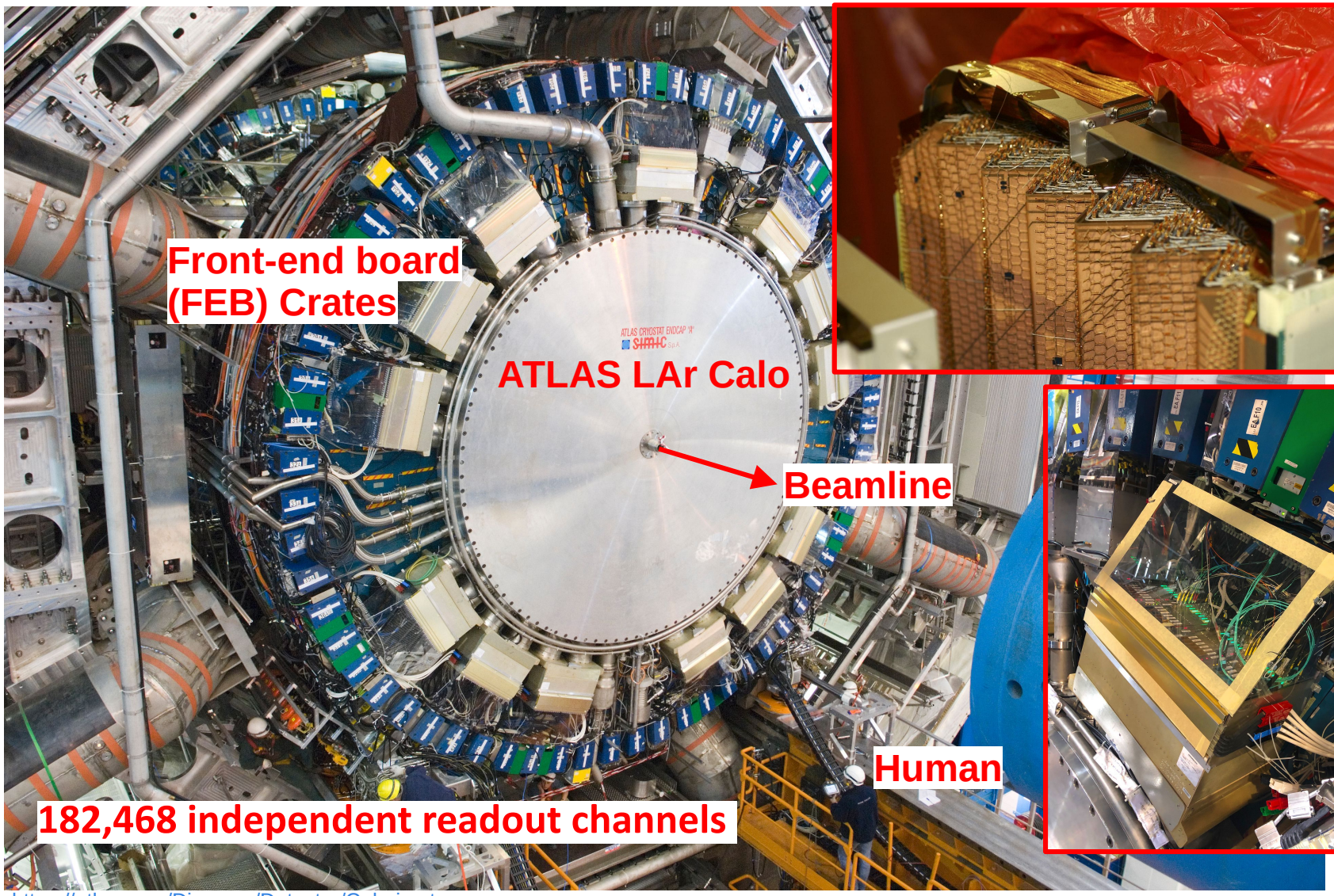


Image: https://atlas.cern/Discover/Detector/Calorimeter

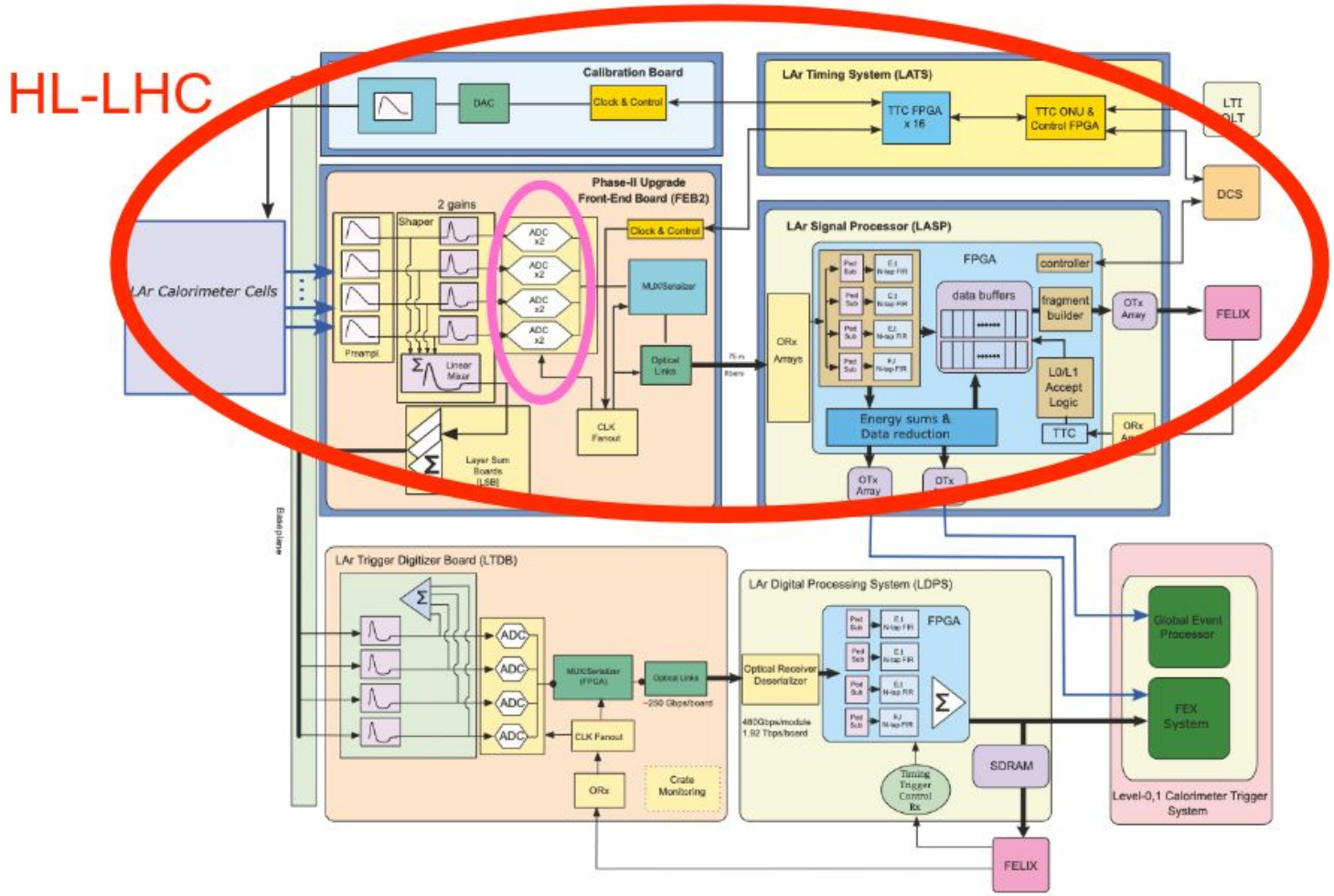
Upgrade: Motivation

- Higher luminosity → more events → requires faster trigger
  - HL-LHC: up to 200 *pp* collisions per bunch crossing
  - Current readout (circa 2008): ≤100 kHz L1 trigger rate, 2.5 μS latency
  - Analog data is stored in a buffer *on-detector* until a trigger is asserted
  - HL-LHC requirement: ≤1 MHz L1 trigger rate, 10 μS latency
  - **Original readout architecture cannot handle the full HL-LHC trigger requirement**
  - Concerns of aging and HL-LHC radiation tolerance

A new LAr readout architecture is needed to meet the HL-LHC requirements.

- "ATLAS Liquid Argon Calorimeter Phase-II Upgrade: Technical Design Report," Sep. 2017. [Online]. Available: https://cds.cern.ch/record/2285582
- "Safety Factor and Testing Procedure Recommendations of the Radiation Effects Task Force," [Online]. Available: https://cds.cern.ch/record/2718449

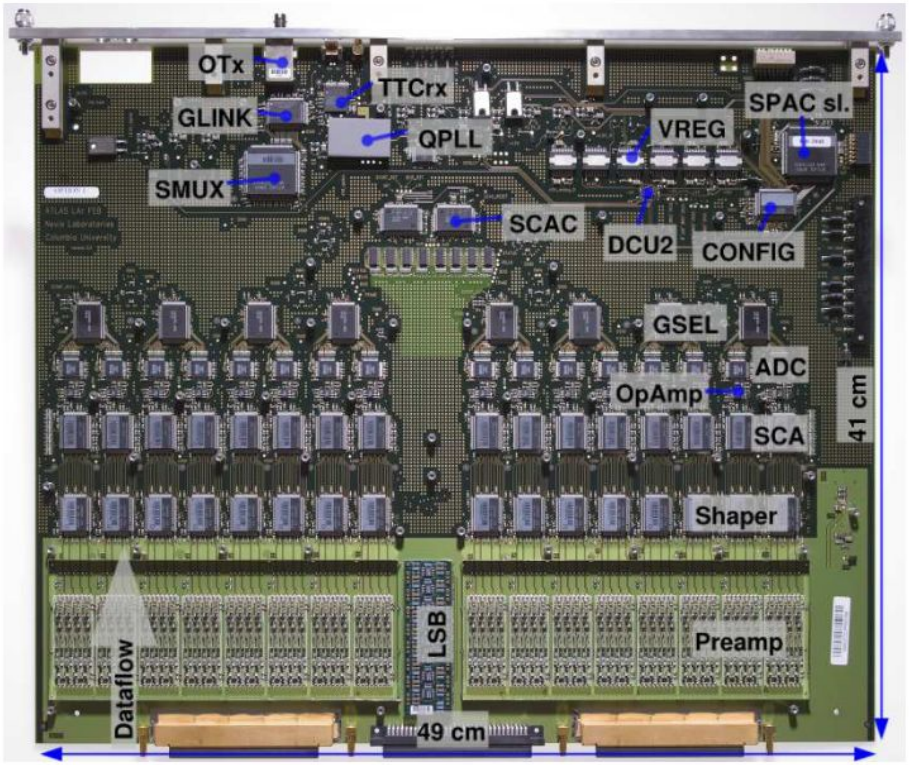
Upgrade: Motivation



The new architecture will digitize and read out *all* detector data with full precision at the full rate of 40 MSPS. No buffering will be done on-detector.

Original FEB (2008)

- Each FEB reads 128 LAr channels
- Features 11 unique custom ASICS
- ADC, opamp, and others are COTS
- Requires 7 different voltage rails



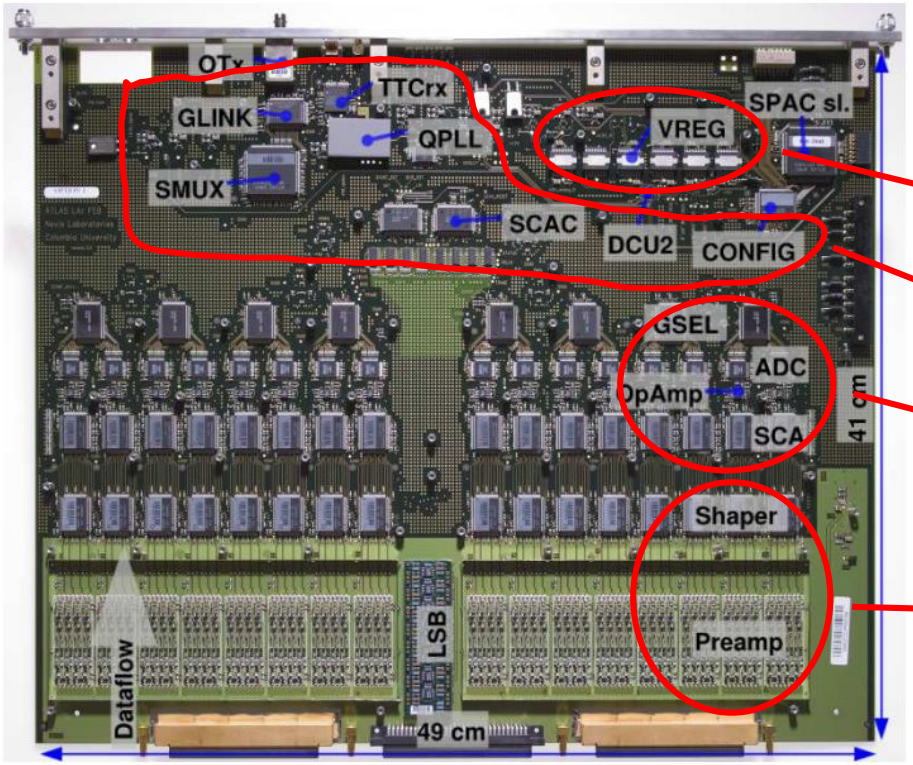
We can integrate all present functionality/capabilities *and* improve on analog performance into three custom ASIC's

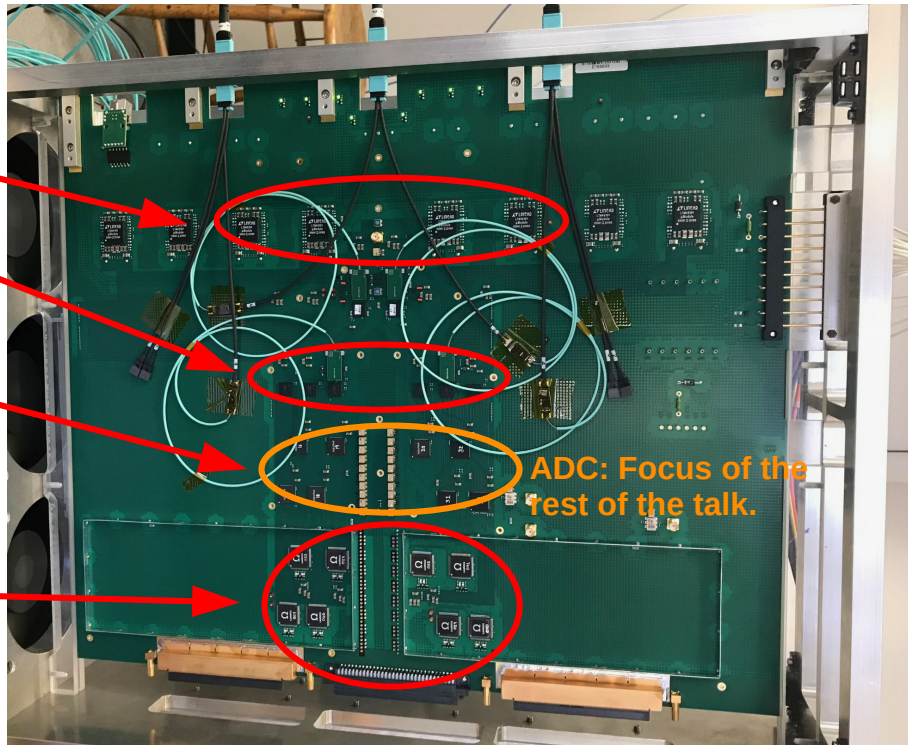
N. J. Buchanan et al., "Design and implementation of the Front End Board for the readout of the ATLAS liquid argon calorimeters," J. of Inst., vol. 3, Art. no. 03, Mar. 2008, doi: 10.1088/1748-0221/3/03/p03004.

Upgrade: FEB2 Readout (~2025)

- Each FEB reads 128 LAr channels
- Features 11 unique custom ASICS
- ADC, opamp, and others are COTS
- Requires 7 different voltage rails

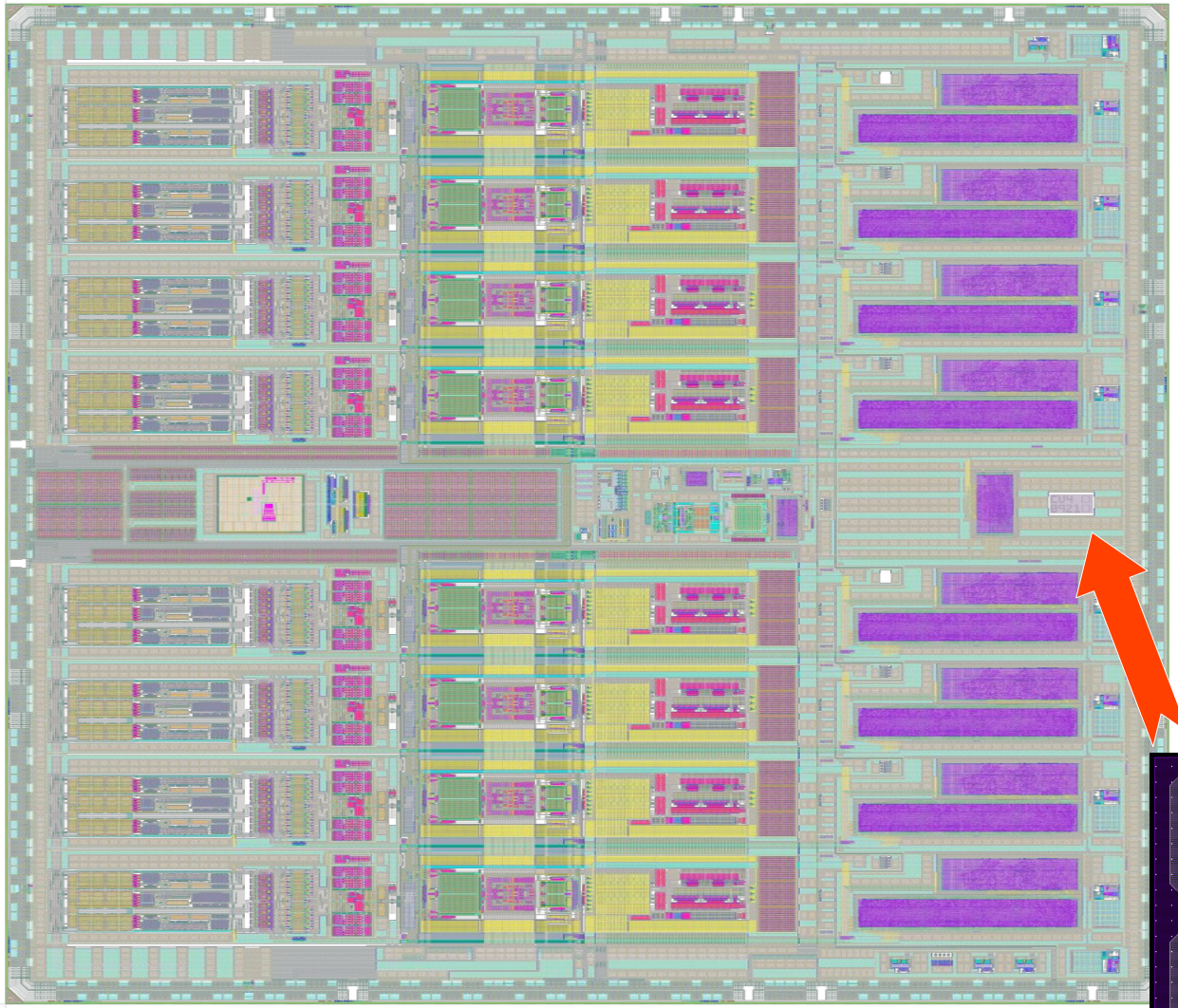
- ¼ scale prototype of 128-ch
- Features 4 unique custom ASICS
- DC-DC is COTS
- Requires 3 different voltage rails





N. J. Buchanan et al., "Design and implementation of the Front End Board for the readout of the ATLAS liquid argon calorimeters," J. of Inst., vol. 3, Art. no. 03, Mar. 2008, doi: 10.1088/1748-0221/3/03/p03004.

COLUTAV4



8-ch, 40 MSPS,
11.5-ENOB, 15b DR ADC

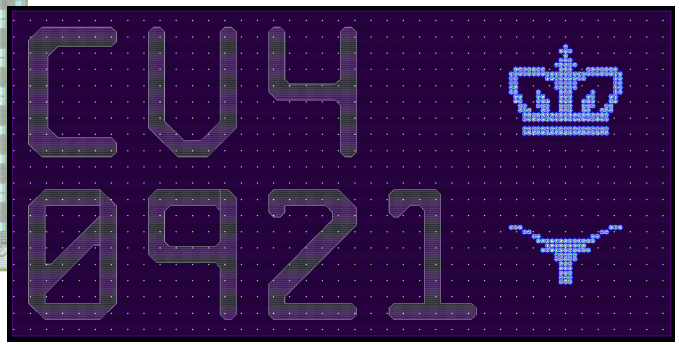
Submitted Sept 1, 2021

TSMC 65nm LP 1.2V

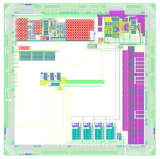
5.584 x 5.456 mm^2

100 I/O & 366 bondpads

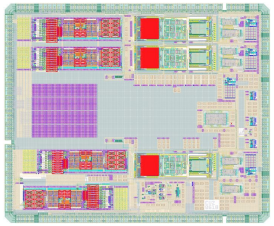
4.3 million transistors



Historical Background

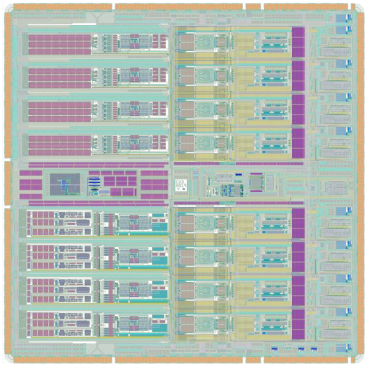


COLUTAV1
Summer 2017
1-ch DRE
1-ch SAR
4 mm^2

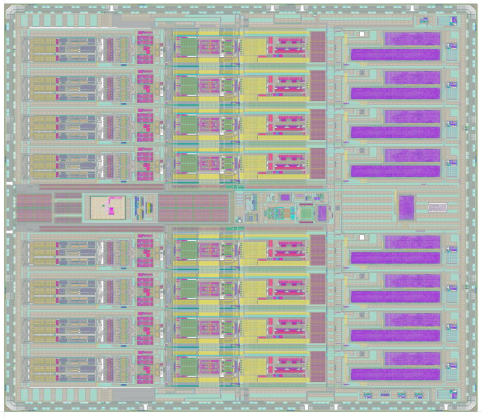


COLUTAV2
Summer 2018
2-ch DRE+SAR

7.39 mm^2



COLUTAV3
Summer 2019
4-ch DRE+SAR
4-ch MDAC+SAR
24.79 mm^2



COLUTAV4
Summer 2021
8-ch MDAC+SAR

30.47 mm^2

CV3 PDR passed with recommendations; V4 tapeout permitted

Oct. 7, 2022: Final Design Review

COLUTA Design Team Personnel

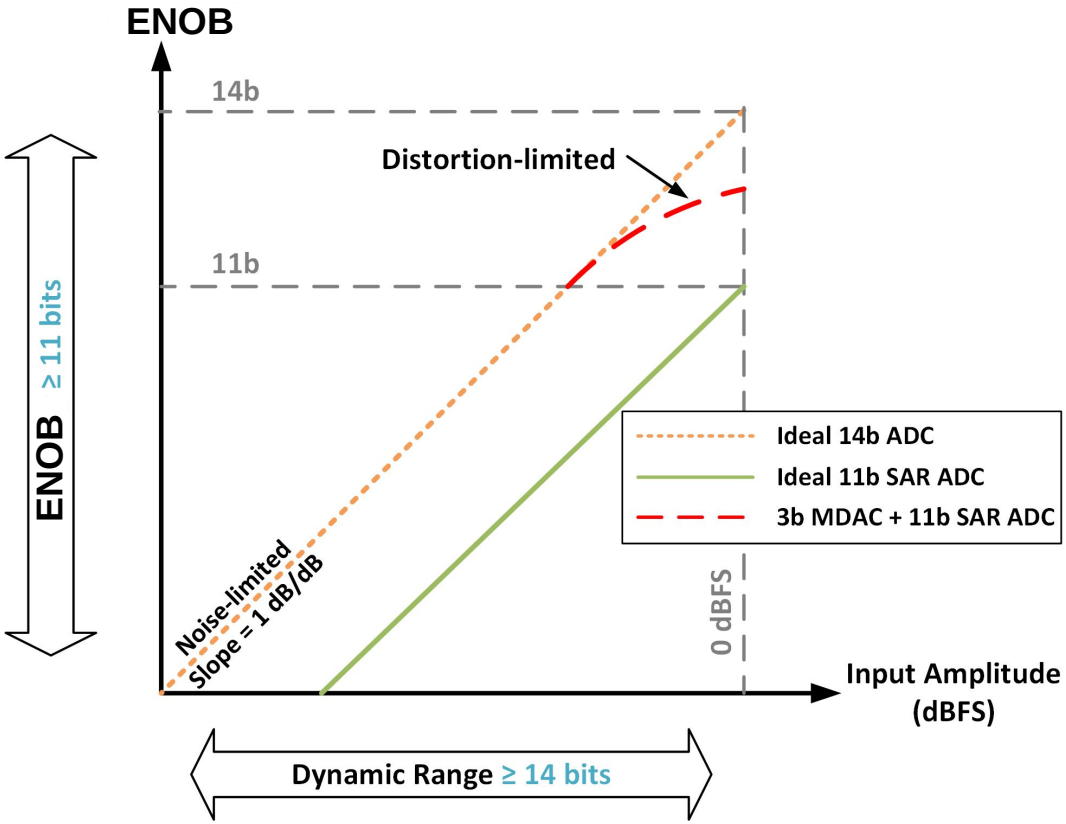
- Columbia University, Nevis Labs (John Parsons, Prof., Physics Lead)
  - Jaroslav Ban, EE – Digital design, Integration
  - Physicists (Testing) – Drs. Julia Gonski, Brian Kirby, Ines Ochoa; *PhD students*: Elena Busch, Kiley Kennedy, Andrew Smith, Daniel Williams, Gabriel Matos, Sylvia Mason, Kiryeong Park, Eleanor Woodward
- Columbia University, Electrical Engineering Department (Peter Kinget, Prof., Analog Lead)
  - Rui (Ray) Xu, PhD Student (previously at UT-Austin) Analog/digital design, Integration
  - Sarthak Kalani (PhD 2019, currently at Qualcomm)
  - Subhajit Ray, PhD Student, Analog Design
  - Michael Unanian, Analog Design (MS 2019, currently at Apple)
- University of Texas at Austin, Physics Department (Tim Andeen, Associate Prof., Physics Lead)
  - Michael Himmelsbach – Mass Production Testing/Validation, Packaging
  - *PhD students*: Chuck Burton, Devanshu Panchal, Mesut Unal, Lauren Larson, Michelle Contreras Cossio
- University of Texas at Austin, Electrical and Computer Engineering Department (Nan Sun, Associate Prof., SAR Design Lead)
  - Chen-kai Hsu, Analog Design (PhD 2020, currently at Analog Devices)
  - Xiangxing Yang, PhD Student, Analog Design

COLUTA Design Team

- The COLUTA team has extensive experience with ASIC development
  - Faculty involved are leaders in their field and have designed dozens of successful, highly complex chips.
  - All EE students are senior PhD students with several chip designs in their past.
  - They also have industrial experience from internships, including at leading companies (e.g. Analog Devices, Silicon Labs, Texas Instruments).
  - Our labs are equipped with industrial grade tools and computing infrastructure.
  - We have a rigorous design review process and design methodology.
- Examples of contributions within ATLAS
  - Nevis Labs led development of 5 custom rad-tol ASICs for the original FEB LAr readout (e.g. 40 MHz 13-bit 12-ch rad-tol SCA analog memory)
  - Nevis + Columbia EE + UT Austin developed and produced 40 MSPS 12-bit rad-tol ADC in 130 nm CMOS for LAr Phase 1 trigger upgrade
- Team structure follows industry practices:
  - Chip architecture, Analog and digital leads are all senior engineers (faculty and staff).
  - Design carried out by design engineers (advanced PhD students).
  - Channel and top-level integration and verification done by design engineers in collaboration with leads.
  - Typical graduation turnover managed by adding new students to overlap with advanced students.
- The team's experience and resources are well matched to the project

Target Specifications

- *ENOB (precision)* – ratio of a single-tone sinusoid to noise and distortion
- *Dynamic range* – ratio of largest quantization range over the smallest LSB



ENOB ≥ 11 bits → Limited by intrinsic analog linearity of transistors and circuits
Dynamic range ≥ 14 bits → Limited by thermal noise

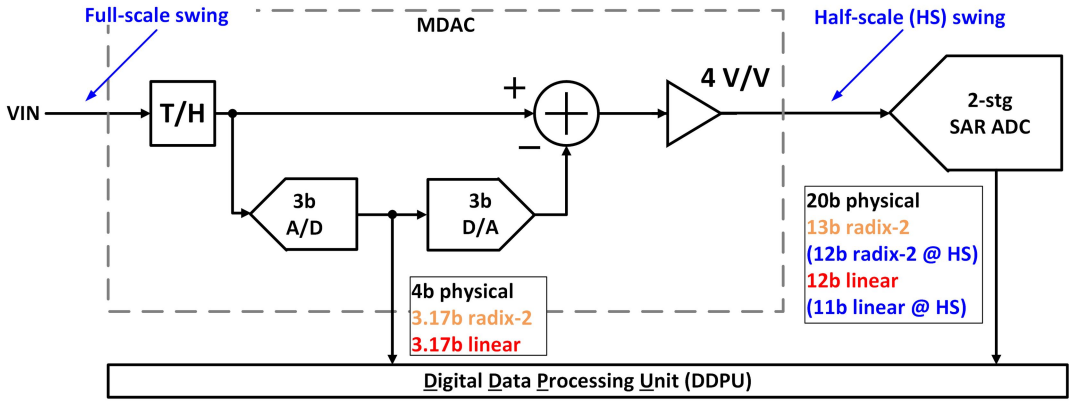
Target Specifications (cont.)

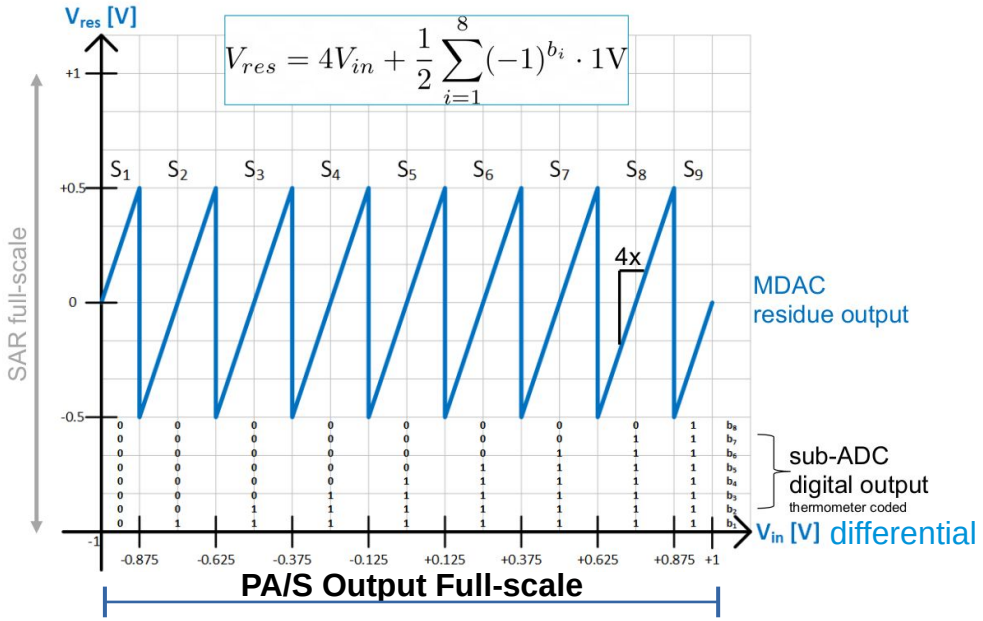
Parameter	Specification
Channels/Chip	8 preferred/4 minimum
Sampling Frequency	**40 MSPS**
Dynamic Range	**≥14 bits**
Precision	**≥11 bit ENOB @ 8 MHz**
Power	< 100 mW/channel
Input	2 V differential
Output	E-link interface operating at 640 Mbps
Operating temperature	From 10 to 50° C (optimal 20° C)

- Radiation hardness requirements
- Seamless integration
- INL < 0.1% up to 60% of total D.R.
- DNL within ± 1.0 LSB at the 12-bit level; No missing codes
- Gain and offset error to be correctable with calibration. Calibration frequency at most once/day and duration less than several minutes.
- TSMC 65nm LP CMOS 1.2V, use of MOS thin-oxide devices only
- More discussion: see Technical Design Report

  "ATLAS Liquid Argon Calorimeter Phase-II Upgrade: Technical Design Report," Sep. 2017. [Online]. Available: https://cds.cern.ch/record/2285582

Channel Architecture

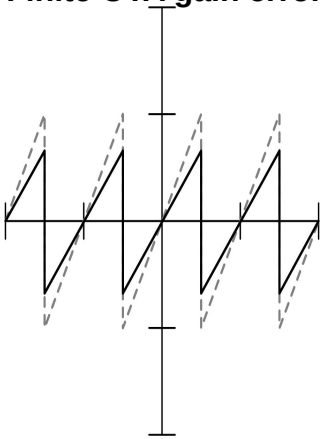




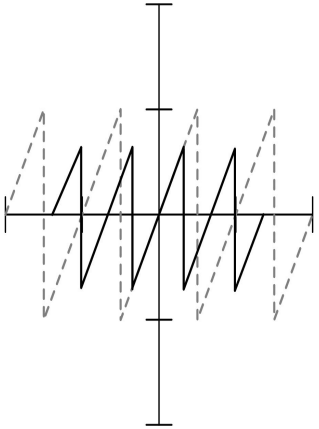
ENOB and D.R. specifications are met by using an MDAC to "extend" the D.R. of a SAR ADC to 15b.

Interstage Redundancy

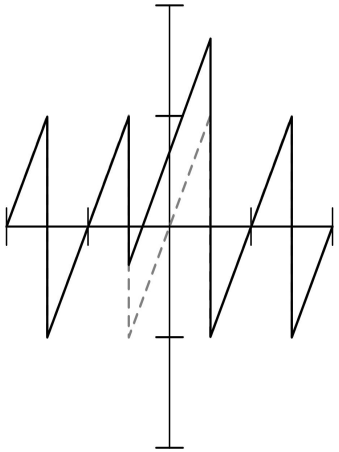
Finite OTA gain error:



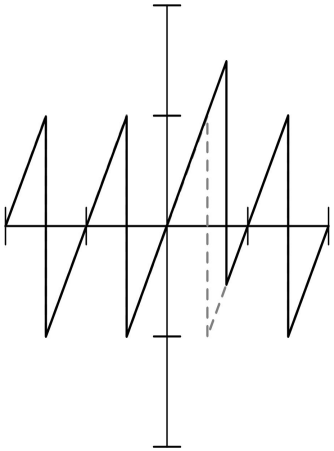
Reference error:



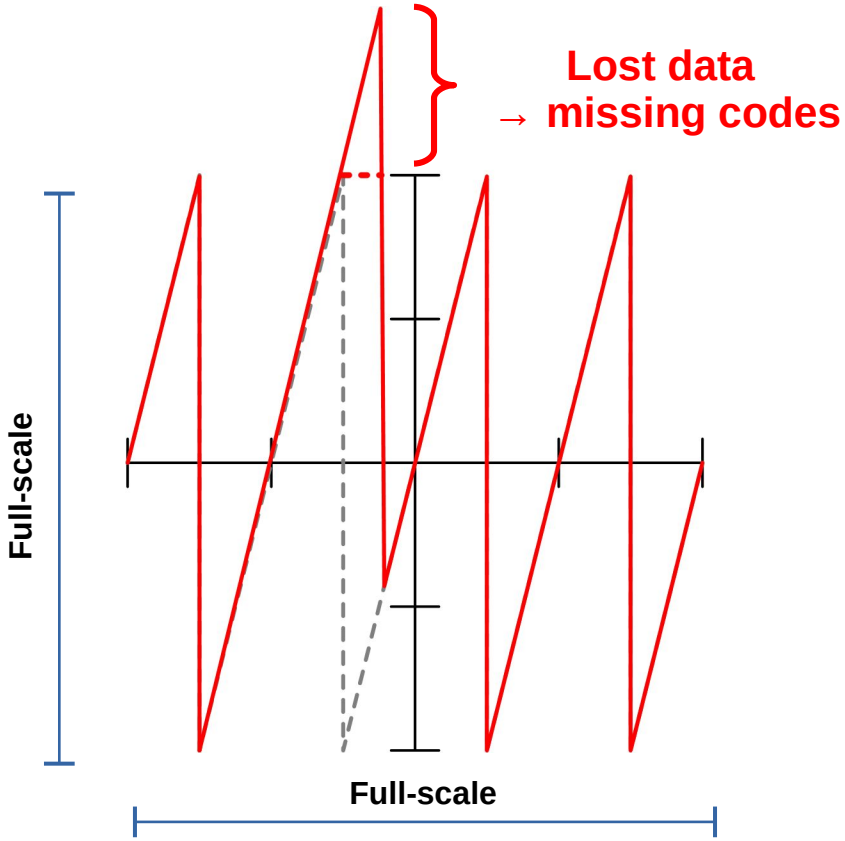
DAC mismatch error:



Sub-ADC error:



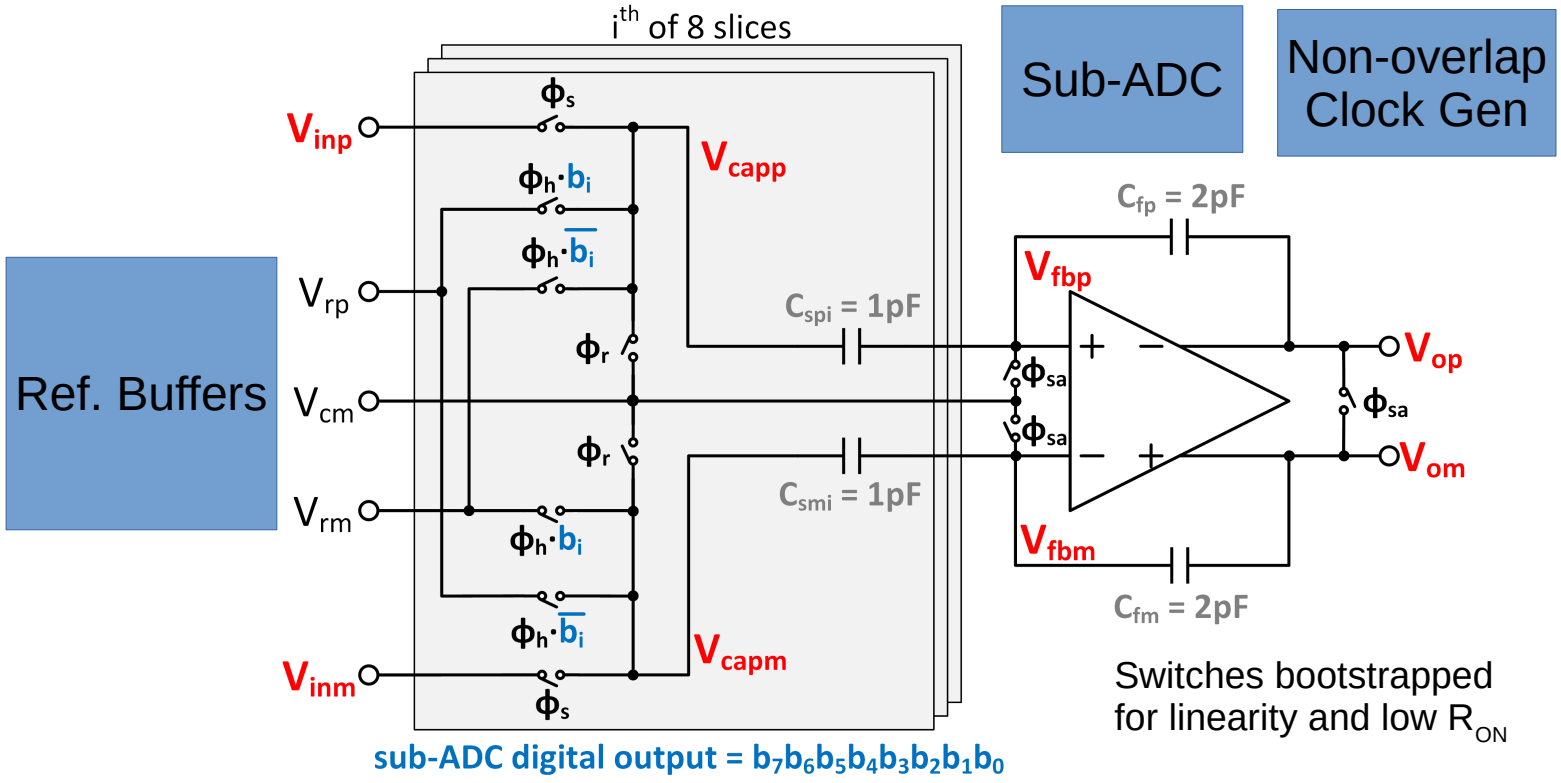
No redundancy:



Half-swing (interstage redundancy) is used to avoid missing codes.

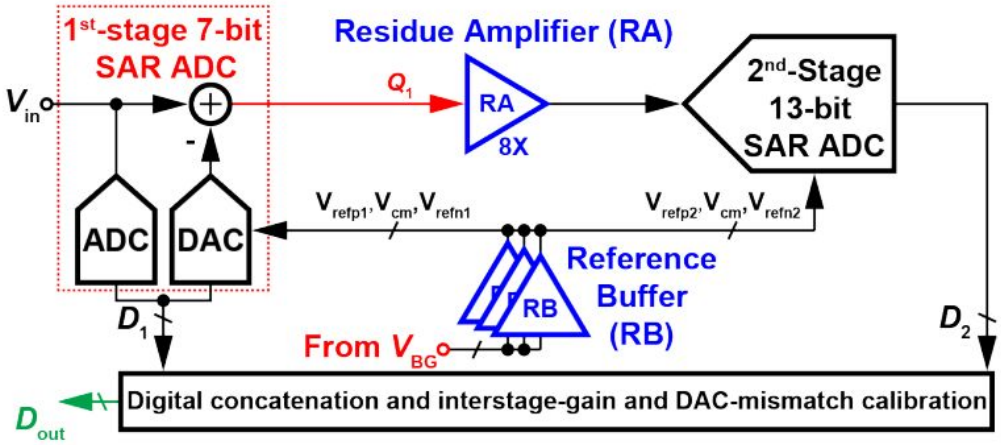
MDAC Implementation

- MDAC maps (1/8)*FS at the input → (1/2)*FS at the back-end ADC
- Input S/H cap = 4 pF diff. = 32 μV_{rms} kT/C noise. Compare against $V_{LSB} = 2\ V_{pp,diff} / 2^{15} = 61\ \mu V_{pp,diff}$
- Residue gain of $2^2 = 4$ V/V (instead of 2^3) provides 1-b of inter-stage redundancy



Input S/H capacitors are sized for noise considerations to meet ≥ 14 bit dynamic range specification. Thermometer encoding guarantees monotonicity.

SAR Implementation



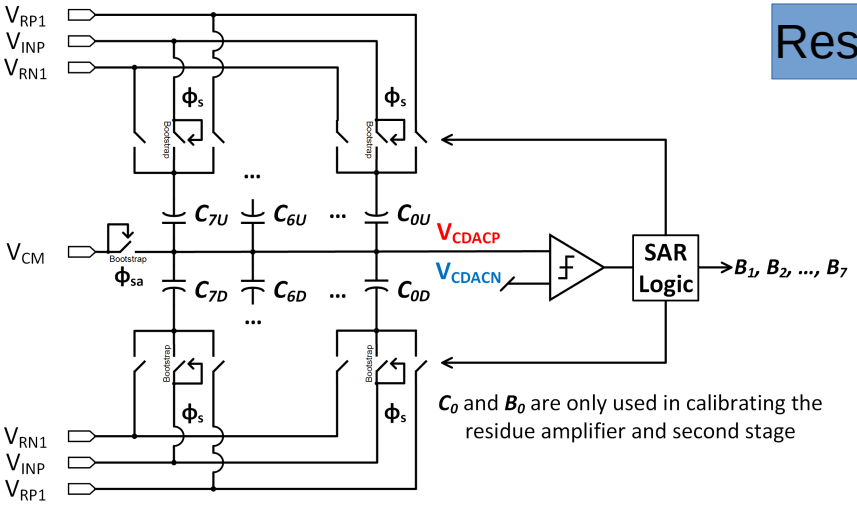
Actual circuit is fully-differential

- 20 physical bits → 13 radix-2 bits
  - 1-bit redundancy in 1st stage & 2-bit redundancy in 2nd stage to account for conversion errors via sub-radix-2 DAC scaling
  - 2-bit redundancy for interstage errors, e.g. comparator offset or reference offset
  - 2 LSB's in 2nd stage are for calibration only
  - 20 – 1 – 2 – 2 – 2 = 13 bits of radix-2 code
- 1st stage and 2nd stages are asynchronous and have their own reference buffers
  - They digitize simultaneously
- Common-mode buffer can be shared since they sample at different times

SAR designed to meet ≥ 11 bit ENOB.
MDAC+SAR: front stages emphasize analog accuracy; later stages emphasize speed.

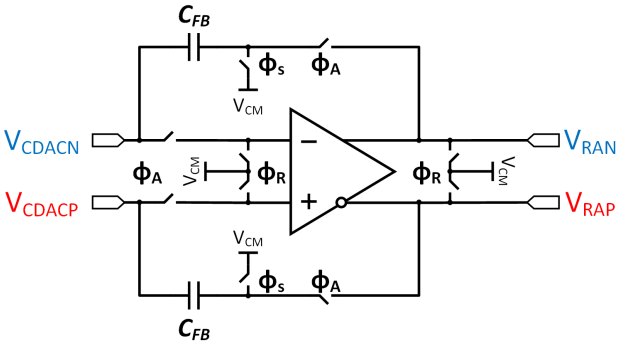
SAR Schematics

First Stage:

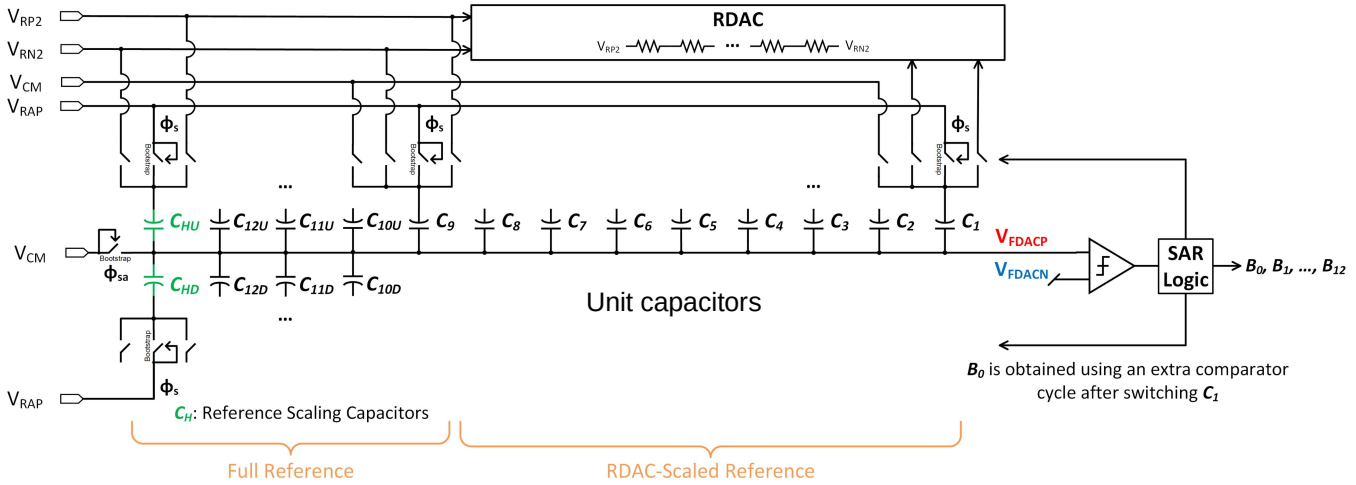


C_0 and B_0 are only used in calibrating the residue amplifier and second stage

Residue Transfer: (x8 gain)



Second Stage:



B_0 is obtained using an extra comparator cycle after switching C_1

- B. P. Ginsburg and A. P. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS With Split Capacitor Array DAC," IEEE JSSC, vol. 42, no. 4, pp. 739–747, April 2007, doi: 10.1109/JSSC.2007.892169.
- Y. Zhou, et al., "A 12 bit 160 MS/s Two-Step SAR ADC With Background Bit-Weight Calibration Using a Time-Domain Proximity Detector," IEEE JSSC, vol. 50, pp. 920–931, 2015.
- M. Kim, et al., "A 12-bit 200-kS/s SAR ADC with hybrid RC DAC," 2014 IEEE Asia Pacific Conf. on Circ. and Sys. (APCCAS), pp. 185–188, 2014.

SAR DAC Scaling

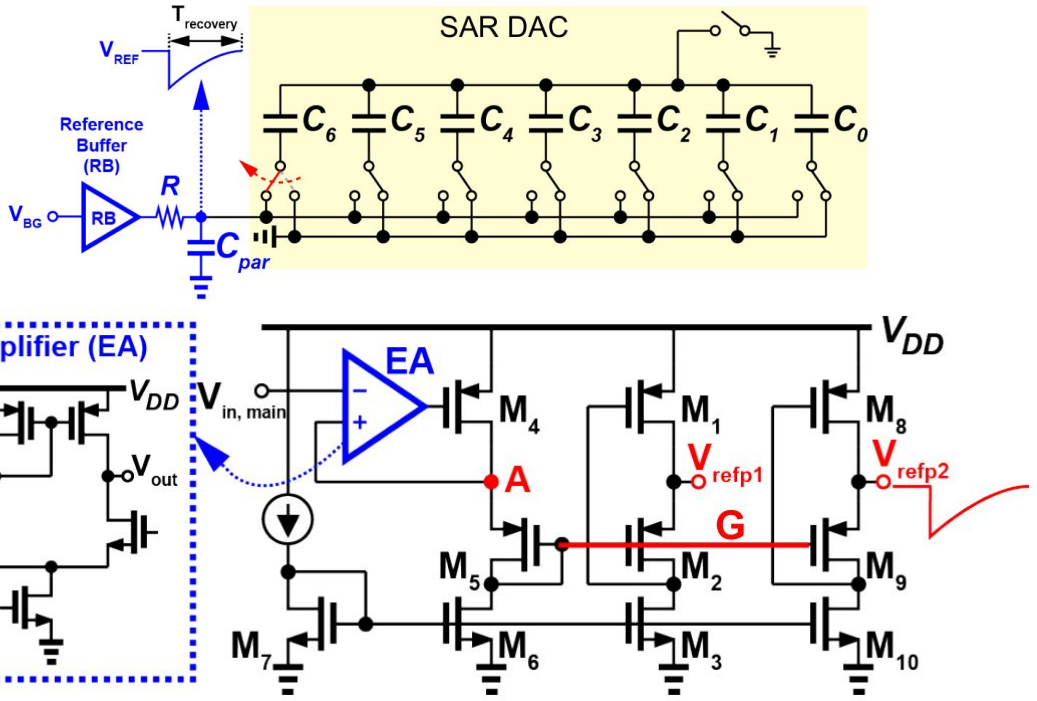
Bit Number		RDAC Total Units	RDAC Weight	RDAC Ratio	CDAC Weight	CDAC Total Units	CDAC Ratio	Combined Ratio	Weighting, normalized	Cumulative Weight	Cumulative Redundancy range
	1	Comparator-only Conversion Cycle							0.25	0.25	
2nd Stage	2	64	1	0.015625	1	32	0.03125	0.00048828125	0.5	0.75	0.75
	3		2	0.03125	1		0.03125	0.0009765625	1	1.75	0.75
	4		4	0.0625	1		0.03125	0.001953125	2	3.75	0.75
	5		8	0.125	1		0.03125	0.00390625	4	7.75	0.75
	6		12	0.1875	1		0.03125	0.005859375	6	13.75	2.75
	7		20	0.3125	1		0.03125	0.009765625	10	23.75	4.75
	8		32	0.5	1		0.03125	0.015625	16	39.75	8.75
	9		48	0.75	1		0.03125	0.0234375	24	63.75	16.75
	10	N/A	N/A	1	1		0.03125	0.03125	32	95.75	32.75
	11			1	2		0.0625	0.0625	64	159.75	32.75
	12			1	4		0.125	0.125	128	287.75	32.75
	13			1	7		0.21875	0.21875	224	511.75	64.75
1st Stage	14	N/A	N/A	1	2	128	0.015625	0.015625	128	639.75	384.75
	15			1	4		0.03125	0.03125	256	895.75	384.75
	16			1	6		0.046875	0.046875	384	1279.75	512.75
	17			1	10		0.078125	0.078125	640	1919.75	640.75
	18			1	16		0.125	0.125	1024	2943.75	896.75
	19			1	32		0.25	0.25	2048	4991.75	896.75
	20			1	56		0.4375	0.4375	3584	8575.75	1408.75

- Sub-radix-2 DAC scaling can undo a "wrong" SAR decision
  - Guarantee no missing codes
  - Immune to comparator decision errors (incl. SEE)
  - Necessary for foreground calibration hardware to function
- Two physical bits allocated for inter-stage redundancy (highlighted) between 1st and 2nd SAR stages
- RDAC is used to help derive the smaller bit-weights without $O(2^n)$ scaling of capacitors
  - RDAC adds loss to mitigate reference ringing due to bondwires when evaluating the LSB's

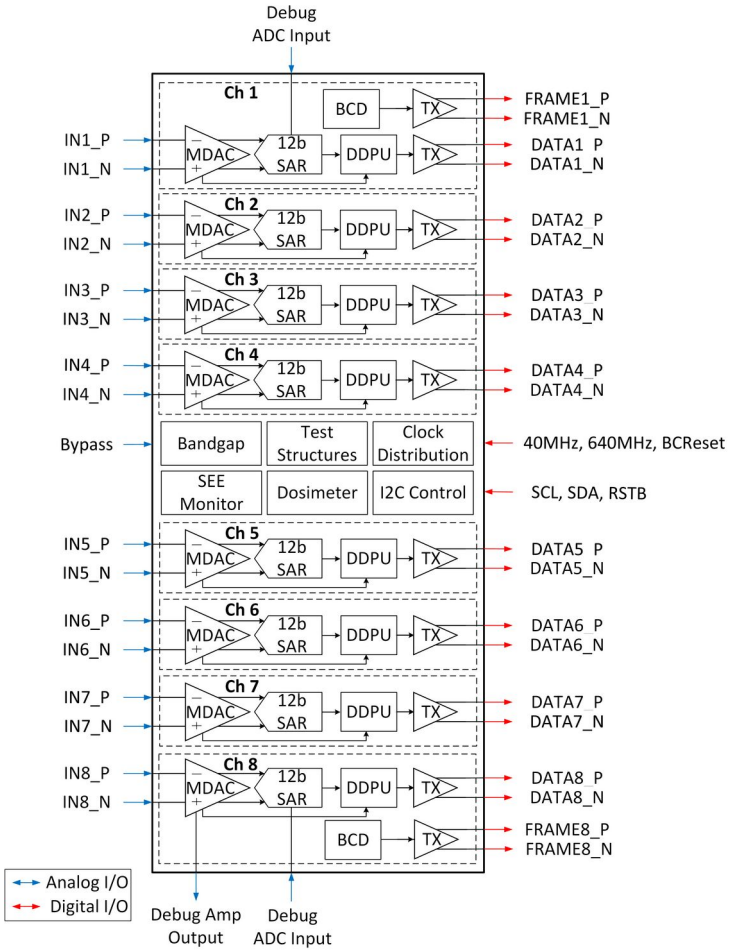
Sub-radix-2 DAC scaling is used to guarantee analog accuracy at the expense of code dynamic range.

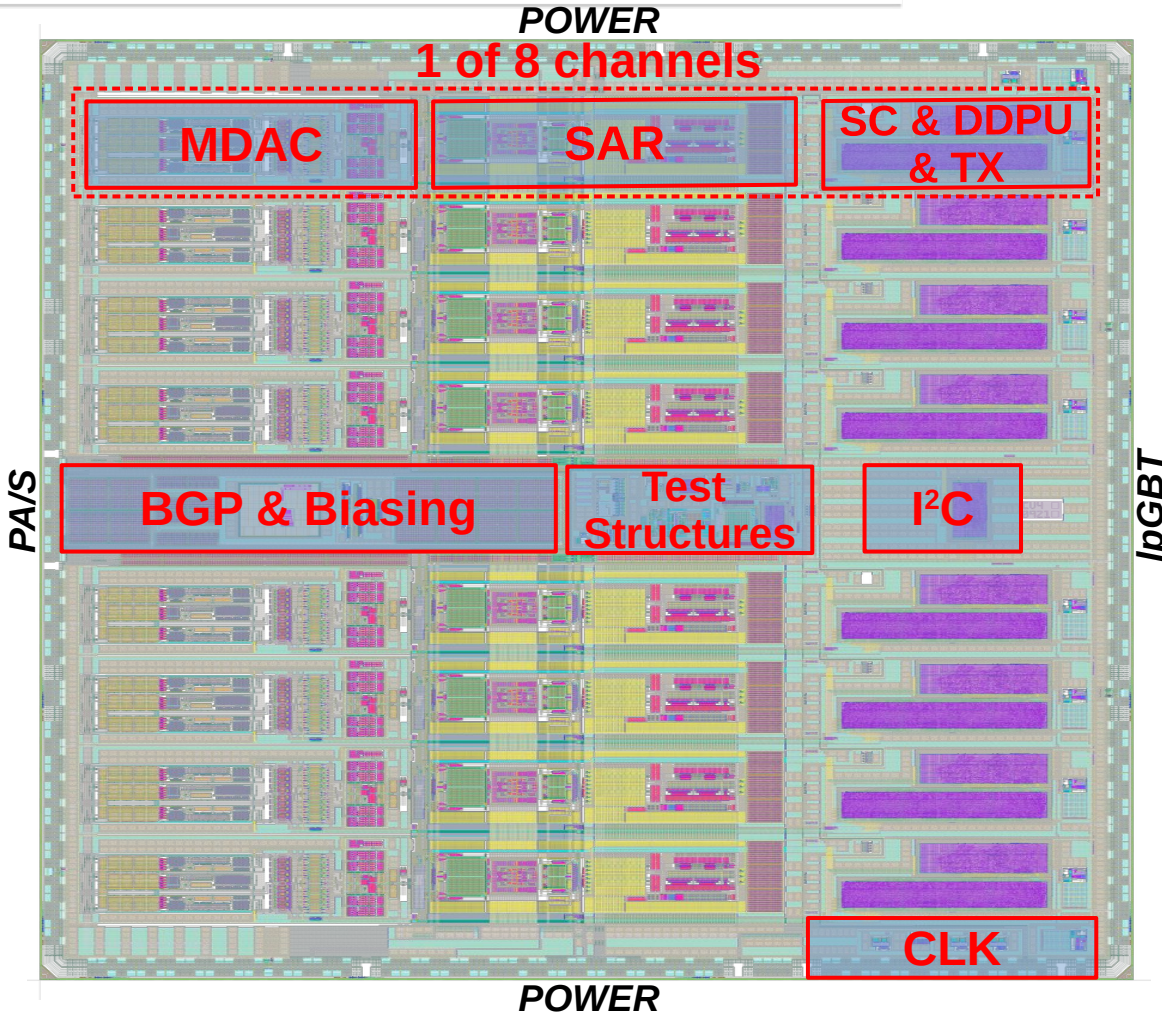
SAR Reference Buffer

- **Goal**: Deliver a stable voltage by tracking the output of the on-chip bandgap
- $T_{recovery}$ has to be short, on the order of ~1 nS
- Replica-based flipped-voltage follower (FVF):
  - Very low output impedance and excellent current sourcing capability that can minimize $T_{recovery}$
  - Replica biasing compensates PVT variations
- Shown for VREFP = 1.1V; VREFN = 0.1V use the complementary version
  - Headroom is challenging → large transistor areas for lower $V_{DS,SAT}$
  - VREF designed to maintain a "constant dropout" with respect to VDD



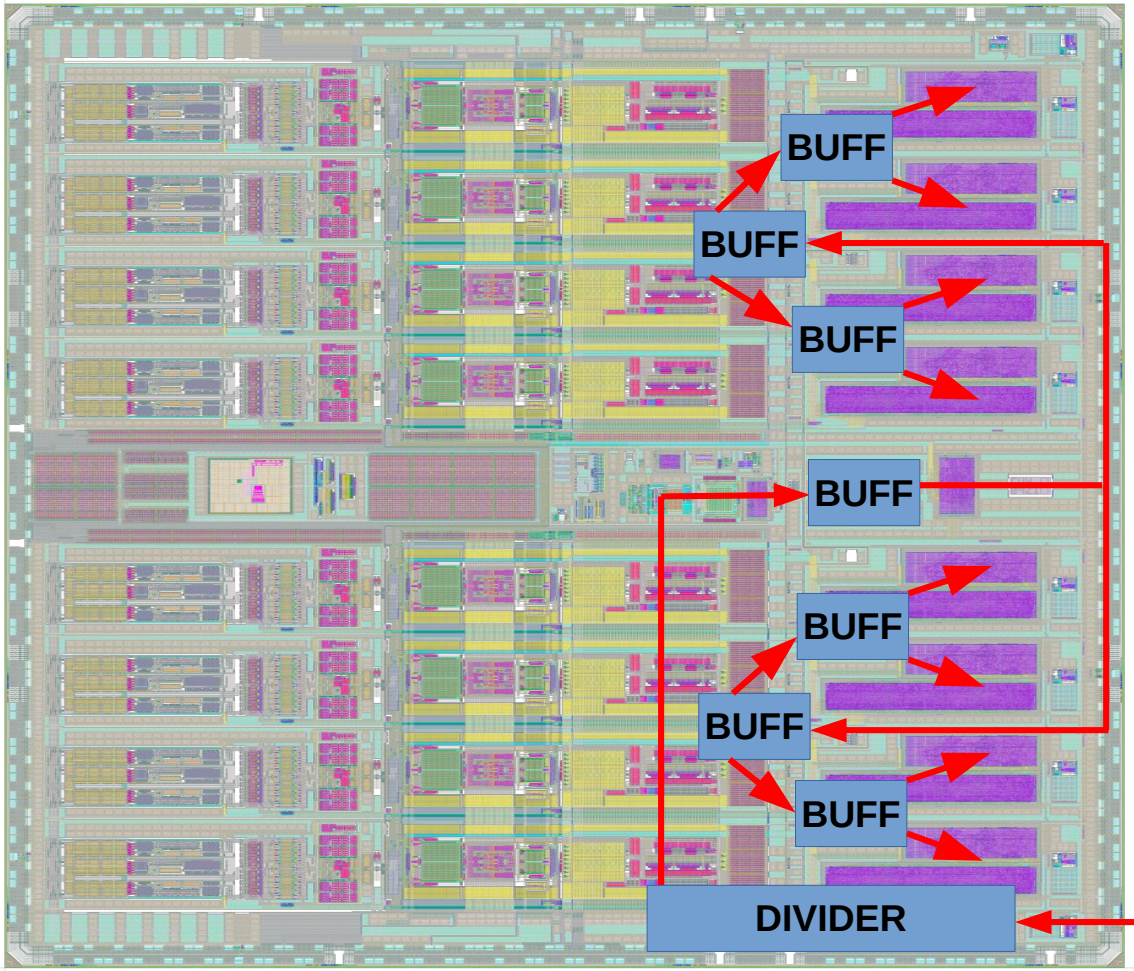
Chip Architecture





Eight independent and identical channels implemented. Seamless logical and physical (electrical) interconnection between PA/S and lpGBT.

Chip Implementation: Clock Distribution

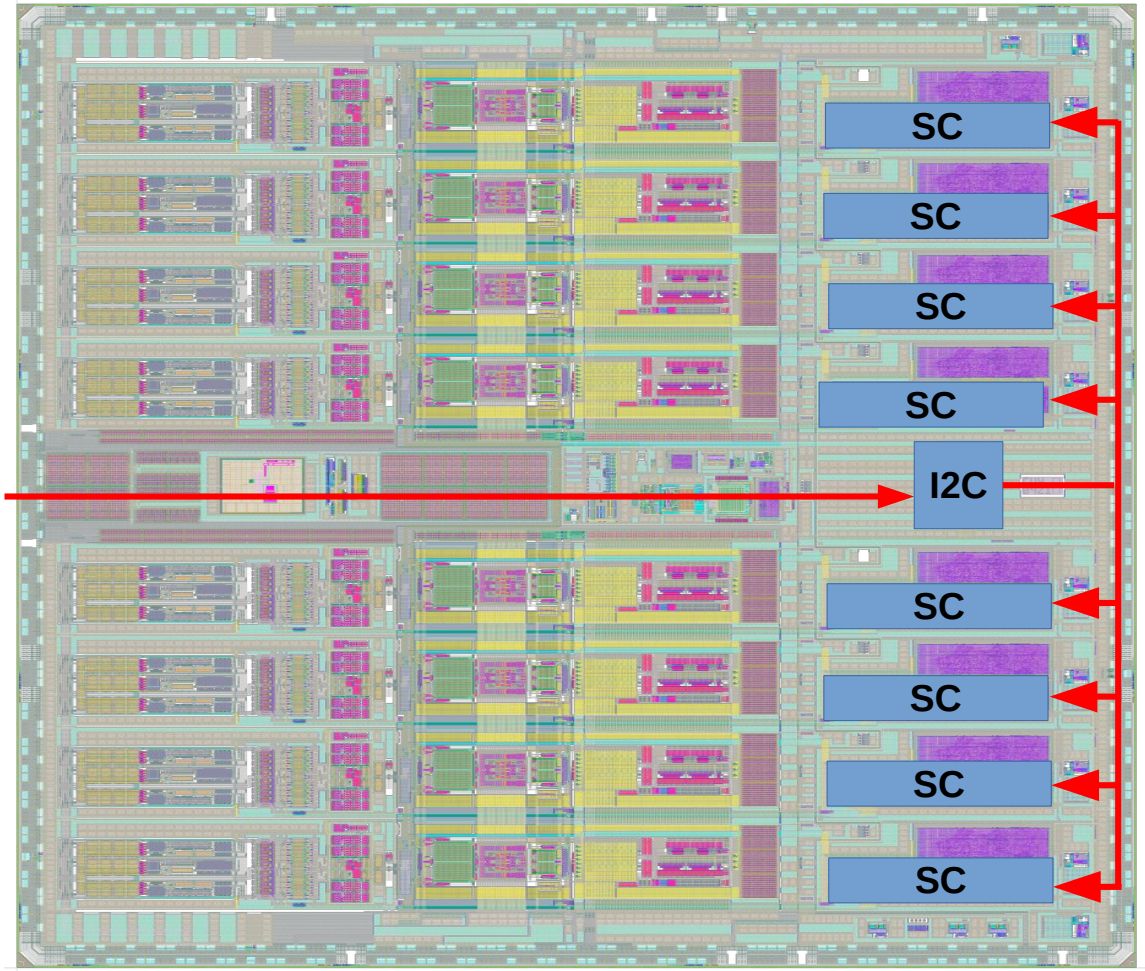


Clock inputs to divider:

- 640 MHz
- 40 MHz precision clock
- BCReset

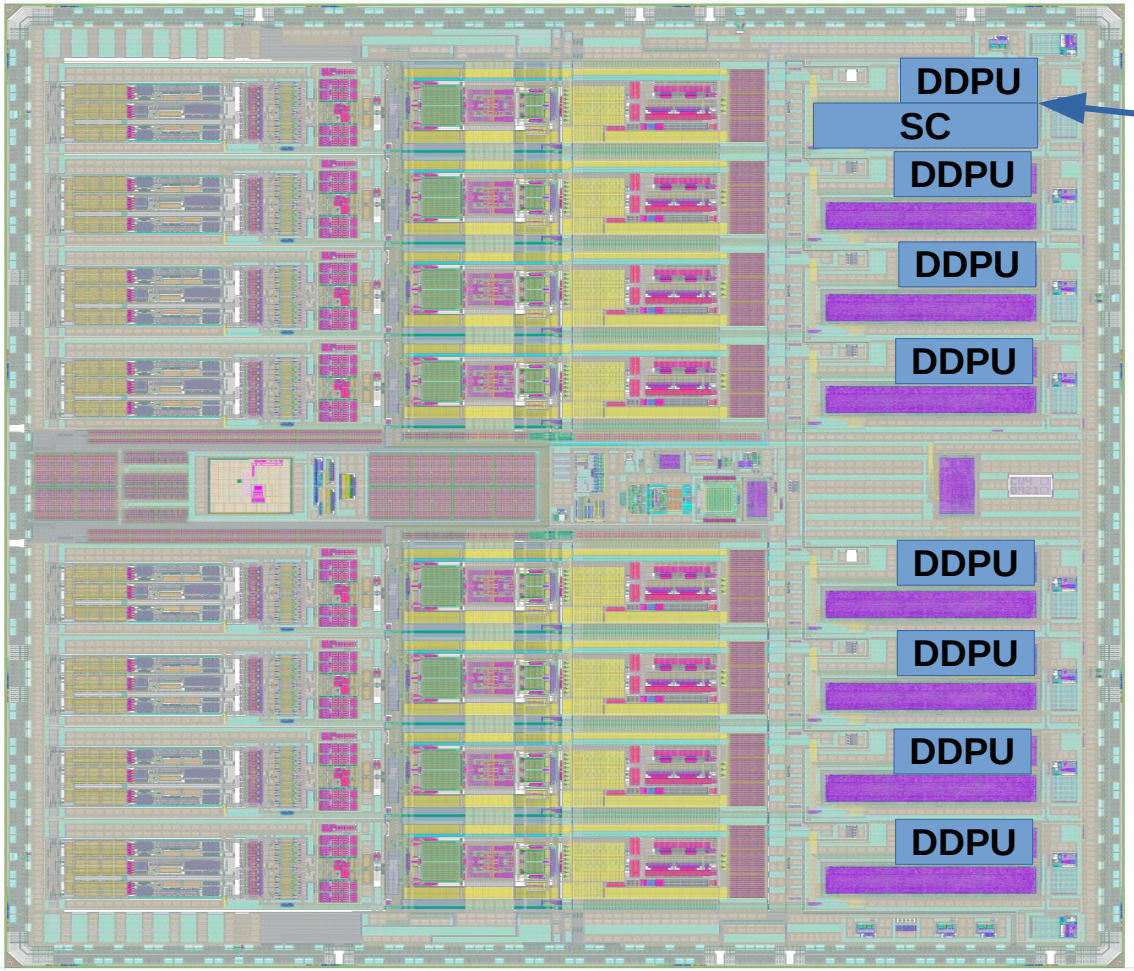
Binary clock tree is used to distribute clocks to all channels with minimal skew.
40 MHz: precision, analog clock. 640 MHz: digital logic

Chip Implementation: Slow-Control



Slow-control used to configure each block individually (e.g. clock phase, biasing, etc) via I2C. 4480 R/W bits in total.

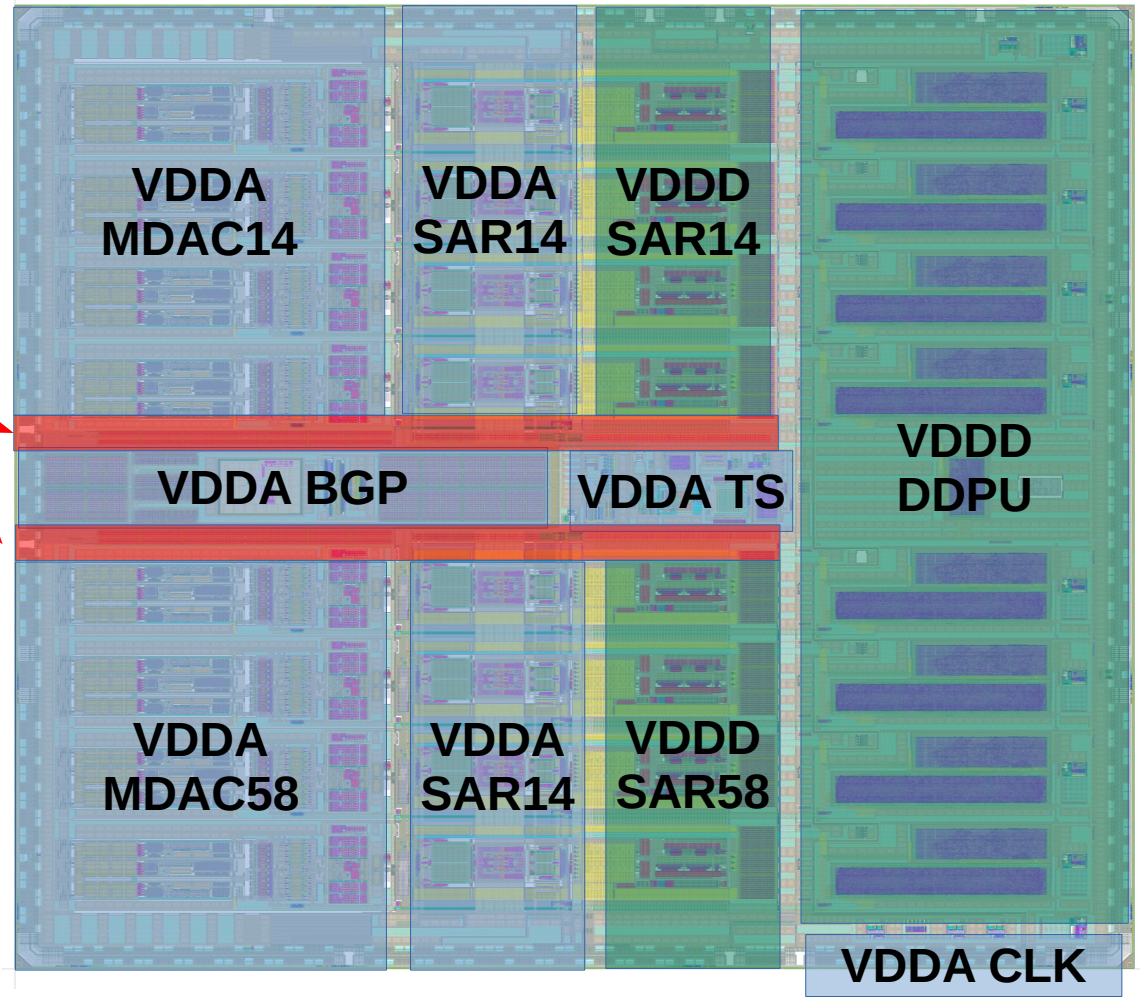
Chip Implementation: DDPU



Digital Data Processing Unit converts the MDAC+SAR physical bits into a radix-2 number, applies calibrated bit weights, and serializes for sLVS TX for each channel.

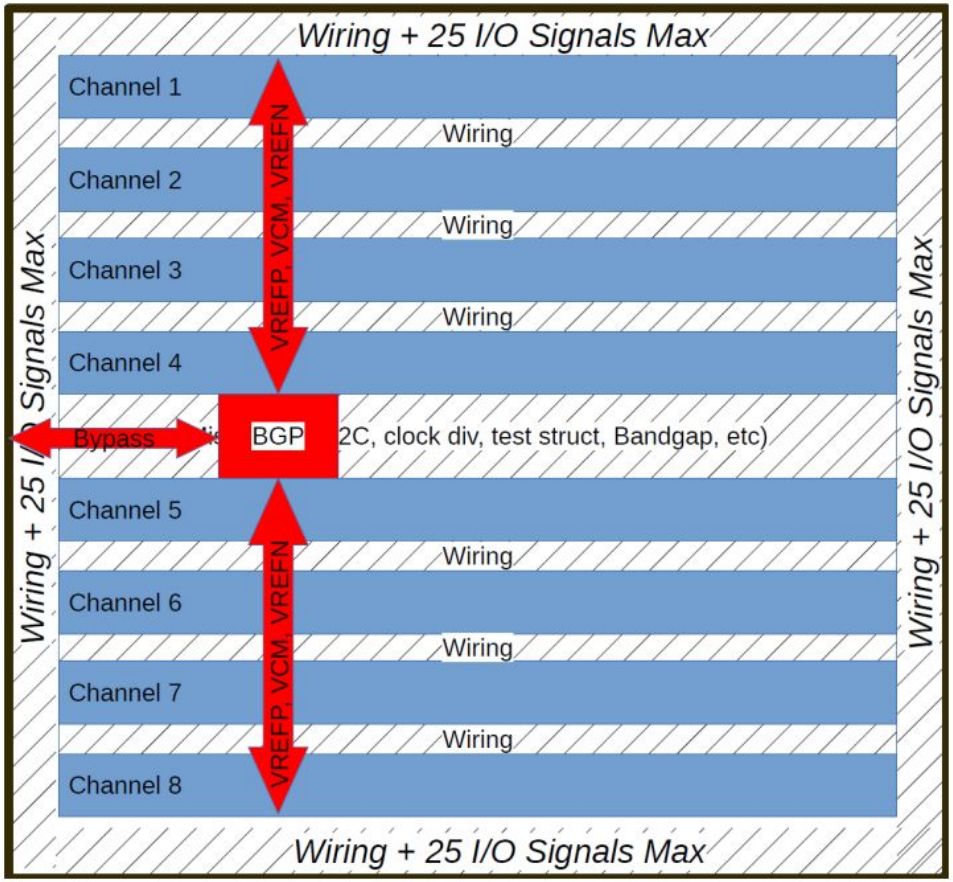
Chip Implementation: Power Distribution

Bulk decap imitates AC ground



Supplies split between analog/digital and pipeline stages to avoid crosstalk via VDD. Bulk decap especially located in the center where it is farthest from the pins.

Chip Implementation: Bias Distribution

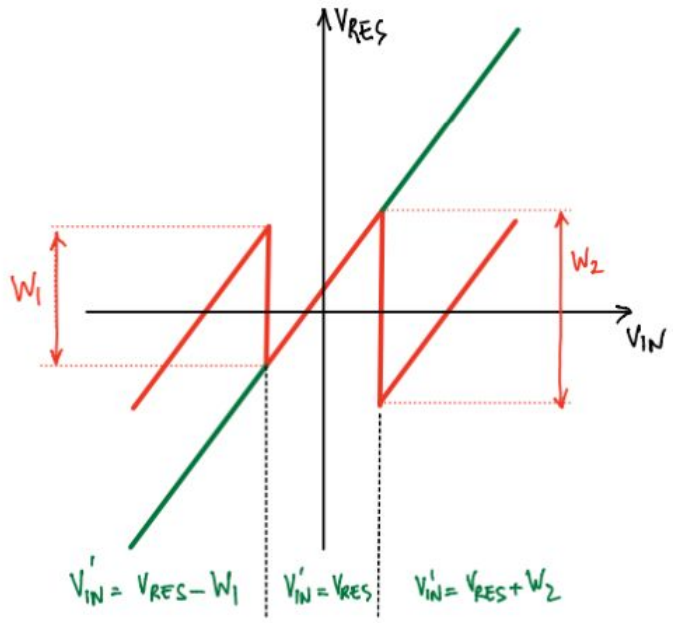


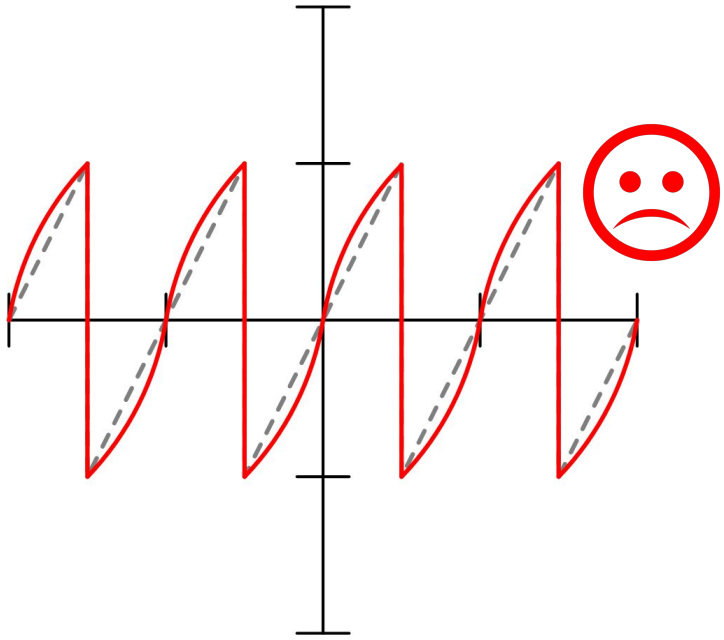
Due to a nom. VDD of 1.2V, VREFN and VREFP are designed to maintain nom. 100mV from the rails; VCM is designed to maintain half-VDD.

VREF distribution to all channels → individually buffered in each channel.
Bias current distributed as current → robust against PVT variations and TID.

Foreground Calibration Concept

- Philosophy: *measurement* of calibrated bit weights → *actuation* mechanism on-chip
  - Conditions during *measurement* should be as close as possible to the conditions during *actuation* when the SAR ADC is operating normally.



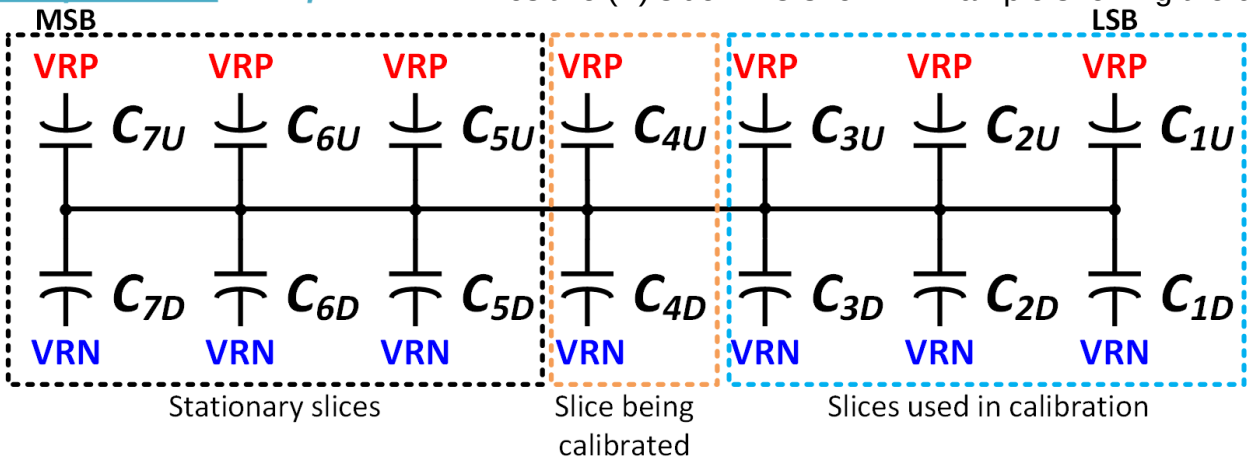


Foreground calibration is a piece-wise linear transformation of the ADC's transfer function. Higher-order nonlinearity cannot be calibrated out.

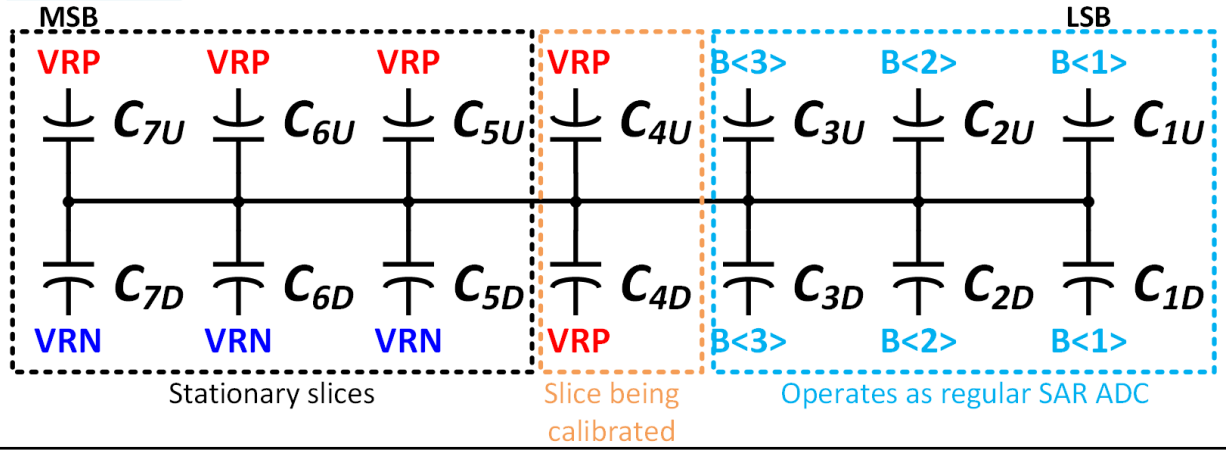
- A. N. Karanicolas, et al., "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC," IEEE JSSC, vol. 28, pp. 1207–1215, 1993.

Foreground Calibration (SAR)

***Sample Phase*: Sample VCM** Positive (P) side DAC shown. Example showing the calibration of C_4.



***Hold Phase*: Assert Value Then Search**



Bits are calibrated in the LSB → MSB order.

Lower 6 physical bits (out of 20) in the SAR have a fixed weighting.

Sampling switch is disabled in calibration mode.

Existing hardware used in regular SAR conversion is re-used for calibration.

Comparator offset: Repeated pseudo-differentially for the N side.

Sampling Offset/Charge Injection: Repeated by forcing **VRN.**

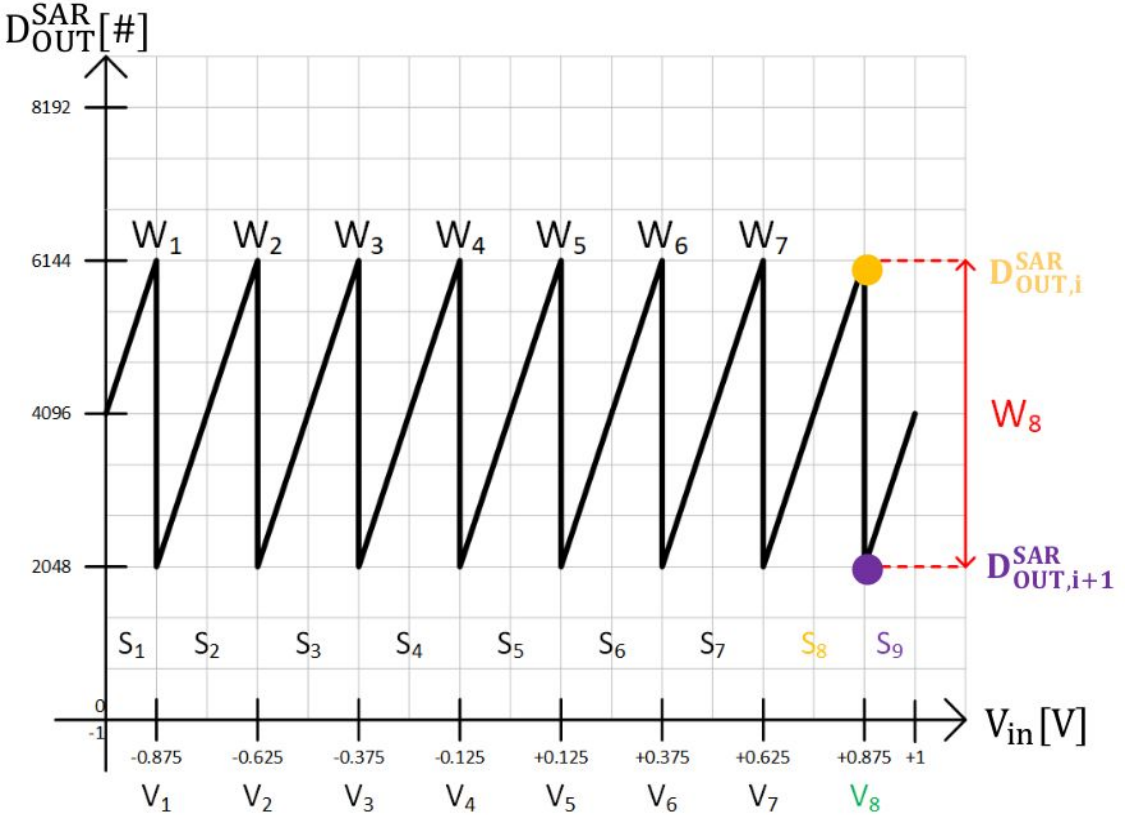
SAR recursively measures capacitor weights to stitch together the transfer function.

- W.-H. Tseng et al., "A 12-bit 104 MS/s SAR ADC in 28 nm CMOS for Digitally-Assisted Wireless Transmitters," IEEE JSSC, vol. 51, no. 10, pp. 2222–2231, Oct. 2016, doi: 10.1109/JSSC.2016.2582861.
- J. L. McCreary and D. A. Sealer, "Precision Capacitor Ratio Measurement Technique for Integrated Circuit Capacitor Arrays," IEEE Trans. on Instr. and Meas., vol. 28, no. 1, pp. 11–17, March 1979, doi: 10.1109/TIM.1979.4314753.

Foreground Calibration (MDAC)

- Procedure
  1. Assert V_i
  2. Force S_i

  (1 and 2: carried out by calibration circuit)
  3. Measure & average
  4. Force S_{i+1}
  5. Measure & average
  6. Calculate $W_i = \mathbf{D}^{\mathbf{SAR}}_{\mathbf{OUT,i}} - \mathbf{D}^{\mathbf{SAR}}_{\mathbf{OUT,i+1}}$
  7. Repeat for i = 1 to 8



- DDPU uses $W_1,\ldots,W_8$ to "stitch together" the segments: $D_{out}^{MDAC+SAR} = D_{out}^{SAR} - 4096 + \sum_{i=1}^{8} W_i \cdot b_i$
- Existing circuitry used in conversion are also used to extract calibration constants
- MDAC calibration is done after SAR calibration

Radiation Hardening By Design

- Total Ionizing Dose (TID) Effects:
  - **Thin-oxide** devices in **TSMC 65nm LP process** are inherently rad-hard
  - Avoid use of thick-oxide devices at all costs
  - Enclosed-layout transistors utilized in on-chip bandgap (Si-proven IP block)
- Single-event Event (SEE) Effects:
  - MiM capacitors instead of MoM capacitors
  - Unit SAR DAC capacitor set to 10 fF & RC-hybrid DAC used in SAR 2nd stage smaller bits → reasonable tradeoff between power/area
  - Triple redundancy for all custom digital circuits inside mixed-signal blocks
  - TMRG Tool used in all synthesized logic blocks
  - TMR logic cells spaced > 15 μm apart

Radiation hardening steps taken at the circuit design level that may otherwise not be present in a COTS ADC device

- F. Faccio and G. Cervelli, "Radiation-induced edge effects in deep submicron CMOS transistors," IEEE Trans. on Nucl. Sci., vol. 52, no. 6, pp. 2413–2420, Dec. 2005, doi: 10.1109/TNS.2005.860698.
- F. Faccio *et al.*, "Radiation-Induced Short Channel (RISCE) and Narrow Channel (RINCE) Effects in 65 and 130 nm MOSFETs," IEEE Trans. on Nucl. Sci., vol. 62, no. 6, pp. 2933–2940, Dec. 2015, doi: 10.1109/TNS.2015.2492778.
- M. McLain et al., "Enhanced TID Susceptibility in Sub-100 nm Bulk CMOS I/O Transistors and Circuits," IEEE Trans. on Nucl. Sci., vol. 54, no. 6, pp. 2210–2217, Dec. 2007, doi: 10.1109/TNS.2007.908461.
- TMRG Tool, https://tmrg.web.cern.ch/tmrg/

Third-Party IP

- Si-proven IP blocks leveraged for interfacing with other chips to guarantee compatibility
  - Tested against varying conditions, especially radiation tolerance
- ESD I/O padframe + Schmitt trigger I/O for I^2C: Sofics / CERN Microelectronics
  - Designed to be latch-up immune
- I2C core: RTL Verilog provided by CERN Microelectronics
  - Meets or exceeds I2C industry specification
  - Internal watchdog + immune to false start condition
- sLVS TX/RX: Univ. of Bergamo / INFN Pavia
  - Interfaces directly with lpGBT
- Bandgap reference: Univ. of Bergamo / INFN Pavia

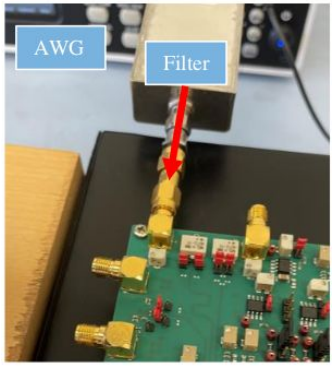
We incorporate silicon-proven 3rd party IP blocks to guarantee electrical compatibility with other chips in the system.

Verification Strategy

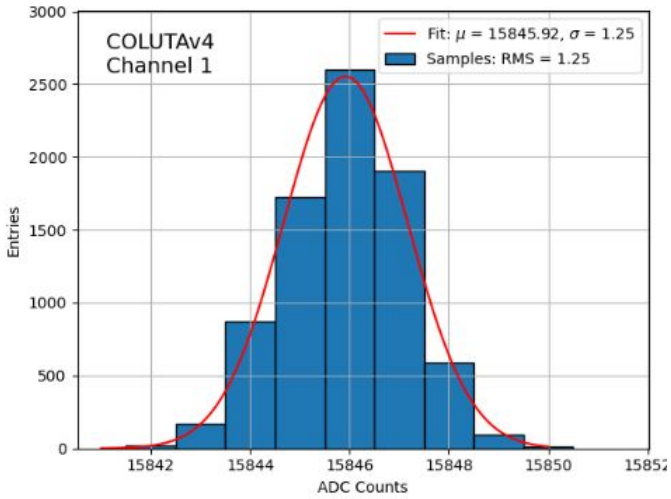
- Philosophy: simulate methodology should match measurement methodology
  - Example: calibration → sine wave performance
  - Use M.C. to see if randomized DAC values are captured in simulation
- Schematic vs. C+CC vs. R+C+CC
  - R+C+CC: most time-consuming, reserved for critical analog blocks
  - C+CC: fine for most corner/operating margin simulations given the breadth
  - Schematic: a full-chip "signal in signal out" simulation for LVS, at minimum
- Analog vs. Digital
  - More "stress testing" can be performed on the digital blocks
- Model abstraction
  - Certain blocks can be replaced with behavioral models to avoid lengthy simulation times. E.g., simulation of a channel will use a slow-control block model to avoid having to individually program all 544 bits. A separate, digital, simulation is then ran on the slow-control block by itself.
  - Chip level: Interconnect between blocks can be extracted and simulated.

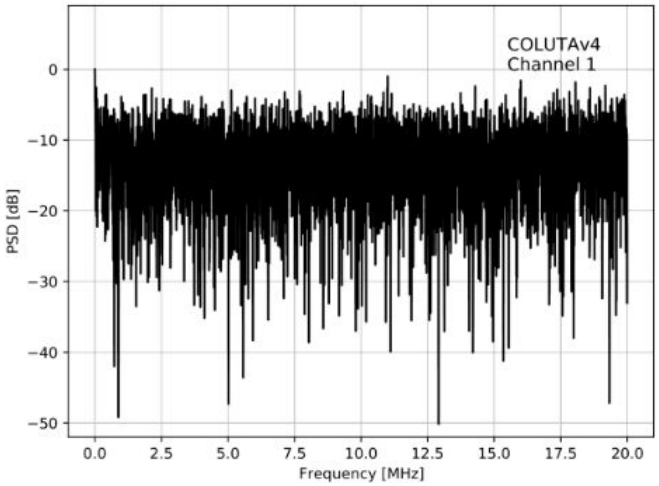
The simulation strategy was designed to imitate the measurement procedure while minimizing simulation time where possible.

Precision Measurement Setup



CV4 die packaged into 100-pin QFN for testing purposes





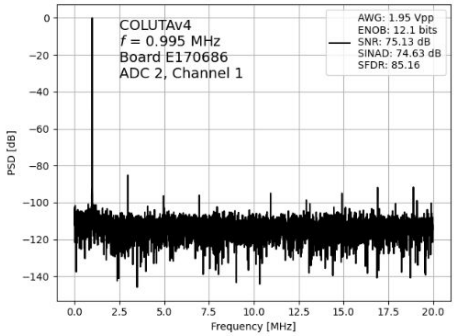
- Testboards with socketed or soldered QFN chips
  - Ch. 1,4: passive transformer input
  - Ch. 2: commercial amplifier input
  - Ch. 3: 16-bit DAC input
  - Ch. 5,6,7,8: PA/S input (LAr pulse testing only)
- Socketed for QA/QC tests; soldered for precision analog tests
- Feature-less pedestal; ~1.2 ADC counts RMS of noise out of 2^{15}; ~1.17 W power draw

CV4 meets dynamic range spec (c.f. ≥ 14 bits)

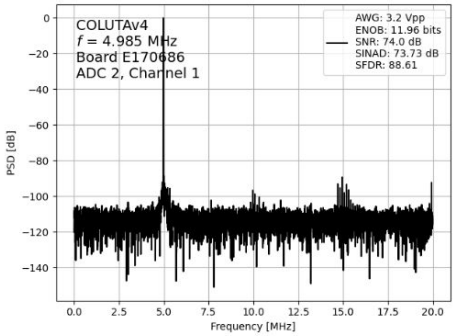
Sine Wave FFT

Co-prime sine wave applied at full-scale via bandpass filter

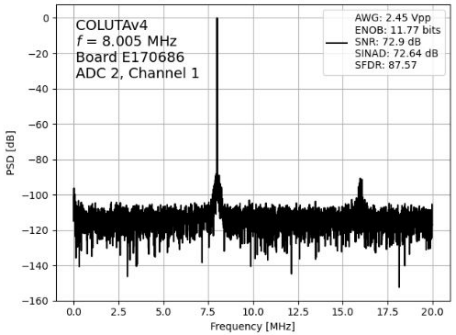
Ch 1:



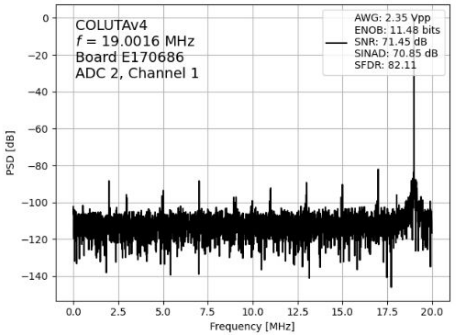
(a)



(b)

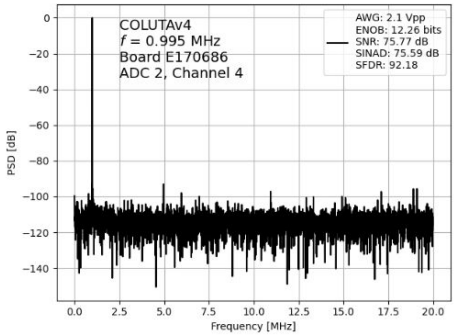


(c)

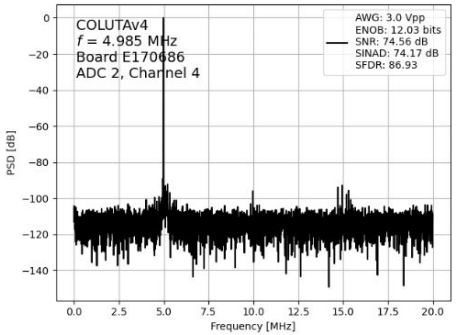


(d)

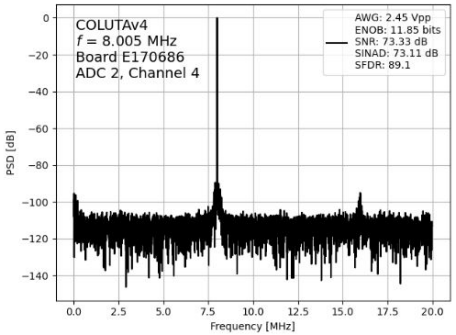
Ch 4:



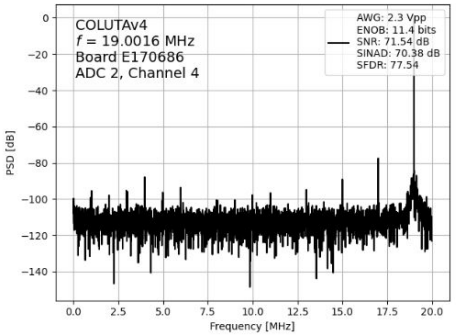
~1 MHz



~5 MHz



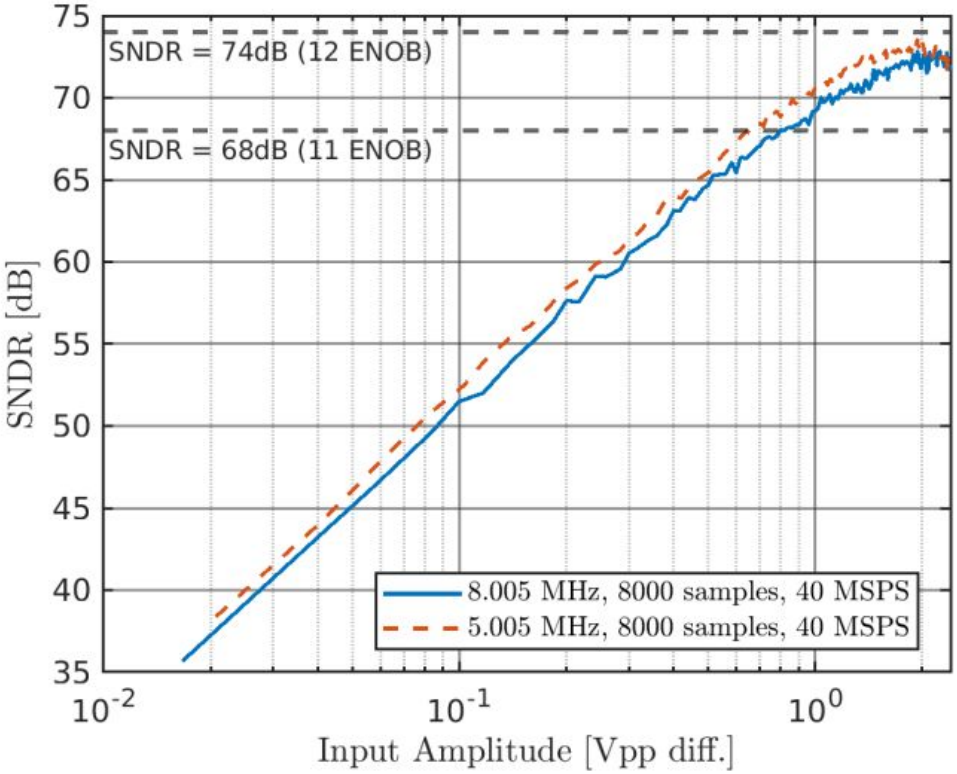
~8 MHz

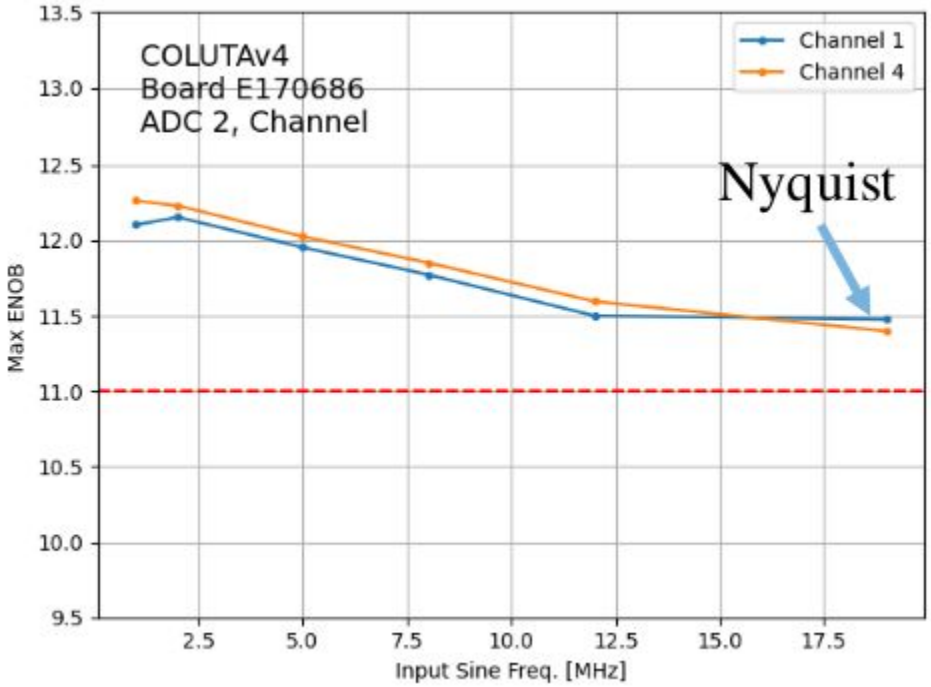


~19 MHz

CV4 meets sine wave SNDR at full-scale across DC to Nyquist (c.f. ≥ 11 ENOB). Harmonics ≤ -80 dBc

Sine Wave Sweeps





Sine wave sweeps across amplitude and frequency show well-behaved performance exceeding specifications.

INL/DNL

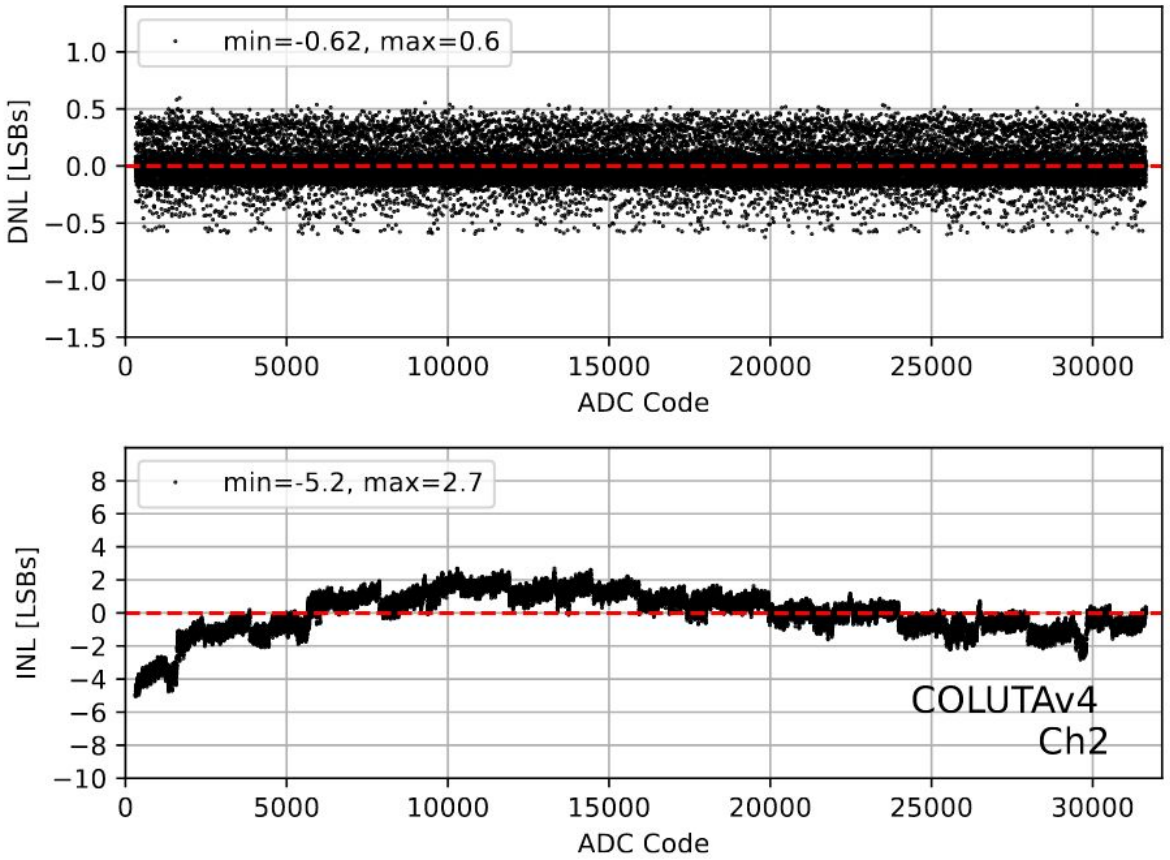
- Slow sine wave/histogramming used to test DNL; linear DAC ramp used to test INL

$$\mathrm{DNL}_j = \frac{V_{j+1} - V_j}{1\ \mathrm{LSB}} - 1$$

-0.62/+0.60 15b LSB_{15}
(-0.08/+0.08 12b LSB_{12})

$$\mathrm{INL}_j = \frac{V_j - V_{\mathrm{fit},j}}{1\ \mathrm{LSB}}$$

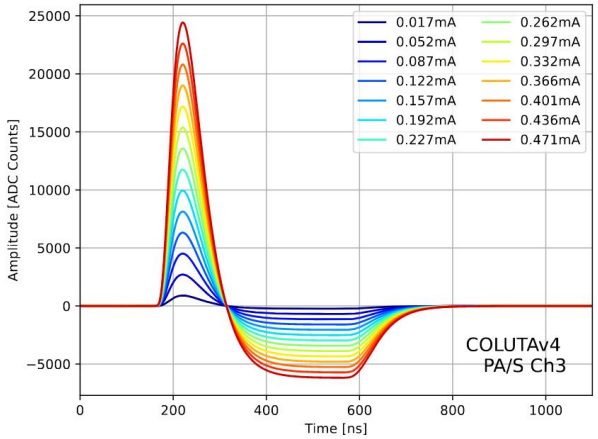
-5.20/+2.70 15b LSB_{15}
(-0.65/+0.34 12b LSB_{12})

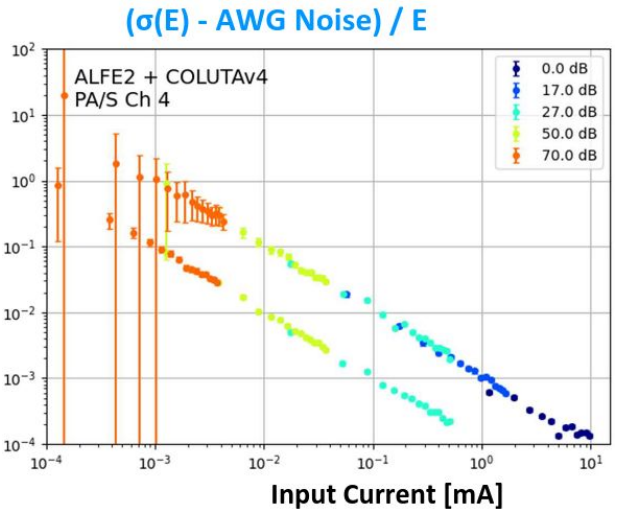


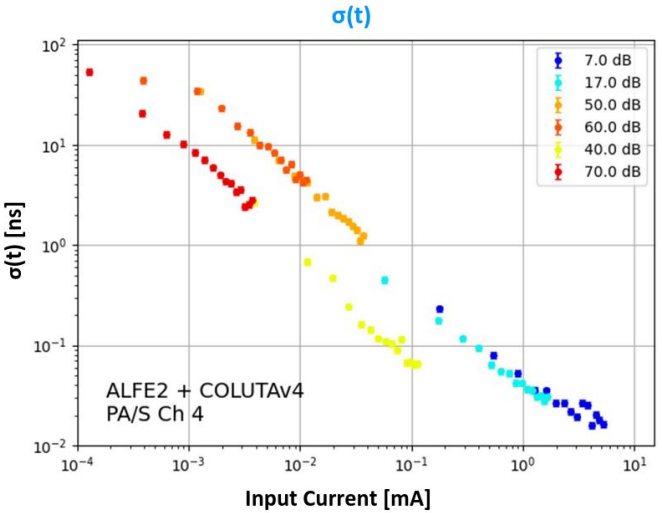
DNL meets spec (c.f. ± 1.0 LSB_{12}) and has no missing 2^{15} codes (c.f. 2^{14} D.R.)
INL meets spec ≤ 0.03% (c.f. ≤ 0.1%)

LAr Pulse Performance

- Pre-programmed triangle LAr pulse shape → AWG → shaped by ALFE PA/S → CV4 channels 5,8 (low gain) and 6,7 (high gai



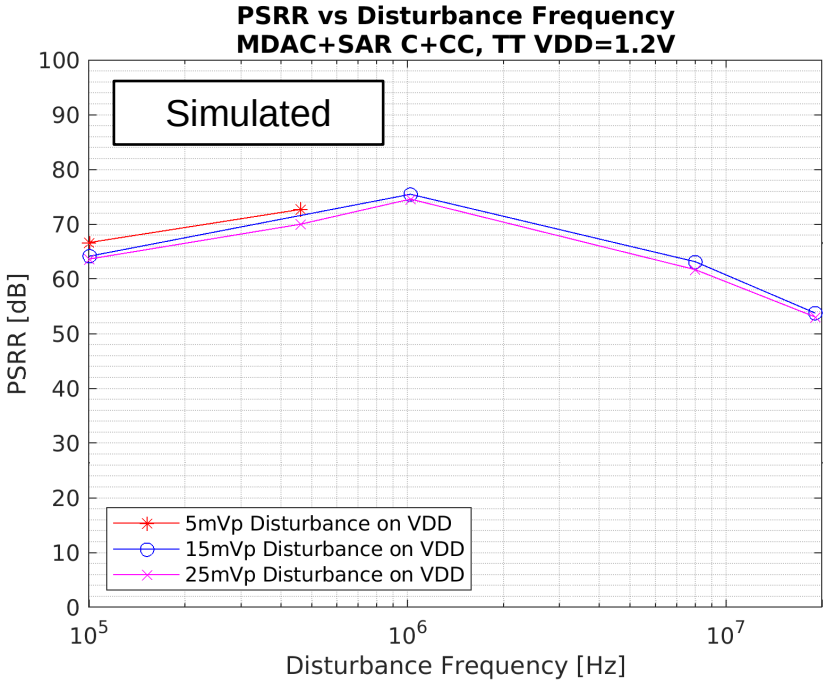


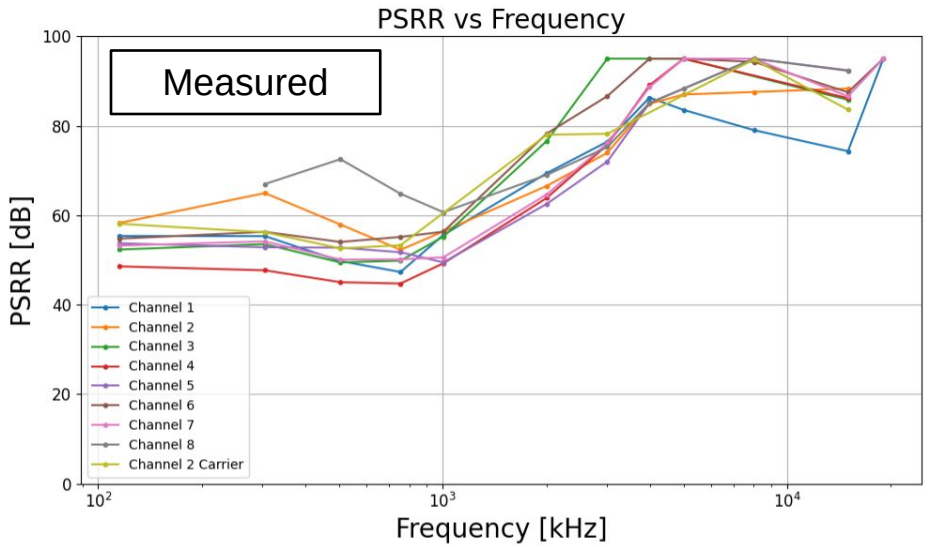


The ALFE PA/S + CV4 demonstrates, at highest amplitudes, an energy res. of 0.01% (c.f. 0.25%) and a timing res. of 16 pS (c.f. 100 pS), dominated by trigger test setup.

Power Supply Rejection Ratio (PSRR)

- A sinusoid is superimposed on the CV4's VDD, and the output digital code is observed for the sine wave disturbance. No AC input is given to the ADC input.
- Higher measured PSRR at higher frequencies might be explained by a limited simulation model and higher transmission losses

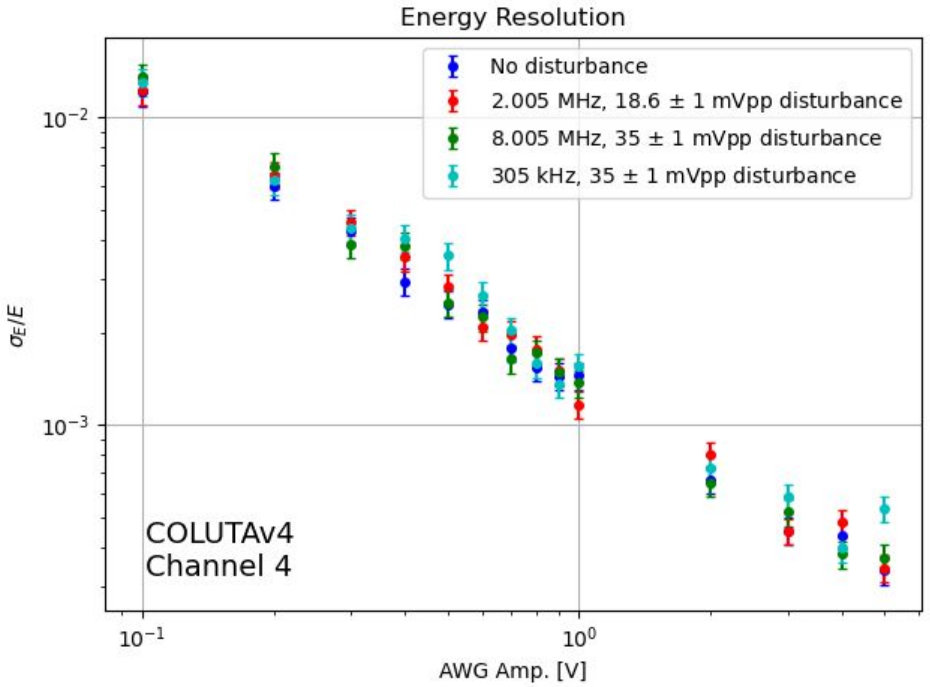


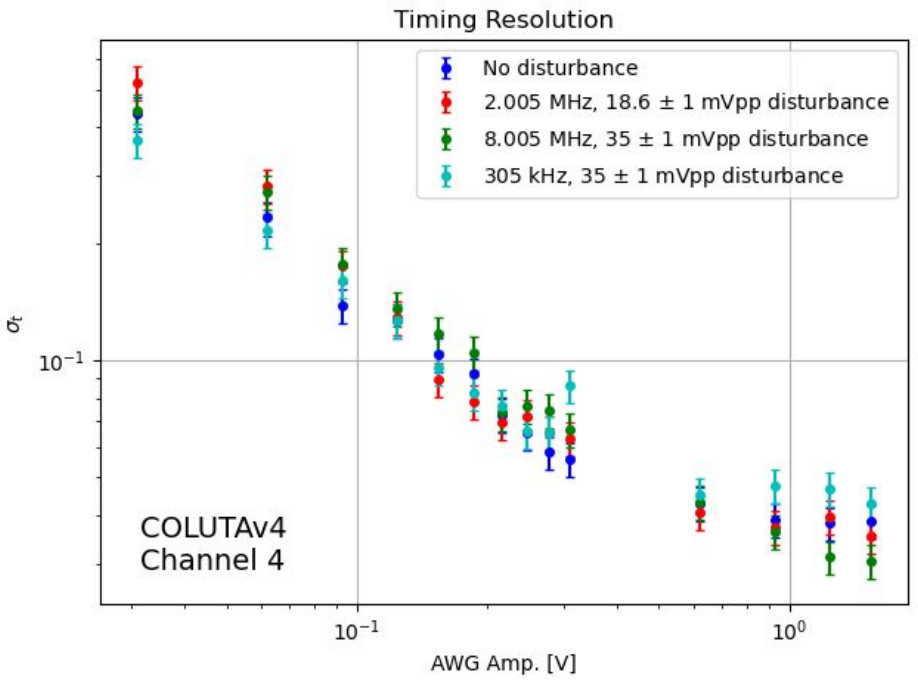


The CV4 demonstrates a PSRR sufficient for the application; simulation agrees with measurement at lower frequencies.

PSRR: Impact on LAr Pulse

- The impact of a VDD disturbance is measured in the context of LAr pulses.
- Measured using LAr pulse given to the ADC input while disturbing VDD



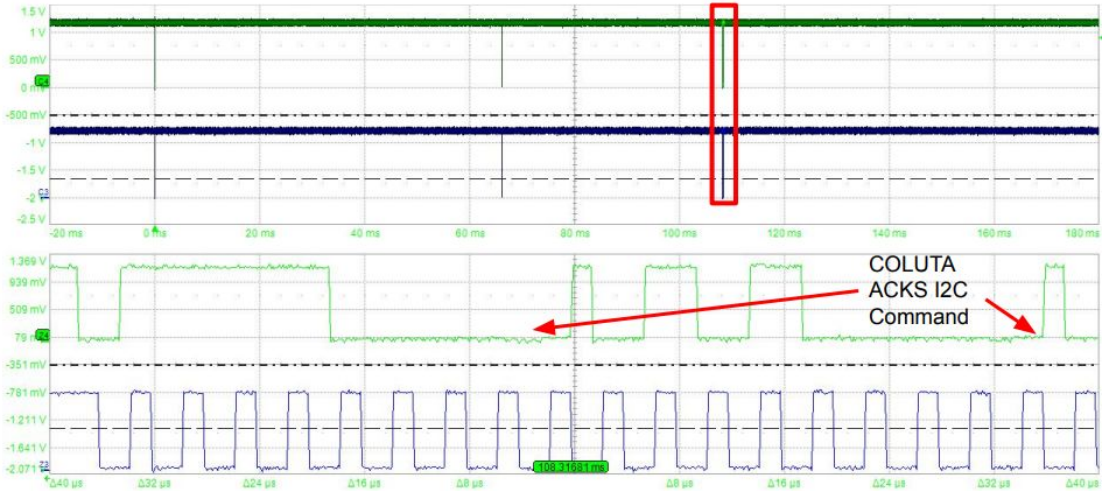


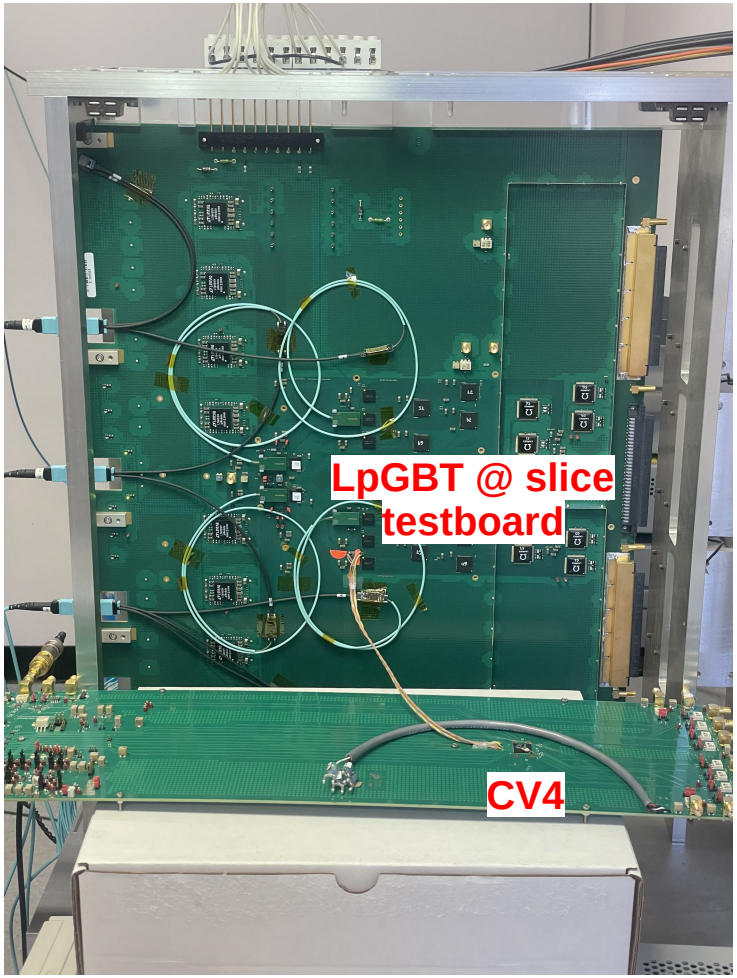
Disturbance on VDD does not significantly degrade energy and timing resolutions; all stay within spec (c.f. 0.25% σ_E/E and 100 pS)

I²C Reliability

- Tested by using an lpGBT as the I²C bus master
- 1.2M I²C transactions sent by lpGBT were successfully understood by the CV4
- I²C state machine in CV4 successfully recovers from false starts

I2C Write Command AFTER I2C False Start

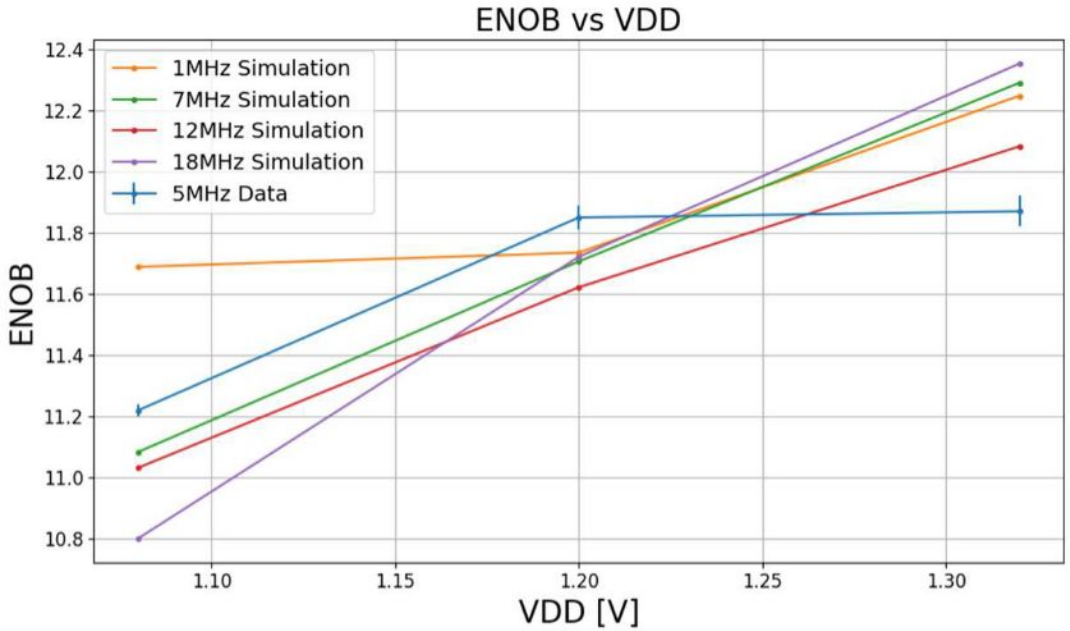




The lpGBT + CV4 I²C interface is robust.

Stress Testing: VDD

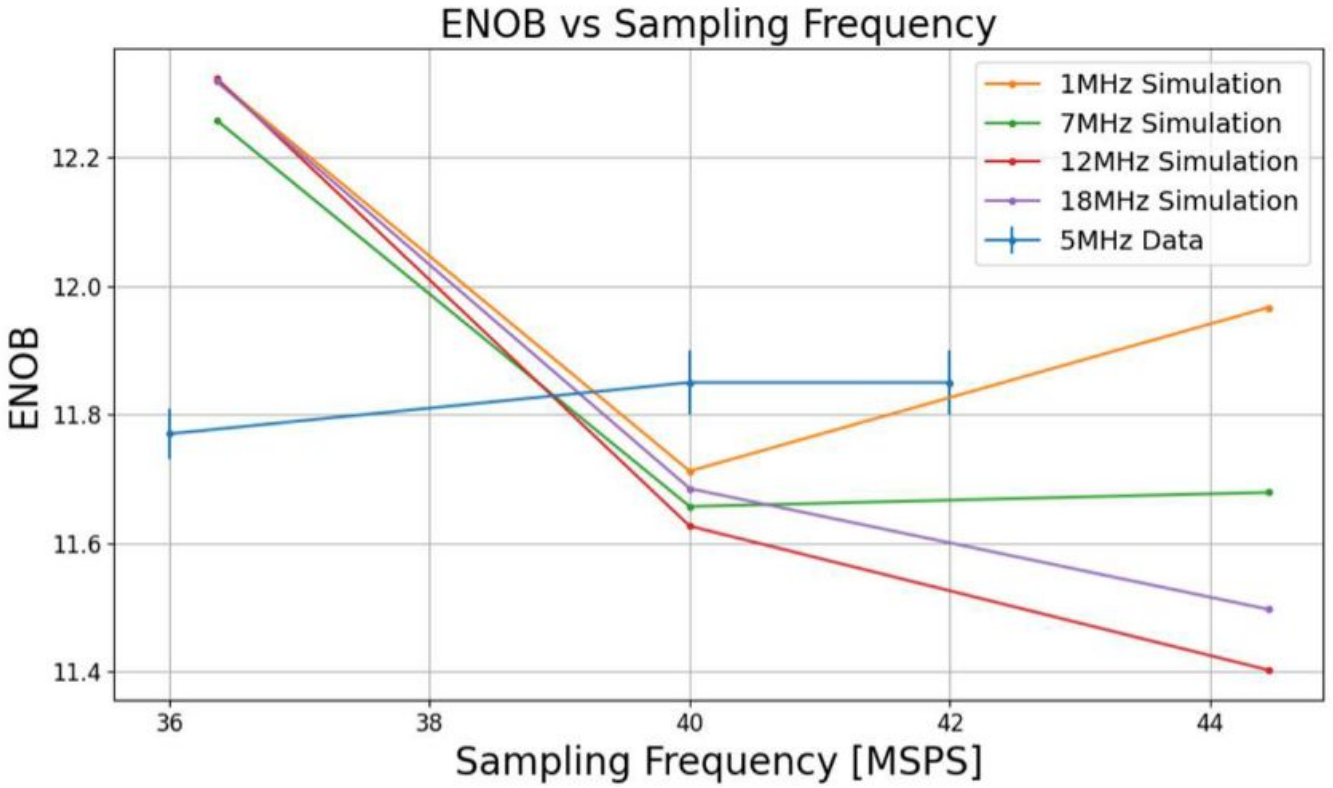
- Robustness and operating margins also part of verification strategy, in addition to nominal performance
- On-chip references designed to maintain fixed dropout w.r.t VDD
  - FEB2 and PA/S + CV4 interface designed with this implication in mind.



CV4 analog performance meets ENOB spec across ±10% VDD variation (c.f. VDD = 1.2 ±10% V)

Stress Testing: Samp. Frequency

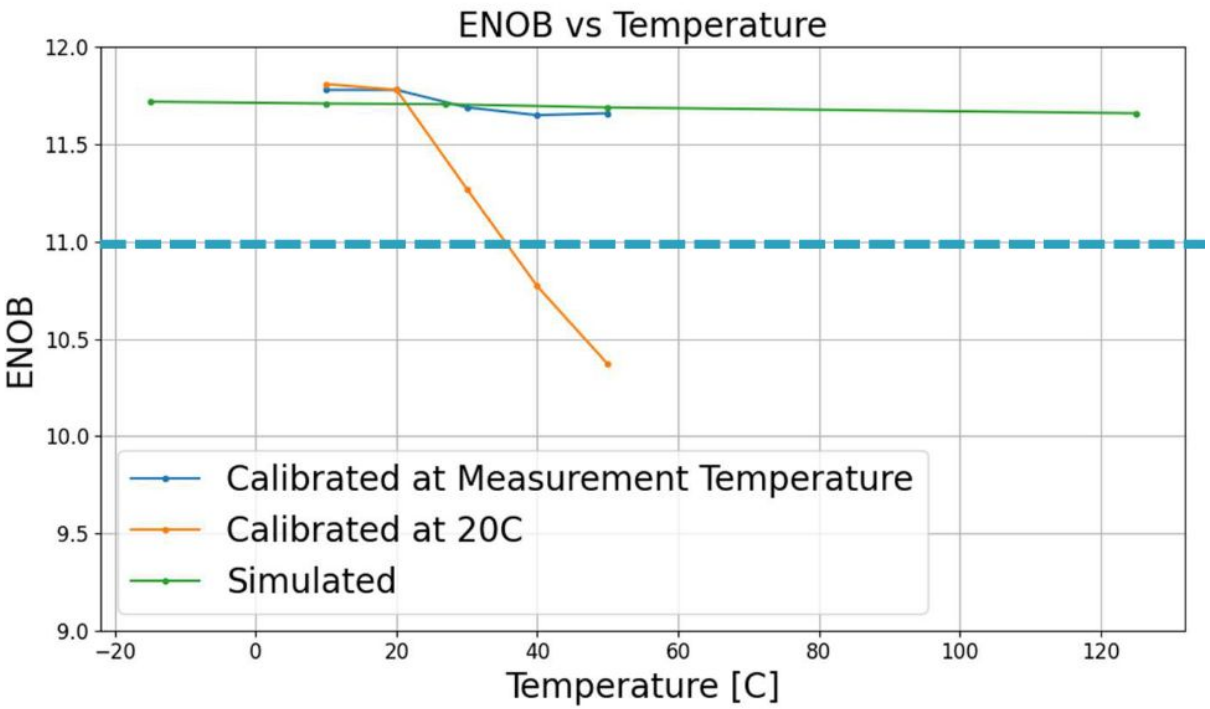
- CV4 is validated across sampling frequency margin
- Test board FPGA limitation prohibits testing faster than 42 MSPS.



CV4 maintains performance across sampling frequency margin specification of 40 MSPS ± 10%

Stress Testing: Temperature

- CV4 will be water-cooled to near room temp., however the junction temperature will be warmer



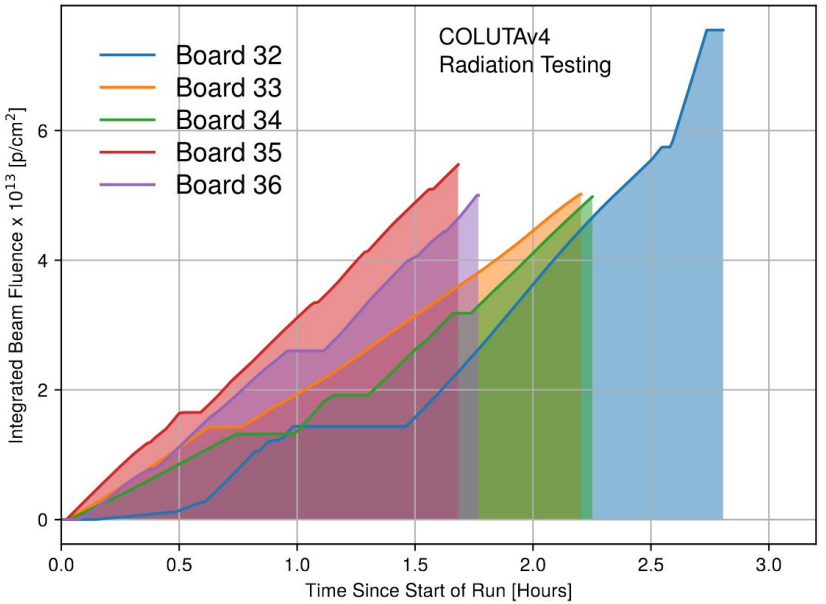
CV4 maintains performance across temperature specification of 10 – 50 degC, given calibration is performed at a particular temperature.
CV4 is performant between 10 – 30 degC when calibrated at 20 degC.

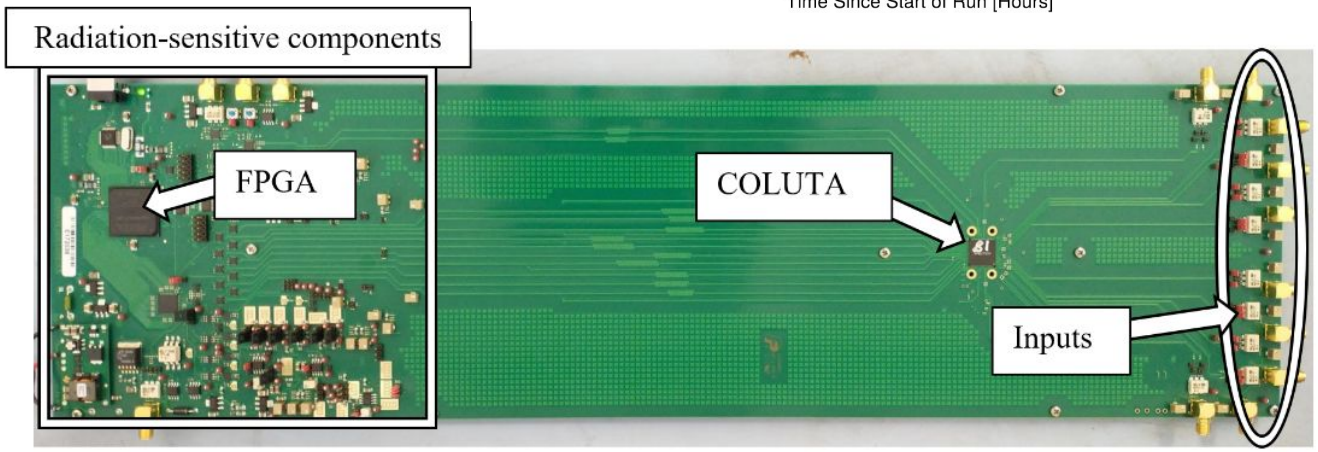
Radiation Test Setup

- Elongated and 8-ch passive input version of the precision test board
- Irradiation at Boston Massachusetts General Hospital using 229 MeV proton beam
- Irradiated five chips beyond spec (~5 x 10^{13} p/cm^2) with **no chip latch-ups**
- Real-time data monitoring/acquisition and beam control
  - Accurate counting of dose from the beamline

	TID $[Gy]$	NEIL $[n_{eq}/cm^2]$	**SEE** $[h_{>20Mev}/cm^2]$
ASIC	4100	4.1×10^{13}	1.0×10^{13}

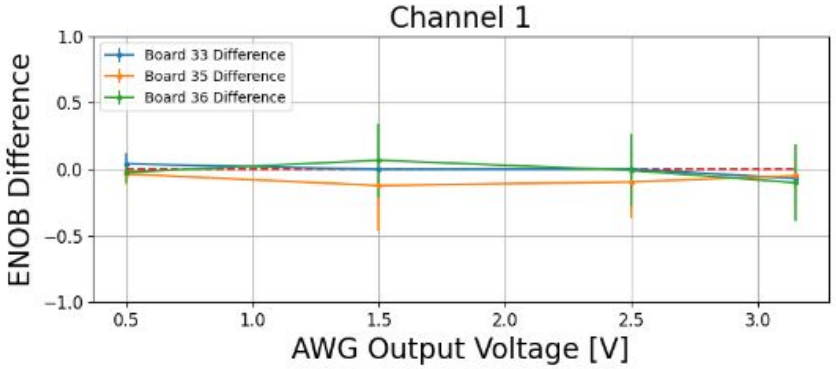
TID requirement was actually 1.4 kGy after the fact …

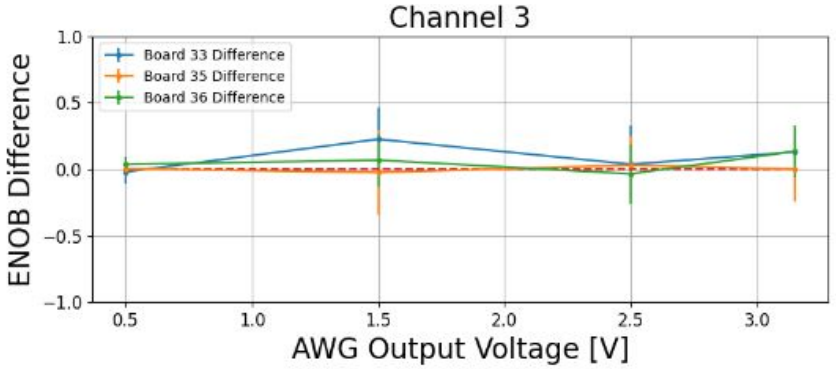


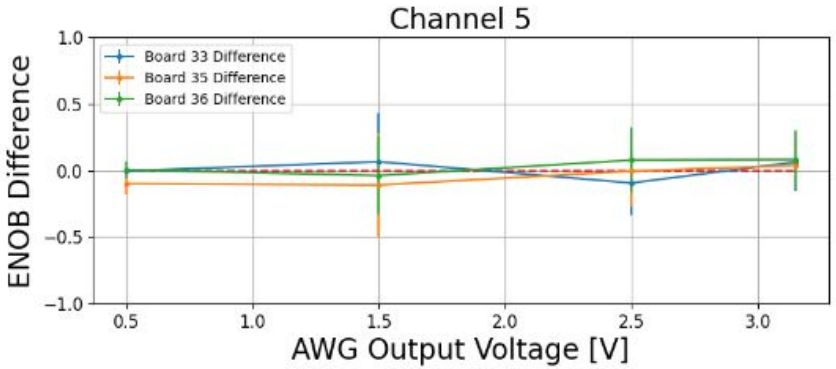


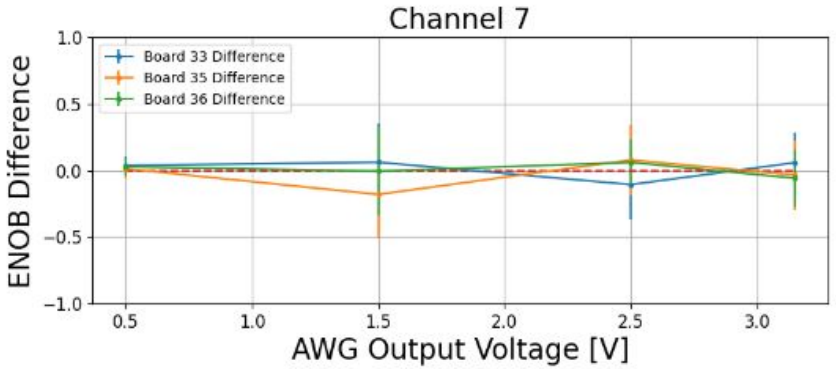
TID Sensitivity

- TID measured by calibration and quantizing a sine wave before and after irradiation







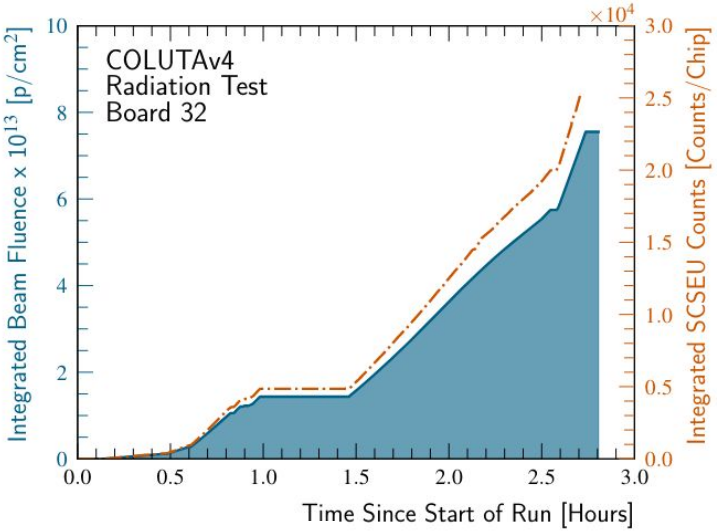


CV4 analog performance does not degrade over the total irradiated dose and remained ≥ 11 ENOB.

TID Sensitivity (cont.)

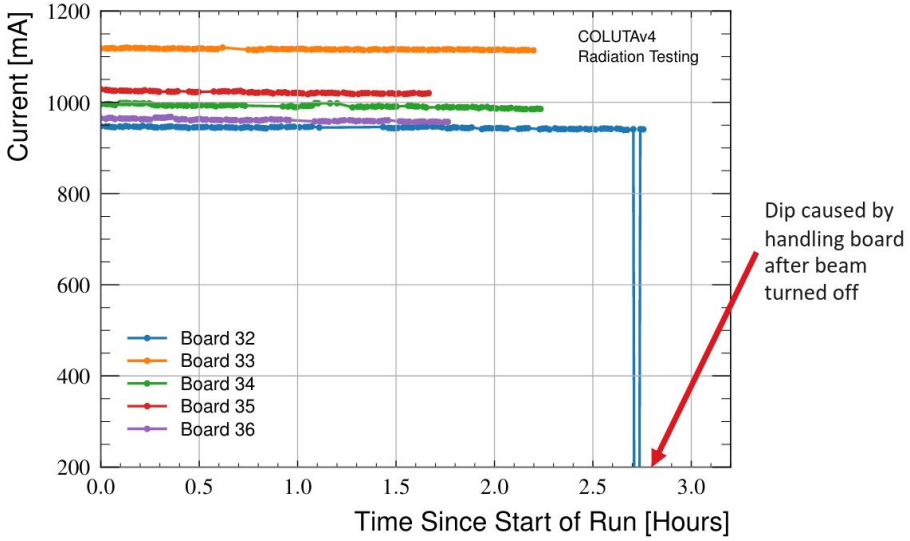
- General chip health (power draw, temperature, etc) stable throughout total dose

Proton dose as observed by beamline instruments

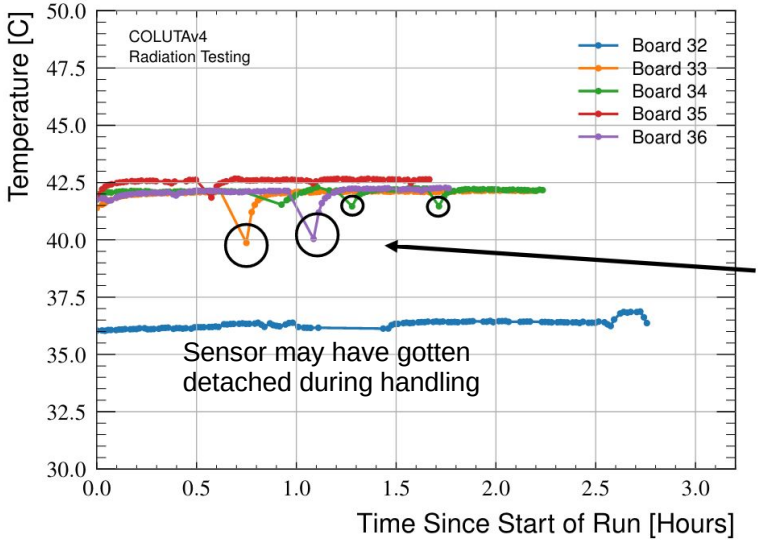


Number of single-DFF corruptions.

(These errors are TMR-corrected hence they do not impact the chip operation)



Dip caused by handling board after beam turned off



Dips caused by combination of pauses in beam and board reconfigurations

SEE Sensitivity

- Slow-control settings read out every ≤ 5 minutes to validate chip state during beam.
  - If slow-control is corrupted: re-configure chip and discard recorded data
  - Over the entire irradiation test, 11 TMR corruptions were observed

Chip	$\sigma_{\text{config. bit}}$ [cm^2]	Uncertainty [cm^2]
COLUTAv3	2.39×10^{-15}	$\pm 0.47 \times 10^{-15}$
COLUTAv4	8.76×10^{-18}	$\pm 2.64 \times 10^{-18}$

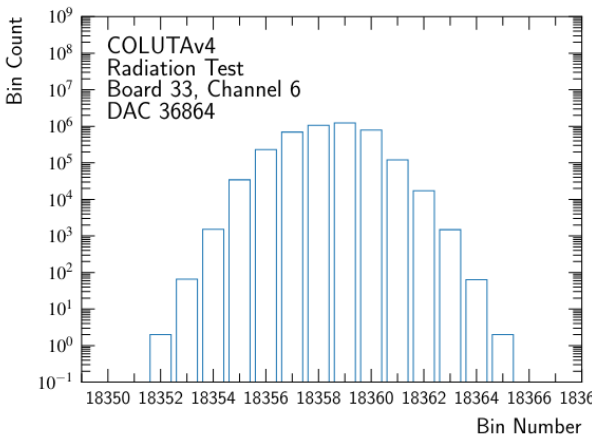
Observed single DFF corruption $\sigma = (3.08 \pm 0.01) \times 10^{-10}$ cm^2

- CV3 observed higher than expected rates of TMR corruption
- CV4 improved on CV3 slow-control by *spacing apart* TMR'd DFF's (≥ 15 µm)
  - Observe a ~270 times lower cross-section than CV3

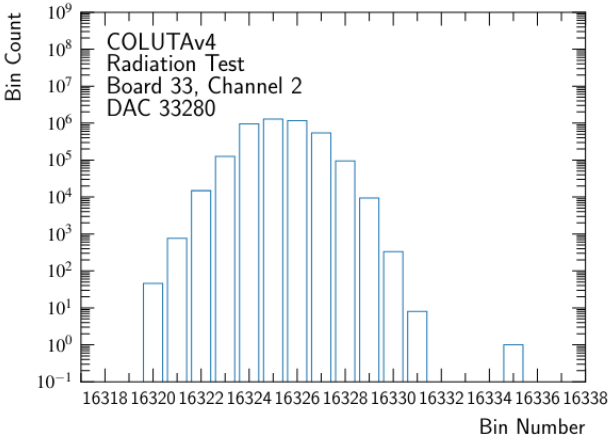
Over the course of the HL-LHC, we expect a 10% chance that one LAr channel (two ADC channels) suffer one slow-control bit corruption

SEE Sensitivity (cont.)

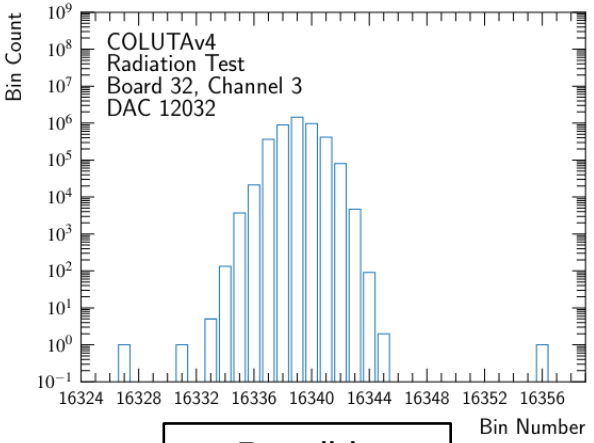
- SEE measured by having ADC quantize a slow DAC ramp and histogramming the CV4 digitized output.
  - Exercise as much of the code range as possible
  - Each histogram captures 2^{22} (~4.2M) consecutive samples
  - SEU defined as a hit that is >2 counts away from the noise edge
  - Extensive dry-run data collected pre-irradiation as a controlled comparison



No SEU



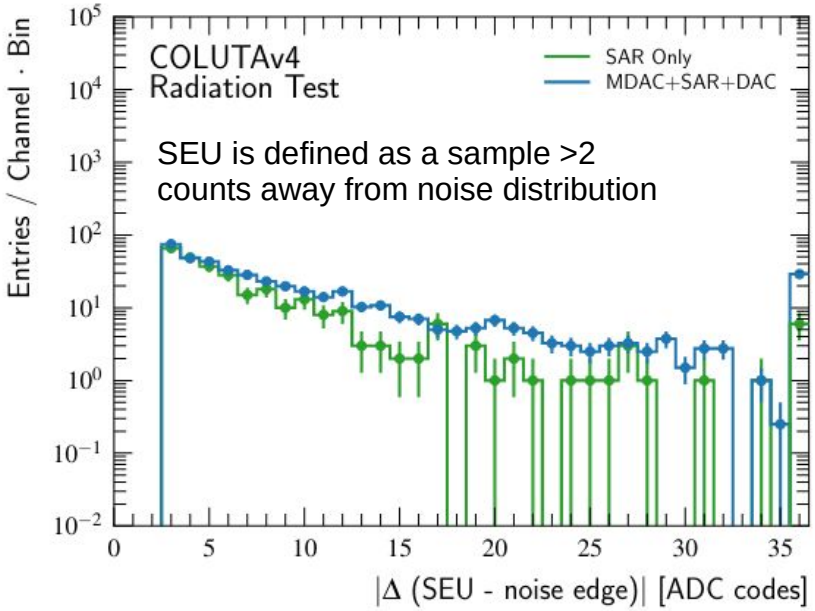
Possible SEU

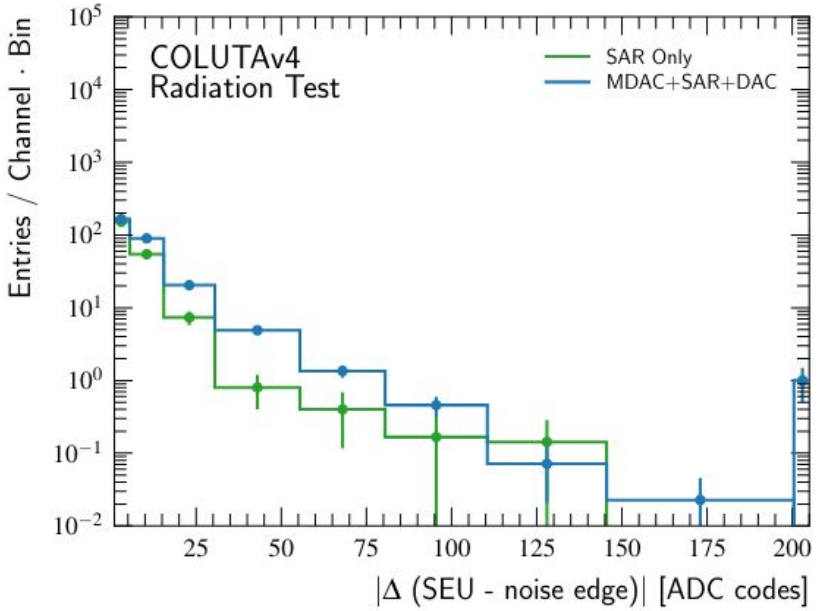


Possible multiple SEU's

SEE Sensitivity (cont.)

- SEU's *near* the noise distribution are probably "analog" errors
  - E.g. ionizing particle disturbing charge in the S/H capacitors
- SEU's *far* from the noise distribution are probably "digital" errors
  - E.g. ionizing particle flipping a DFF that holds data





Measurement	$\sigma_{SEU} \times 10^{-10}$ [cm^2]
COLUTAv4 $\sigma_{SEU/ch.}$	6.14 ± 0.15

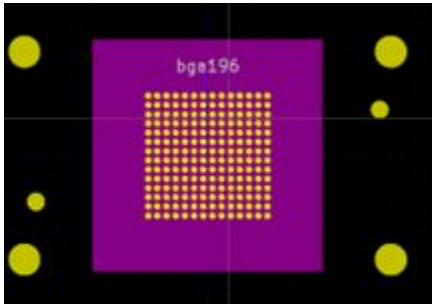
Over the course of the HL-LHC, we expect a total of 6140 SEU's per channel. 75% will be within 20 ADC counts of the correct code; less than 1% will be greater than 100 counts away.

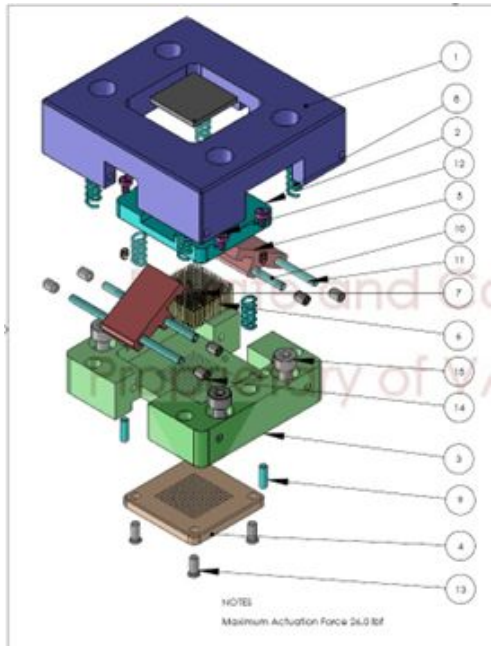
Forward Plans

- Design and development has concluded
  - CV4 has been characterized and understood
  - CV4 integration with the PA/S (ALFE) and lpGBT has been validated
- Currently on-going:
  - BGA packaging
  - Preparing for mass production testing
- Final Design Review: October 7, 2022 (last week!)
- Pre-Production Engineering Run: End of 2022
  - Includes production masks
  - QC testing on pre-production chips
- Production Readiness Review: Summer 2023
- Production and Testing of ~80k chips: 2023 thru 2024

BGA Packaging

- BGA interposer and packaging outsourced to JCET
  - CERN-approved and same vendor used for ALFE PA/S chip
- 196-ball BGA, 12 x 12 mm, 0.8mm ball pitch
  - More pins dedicated to power/ground, less bondwire parasitics
  - Less stringent mechanical tolerance requirements
- Compare this against the current 100-pin 0.4mm pitch QFN:
  - Number of pins limited by package periphery
  - Tighter mechanical tolerances for less pins



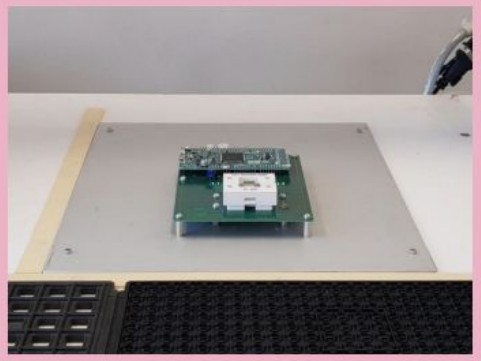


The BGA package offers both electrical and mechanical advantages over the QFN.

Mass Production Testing

- Split effort with UT Austin and University of Paris-Saclay
- Will need to test ~80k chips
- BGA package eases mechanical tolerances → less human intervention

Paris-Saclay



- Existing robotic test setup being prepared for testing
- Initial socket testing studies

Austin

- Assembling robotic arm setup
- Long duration tests checking placement of “dummy” chips

Conclusion

- The readout electronics in the ATLAS LAr calorimeter are being upgraded to meet the HL-LHC requirements
- The radiation requirements motivates an in-house, custom ADC ASIC
  - Close working relationship between both physics and EE departments at Univ. of Texas at Austin and Columbia Univ.
- **COLUTAV4: 8-channel 40 MSPS 11.5-ENOB/15-bit dynamic range ADC**
- Standard CMOS → radiation hardening by design
- FEB2 system → seamless integration with other custom ASIC's in the signal path (ALFE PA/S and lpGBT)
- Validated using standard ADC techniques (sine wave, INL/DNL, etc), integration tests with ALFE PA/S and lpGBT, and radiation tested to specification
- Preparations for BGA packaging, mass production, and mass validation

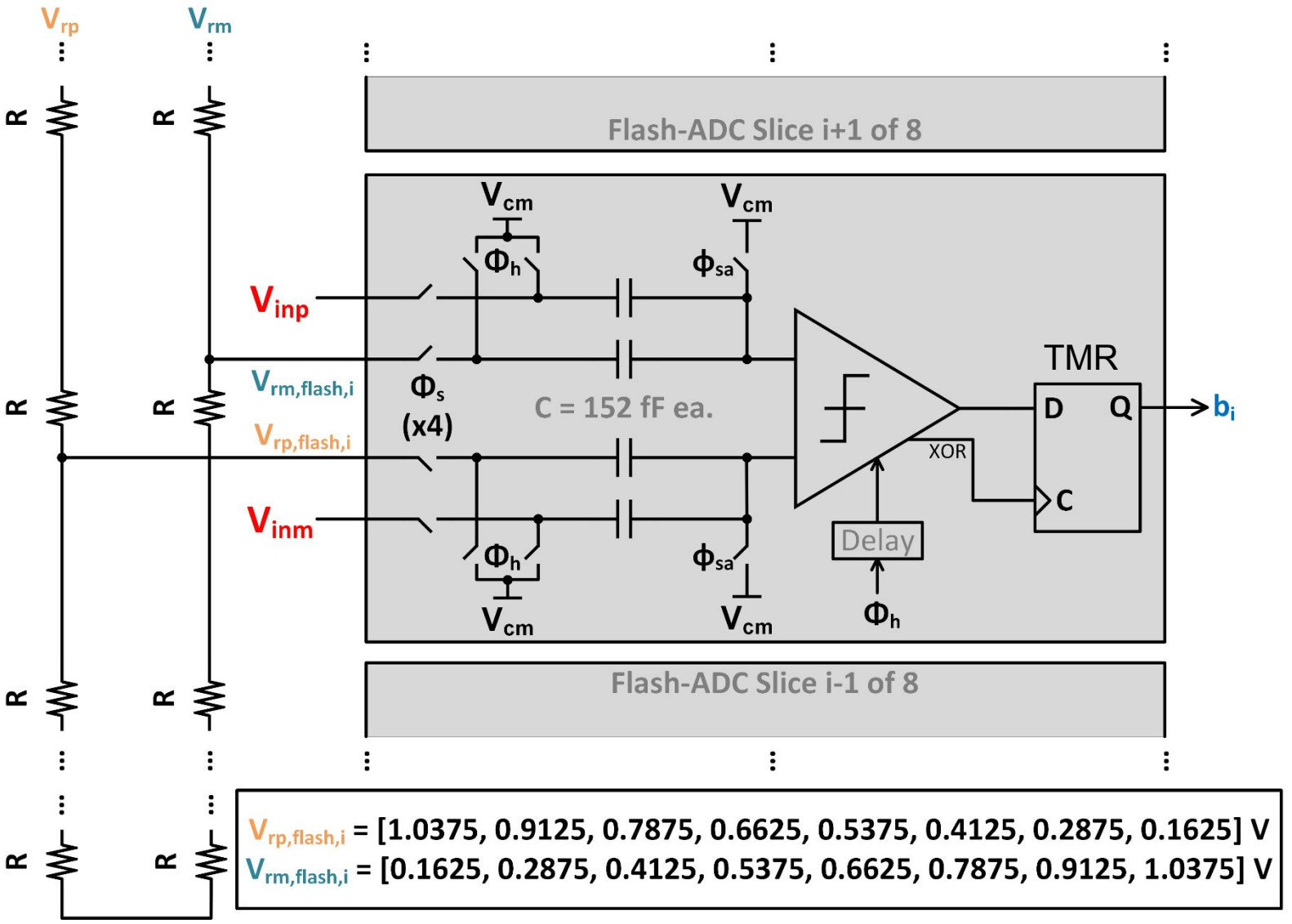
Thank you! Questions?

This research is supported by the US National Science Foundation under Grant No. PHY 1948993, PHY 2013070, and US Department of Energy Grant No. DE-SC0007890

BACKUP

- CV4 Documentation: https://twiki.nevis.columbia.edu/twiki/bin/view/ATLAS/COLUTAv4Testboard
- FEB2 talk @ TWEPP 2022: https://indico.cern.ch/event/1127562/contributions/4904500/
- MDAC
  - Sub-ADC
  - Residue OTA
  - Reference buffers
  - Clock Generator
- SAR
  - Asynchronous vs. Synchronous
  - Comparator
  - Residue Amplifier
  - TMR
- Radiation Analysis
  - Dose equivalence
  - Cross Section Calculations

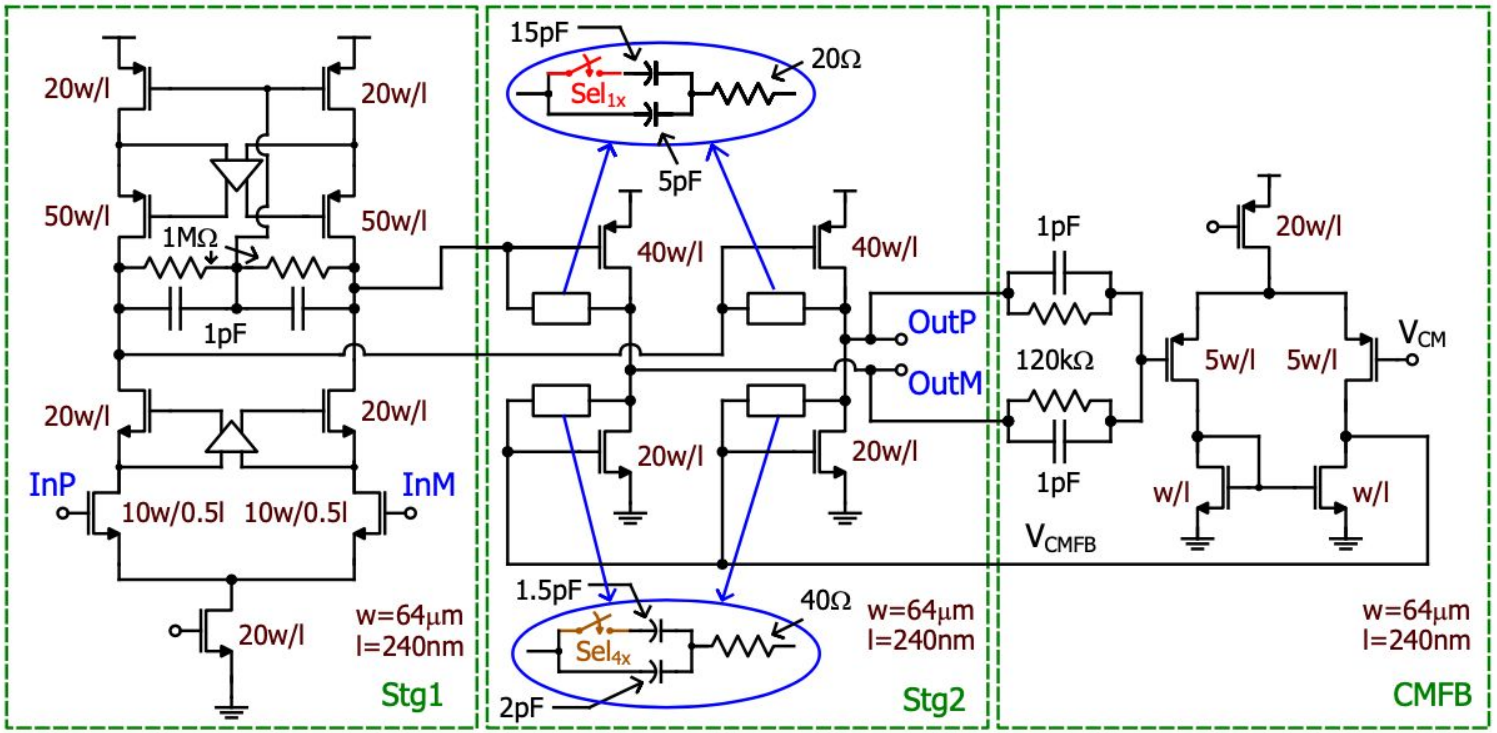
MDAC: Sub-ADC



$V_{rp,flash,i}$ = [1.0375, 0.9125, 0.7875, 0.6625, 0.5375, 0.4125, 0.2875, 0.1625] V

$V_{rm,flash,i}$ = [0.1625, 0.2875, 0.4125, 0.5375, 0.6625, 0.7875, 0.9125, 1.0375] V

MDAC: Residue OTA

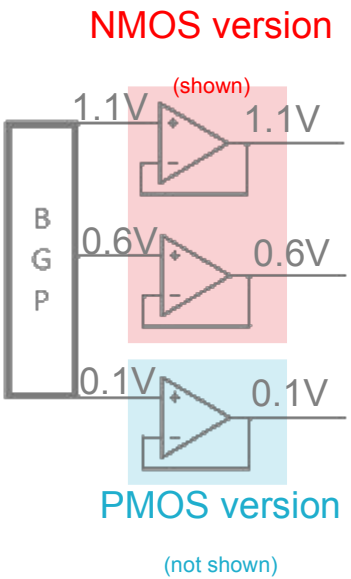


Two-Stage Gain-Boosted Telescopic Miller-Compensated OTA	
Gain (open-loop)	90 dB
Bandwidth (unity-gain)	300 MHz
Power	24mW

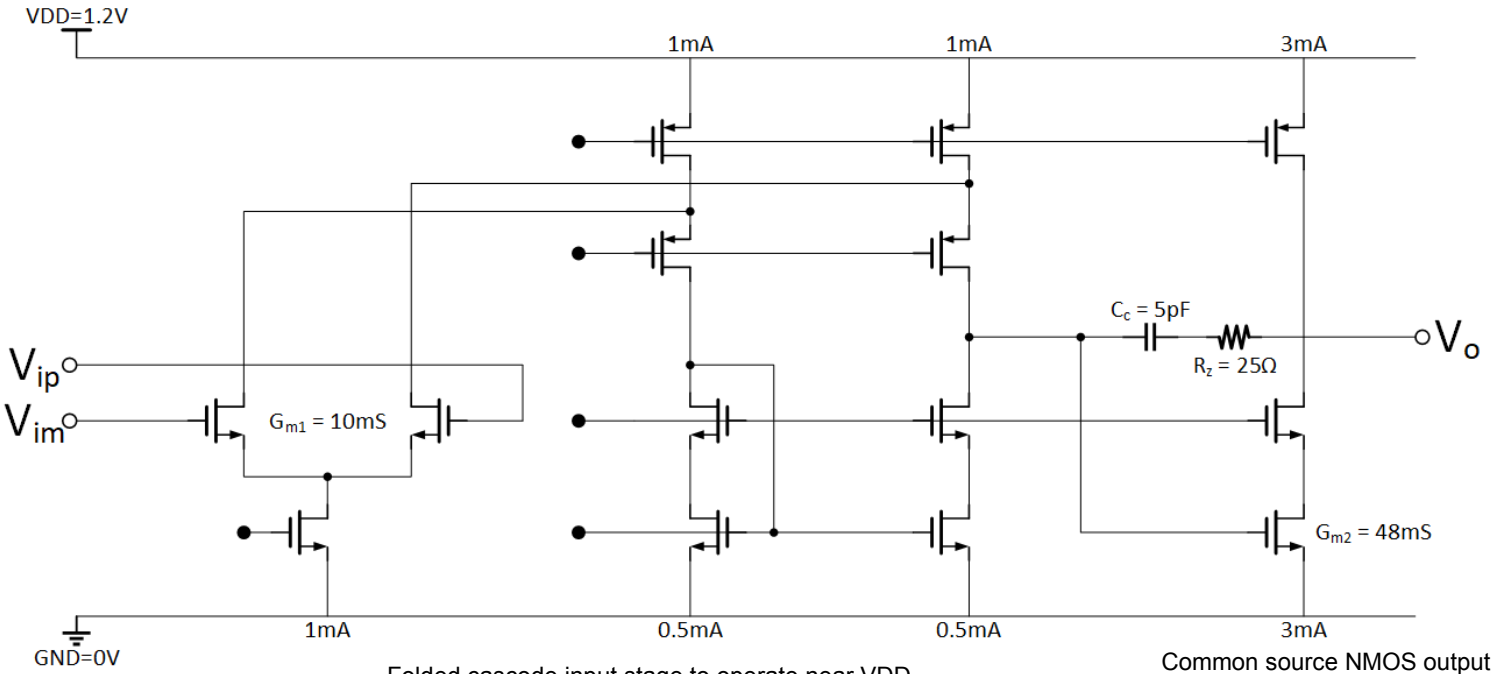
OTA for Residue Amplifier

- Operational Transconductance Amplifier (1.2V)
  - Gain boosted two-stage Miller-compensated topology
  - Using mostly LVT devices → smaller V_{GS}
  - Large output swing, centered around $V_{DD}/2$
  - Input Common-mode at $V_{DD}/2$
- Open-loop DC gain > 90dB
  - Guarantees no amplifier errors when in 4x configuration with ¼ feedback factor → loop gain still 86dB
  - L = 2 or 4 x L_{min} → larger DC Gain
  - Gain-boosting in first stage
- Differential Mode BW
  - Sel1x=0 for MDAC → UGB >= 300MHz
- CMFB
  - Local CMFB first stage → controls current second stage
  - 50dB CMFB amplifier for second stage, compensated with 3.5pF (sel4x=1)

MDAC: Reference Buffers



Bias circuits not shown

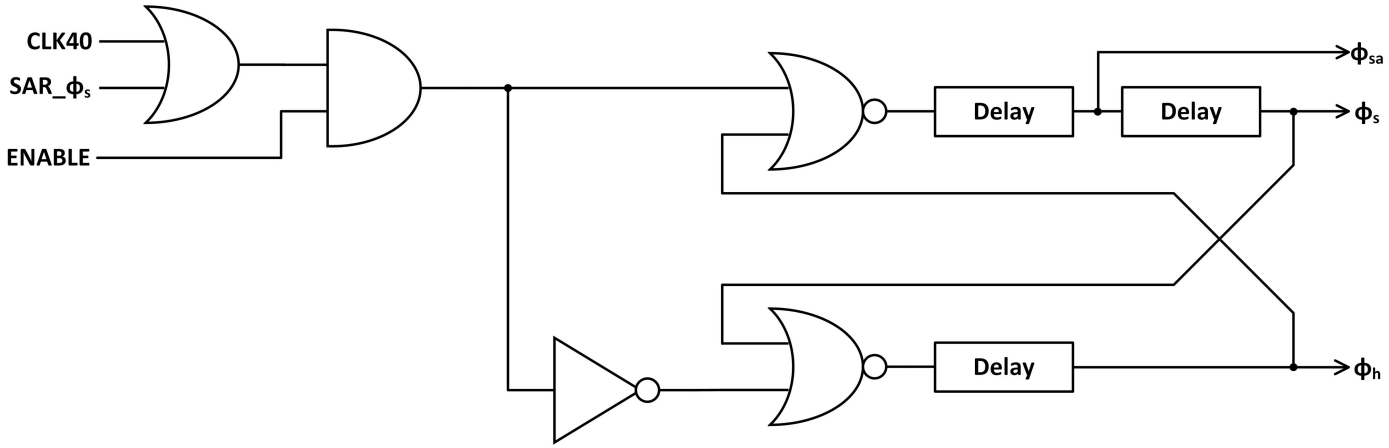


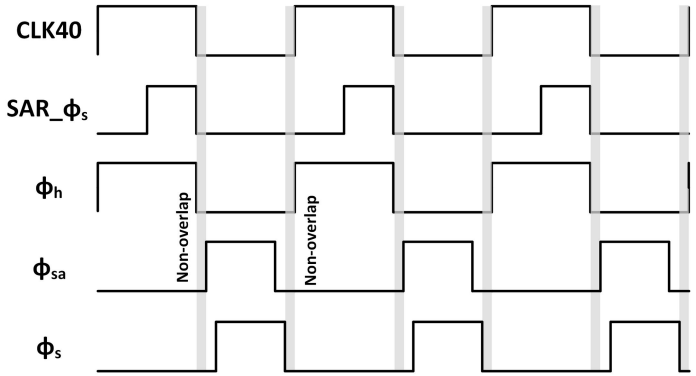
Folded cascode input stage to operate near VDD

Common source NMOS output stage to operate near VDD

Two-Stage Folded Cascode Miller-Compensated OTA in Unity-Gain Negative Feedback	
Power (per buffer)	7.8 mW
Gain (open-loop)	40 dB
Bandwidth (unity-gain)	170 MHz
Time to settle to 14-bit precision (for 8pF load)	9.7 ns

MDAC: Clock Generation





input

sample SAR

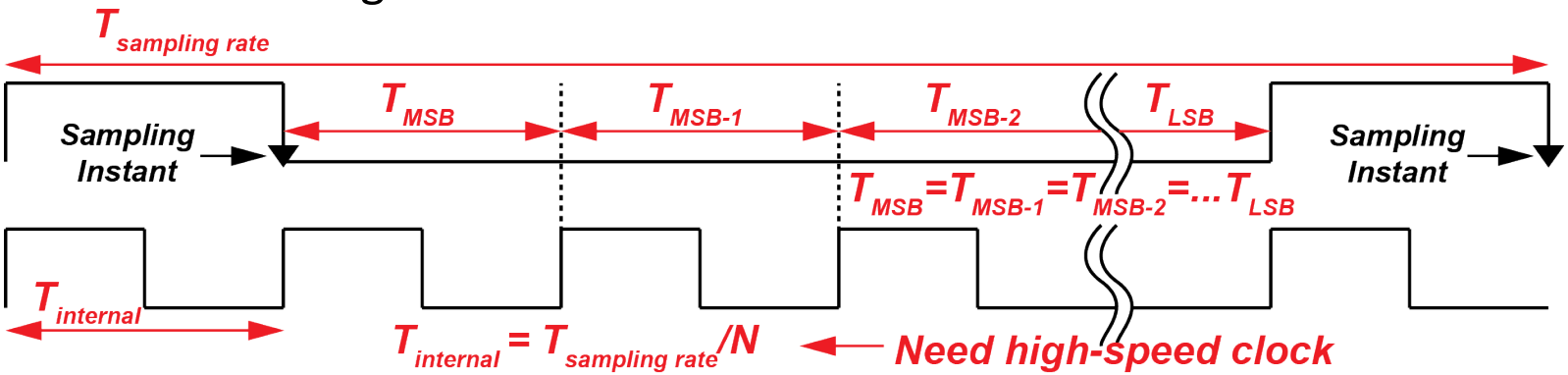
hold = residue calc.

sample advanced

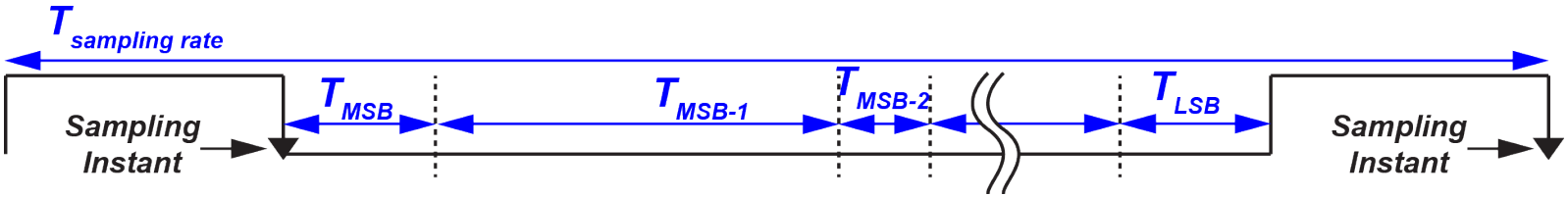
sample

SAR: Asynchronous vs. Synchronous

- SAR ADC does a handful of bit trials.
- Synchronous SAR ADC:
  - Each trial is given the same amount of time.

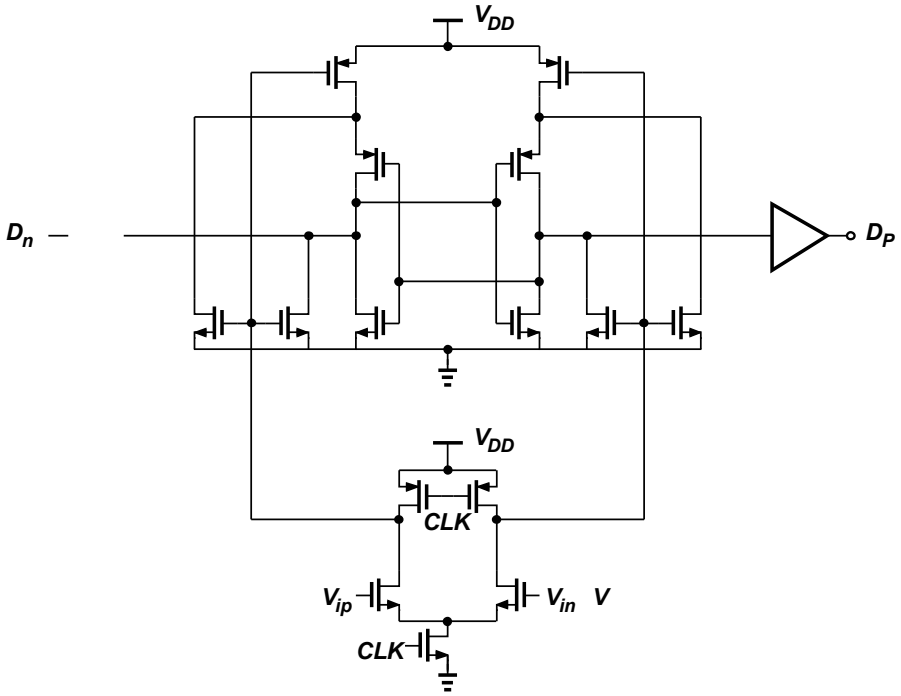


- Asynchronous SAR ADC:
  - Assign amount of time based on the time needed for each bit trial.

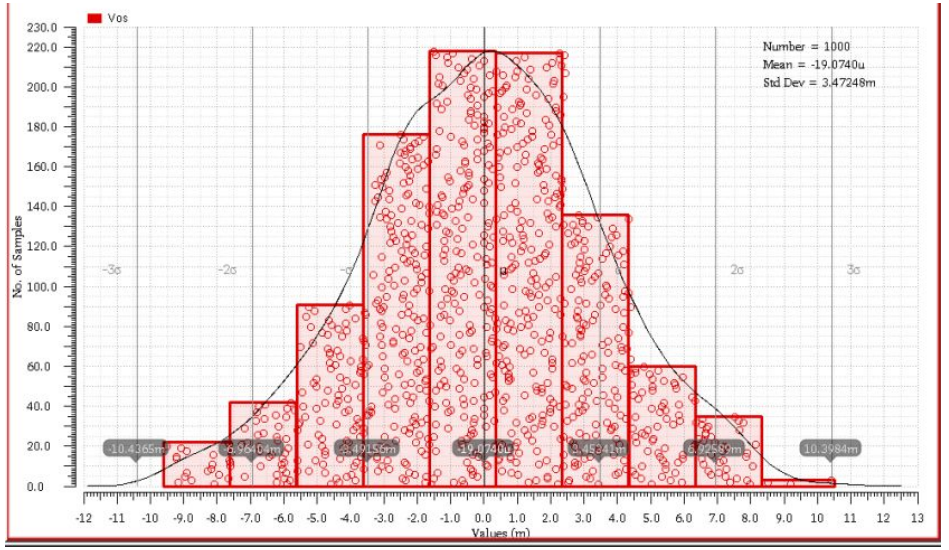


  - Avoid high-speed clock
  - Self-timing can ensure more time for metastability bit

SAR: Comparator

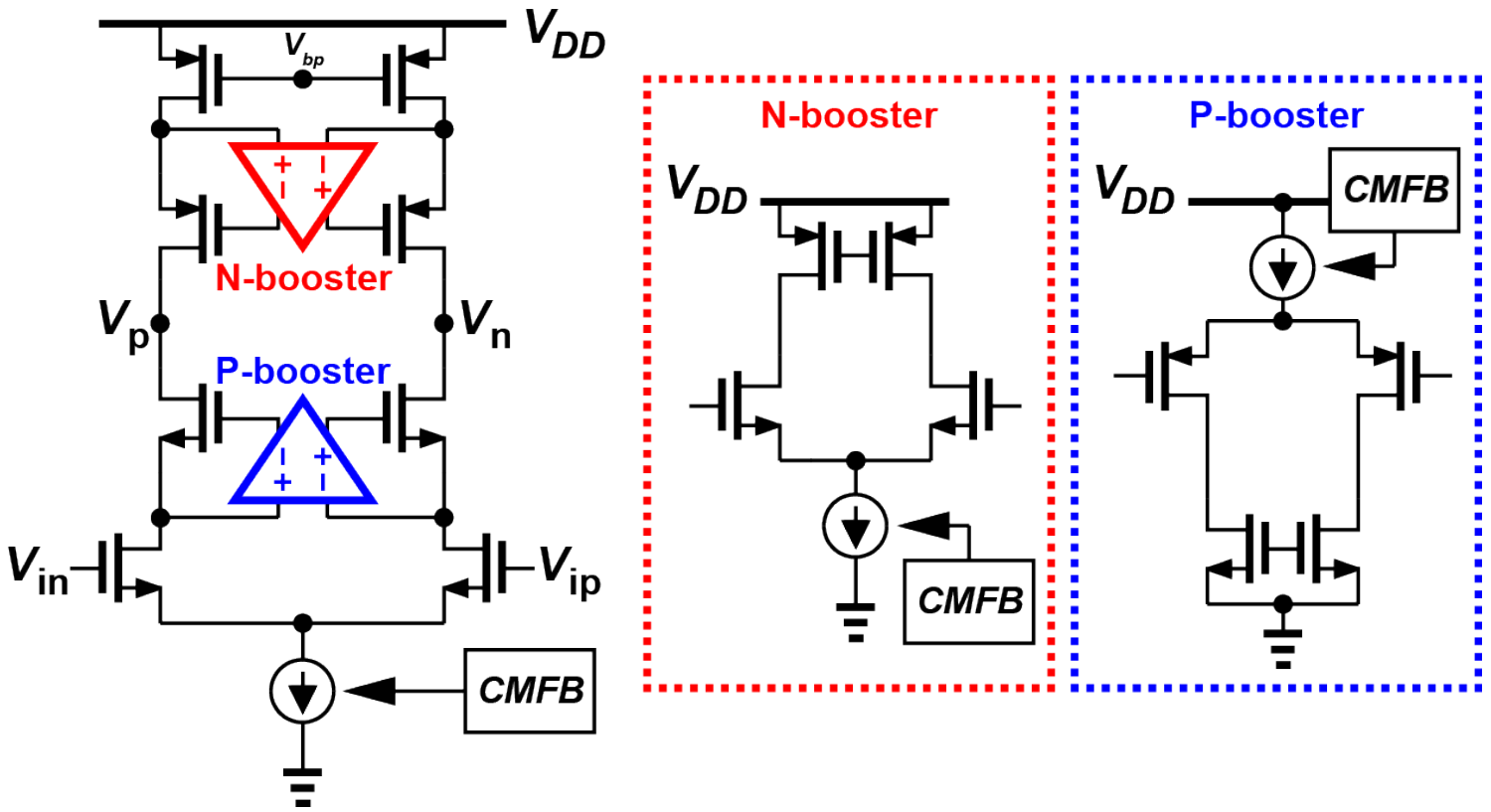


Monte-Carlo Simulation for Offset



	Value
Simulated offset (σ)	3.4mV
Simulated noise	300uV$_{RMS}$

SAR: Residue Amplifier

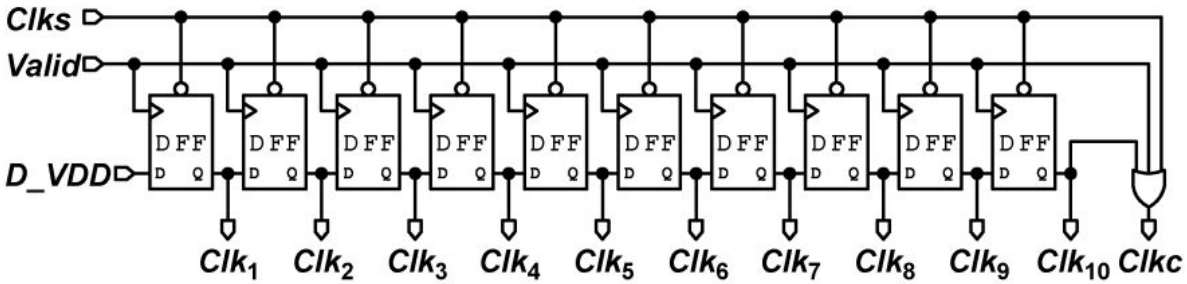


Gain-Boosted Telescopic Fully Differential Amplifier	
Required Output Swing (s/e)	$V_{DD}/8$
Gain (open-loop)	66 dB
Bandwidth (unity-gain)	7 GHz

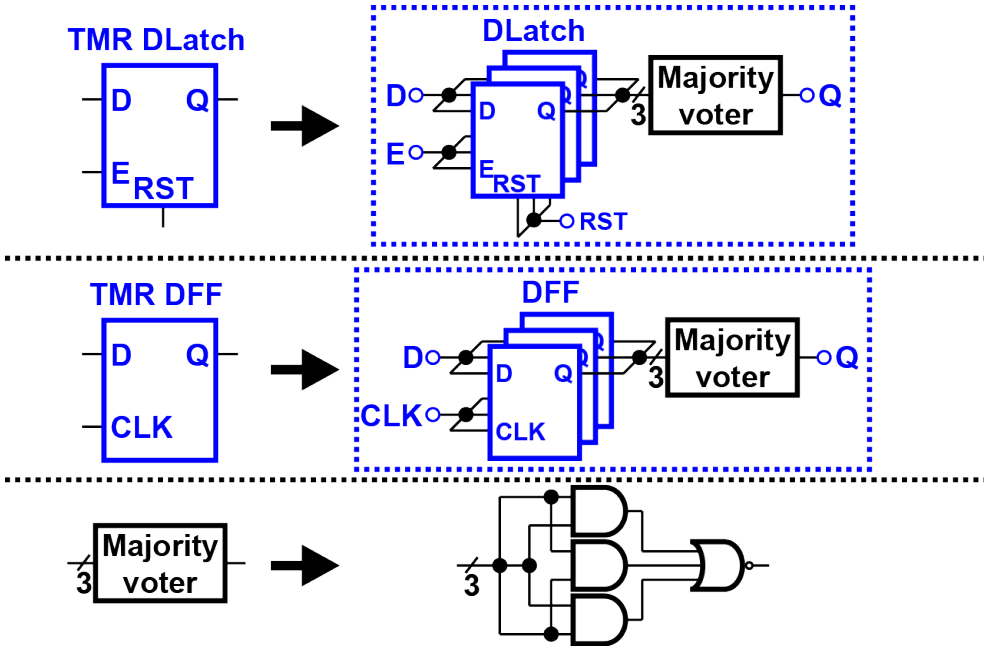
SAR: TMR

All DFF, latches and registers in SAR are TMR protected

- Asynchronous SAR logic:



- Calibration control uses lots of DLatches:



Radiation: Dose Equivalence

- For a charged particle, the fluence required to get the TID of 1 Gy in Si:

$$1\mathrm{Gy} = \frac{1.453 \times 10^{10}\ \mathrm{cm}^{-2}}{\langle dE/dx \rangle\ /1\ \mathrm{MeV/cm}}$$

- For 225 MeV protons, $\left\langle \frac{dE}{dx} \right\rangle = 7.87\ \frac{\mathrm{MeV}}{\mathrm{cm}}$
- Thus, $1\mathrm{Gy} = 1.85 \times 10^{9}\ \mathrm{p/cm}^2$
- NIEL factor is very close to 1 for ~200 MeV protons.
- The NIEL damage for a proton at 225 MeV is $0.95\ \mathrm{n}_{eq}/\mathrm{cm}^2$

Courtesy of Sven Menke

Radiation: Cross Section Calculations

- **SEU cross section:**

$$\sigma_{SEU/channel} = \frac{\#\,SEUs}{\#channels \times protons/cm^2 \times LiveFraction_{Hist} \times LiveFraction_{time}}$$

- **Histogram live fraction:**

$$LiveFraction_{hist} = \frac{total\ \#\ Hists\ -\ MDAC\ transitions\ Hists\ -\ i2c\ readback\ failures\ Hists}{total\ \#\ of\ Histograms}$$

- **Live time:**

$$LiveFraction_{time} = \frac{total\ \#\ Hists\ \times 2^{22}}{40\ MHz \times total\ beam\ time}$$

- **Uncertainty:**

$$\frac{\sqrt{\#SEUs}}{protons/cm^2 \times LiveFraction_{Hist} \times LiveFraction_{time}}$$