HGCAL at Minnesota

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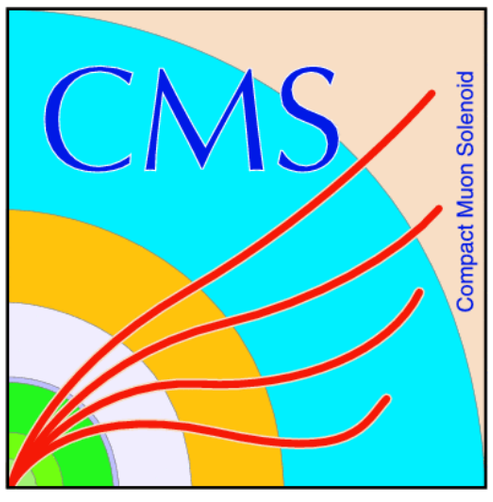
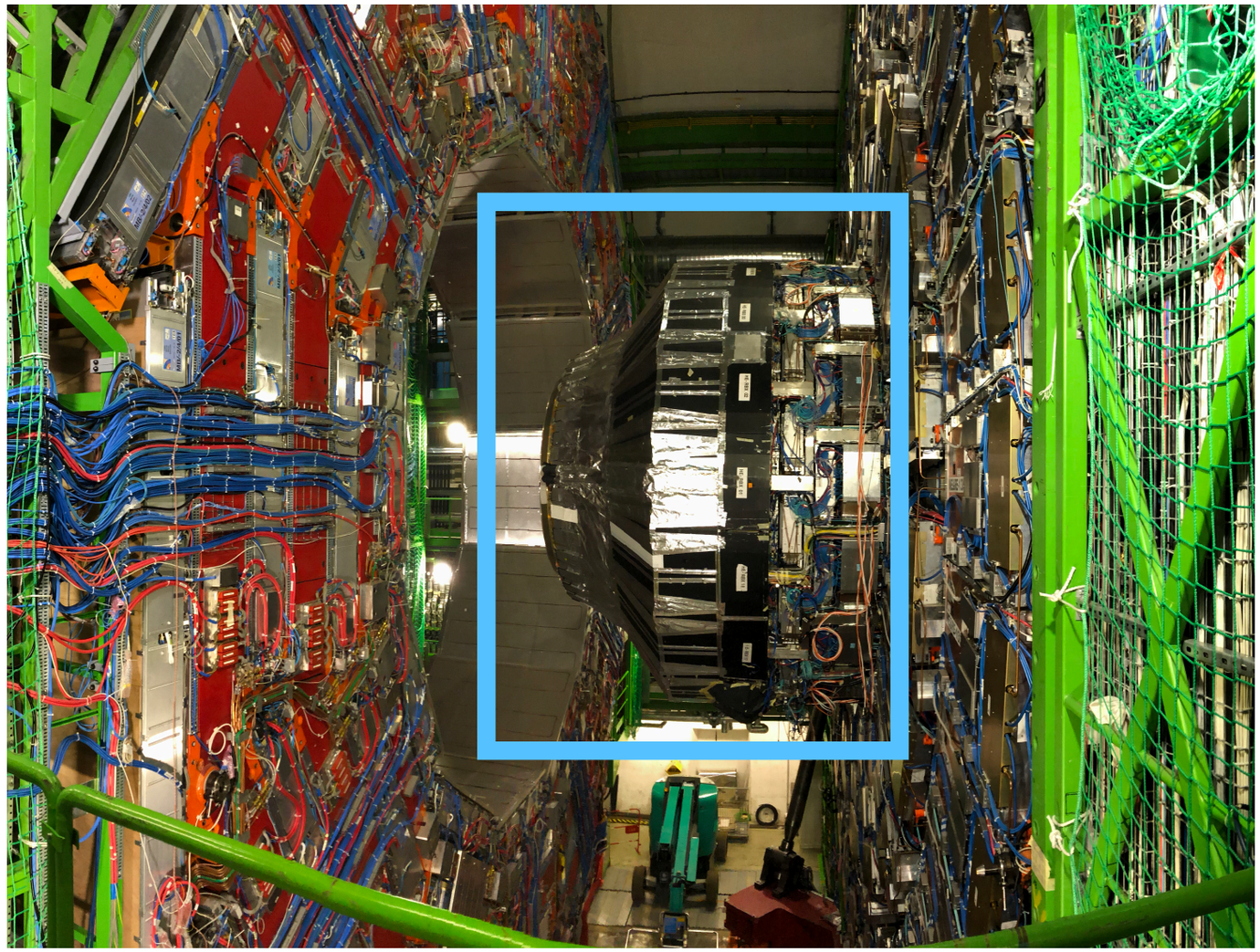
2021/8/16



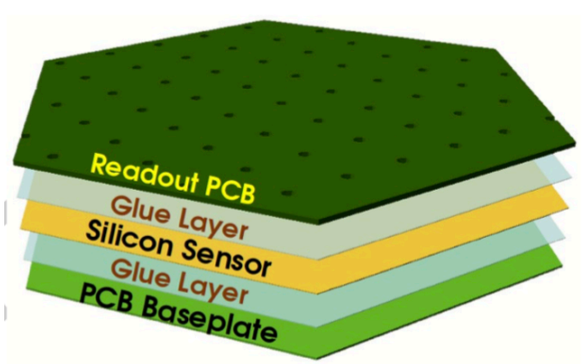
Motivation for replacing the endcap calorimeter

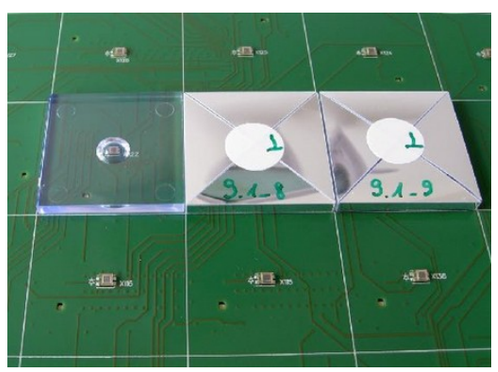
- Radiation-induced darkening is reducing the signal from the current scintillator-based endcap calorimeters
  - Up to 90% signal loss expected
  - HL-LHC will require good operation with radiation loads 10-20x higher
- Need smaller cell sizes to handle large pileup of 200 interactions/crossing

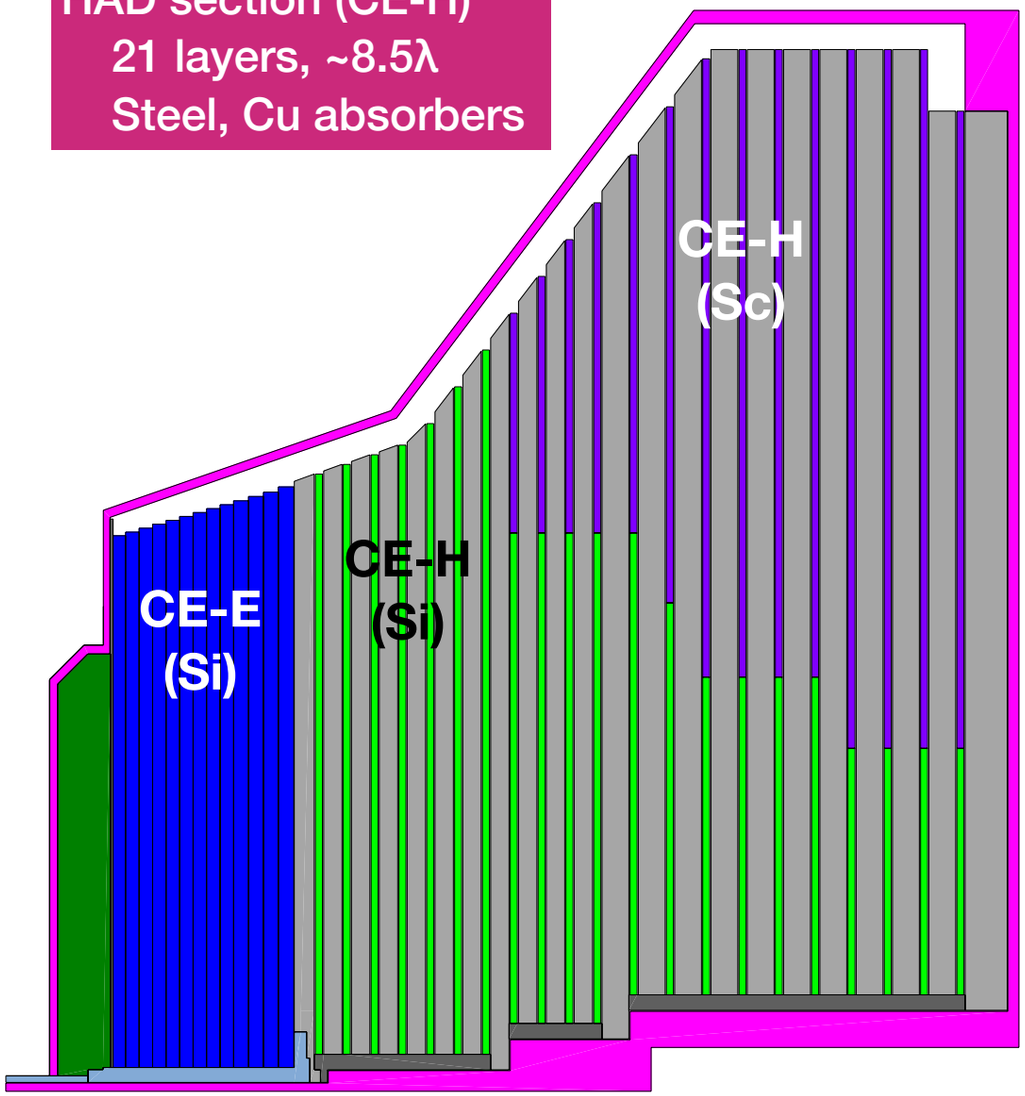


Detector design

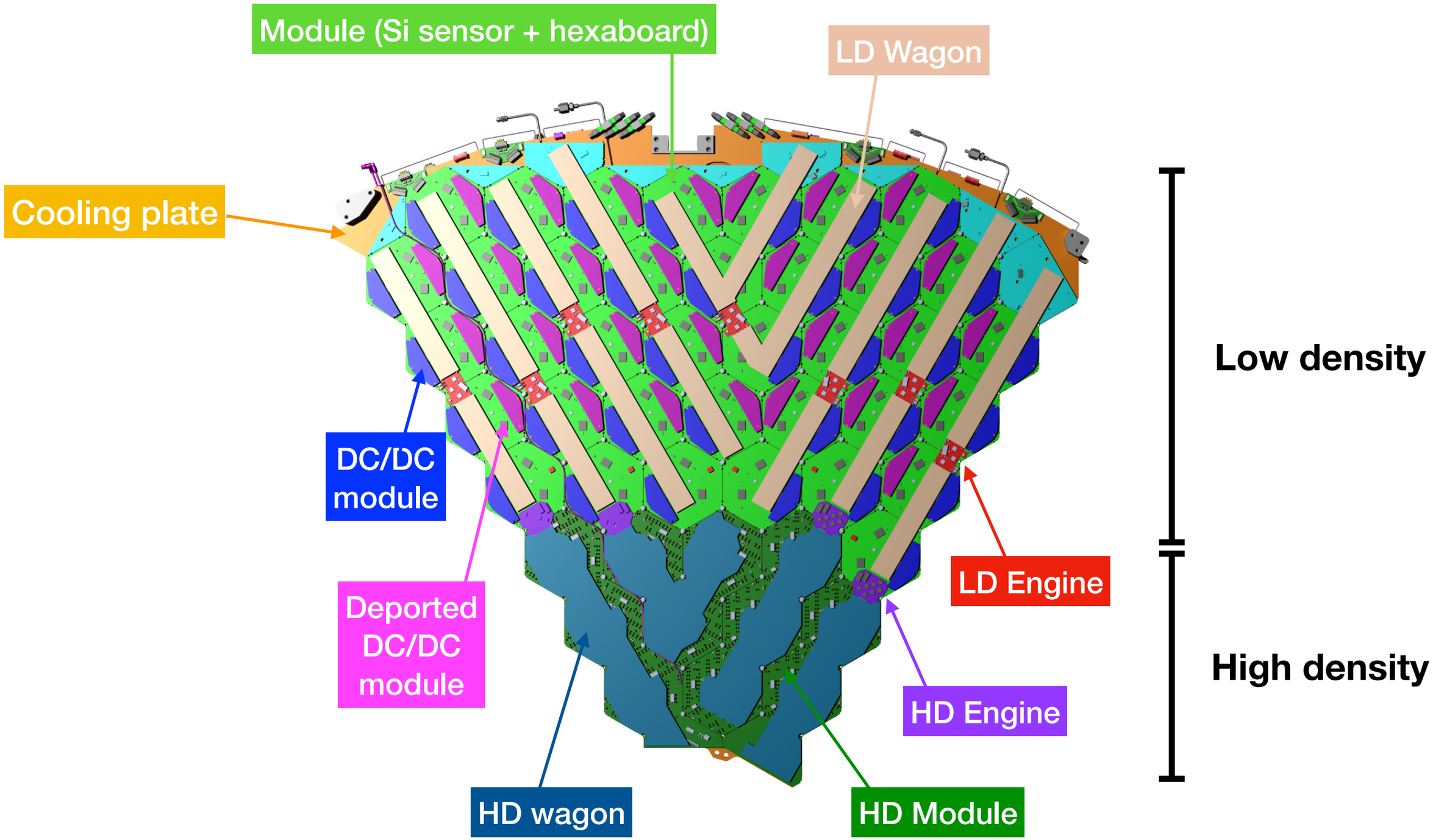
- Active Elements:
  - Hexagonal modules based on Si sensors in CE-E and high-radiation regions of CE-H
  - Scintillating tiles with SiPM readout in low-radiation regions of CE-H
- "Cassettes": multiple modules mounted on cooling plates with electronics and absorbers
- Key Parameters:
  - 215 ton/endcap, full system at -30°C
  - 620 m^2 of silicon sensors in 30k modules
    - 6M Si channels, 0.5 or 1 cm^2 cell size
  - 400 m^2 of scintillator in 4k boards
    - 240k sc. channels, 4-30 cm^2 cell size



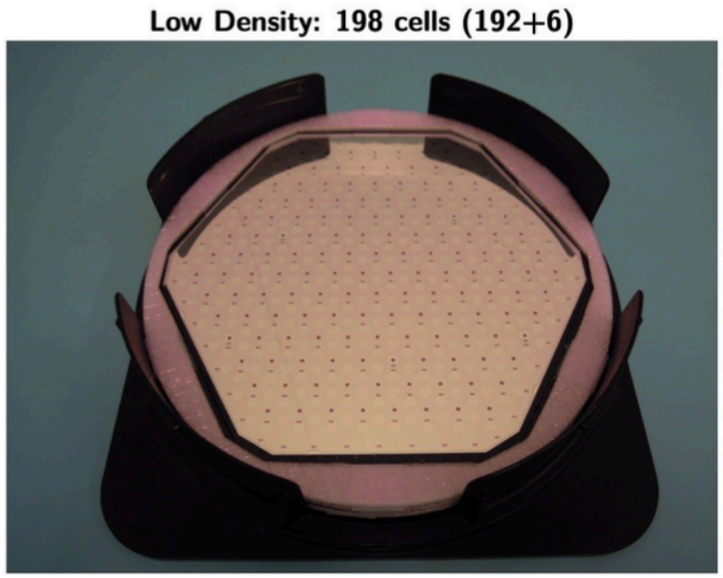




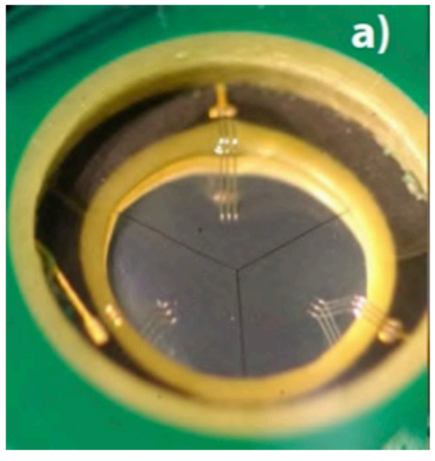
Silicon cassette components

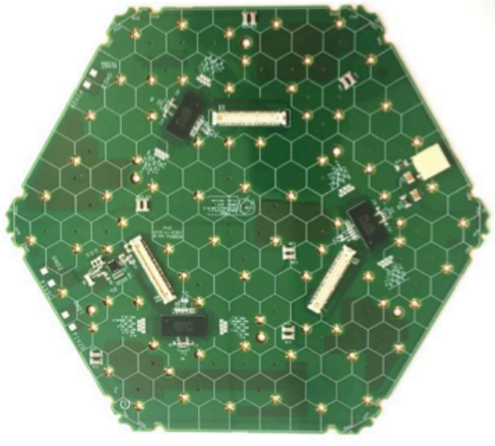


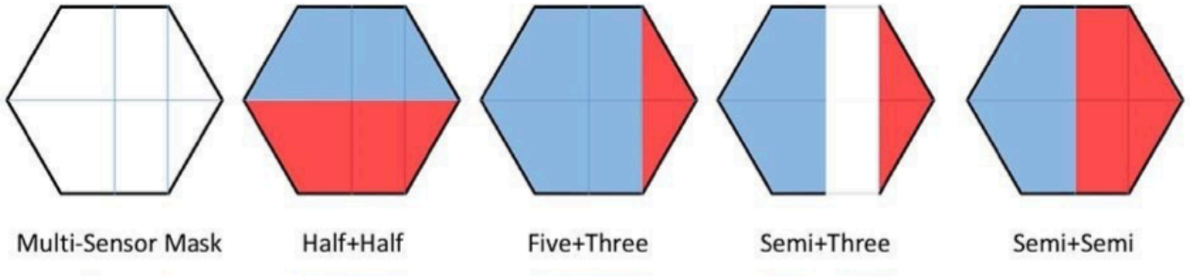
Silicon sensors: forming a circle with hexagons

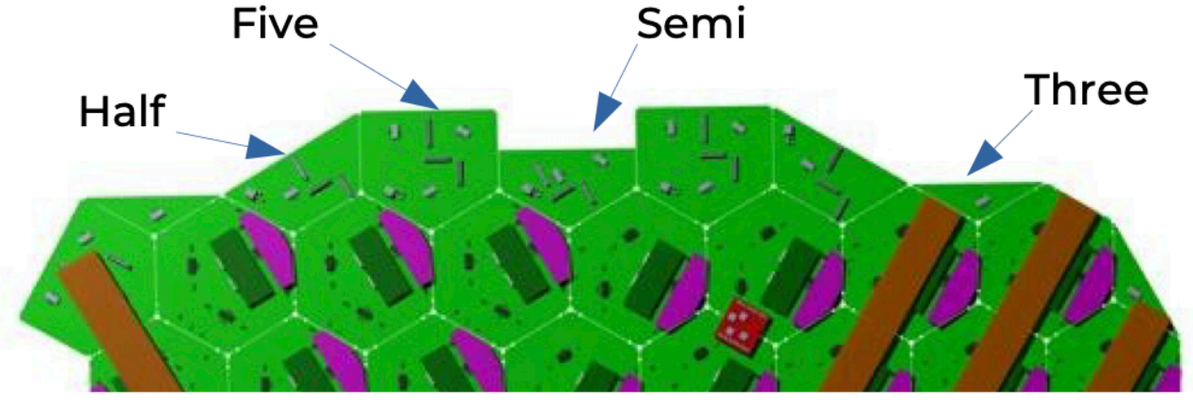


- Silicon sensors are first use of 8” technology for large-scale HEP sensors
  - Hexagonal geometry to maximize use of wafer area
- The inner and outer envelopes of the detector are circles
- To improve the filling along the edge, we use partial sensors of various types to fill in the gap
- Sensors are wirebonded to “hexaboard”

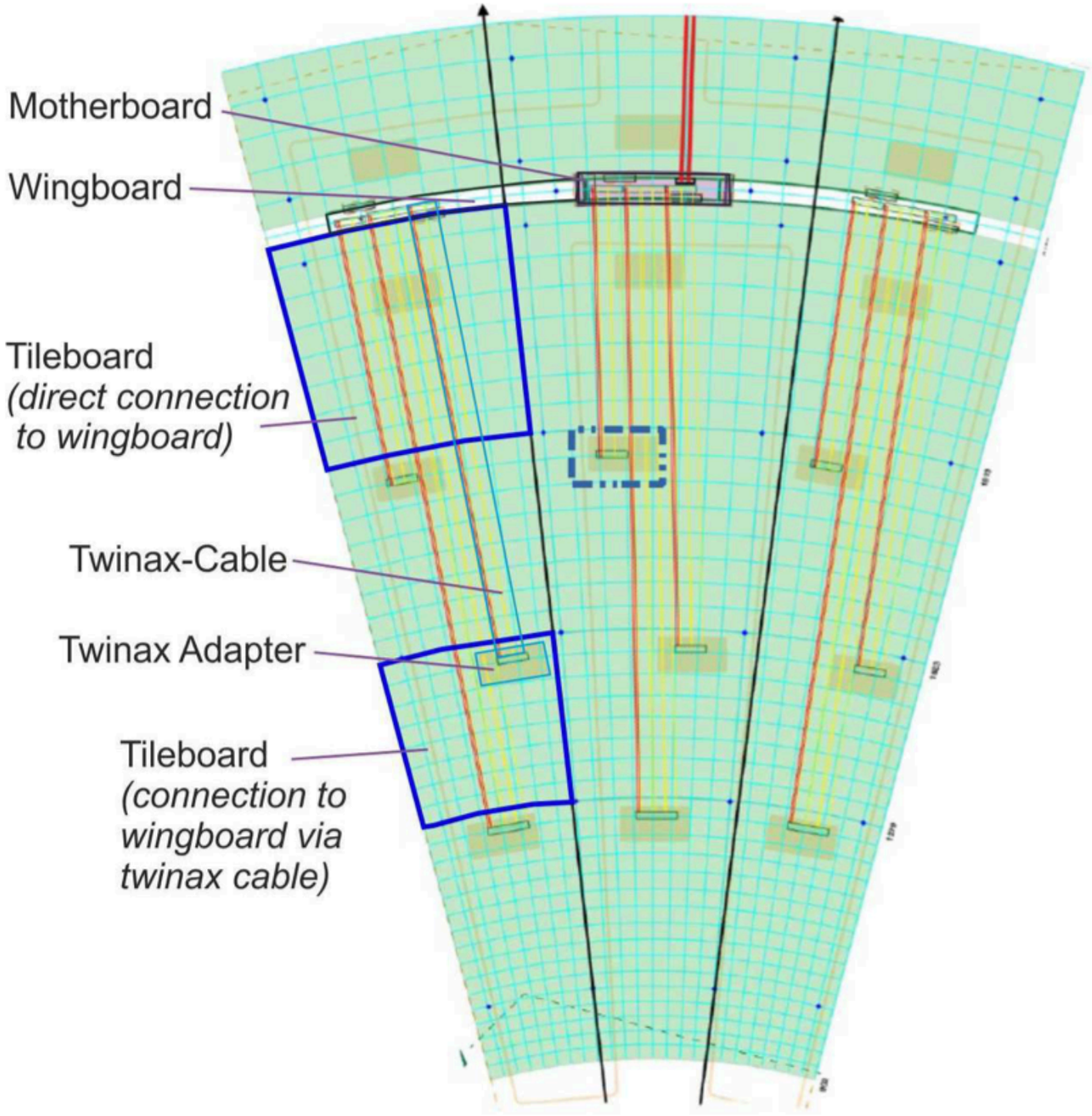








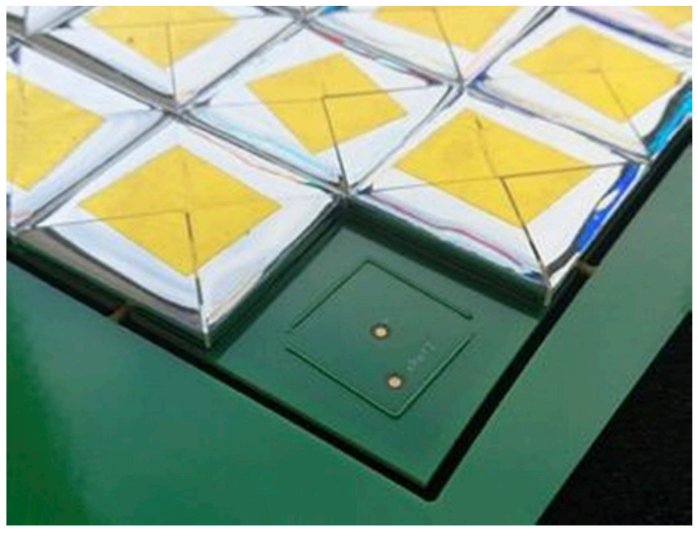
Scintillator cassette components

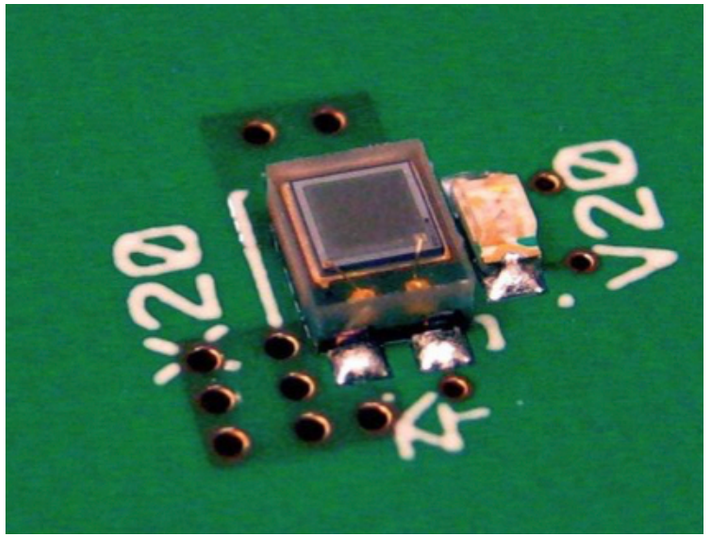


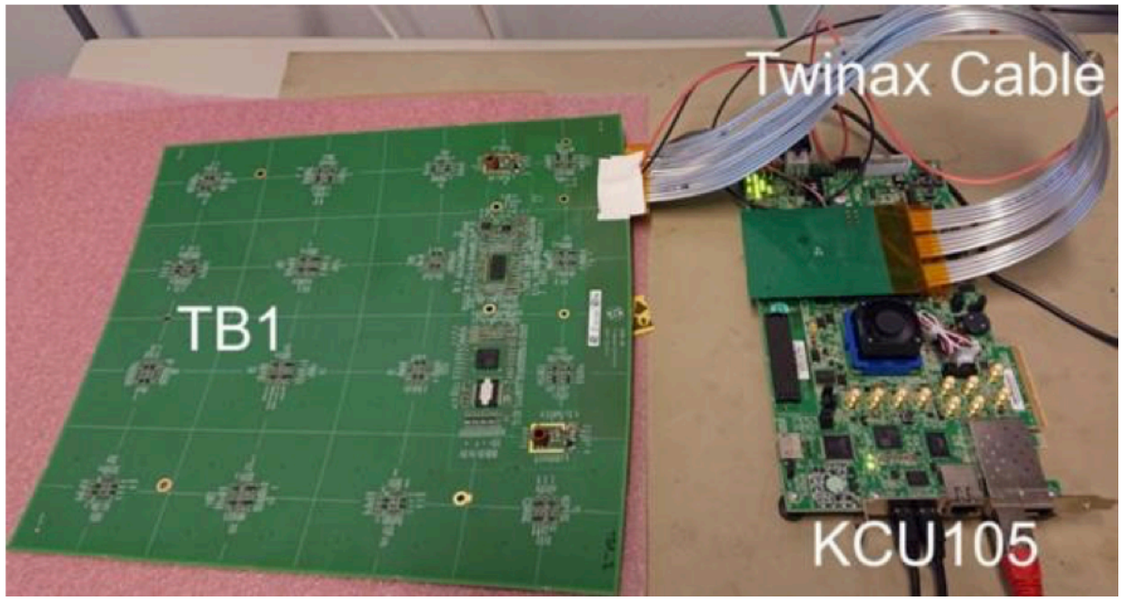
Silicon sensors here

Scintillator cassette components

- Scintillator tiles will be produced using both injection molding and machining of cast scintillator
- Tiles will be wrapped with ESR foil using an automated wrapping machine
- SiPM photodetectors have been produced which provide sufficient signal-to- noise over the life of the experiment
- Tiles and SiPMs will be mounted on “tileboard” PCBs



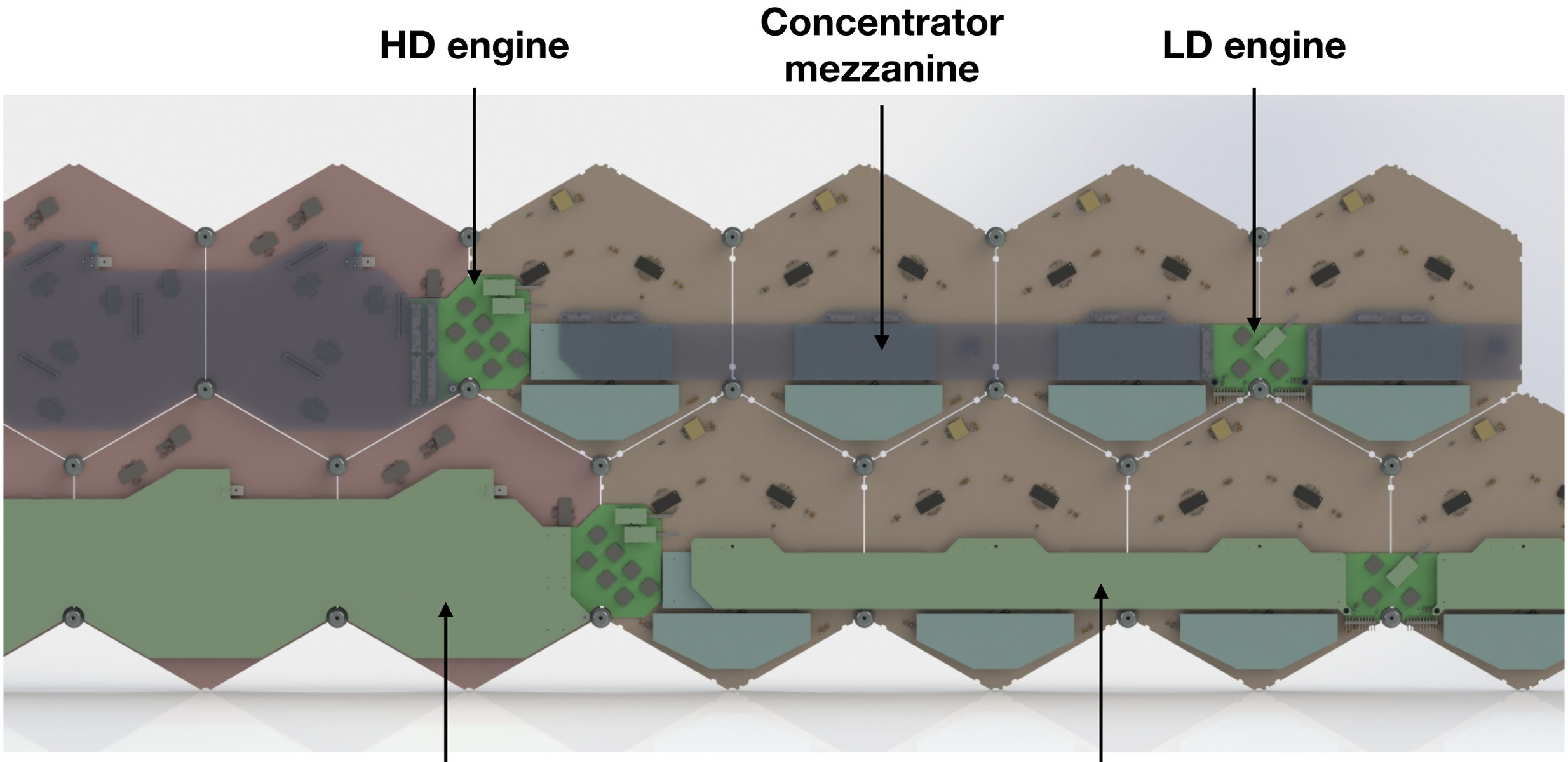




HGCAL frontend electronics

- **Purpose:**
  - Digitize, concentrate, and transmit detector data to the off-detector trigger and data acquisition electronics
  - Distribute clock and control signals (both “fast” and “slow”)
  - Provide monitoring of e.g. temperature
- **Requirements:**
  - Radiation tolerant
  - Fit in limited physical space
  - Support transfer of required data volume for good physics performance
- Implemented as **modular system**:
  - Modules, **engines, wagons**, concentrator mezzanine
  - Optimized for low- and high-density regions separately

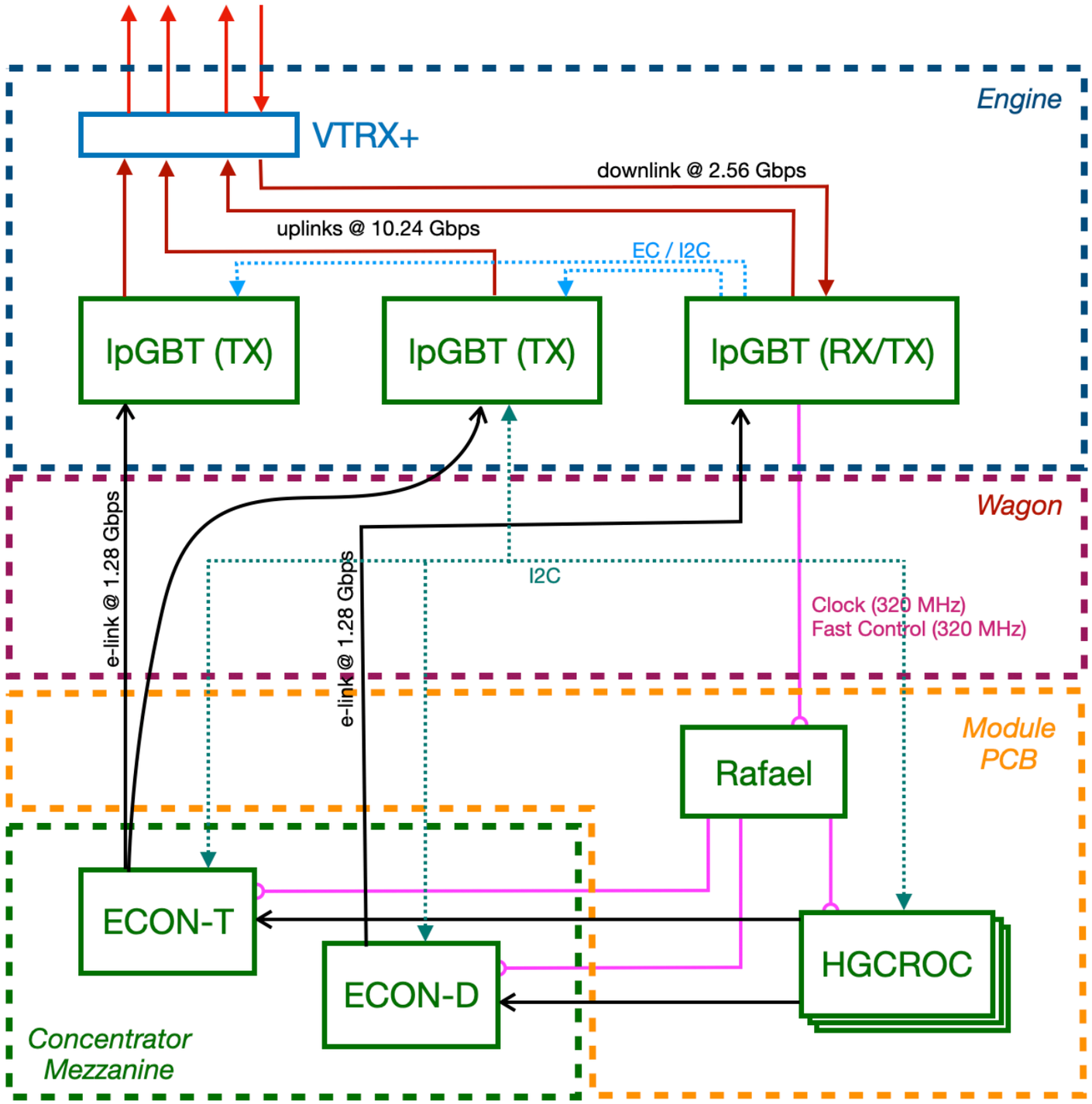
Frontend implementation



Note: design has changed a bit since this picture was made

Frontend architecture

LD region

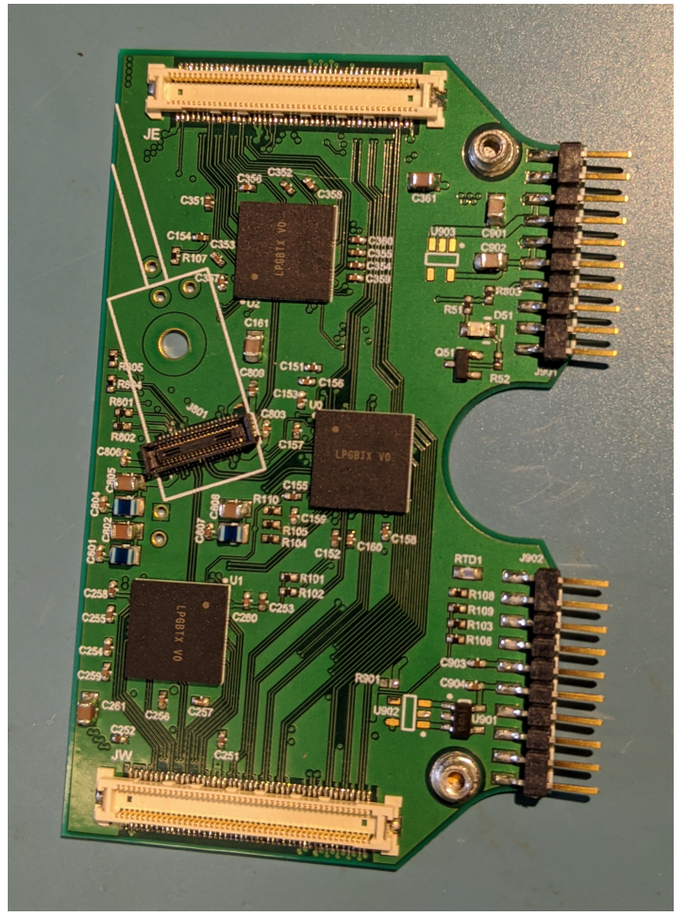


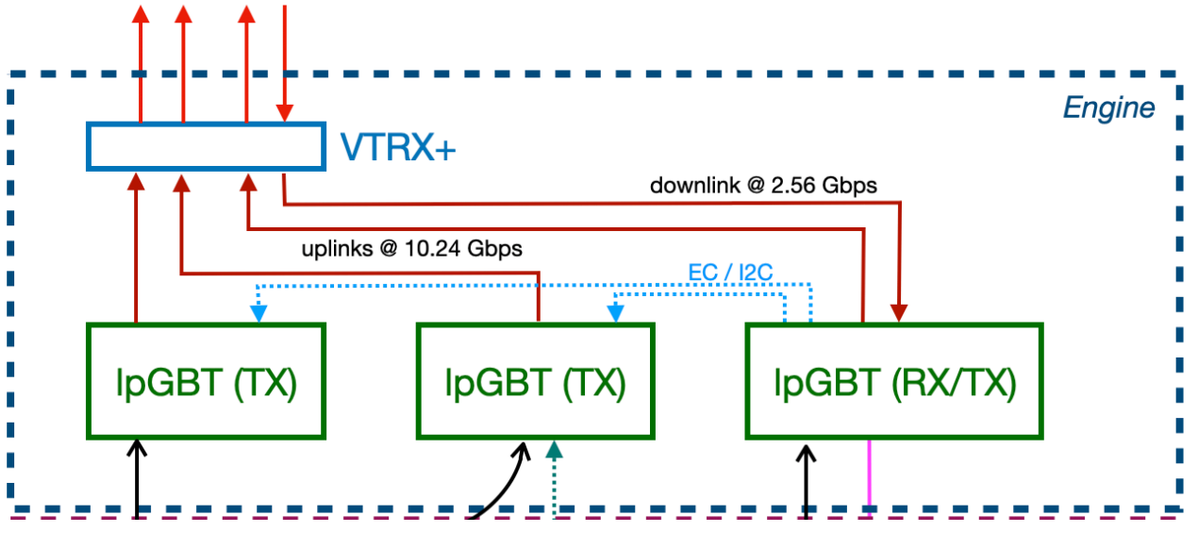
Engines and Wagons are UMN responsibility

LD Engine

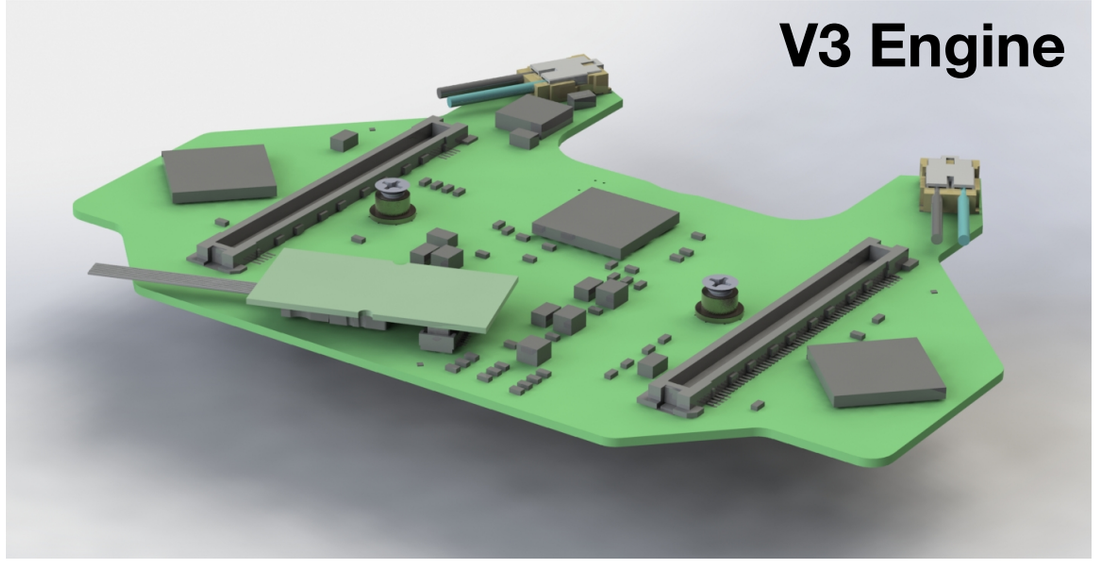
- Aggregates trigger and DAQ data from up to 6 (7) modules and transmits to backend electronics via optical link
- Distributes fast control, clock, and slow control signals
- Holds lpGBTs, VTRX+
- Small, complex board with fine-pitch components

V2 Engine



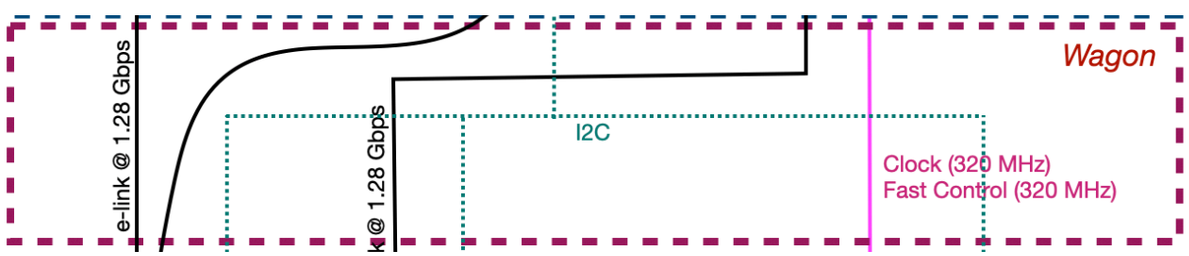


V3 Engine

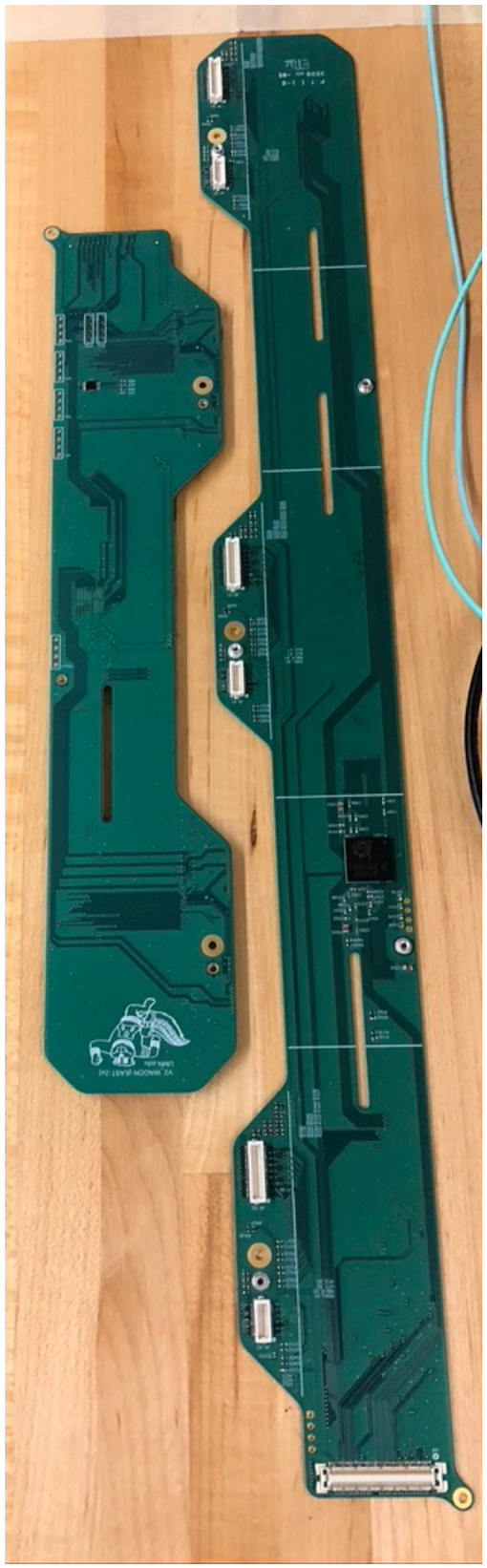


LD Wagon

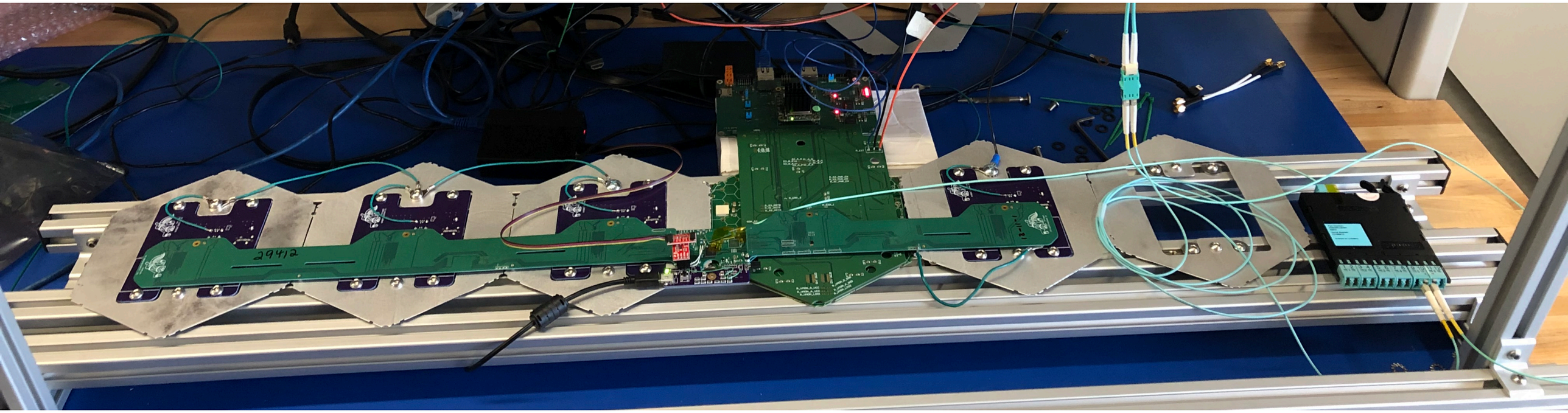
- Connection between modules and engine
  - Current version contains the GBT-SCA slow control ASIC, will not be there in final design
- Large boards, up to 3 full modules long
  - Simpler technology compared to engine
- Many(!) variants are needed to accommodate geometrical and bandwidth constraints
  - 1—3 modules long
  - Straight shape or more irregular
  - Connect to “east” or “west” side of the engine
  - Different allocation of elinks per module



No active components!



Readout “Train”



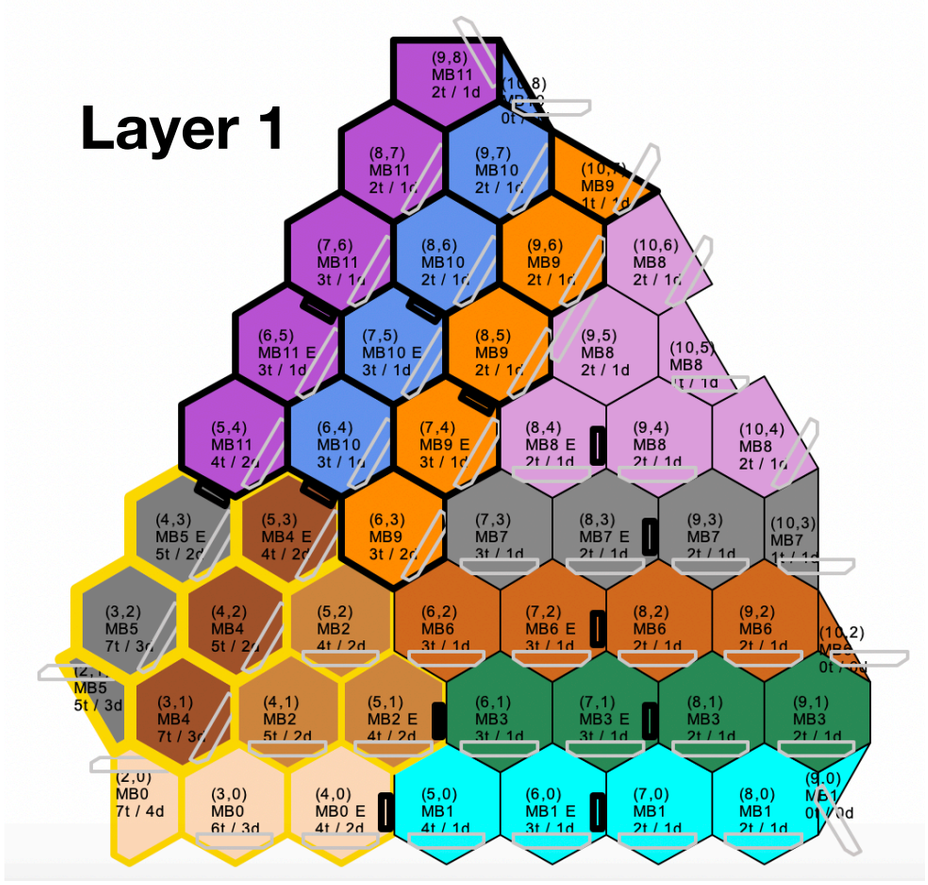
- V2 Engine with 2 wagons
- One hexaboard with interposer and hexacontroller (ECON not yet available)
- Other hexaboard spots filled in with “wagon wheels”

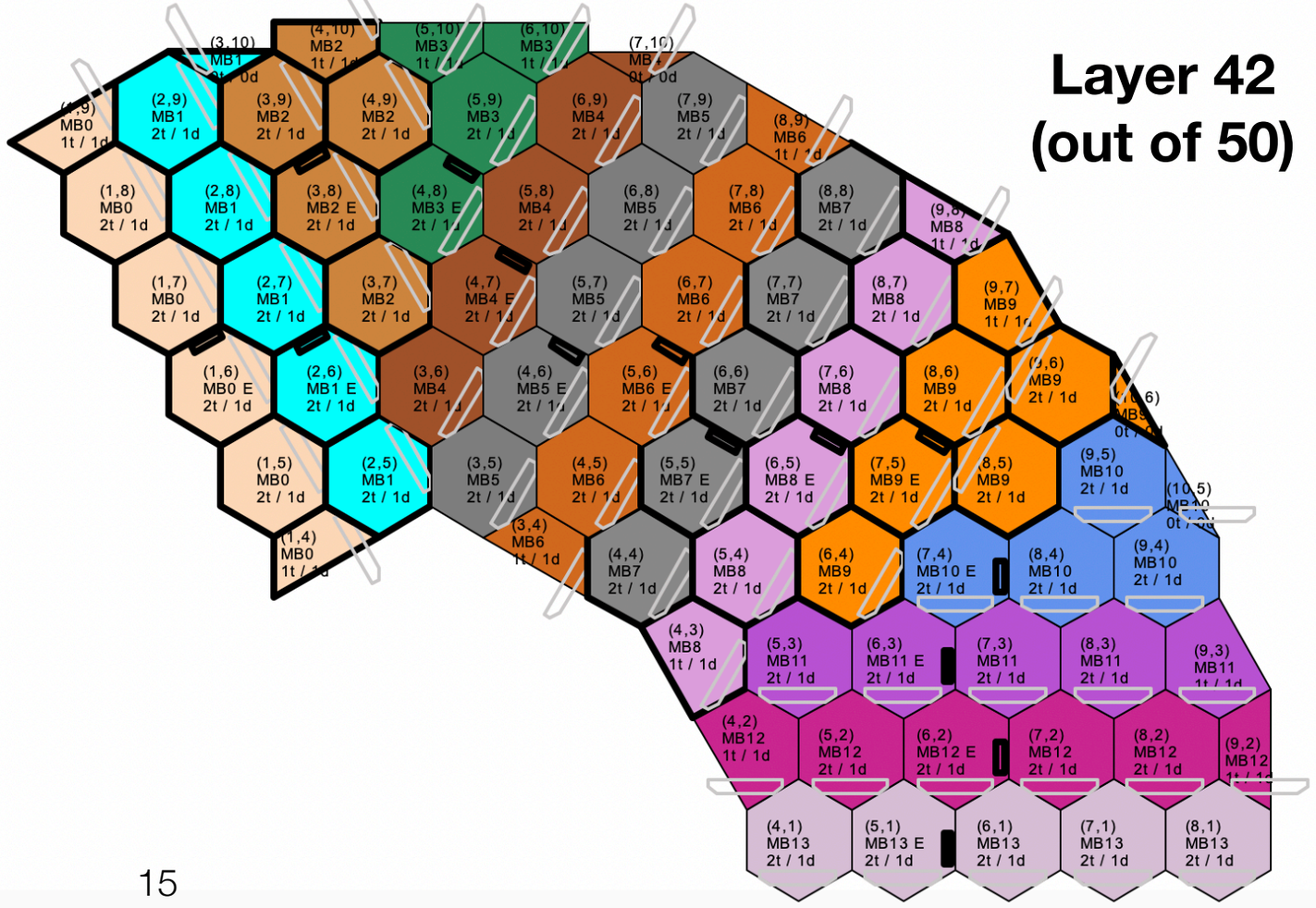
Note on the HD region

- HD modules have more channels and higher occupancy, resulting in much larger #elinks
- Slightly different scheme is used in the HD region:
  - ECONs on the wagon, no concentrator mezzanine
  - Rafael chip on the wagon
  - More lpGBTs (6 or 7, TBD) and VTRX+ (2) to handle the increased bandwidth
- Details still being finalized
- Aiming for more uniform geometrical layout, to reduce # of needed HD wagon designs

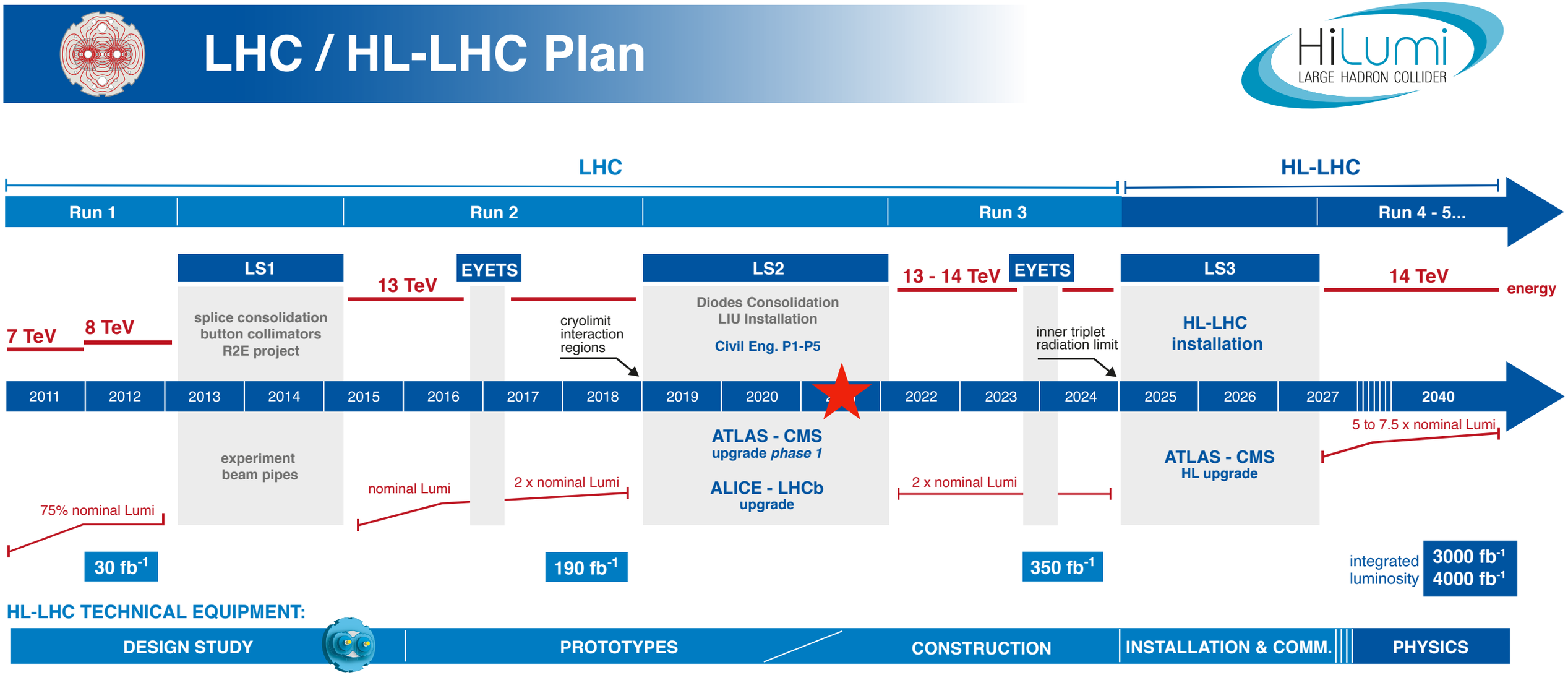
Putting it all together

- Each layer in the detector is different!
  - Different number of modules, different partial modules on the inner and outer edges
  - By design, this mainly affects the wagons





Towards production



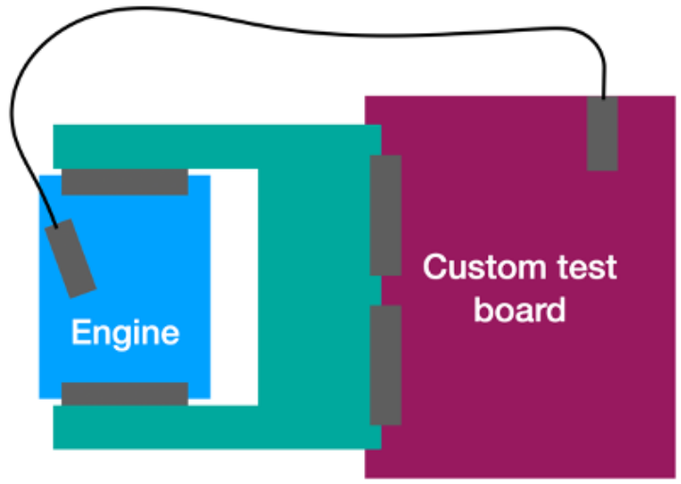
- Finish prototyping in 2022
- Final designs, production, test in 2023–2024
- Ship to FNAL for assembly in cassettes in mid-2024

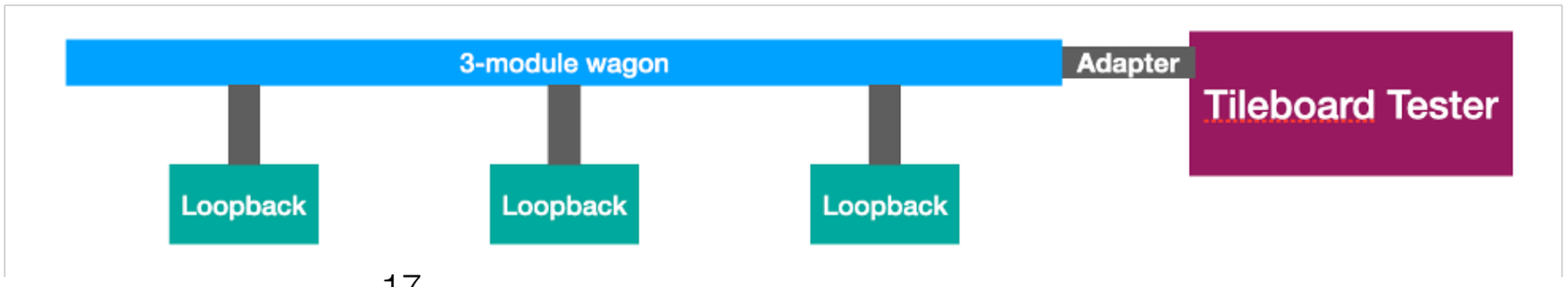
Quality control plans

- Assembled boards arrive in the lab for QC by team consisting of postdoc, graduate students, and undergraduates
- QC in batches to match cassette assembly
- All QC information will be stored in database
- QC starts with visual inspection and labelling, followed by dedicated test of board functionality
  - Engine: functionality of lpGBT, VTRX+, connectivity; and configuring the efuses
  - Wagon: signal integrity across connectors and board

Quantities CE-E + CE-H

Board	LD	HD
Engine	5k	1.5k
Wagon	10k	1.5k



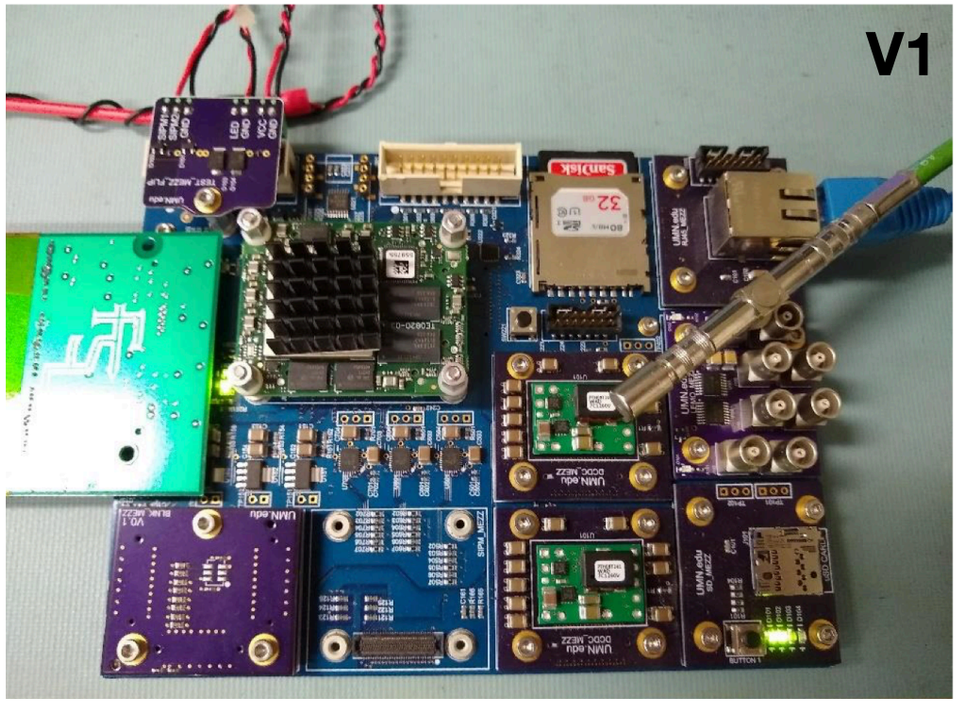


Work ongoing and needed towards final prototypes & production

- “V3” system (Based on HGCROCv3, final prototype):
  - Engine V3 design ongoing, to be produced this Fall
  - Dedicated engine tester to be designed soon
  - Wagon V3 to follow after engine, will produce several varieties
- QC preparations:
  - Develop QC system using V2 and V3 boards
  - Setting up database and interfacing barcode scanner
  - Writing/streamlining testing SW for both engine and wagons
  - Writing necessary firmware for testers
- Design decisions:
  - HD region details (powering, #lpGBTs), interplay with hexaboards
  - How to fit in the partial modules

Tileboard Tester

- Board based on set of mezzanines designed to test tileboards
  - Can communicate to tileboard through direct I2C or via GBT-SCA on tileboard
- Very flexible, so also used for other testing, including for wagon testing and testing of twinax cables
- V1 has been in use in various places, V2 being rolled out now



Other activities

- Overall system integration
- Software for GBT-SCA communication
- Firmware
- Initial study of services space
- Concepts for powering the HD region
- Studies of lpGBT properties
- Test beam for scintillator
- Mockup of mixed cassette at FNAL