

Liverpool (Online), FCC physics workshop

IDEA Preshower and Muon Detector

Status update and future plans

G Mezzadri (INFN Ferrara) on
behalf of the working group

February 9, 2022

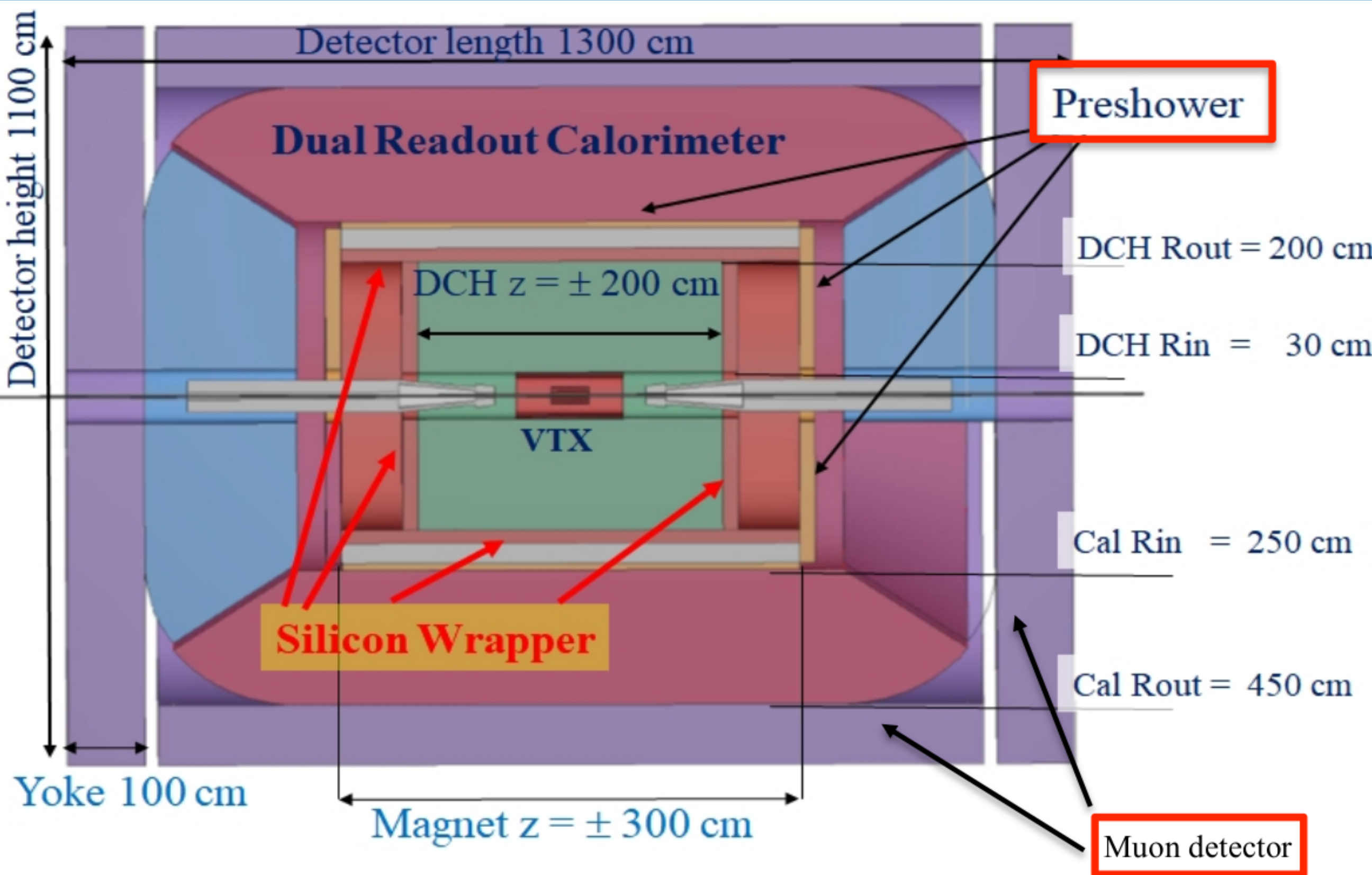


 IDEA Detector @ FCC-ee

Outline

 Pre Shower and Muon Detector

 On going activities



IDEA

Innovative
 Detector
 Electron-positron
 Accelerator

Preshower Detector

High resolution after the magnet
to improve track reconstruction

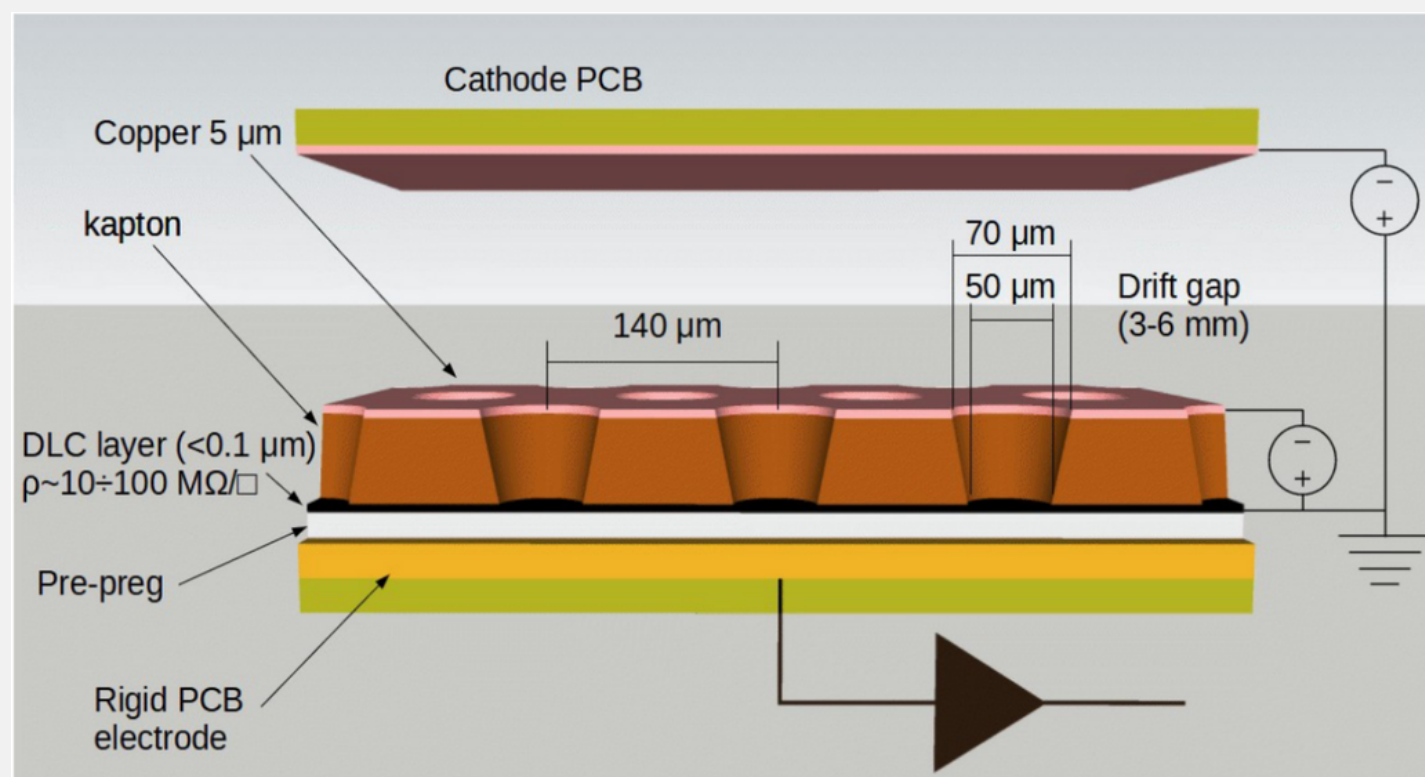
Efficiency > 98%
Space Resolution < 100 μm
Mass production
Optimization of FEE channels/cost

Muon Detector

Identify muons and search for LLP

Efficiency > 98%
Space Resolution < 400 μm
Mass production
Optimization of FEE channels/cost

micro-RWELL detector



50x50 cm^2 2D tiles to cover more than 4330 m^2

Preshower

pitch = 0.4 mm
FEE capacitance = 70 pF
1.5 million channels

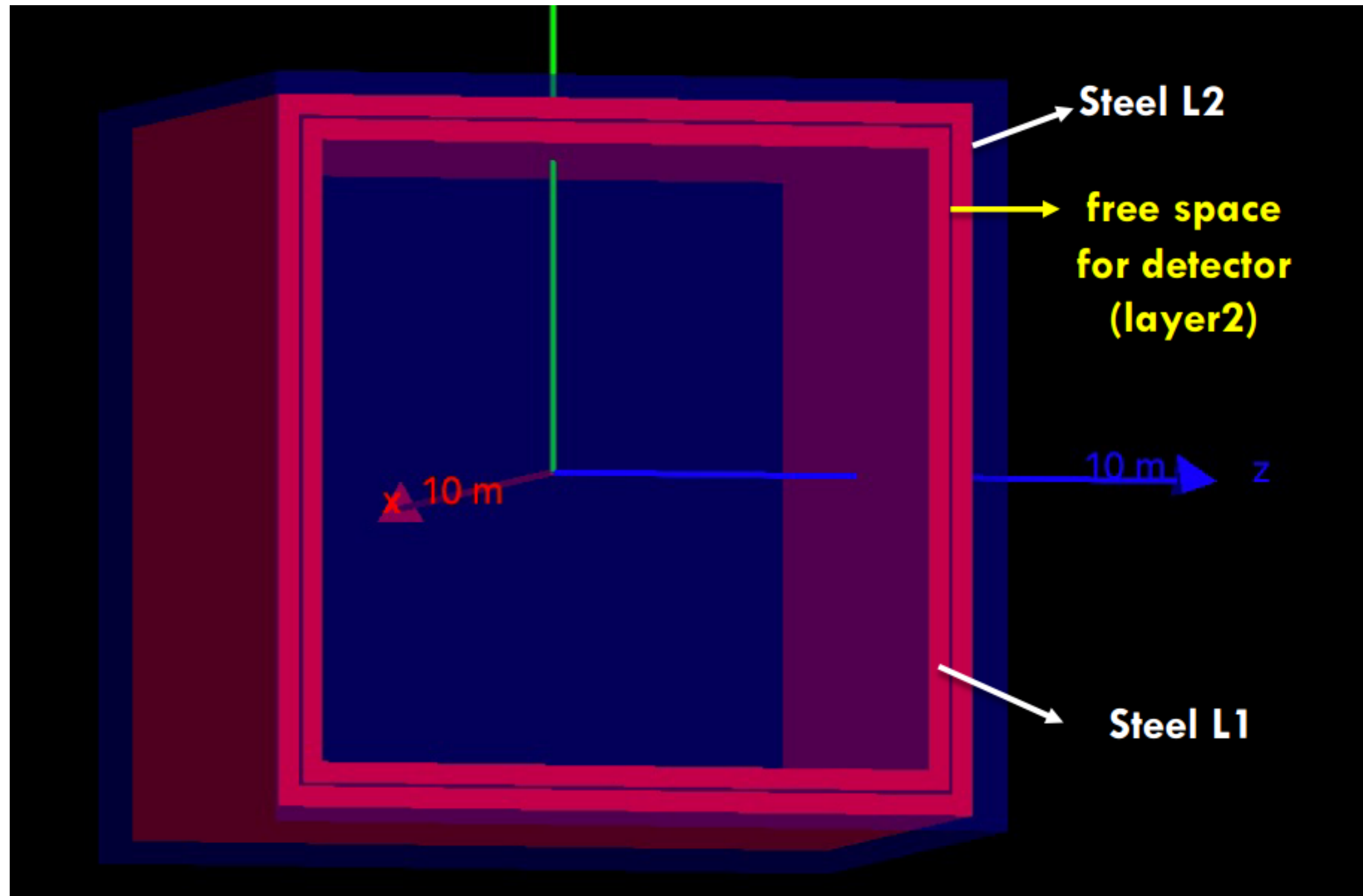
Muon

pitch = 1.5 mm
FEE capacitance = 270 pF
5 million channels

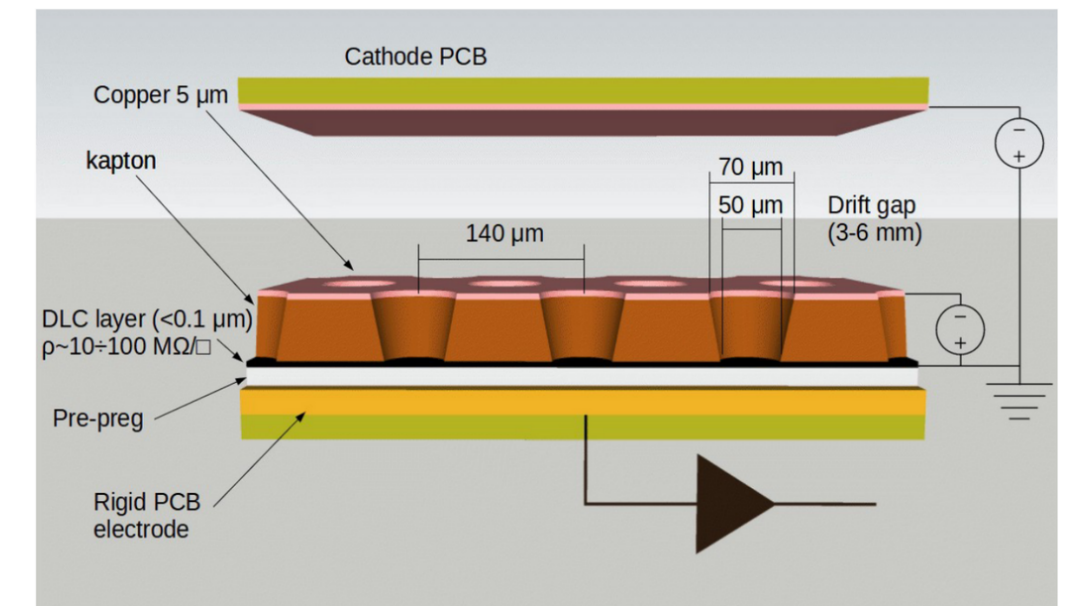


On going activities

Standalone Simulation of the muon detector



To be inserted in official simulation.
Endcap in preparation



From sketch

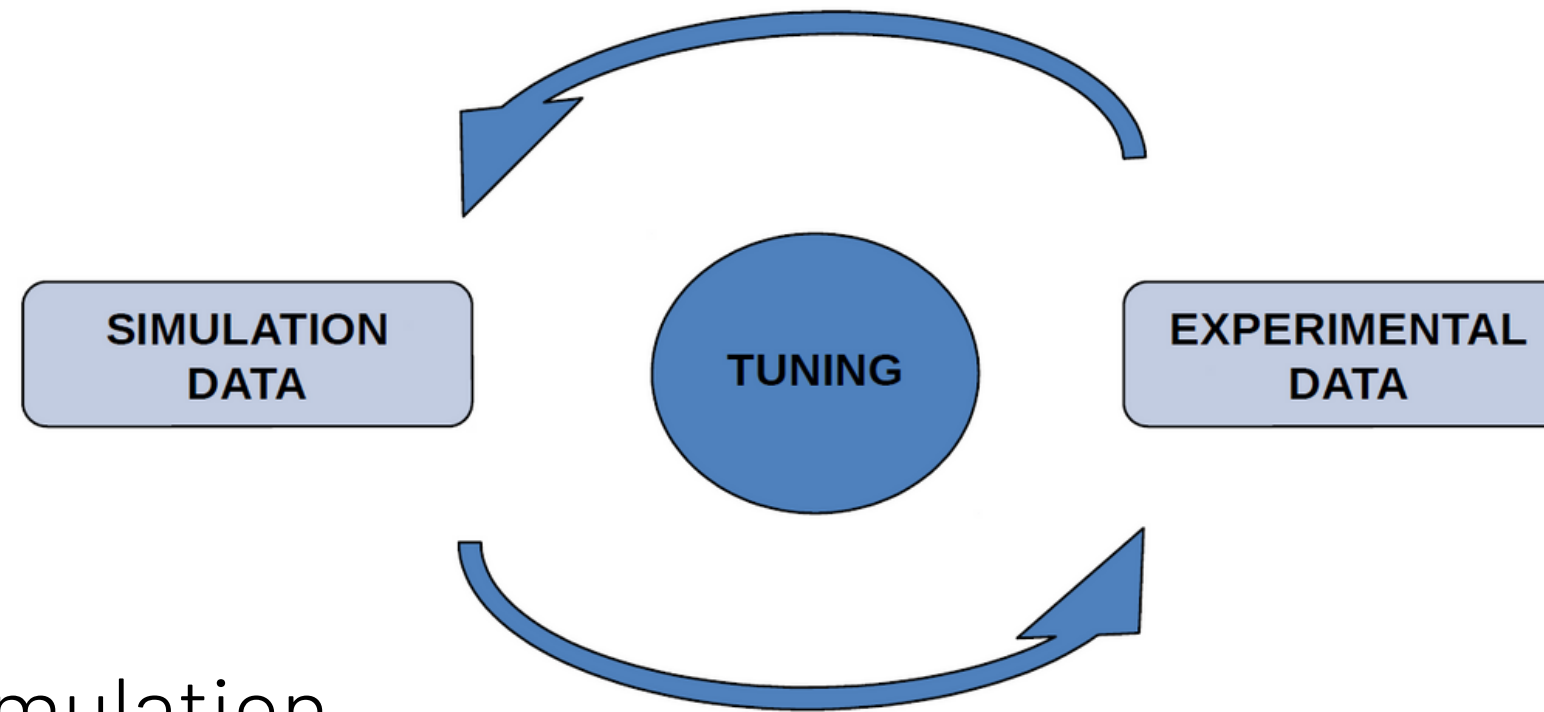


to simulation



Different layers

micro-RWELL parametrization in simulation



- IONIZATION
- DETECTOR GAIN
- ELECTRON DRIFT
- RESISTIVE**
- INDUCTION
- ELECTRONICS
- RECONSTRUCTION
- ANALYSIS

Use test beam data to tune the simulation

Resistivity

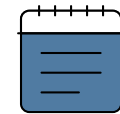
Simulate the charge spread dispersion at the anode using approach of *NIM A 566 (2006) 281-285*

Interstrip cross talk

Study the probability to induce a signal on neighbor strip as a function of

- charge in the central strip
- relative time delay

Resistivity scan

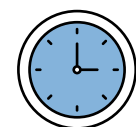
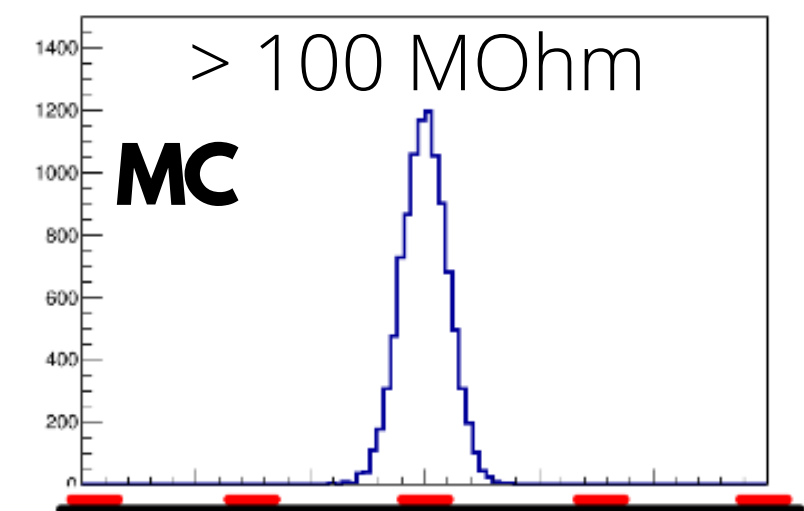
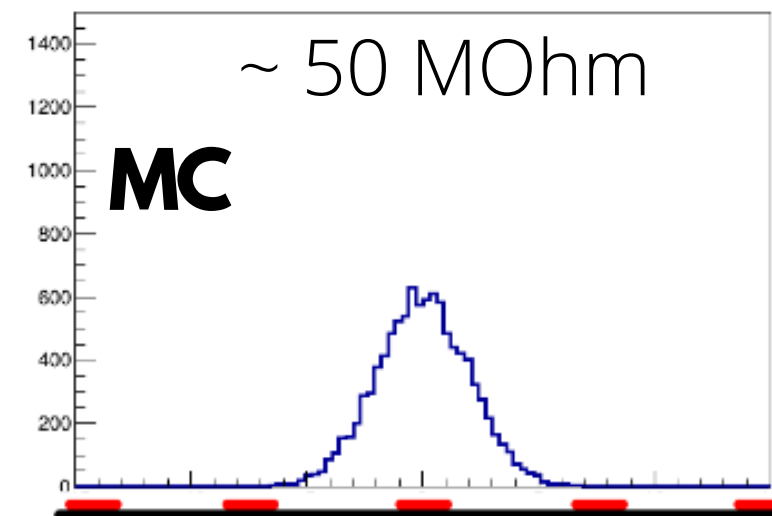
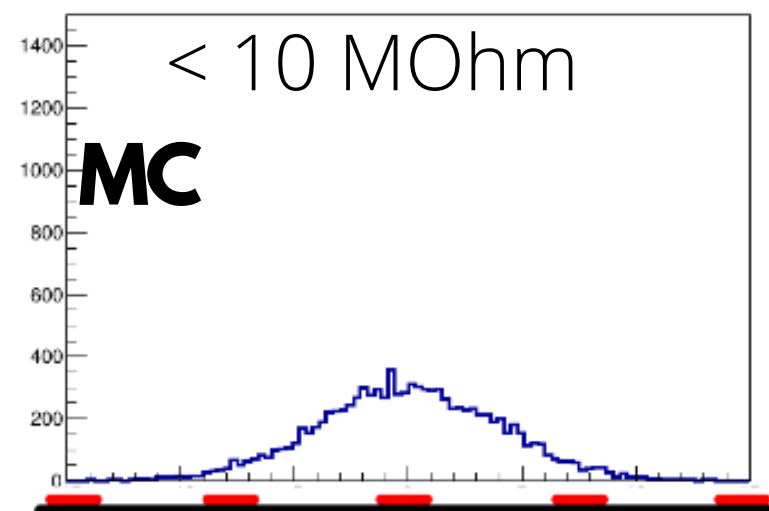


R&D to identify optimal DLC resistivity by studying spatial performance

Preshower: 10, 30, 50, 70, > 100-200 M Ω /square

Muon: 15, 35 M Ω /square

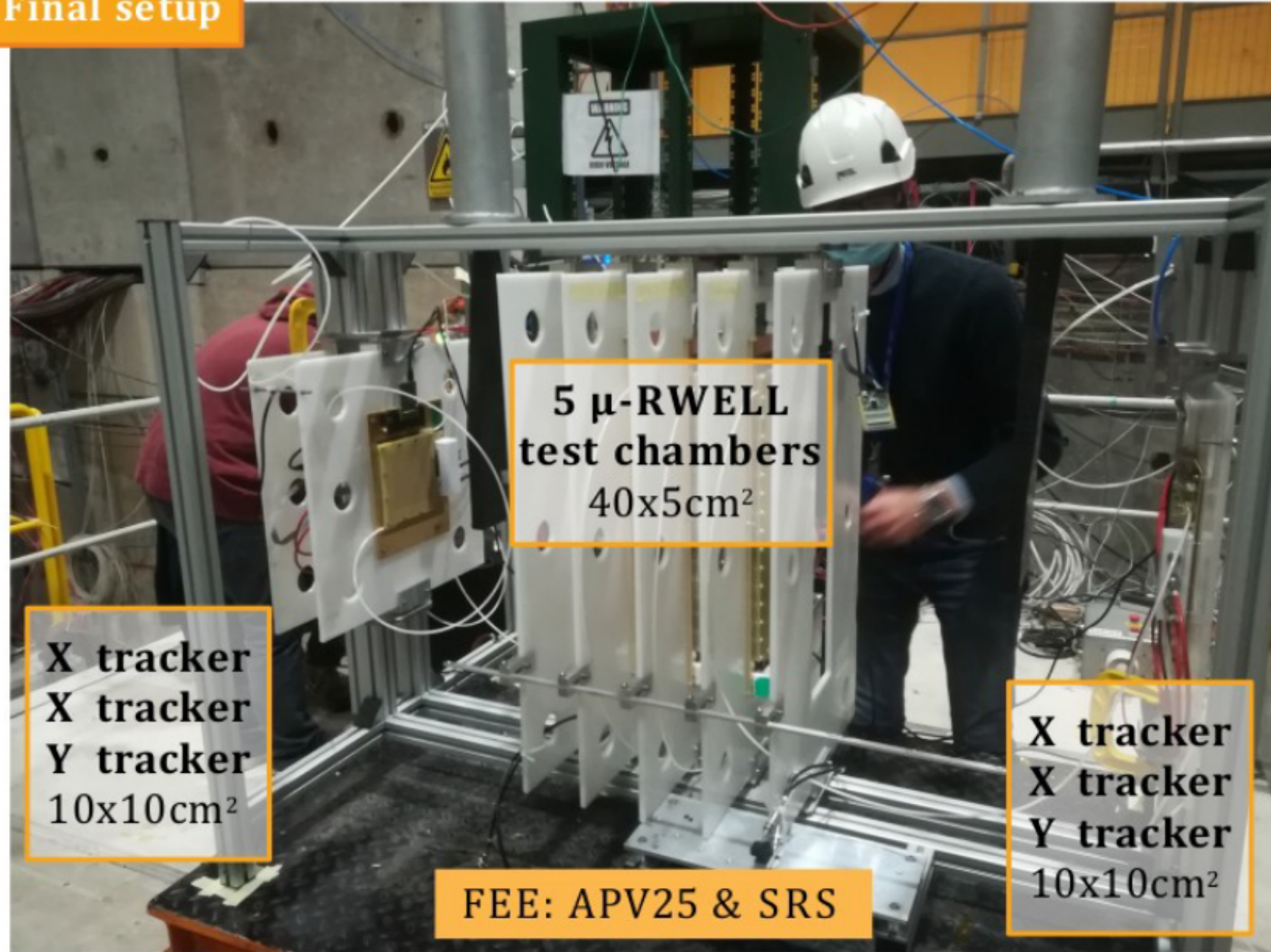
Effect of resistivity on charge spread



Test beam performed in October 2021 at SPS-H8-CERN line

Instrumented 5x40 cm² 1D micro-RWELL modules with SRS DAQ and APV readout to have a comparison with previous results

Final setup



140-180 GeV/c muon and pion beam
Operated in Ar/CO₂/CF₄ (45/15/40)

Test beam

a) **Design optimization:**

- different HV filter applied

b) **Detector characterization**

- HV scan at 0°

- HV scan at different angles and drift field

1- **Signal shape**

(cluster charge, cluster size)

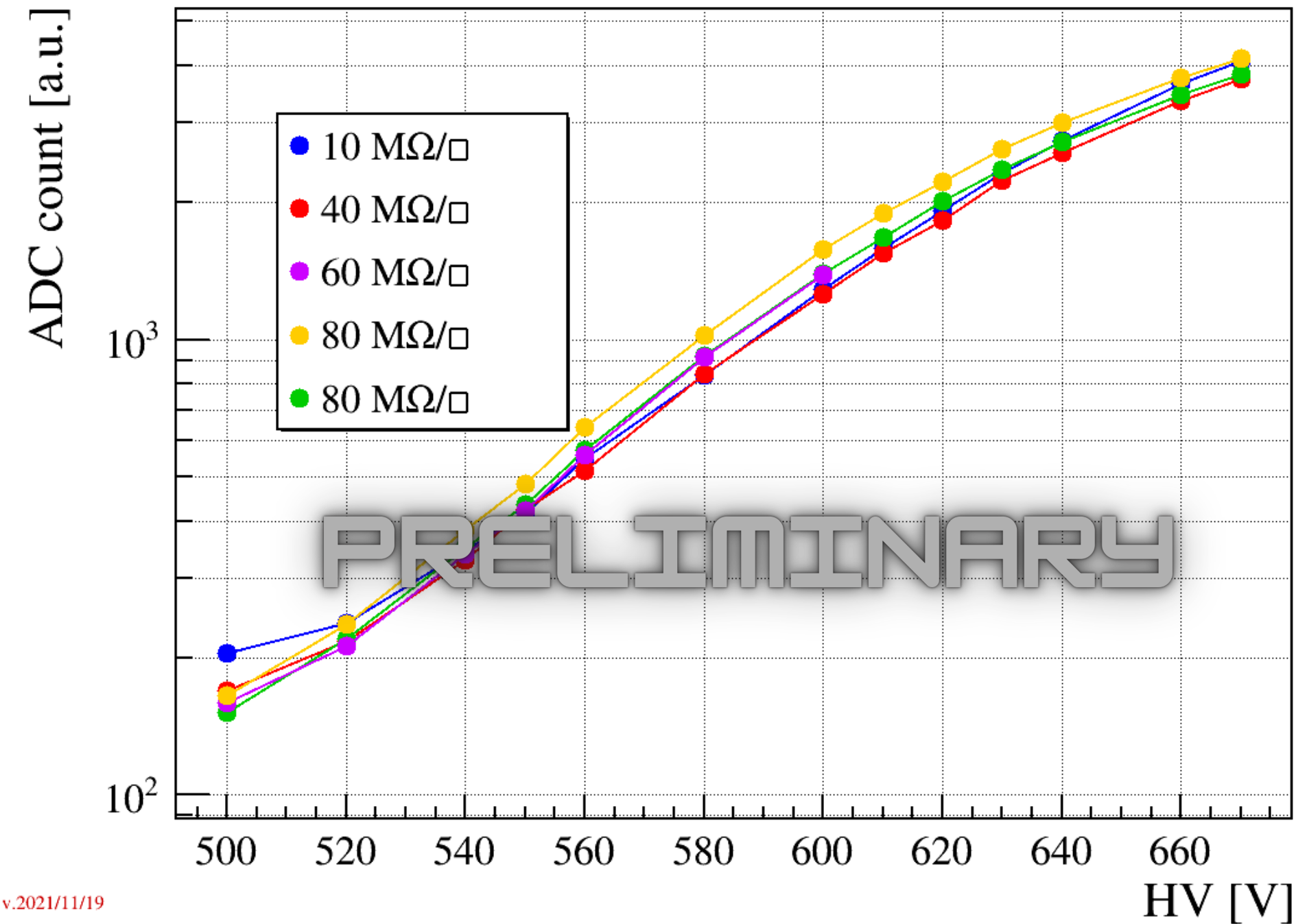
2 - **Detector performance**

(efficiency, resolution)

HV scan

Similar behaviour for all the prototypes

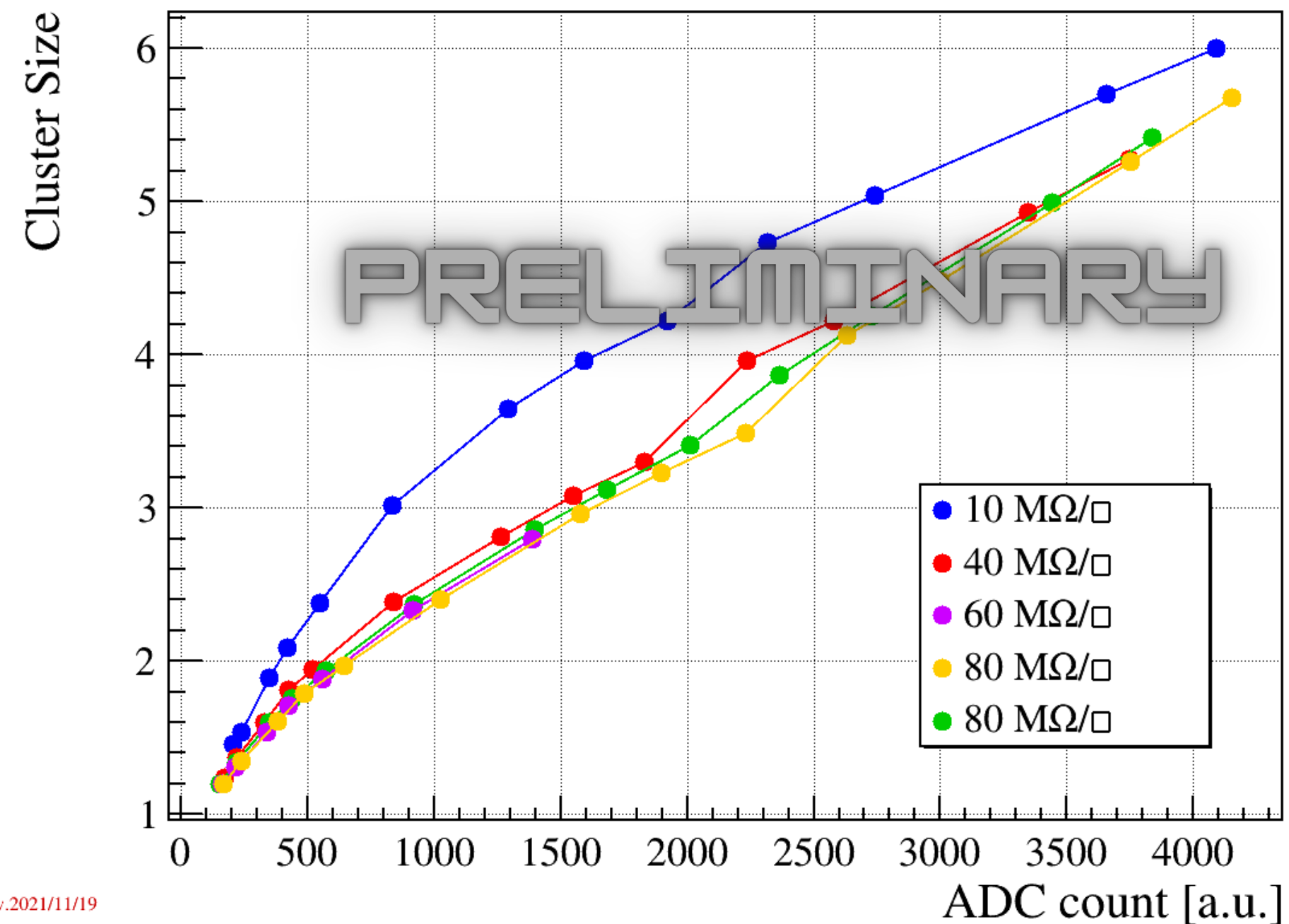
Ok, since the resistivity shall not influence the gain, that depends mostly on HV settings



Cluster size

10 M Ω /square chamber has larger cluster size even with smaller HV settings

Other shows common behavior. No prototypes above 100 M Ω /square due to material shortage

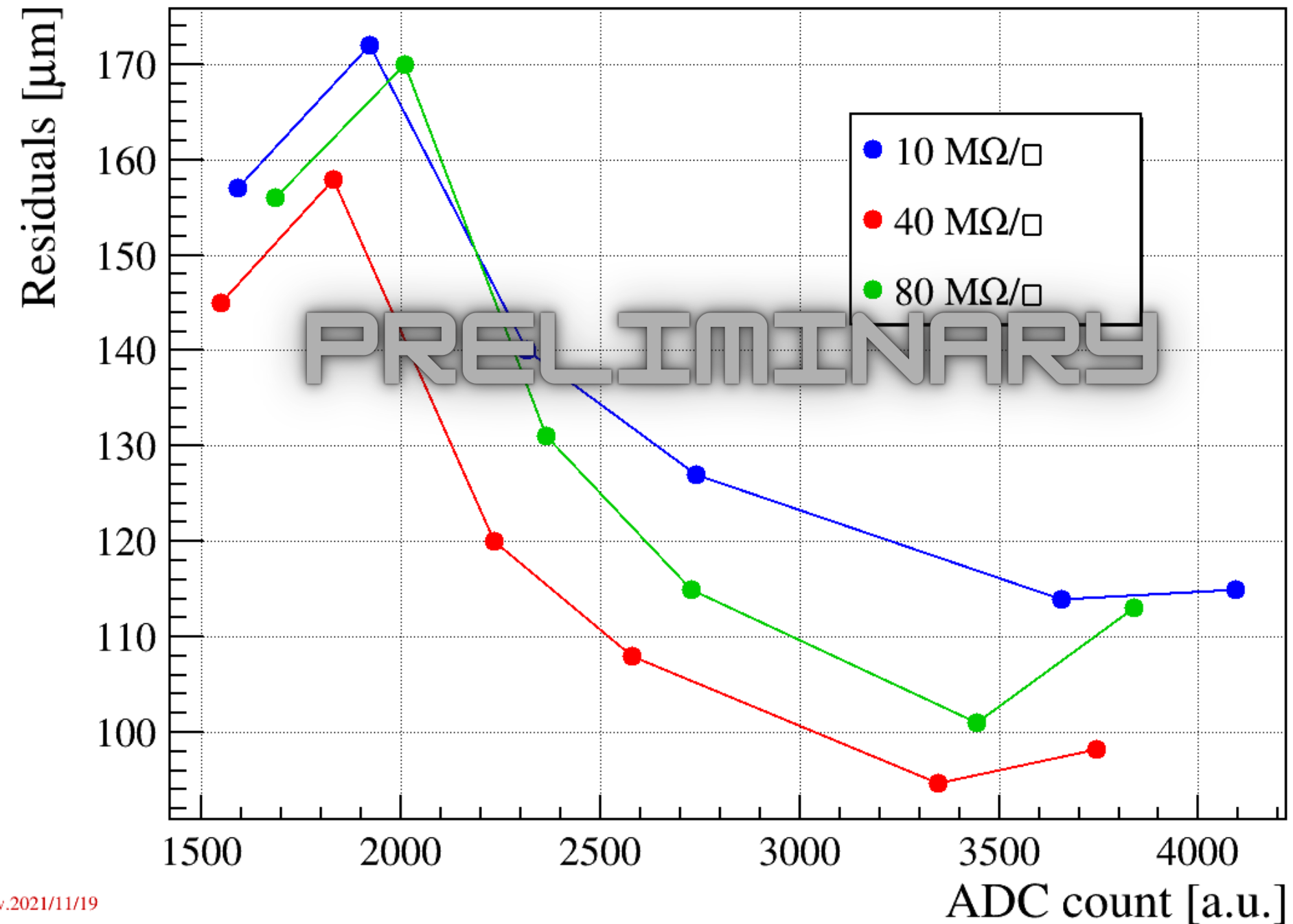


Residual distribution

Residual shrinks with increasing HV settings

The best resolution is for intermediate resistivity:
40 MOhms/square better than the others

No Alignment and tracking contribution
not subtracted



v.2021/11/19

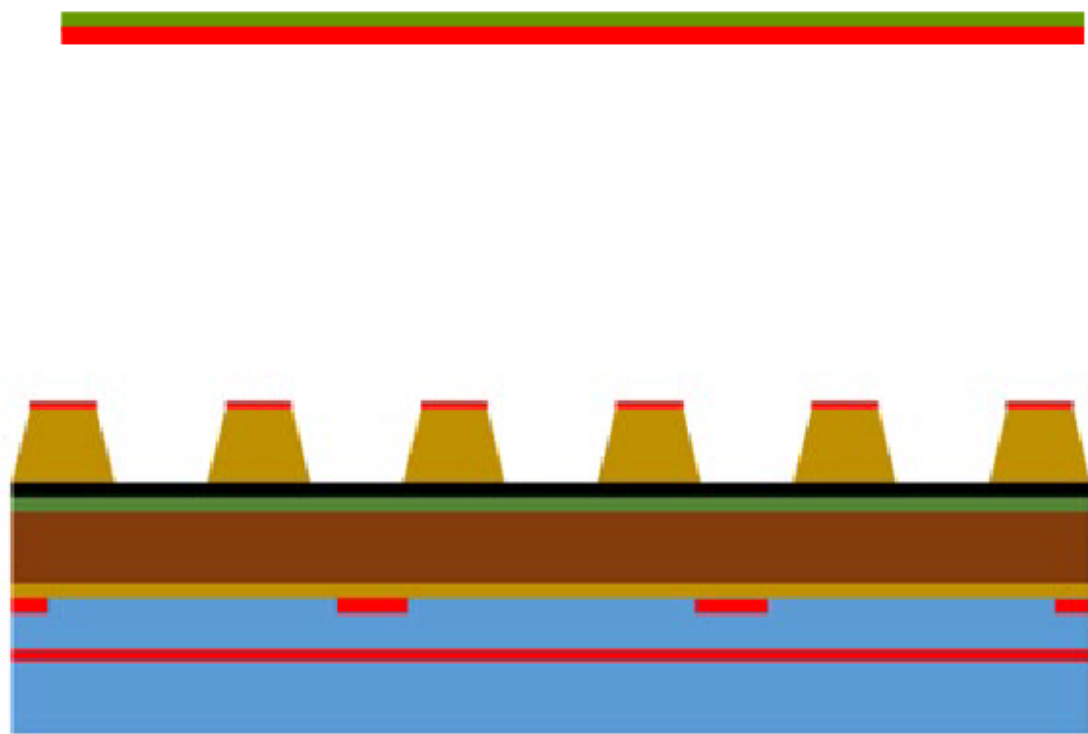
~/DDG/lavori/2021-10_IEEE_RD51/plot wg7 rd51/residuals

2D readout R&D ideas

micro-RWELL with 2D anode readout

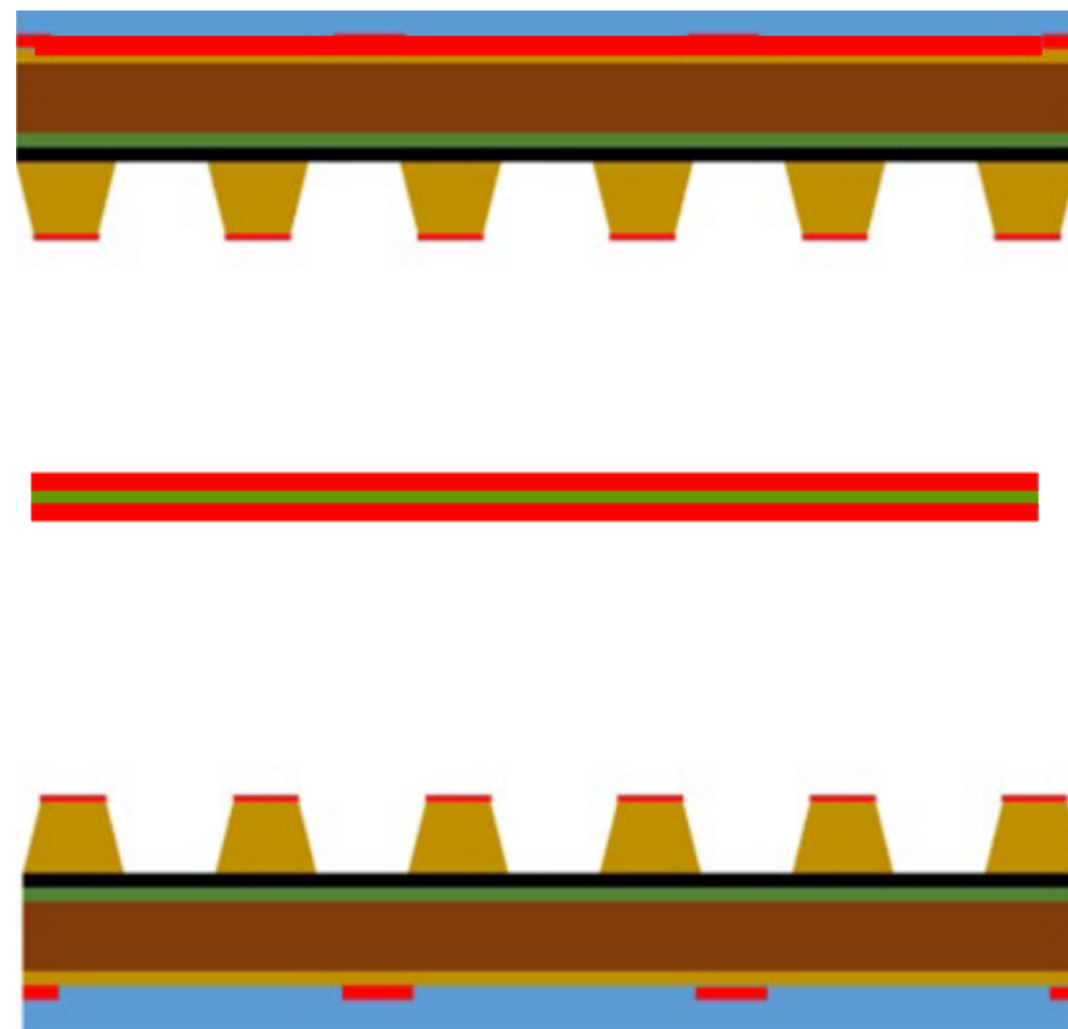
Good performance
but need higher gain wrt to 1D micro-RWELL

More complex PCB construction



2 1D micro-RWELL stacked

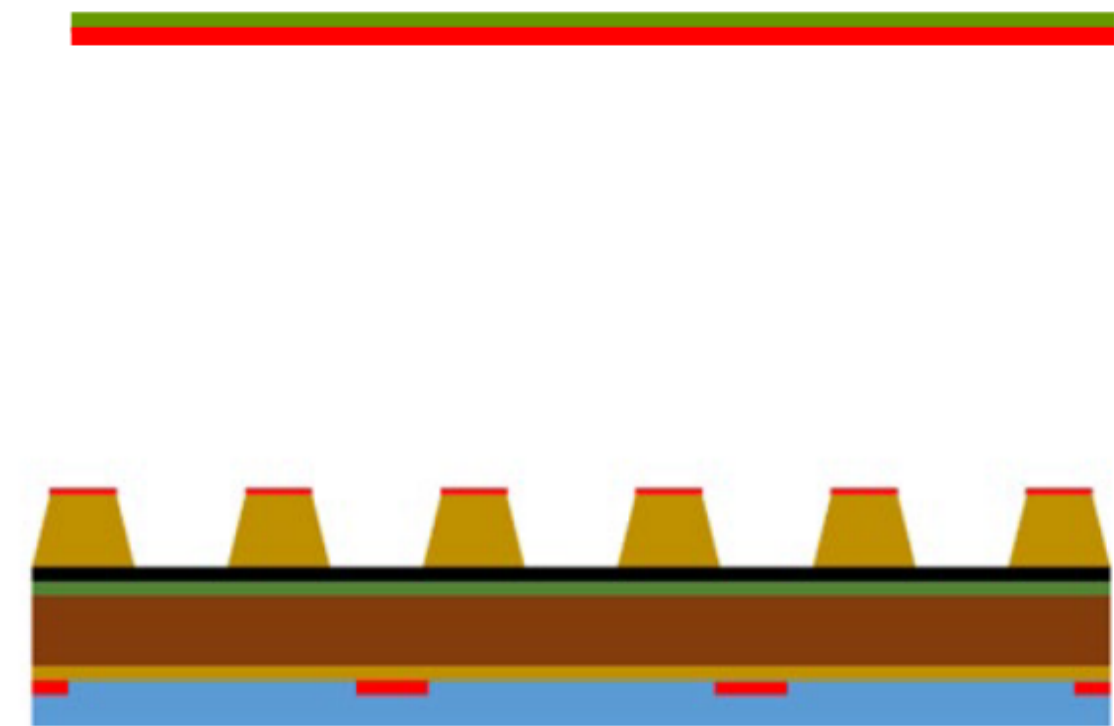
1 view per micro-RWELL easy PCB construction
2D performance to be measured



micro-RWELL with strips on top and anode

HV on DLC,
TOP to ground

2D performance to be measured



Preparation

DLC sputtering with new INFN-CERN machine @ CERN

Technology transfer at ELTOS



Step 1: producing u-RWELL_PCB (1D 10x10 cm²)

- with top patterned (pad/strip)
- without bottom patterned

Step 2: DLC patterning

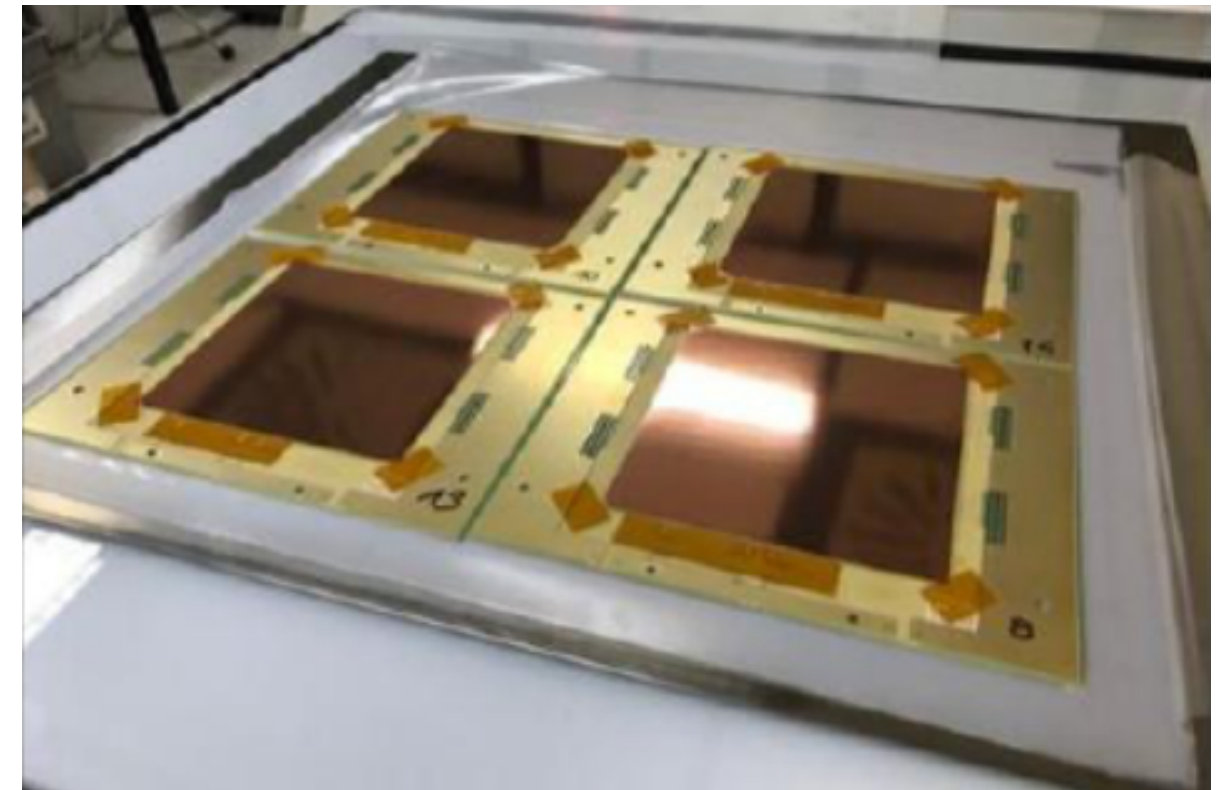
- in ELTOS with BRUSHING-machine

Step 3: DLC foil gluing on PCB

- double 106-prepreg (~2x50 um thick)(already used in ELTOS)
- pre-smoothing + 106-prepreg (~50 um thick)
- single 1080-prepreg (~75 um thick)

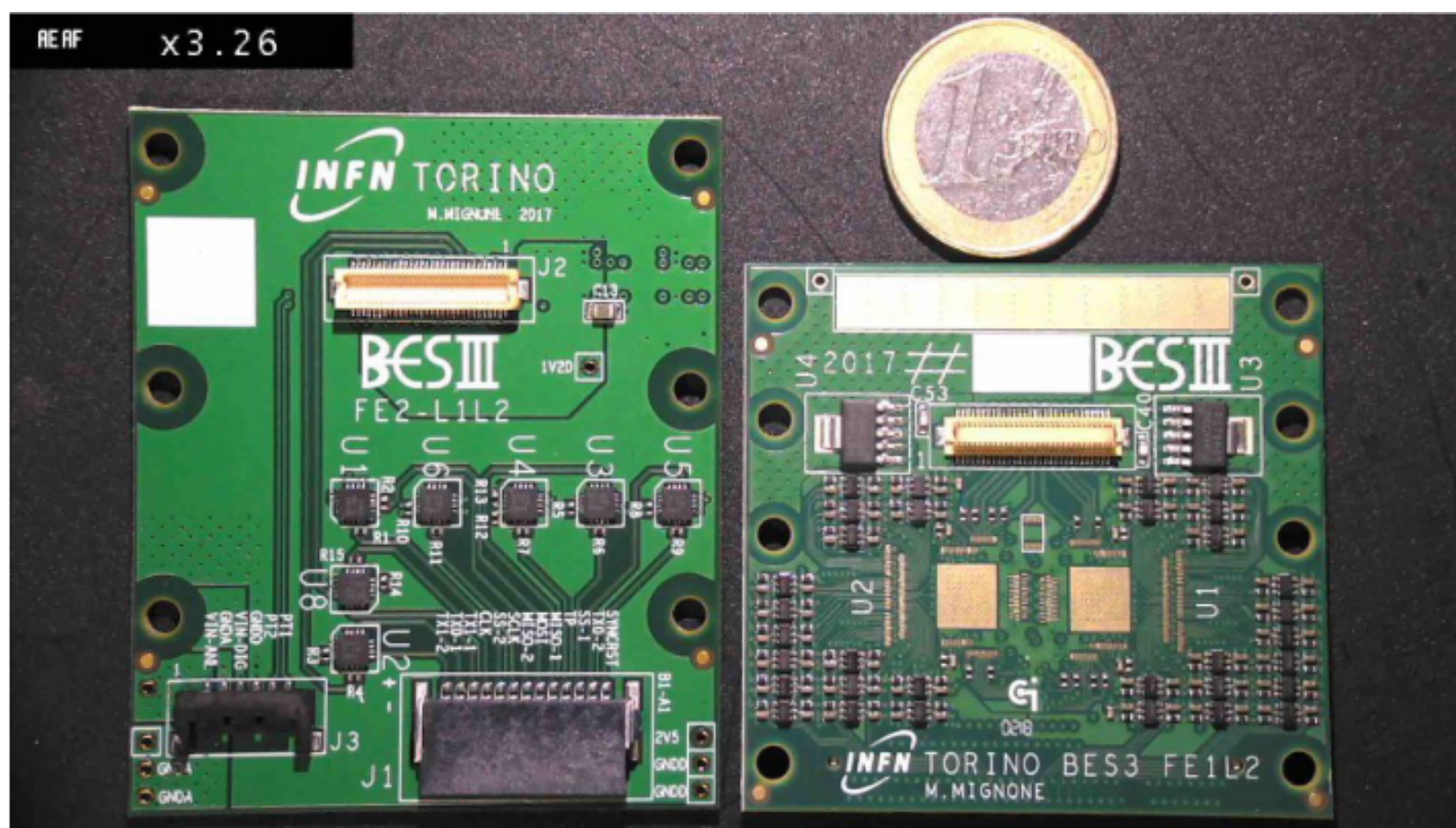
Step 4: top copper patterning

Step 5: Kapton etching on small PCB



Finalization

Detector @ CERN for final preparation



Test with TIGER ASIC

Developed for BESIII CGEM-IT

Prepare new readout card based on System On Modules (SOM)

Table 2
Measured performance of the TIGER ASIC.

Parameters	Values
Input charge	5-55 fC
TDC resolution	30 ps RMS
Time-walk (5-55 fC range)	12 ns
Average gain	10.75 mV/fC
Nonlinearity (5-55 fC range)	0.5%
RMS gain dispersion	3.5%
Noise floor (ENC)	1500 e^-
Noise slope	10 e^- /pF
Maximum power consumption	12 mW/ch

Summary and outlook

Plenty of activities on-going

Contribution to full detector simulation to perform more detailed physics case studies

More results from 2021 test beam coming soon

Another test beam is planned to continue the 2D prototype characterization

Test of the TIGER ASIC with micro-RWELL prototype

Continue partnership with ELTOS (preparation) and CERN (finalization)
to complete technology transfer



Stay
Tuned

*Thank
you!*

Working group:

A. Amoroso, I. Balossino, G. Bencivenni, V. Cafaro, G. Cibinetto, E. De Lucia, D. Domenici, R. Farinelli, G. Felici, I. Garzia, M. Gatta, P. Giacomelli, M. Giovannetti, S. Gramigna, L. Lavezzi, M. Melchiorri, GM, G. Morello, G. Papalino, M. Poli Lener, M. Scodeggio, S. Sosio

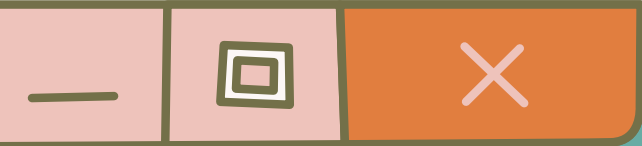
Selected bibliography

- 01 JINST 10 (2015) 02, P02008
- 02 Nucl.Instrum.Meth.A 886 (2018) 36-39
- 03 Nucl.Instrum.Meth.A 924 (2019) 181-186
- 04 JINST 15 (2020) 09, C09034
- 05 JINST 16 (2021) 08, P08036
- 06 Eur.Phys.J.Plus 136 (2021) 11, 1143





New Document - Writepad



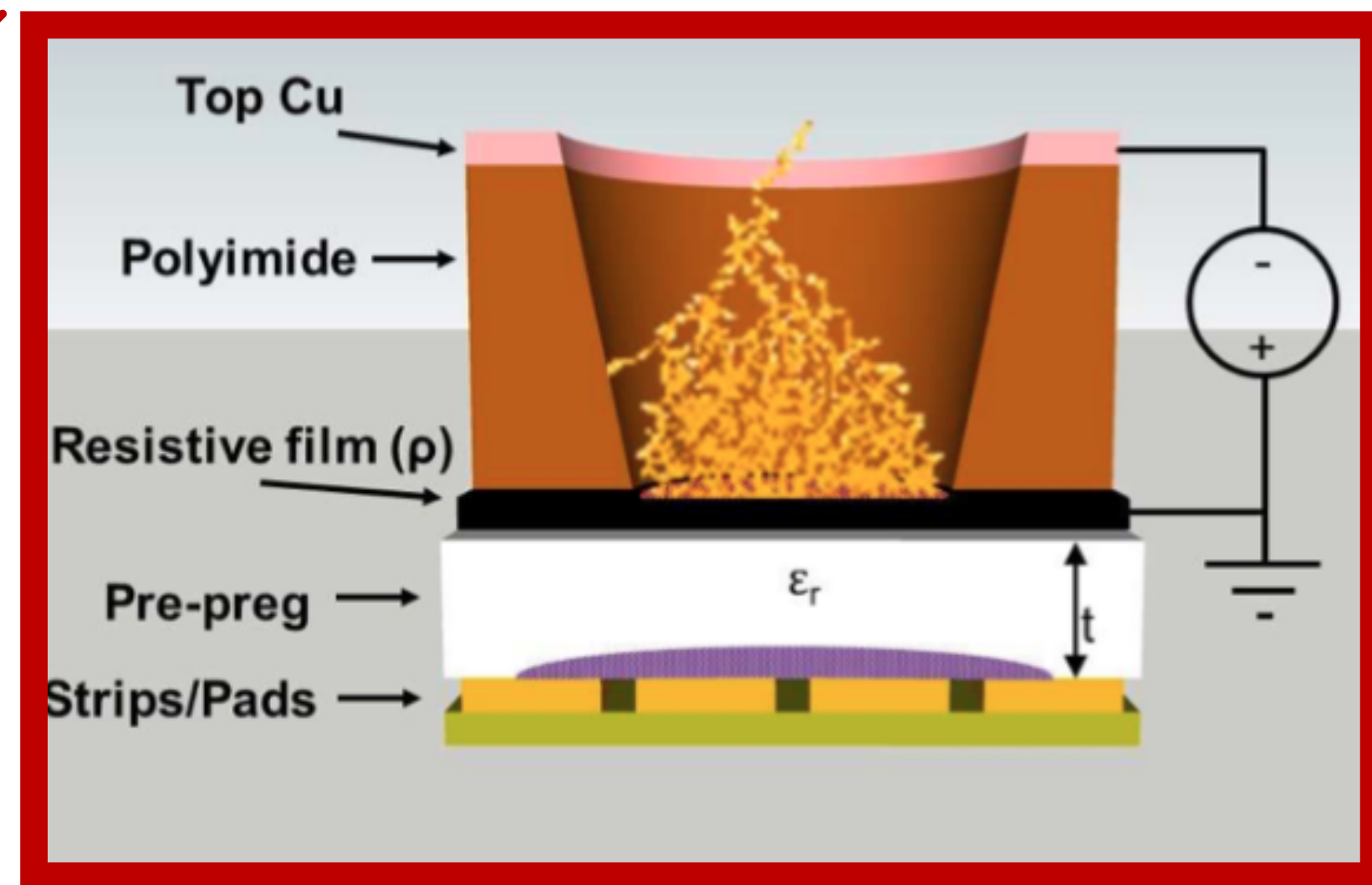
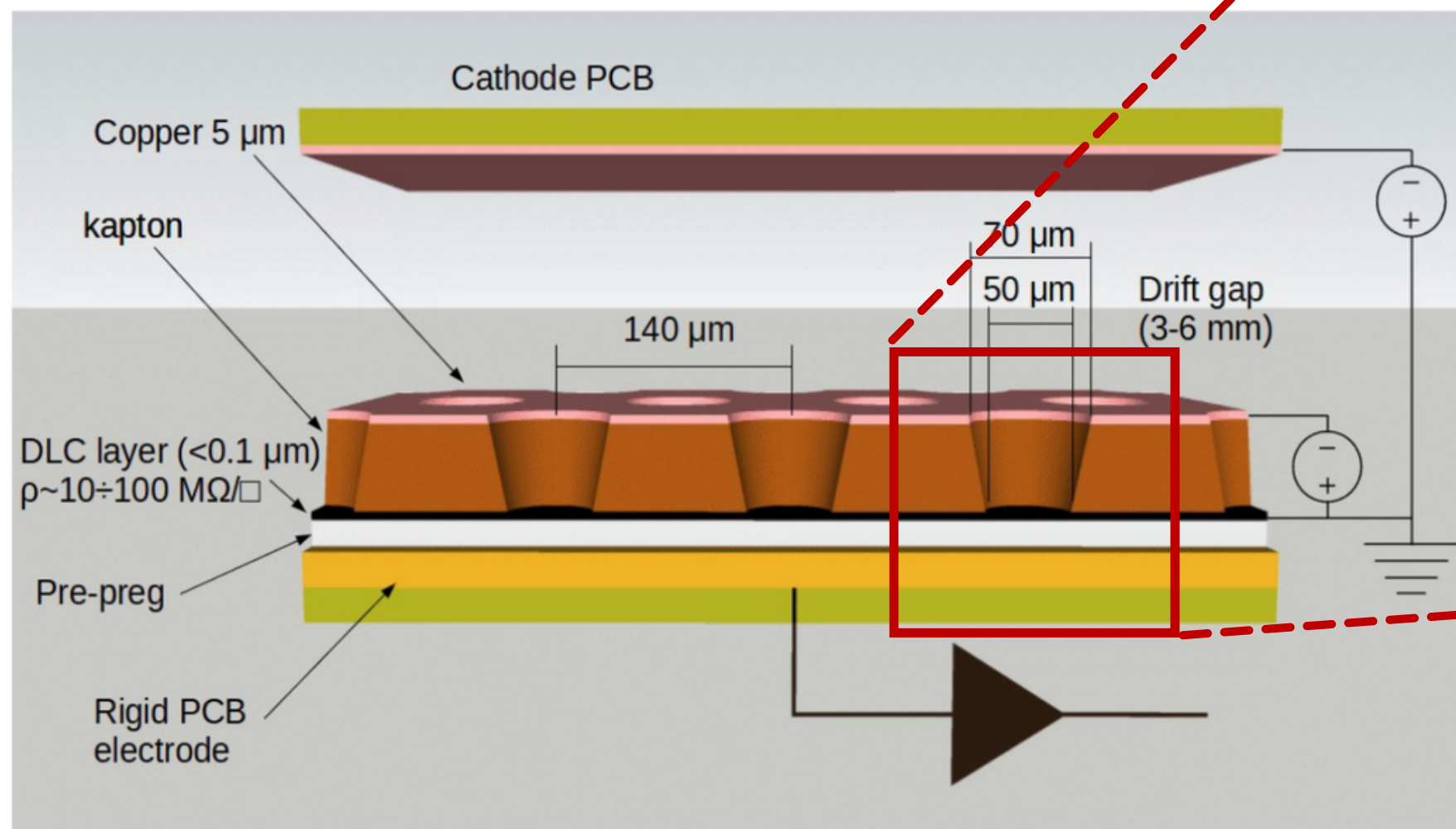
File Edit Format View Help

**Additional
material**

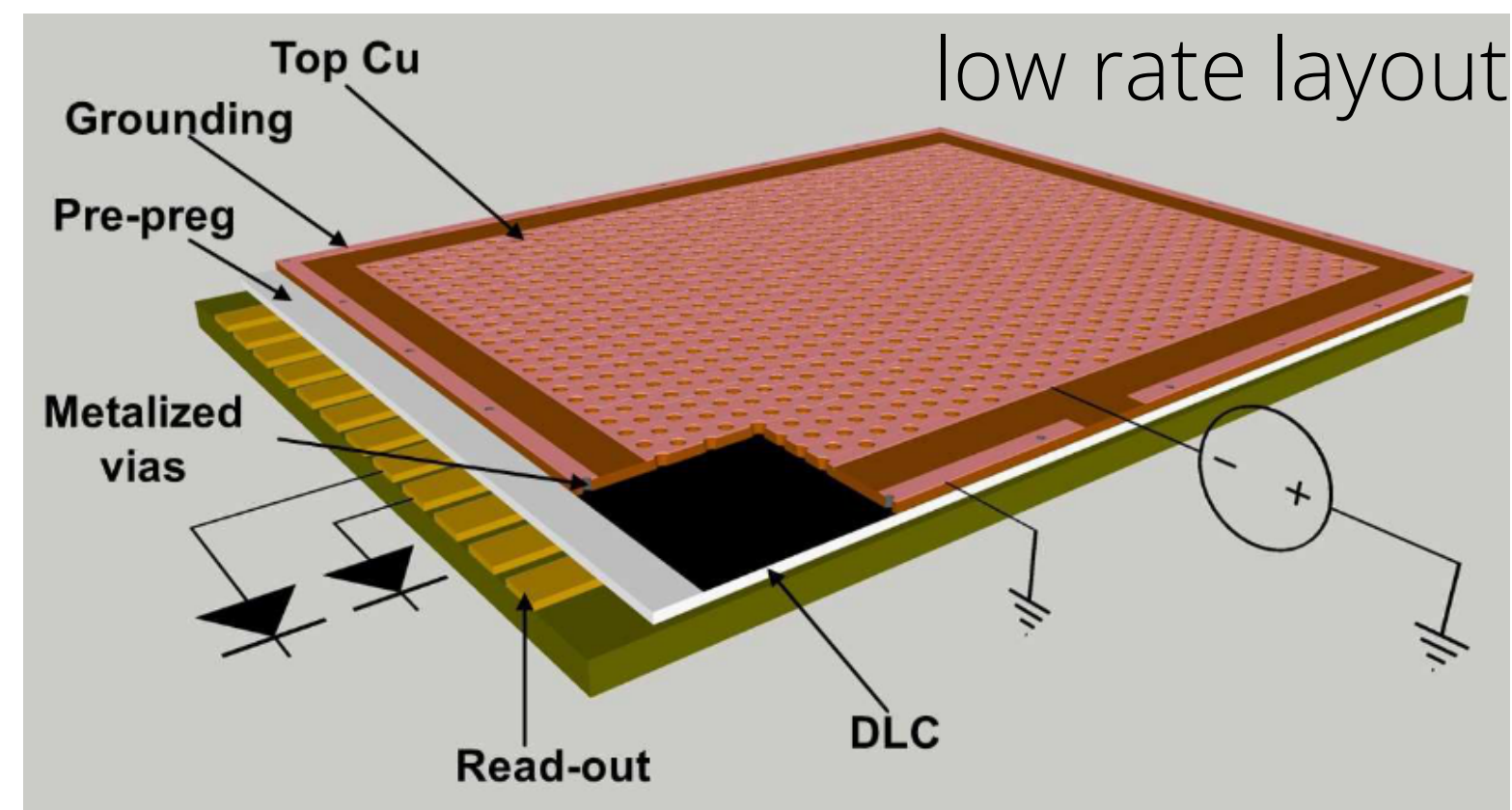


micro-RWELL

A SHORT INTRODUCTION



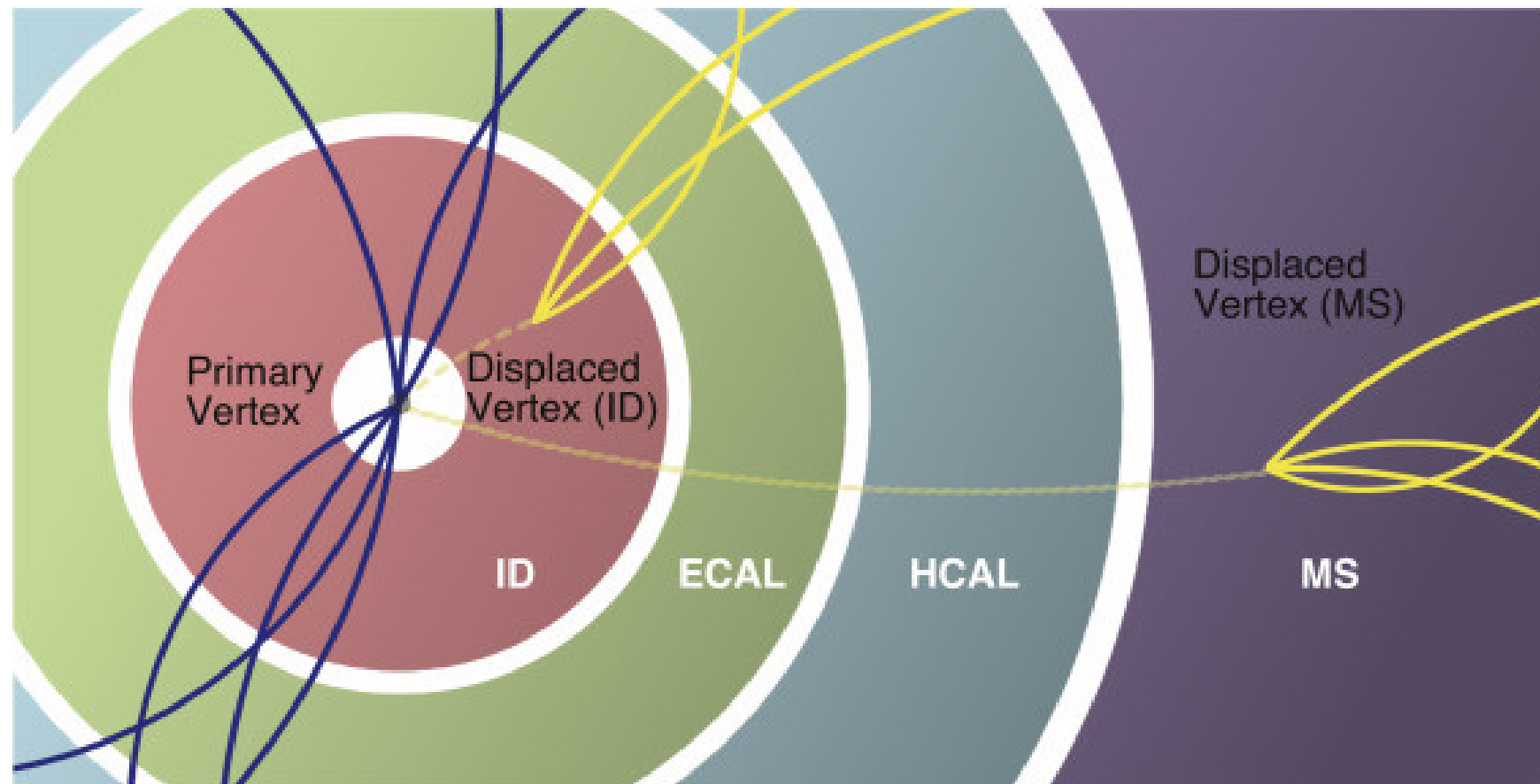
Single stage resistive Micro Pattern Gas Detector firstly designed by G. Bencivenni in 2007



Long Lived Particles (LLP)

Category of BSM particles that, due to feeble interaction, decay far away from the primary vertex

Signatures of different BSM models similar



neutral LLP channels

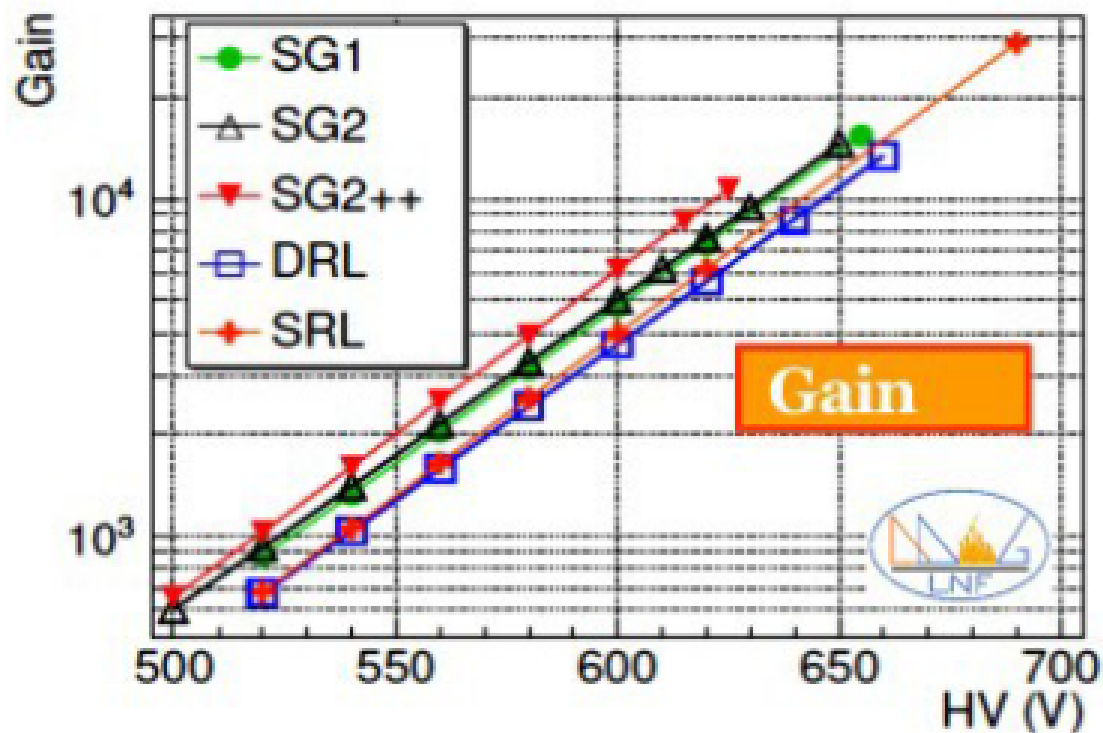
Production \ Decay	$\gamma\gamma(+inv.)$	$\gamma + inv.$	$jj(+inv.)$	$jj\ell$	$\ell^+\ell^- (+inv.)$	$\ell_\alpha^+ \ell_{\beta \neq \alpha}^- (+inv.)$
DPP: sneutrino pair	+	SUSY	SUSY	SUSY	SUSY	SUSY
HP: squark pair, $\tilde{q} \rightarrow jX$ or gluino pair $\tilde{g} \rightarrow jjX$	+	SUSY	SUSY	SUSY	SUSY	SUSY
HP: slepton pair, $\tilde{\ell} \rightarrow \ell X$ or chargino pair, $\tilde{\chi} \rightarrow WX$	+	SUSY	SUSY	SUSY	SUSY	SUSY
HIG: $h \rightarrow XX$ or $\rightarrow XX + inv.$	Higgs, DM*	+	Higgs, DM*	RH ν	Higgs, DM* RH ν^*	RH ν^*
HIG: $h \rightarrow X + inv.$	DM*, RH ν	+	DM*	RH ν	DM*	+
RES: $Z(Z') \rightarrow XX$ or $\rightarrow XX + inv.$	Z', DM*	+	Z', DM*	RH ν	Z', DM*	+
RES: $Z(Z') \rightarrow X + inv.$	DM	+	DM	RH ν	DM	+
CC: $W(W') \rightarrow \ell X$	+	+	RH ν^*	RH ν	RH ν^*	RH ν^*

https://indico.cern.ch/event/714087/contributions/2985914/attachments/1650488/2641192/LHC-LLP_Shuve.pdf

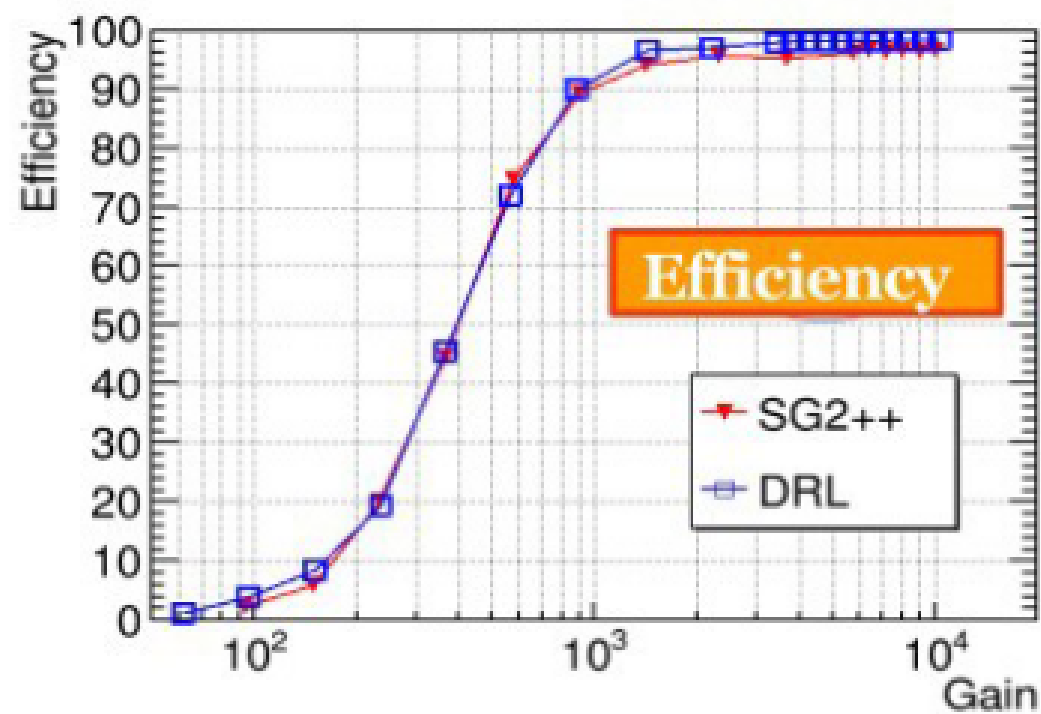
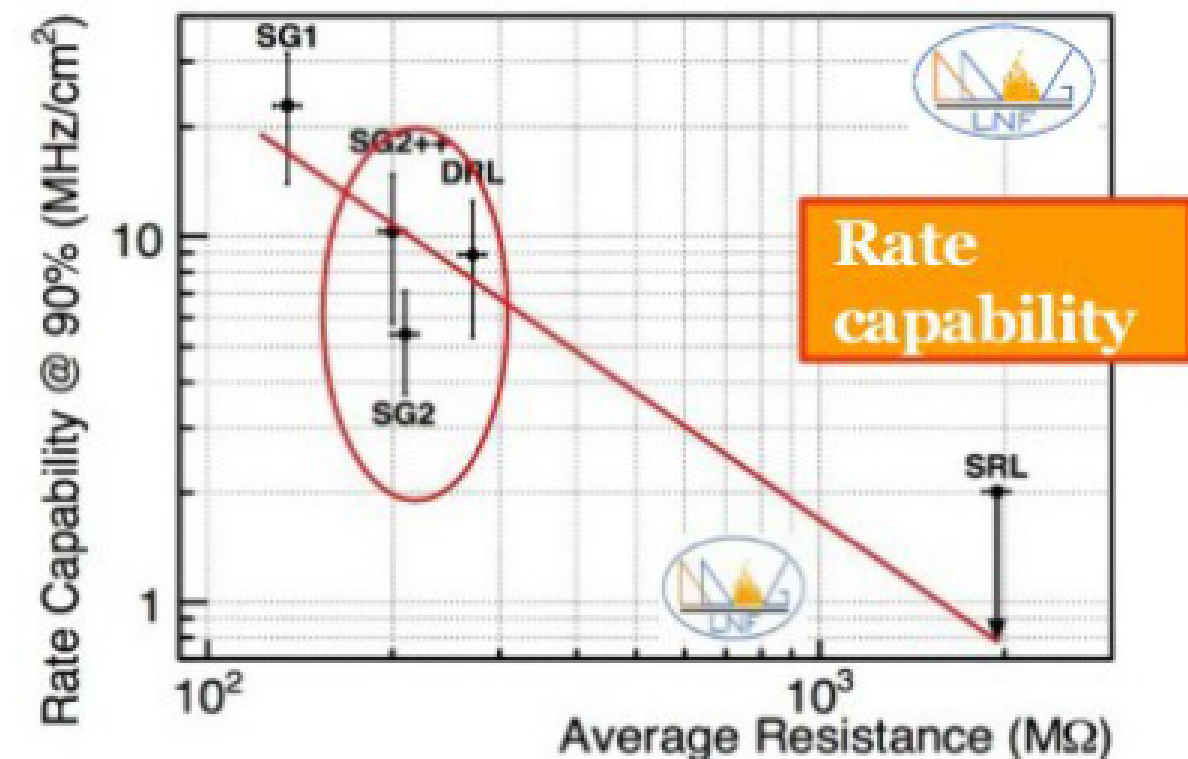
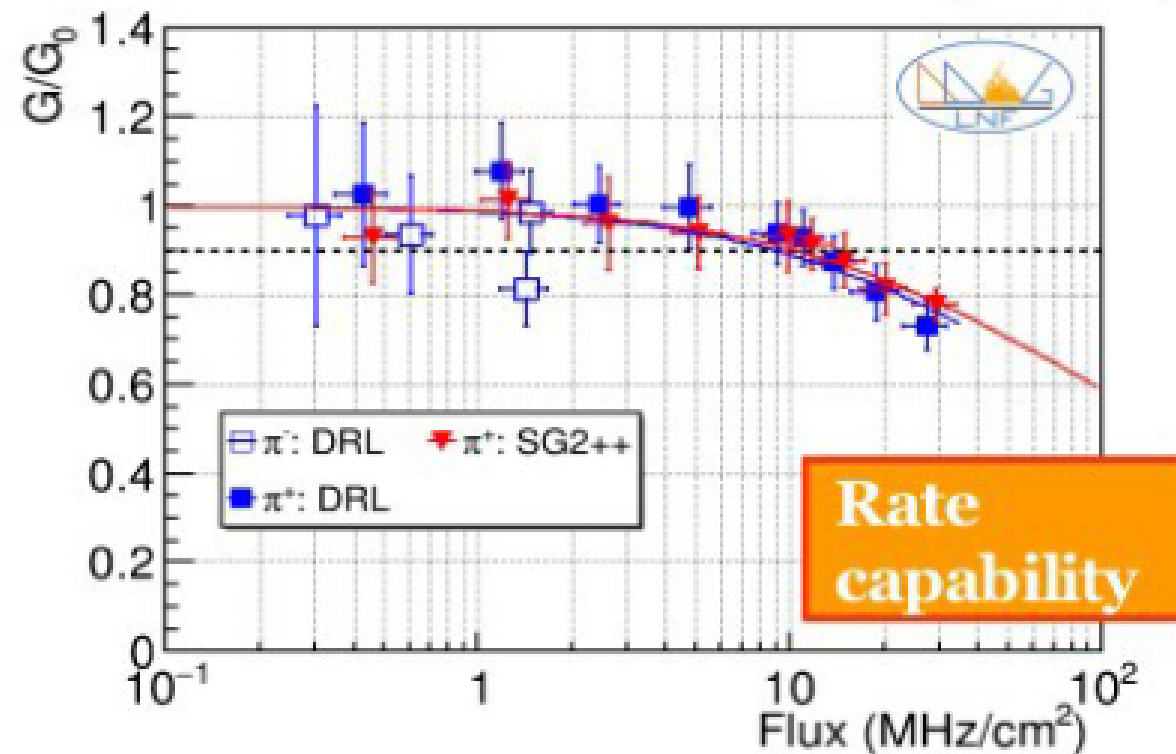
Muon detector with high spatial resolution can be used to measure very long displaced vertexes!

μ -RWELL performance overview

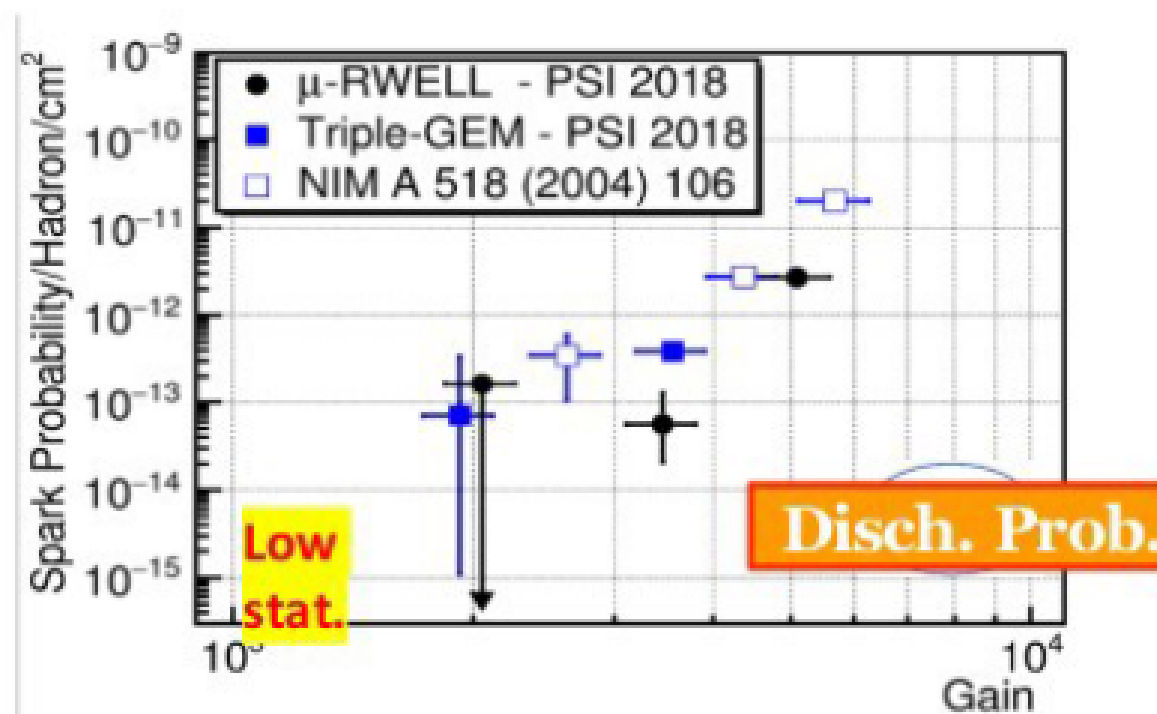
Gain up to 10^4



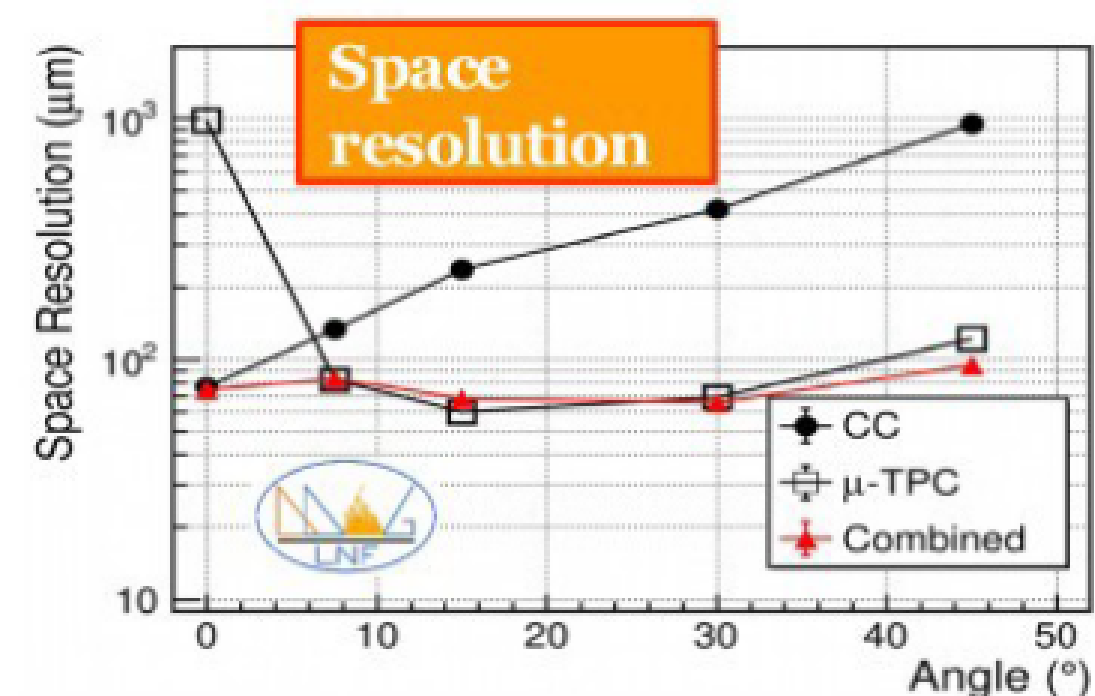
Rate Capability (@ G= 5000) \sim 5-10 MHz/cm²



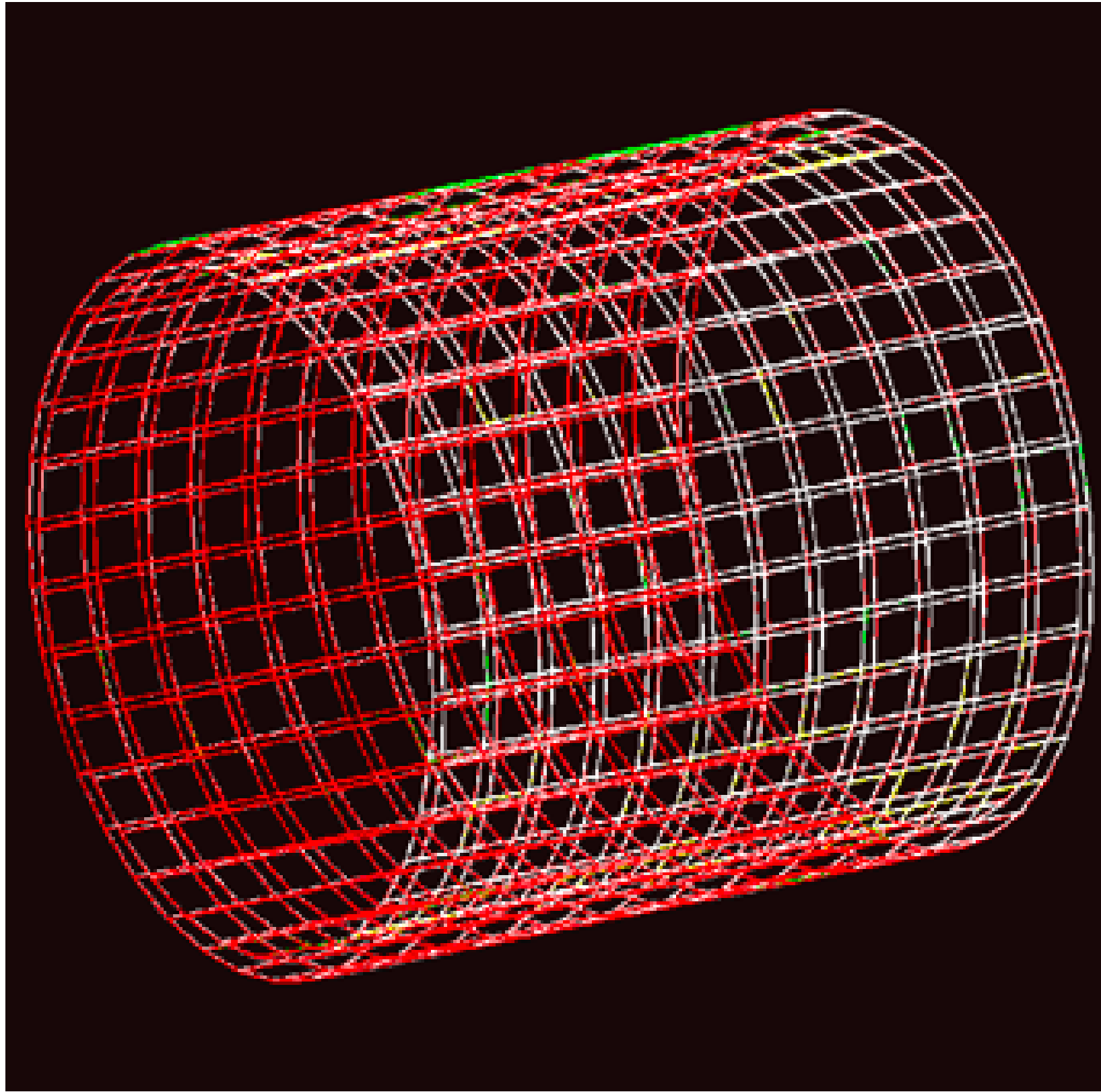
Efficiency \sim 98%



Discharge probability $\sim 10^{-13}$ @ 4000



Space resolution $\sim 100 \mu$ m



Barrel Preshower layout

GEANT4 Simulation by E. Fontanesi, PhD

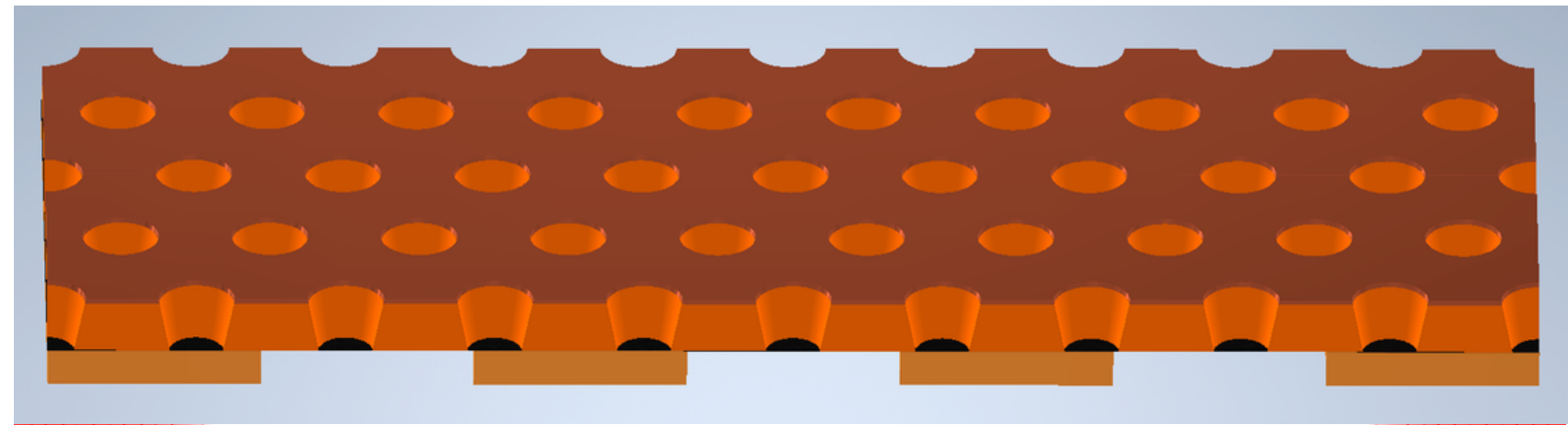
Muon detector similar, but larger

Optimization on-going on reducing input strip capacitance

Few Options:

- pitch to 1-1.2mm but an increasing number of channels -
> to keep low-cost necessary TIGER ASIC
- narrower strips but to understand the charge collection -
> to see signals low threshold TIGER ASIC

The spread of the charge on the resistive layer has been described by M. S. Dixit, A. Rankin,
 NIM A 518 (2004) 721-727, NIM A 566 (2006) 281-285

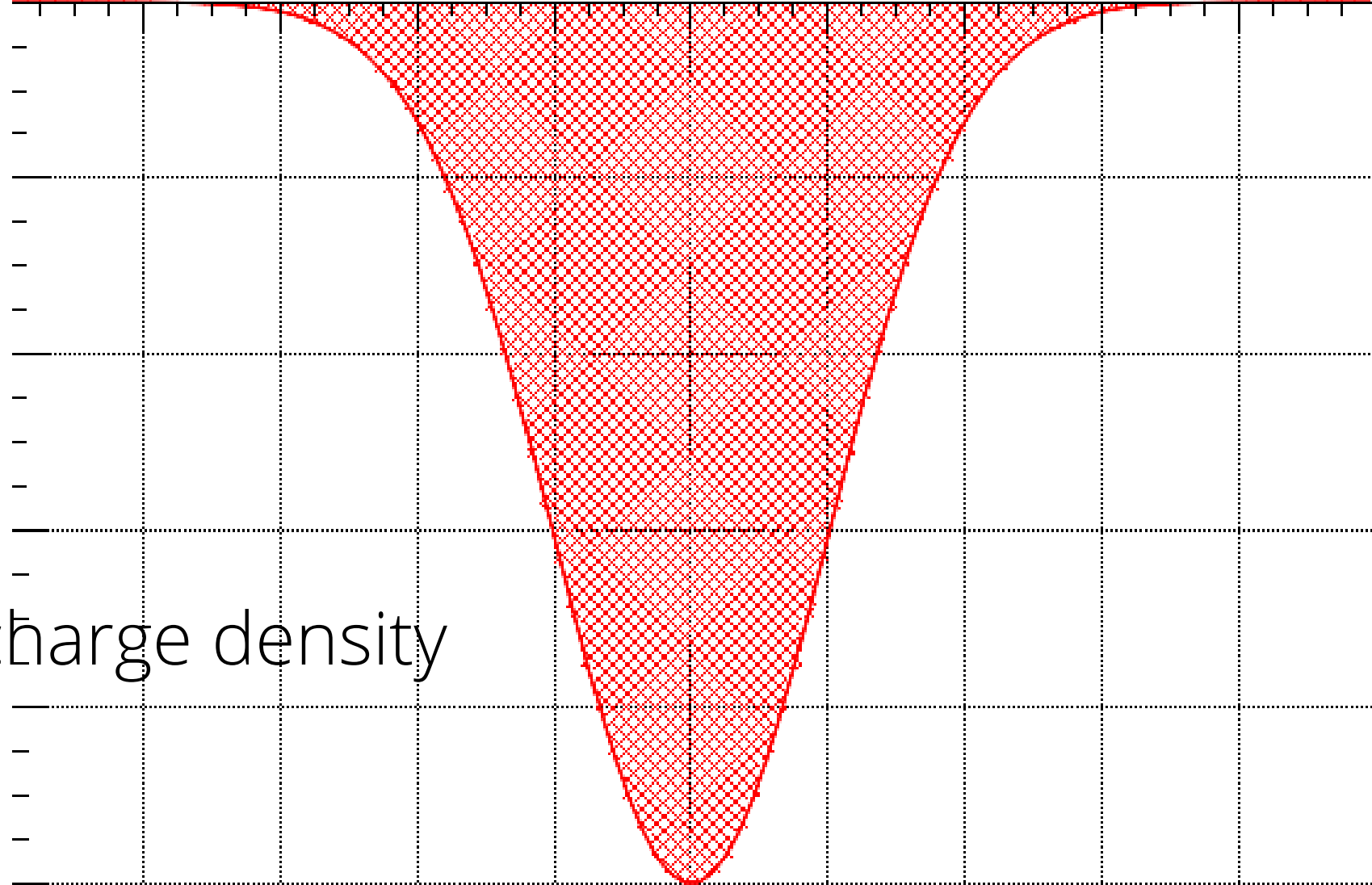


$$\rho(x, y, t) = \frac{Nq_e}{2\pi(2ht + w^2)} \exp\left[-\frac{(x^2 + y^2)}{2(2ht + w^2)}\right]$$

$$\rho(x, t) = \frac{q}{\sqrt{2\pi}\left[\sigma_0\left(1 + \frac{t-t_0}{\tau}\right)\right]} \exp\left[-\frac{(x-x_0)^2}{2\sigma_0^2\left(1 + \frac{t-t_0}{\tau}\right)^2}\right] \Theta(t-t_0)$$

- q the charge produced in an avalanche
- x₀ the position of the primary electron entering the amplification stage
- σ₀ a theoretical charge space extension of the avalanche
- t₀ the starting time of the track
- τ the decay time of the charge density due to the electrons movement towards the ground on the resistive surface.

τ is the parameter to be tuned



TB full dataset

Optimization S/N vs HV resistor filter

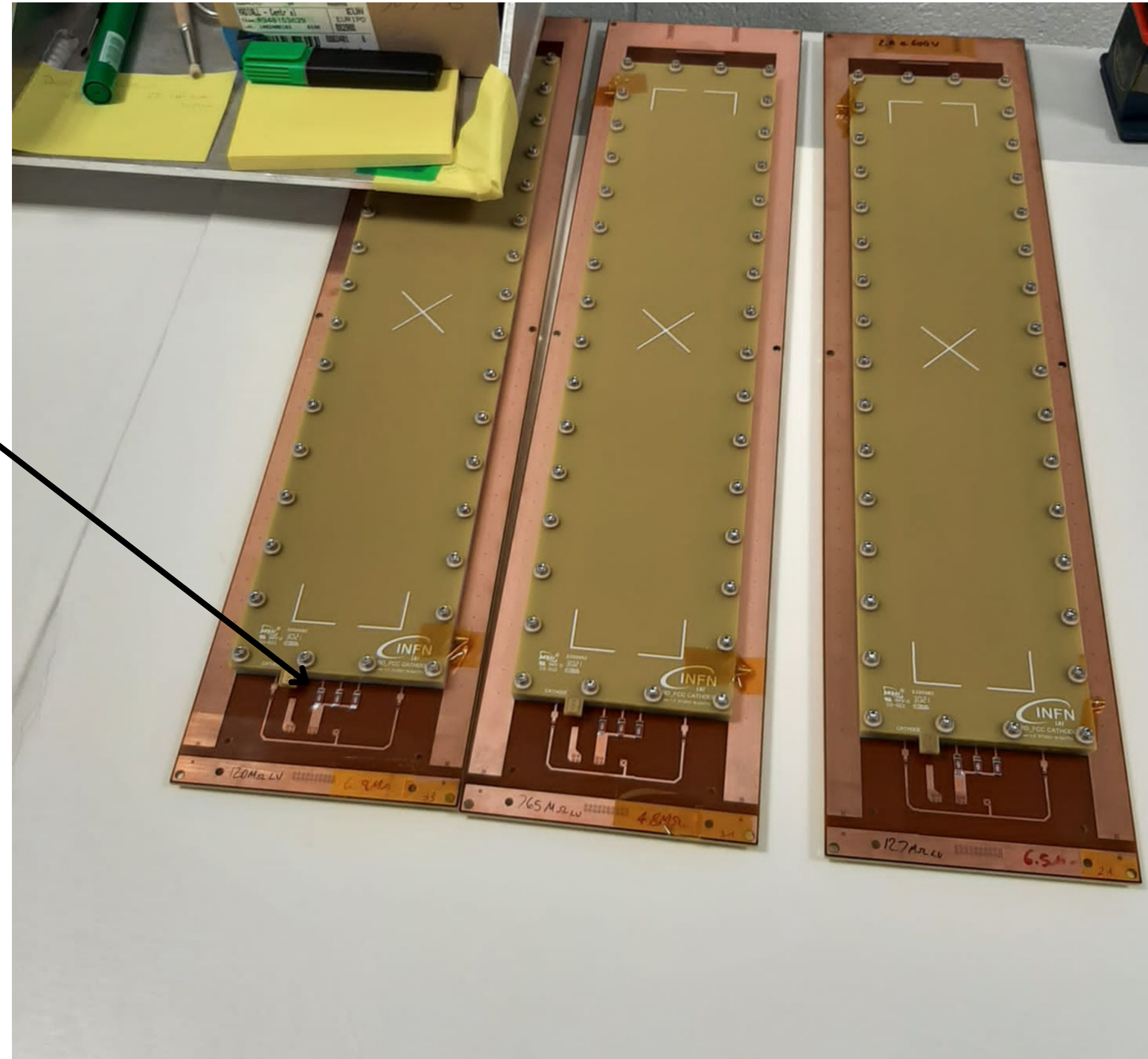
HV scan 0° - for trackers & test chambers

HV Scan 40° for test chambers

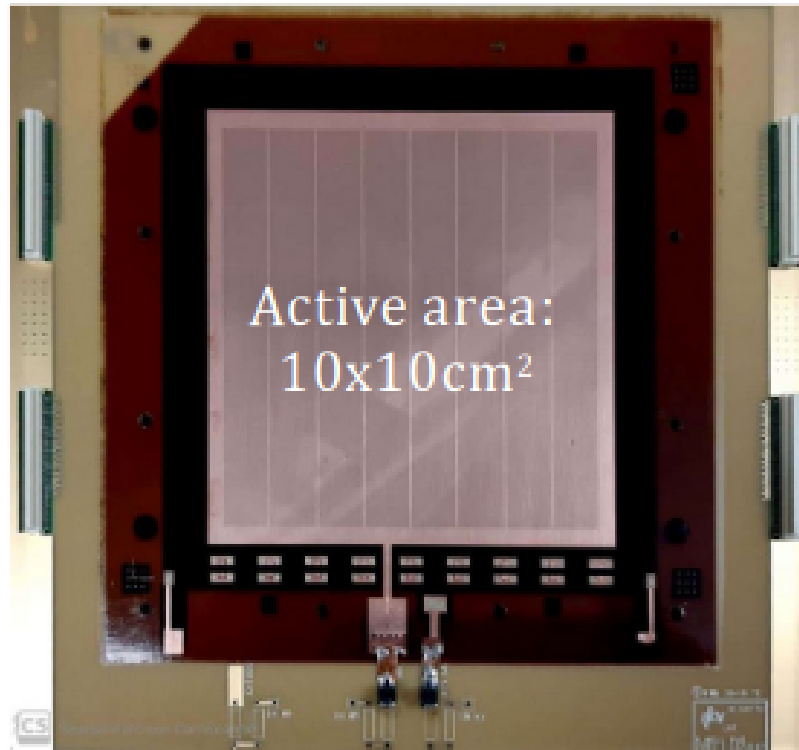
Angle scan $[0,10,20,30,40]^\circ$ test chambers

Drift field 0.5 kV, HV and angle scan

Drift field scan 0°



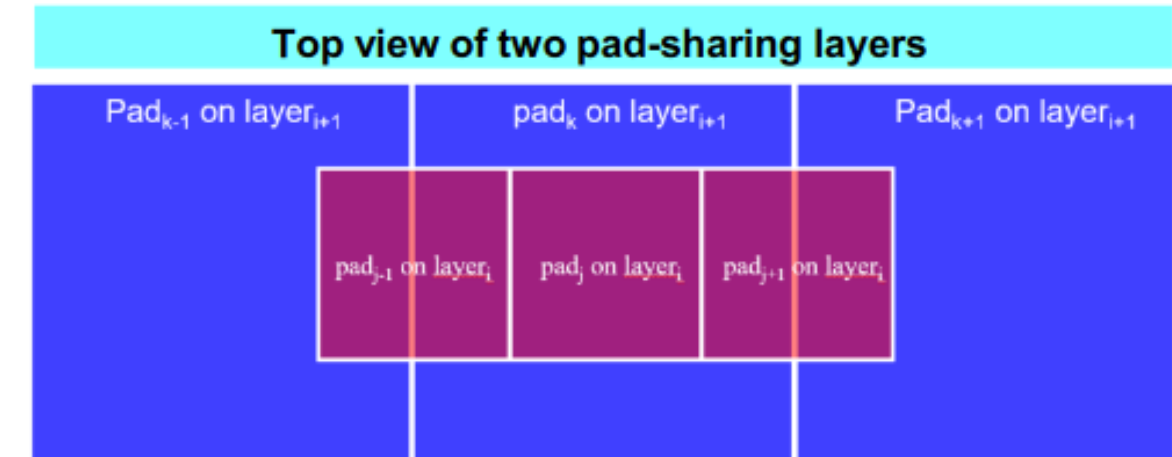
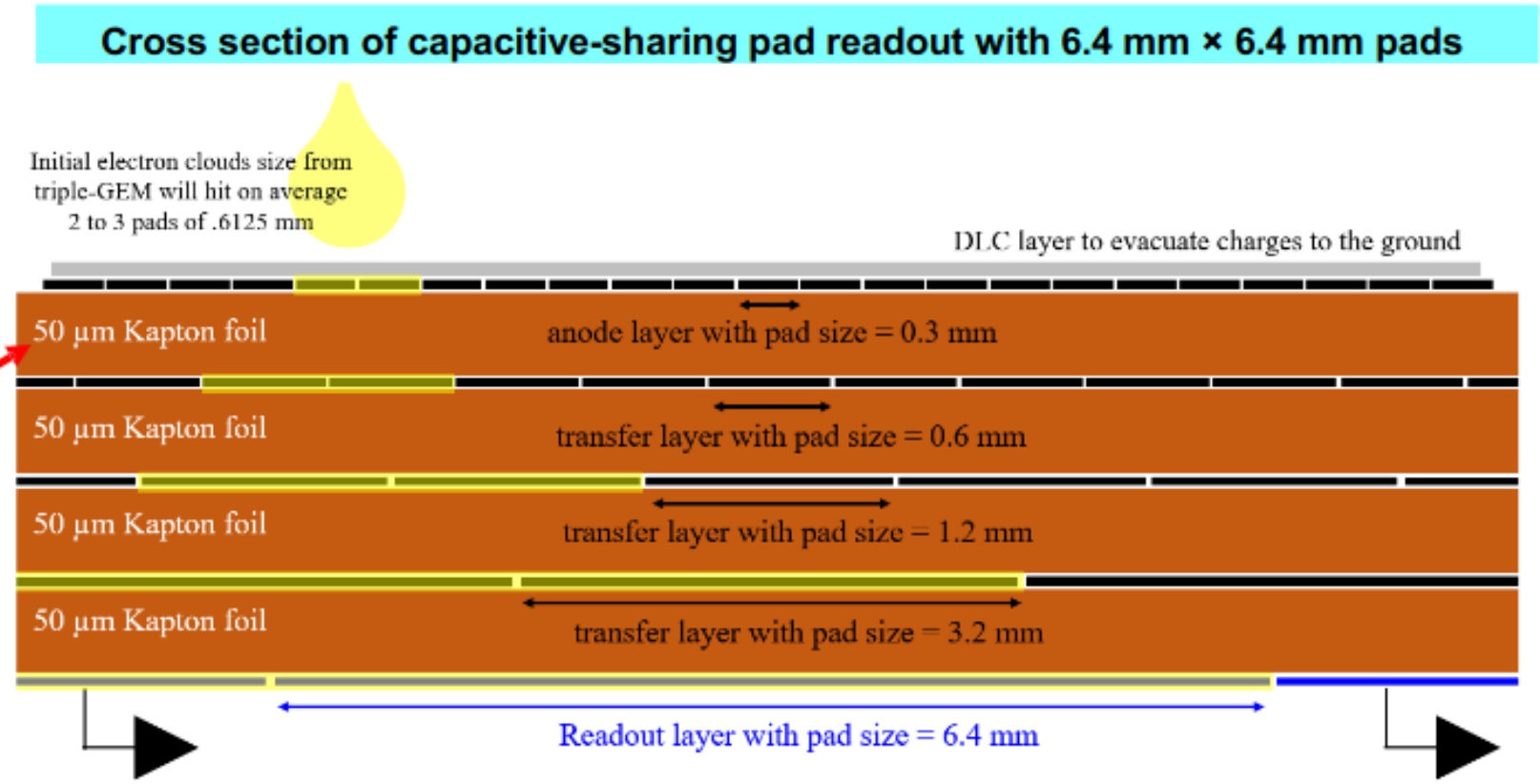
Detector Comparison



μ -RWELL trackers		μ -RWELL test	FEE signal
10x10cm ²	Active area	5x40cm ²	
300 μ m / 400 μ m / 10cm	Strip width/pitch/lenght	150 μ m / 400 μ m / 40cm	$\div 2$
100 μ m	Strip distance from DLC	50 μ m	$\times 2$
Standard (70 μ m)	Amplification WELL diameter	Larger (to be measured)	$\div ?$
30 \div 40M Ω / \square	DLC surface resistivity	10 \div 80M Ω / \square	

Principe of capacitive-sharing readout structures:

- ❖ Vertical stack of pads layers \Rightarrow Transfer of charge from MPGD via **capacitive coupling**
- ❖ A given arrangement of the pads position from one layer to the layer underneath as well as the doubling in size of the pad pitch allows:
 - ❖ Transverse sharing of the charges between neighboring pads of the layer $(i+1)$ from vertical charged transfer from layer (i) through capacitive coupling
 - ❖ Principle of transverse charge-sharing through capacitive coupling i.e., **capacitive-sharing** is illustrated on the cross-section sketch on the left
- ❖ The scheme preserves of the position information i.e. spatial resolution with large readout strips or pads: **Goal $50\ \mu\text{m}$ for 1-mm strip r/o and $150\ \mu\text{m}$ for $1\ \text{cm}^2$ pad r/o**
- ❖ Basic proof of concept established with $800\ \mu\text{m}$ X-Y strip

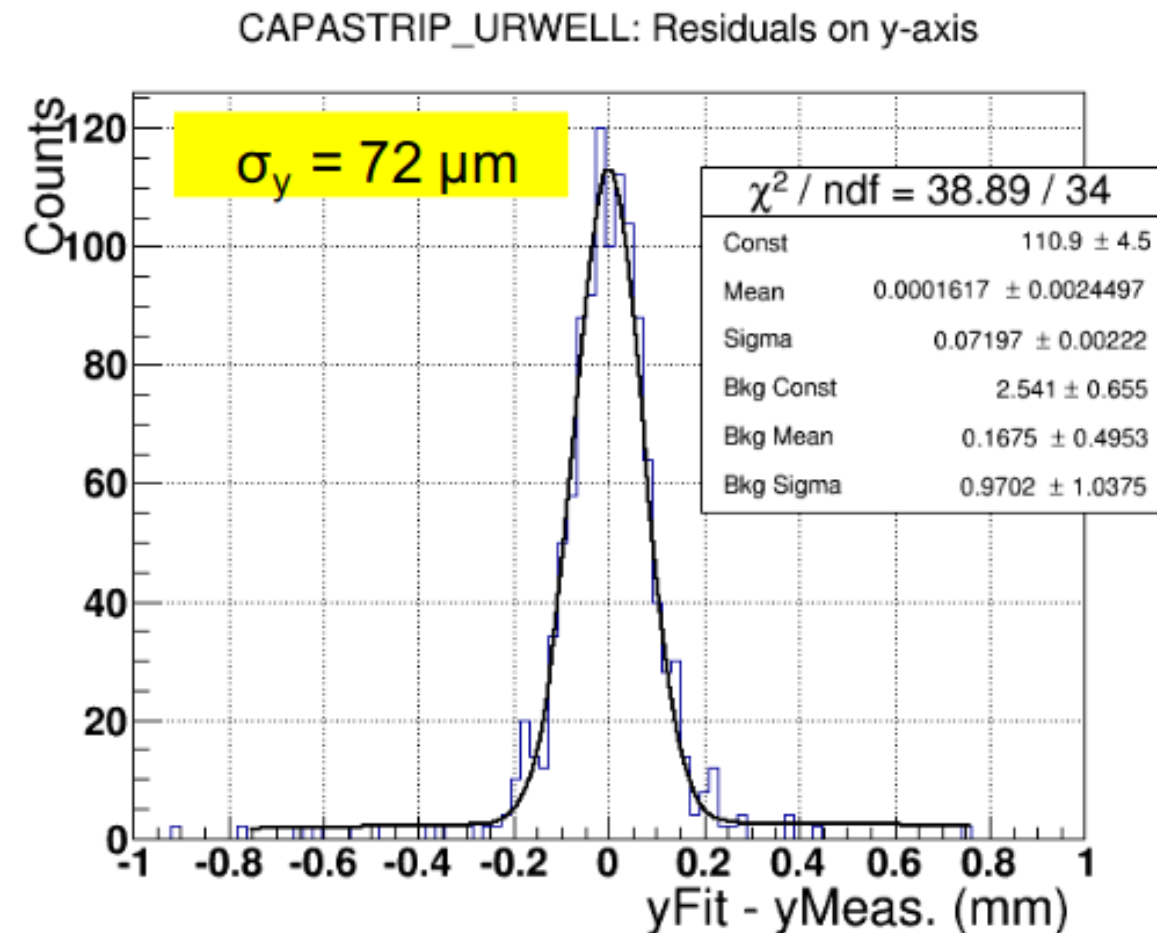
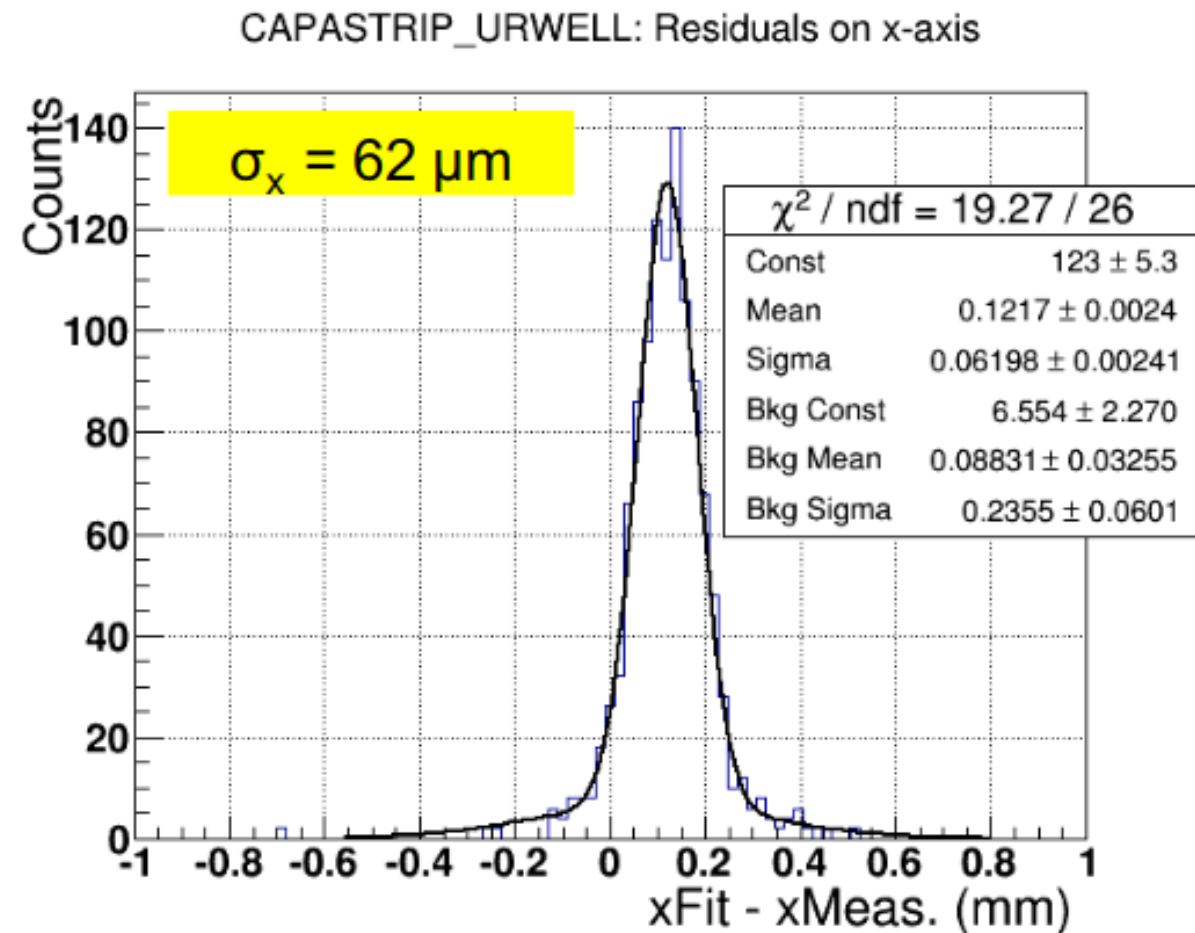


Motivation & some key facts of capacitive-sharing readout:

- ❖ Develop high performance & low channel count readout structures for MPGDs:
- ❖ Reduce the number of readout electronic channels for large area MPGDs
- ❖ Low-cost technology for large area \square standard PCB fabrication techniques

10 cm \times 10 cm μ RWELL with capacitive-sharing 2D strip readout

- ❖ Pitch is 800 μ m \rightarrow twice COMPASS readout strip design
- ❖ X-strip and Y-strips on two separate layers with **No connecting vias** \rightarrow Easy fabrication for large area, low-mass capability
- ❖ Strip parameters: top strip (y-strips) = 250 μ m, bot strip (x-strips): 750 μ m \times 500 μ m \rightarrow require tuning for equal charge sharing
 - ❖ Top and bottom strip area overlap minimized by design to minimize cross talk and capacitance etc ...
- ❖ 3 capacitive-sharing pad layers with: 200 μ m, 400 μ m and 800 μ m pad size respectively
- ❖ Tested in electron beam in Hall D @ JLab (Sept-Oct 2021)



capaSh-XY-Strip μ RWELL

