

GUI development for the ATLAS sMDT MiniDAQ system

University of Michigan ATLAS group US ATLAS SUPER program final presentation

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ATLAS and Muon spectrometer Overview

- ATLAS:
 - general purpose particle detector
 - search for new physics
 - perform precision measurements
- Precision muon chambers Monitored Drift Tubes (MDT):
 - slow response (~800 ns)
 - precise position resolution (~100 μm)
 - determine muon p with resolution of 10% at 1 TeV
- Trigger muon chambers:
 - Resistive Plate Chambers (RPC)
 - Thin Gap Chambers (TGC)
 - fast response (1-20 ns)
 - limited position resolution (~1 cm)



Phase-II MDT upgrade

- Phase-II upgrade
 - collision rate increased by 5-7 factor
 - MDTs improve the trigger muon momentum resolution at first trigger level
 - RPCs/TGCs provide timing and regions of interest for MDT triggers
 - New electronics required due to:
 - larger event rate 1MHz at first trigger level and 10 kHz for data recorded to the tape (100kHz and 1kHz currently)
 - longer latency 10 microseconds for first trigger level (2.5 microseconds currently).
 - Upgrade front-end electronics:
 - Amplifier/Shaper/Discriminator (ASD)
 - Time to Digital Converter (TDC)
 - Chamber Service Module (CSM)
 - L0 MDT trigger processor





MiniDAQ system

- Need a mobile MiniDAQ system to:
 - integrate new electronics
 - test chambers
 - chamber integration/ commissioning on surface and inside collision hall
- MiniDAQ system will connect to:
 - two CSMs
 - each CSM connects to up to 18 mezz cards
 - each mezz card will have 3
 ASD chips and 1 TDC chip
 - Total: miniDAQ handles 108
 ASD and 36 TDC chips





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GUI Outline

- Michigan responsible for building:
 - half of 96 new sMDT chambers
 - 22k TDCs
 - 1.2k CSMs
 - A mobile miniDAQ system to test newly built chambers and front-end electronics
 - Perform detector-electronics integration and commissioning
- The miniDAQ system requirements:
 - configure/control all front-end chips, CSM boards, and FPGA data processing eval. Board (of CSM board).
 - collect data at different running conditions
 - analyze and monitor the output data
 - record data on a PC
- All configure/control/monitor tasks will be done through a GUI running on a PC

GUI connection logic

- Configuration Code:
 - stores TDC, ASD, and CSM values in memory, connects to both the hardware and GUI values.
- Parameters can be determined, loaded, and saved in one of two ways:
 - GUI change individual parameters, easily connect to hardware through config. code, save setup to xml file.
 - Xml files easily load and save all TDC, ASD, and CSM parameters to GUI and connect to hardware through config. code.



GUI current progress

- Have implemented functions to:
 - Tell the FPGA how to configure the TDC
 - Tell PC how to decode data from the TDC
 - Create, load, and save common TDC configs.
 - Perform similar operations for ASD and IpGBT within the CSM.
- GUI created with python, PyQt, and QtDesigner

Hit gen TDC	CSM			
		JTAG IN		
Data Rate:	320Mb •	mode set	TRST	
Mode:	Triggerless •	internal counter	master reset	
Formati	pair •	fine time lut	master reset	
ronnat.	pan	reset option		
EdgeType:	rising •	ePII option	setup_ASD0	
Clk160_phase:	8	TDC status	setup_ASD1	
Clk320_1_phase:	0	Verificate JTAG	setup_ASD2	
Iı	nit			
GUI run information 2020-08-11 09:23	n :05>>Channel enable R	: 0xFFFFFF		~
2020-08-11 09:23 2020-08-11 09:23 2020-08-11 09:23 2020-08-11 09:23 2020-08-11 09:23	:05>>[0, 1, 2, 3, 4, 5, 6 :05>>Channel enable F :05>>[0, 1, 2, 3, 4, 5, 6 :05>>8b10b encoding e :05>>Idle packet insert	5, 7, 8, 9, 10, 11, 12, 13, 14, 15, : 0xFFFFF 5, 7, 8, 9, 10, 11, 12, 13, 14, 15, nabled not enabled	16, 17, 18, 19, 20, 21, 22, 23] 16, 17, 18, 19, 20, 21, 22, 23]	
2020-08-11 09:23 2020-08-11 09:23	:05>>Legacy TTC enabl :05>>BCR from internal	ed for Trigger Event_reset with roll_over = 0xFFF BC and d	elay = 0x000 BC	
1010 00 11 00.12	05>>/////DAO initializ	ation donel//////		~

GUI current progress: TDC and ASD



GUI current progress: TDC and ASD

Example of TDC detailed function- Mode Set:

Setup0			? ×
enable_new_ttc	enable_trigger	enable_legacy	
enable_master_reset_code	channel_data_debug	full_width_res	
enable_direct_bunch_reset	enable_leading	enable_8b10b	
enable_direct_event_reset	🗹 enable_pair	enable_insert	
enable_direct_trigger	enable_fake_hit	enable_error_packet	
✓ auto_roll_over	enable_trigger_timeout	enable_TDC_ID	
bypass_bcr_distribution	enable_high_speed	enable_error_notify	
Channel Options: 0 1 2 3 4 5 6 rising_is_leading:	7 8 9 10 11 12 13 14 15 16 17 18 1	9 20 21 22 23 Select All:	Deselect All: rising is leading
$channel_enable_r: \checkmark \checkmark \checkmark \checkmark \checkmark \checkmark \checkmark$		✓ ✓ ✓ ✓ enable r	enable r
$channel_enable_f: \bigtriangledown \bigtriangledown \checkmark \checkmark \checkmark \checkmark \checkmark \checkmark$		enable f	enable f
TDC_ID: 7AAAA		Width_select: 000	
Apply	ОК	Cancel	

Example of ASD function - ASD0:

ASD0									? ×
	0	1	2	3	4	5	6	7	All Channels On
Channel:	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	All Channels Off
Chip Main 51 Int. C	Mode: Thr (m Gate:	ADC	mode • visc1 Hy L40 isc2 Thi	r:): • Round	d. Curr:	De	ad Time	2:
18	ns	• 9	6 mV	•	5.9 u	A	• 81	0 ns	•
Save	Single	ASD		Sa	ve All A	ASDs			Discard

GUI current progress: lpGBT for CSM board

- Low power GBT (lpGBT) within the CSM is still in the final stages of development.
- Not many people use IpGBT at the moment, GUI for it is needed to enable easy future use
- Current CERN lpGBT configuration method:
 - Web-based control GUI with a raspberry pi board.
- My GUI will allow:
 - Configuration of IpGBT without requiring the internet
 - Will remove the need for a raspberry pi board.

lpGBT general board:

Save LpGBT	IpGBT State	IS		
Core:	Clocks:	High Speed:		
ePortTX	ePort Clock	Equalizer		
ePortRX	Phase Shift Clock	Line Driver		
Chip Mode		Chip Config		
Transmitter Mode				
GUI run information				
GUI run information 2021-08-18 09:16:13>> 2021-08-18 09:16:13>>	Address 97 : value 0 Address 98 : value 0		 	

Example of IpGBT detailed setup - Phase Shift Clock

disabled				
	-	Frequency	disabled	
		Fine Tune		
0000000		Delay	00000000	
0	•	Drive Strength	0	
0	•	PE Strength	0	
disabled	•	PE Mode	disabled	
120	•	PE Width	120	
disabled	*	PS3 Frequency	disabled	
disabled		PS3	displad	
disabled	•	PS3 Frequency Fine Tune	disabled	
disabled	•	PS3 Frequency Fine Tune Delay	disabled	
disabled 00000000 0	•	PS3 Frequency Fine Tune Delay Drive Strength	disabled 00000000 0	
disabled 00000000 0 0	•	PS3 Frequency Fine Tune Delay Drive Strength PE Strength	disabled 00000000 0 0	
disabled 00000000 0 0 disabled	•	PS3 Frequency Fine Tune Delay Drive Strength PE Strength PE Mode	disabled 00000000 0 0 disabled	
	0 0 disabled 120	0 • • 0 • • disabled • 120 •	0 • 0 • Drive Strength 0 • PE Strength disabled • 120 •	0 • Drive Strength 0 0 • PE Strength 0 disabled • PE Mode disabled 120 • PE Width 120

Next steps

- Future Steps:
 - Import similar configuration for further CSM implementation and FPGA evaluation board
 - Add modes for noise runs and cosmic ray runs
 - Implement code to analyze and monitor output data
 - Further test functionality and continue to make necessary improvements
- Expect this system to be in use for the next ten years at Michigan and CERN



Final Remarks

- Thank you!
 - Mentors:
 - Advisor: Junjie Zhu
 - Graduate Student Advisor: Yuxiang Guo
 - Additional thanks to:
 - US ATLAS SUPER Program
- Questions?





Resources

[1] Requirements and Specifications of the Phase-II TDC for the ATLAS MDT Detector[2] Evidence for the production of three massive vector bosons with the ATLAS detector[3] mini DAQ diagram from Xueye Hu